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Features

- Single 1.65V - 3.6V Supply
- Serial Peripheral Interface (SPI) Compatible
    - Supports SPI Modes 0 and 3
    - Supports Dual-I/O Operation
- 70MHz Maximum Operating Frequency
    - Clock-to-Output (t_V) of 6 ns
- Flexible, Optimized Erase Architecture for Code + Data Storage Applications
    - Small (256-Byte) Page Erase
    - Uniform 4-Kbyte Block Erase
    - Uniform 32-Kbyte Block Erase
    - Uniform 64-Kbyte Block Erase
    - Full Chip Erase
- Hardware Controlled Locking of Protected Sectors via $\overline{WP}$ Pin
- 128-byte, One-Time Programmable (OTP) Security Register
    - 64 bytes factory programmed with a unique identifier
    - 64 bytes user programmable
- Flexible Programming
    - Byte/Page Program (1 to 256 Bytes)
    - Dual-Input Byte/Page Program (1 to 256 Bytes)
    - Sequential Program Mode Capability
- Fast Program and Erase Times
    - 2ms Typical Page Program (256 Bytes) Time
    - 45ms Typical 4-Kbyte Block Erase Time
    - 360ms Typical 32-Kbyte Block Erase Time
    - 720ms Typical 64-Kbyte Block Erase Time
- Automatic Checking and Reporting of Erase/Program Failures
- Software Controlled Reset
- JEDEC Standard Manufacturer and Device ID Read Methodology
- Low Power Dissipation
    - 200nA Ultra Deep Power Down current (Typical)
    - 4.5µA Deep Power-Down Current (Typical)
    - 25uA Standby current (Typical)
    - 3mA Active Read Current (Typical)
- Endurance: 100,000 Program/Erase Cycles
- Data Retention: 20 Years
- Complies with Full Industrial Temperature Range
- Industry Standard Green (Pb/Halide-free/RoHS Compliant) Package Options
    - 8-lead SOIC (150-mil)
    - 8-pad Ultra Thin DFN (2 x 3 x 0.6 mm)
    - 8-pad Ultra Thin DFN (5 x 6 x 0.6 mm)
    - 8-lead TSSOP Package
    - 8-ball WLCSP (3 x 2 x 3 ball matrix)

1. Description

The Adesto® AT25XE021A is a serial interface Flash memory device designed for use in a wide variety of high-volume consumer based applications in which program code is shadowed from Flash memory into embedded or external RAM for execution. The flexible erase architecture of the AT25XE021A, with its page erase granularity it is ideal for data storage as well, eliminating the need for additional data storage devices.

The erase block sizes of the AT25XE021A have been optimized to meet the needs of today's code and data storage applications. By optimizing the size of the erase blocks, the memory space can be used much more efficiently. Because certain code modules and data storage segments must reside by themselves in their own erase regions, the wasted and unused memory space that occurs with large sectored and large block erase Flash memory devices can be greatly reduced. This increased memory space efficiency allows additional code routines and data storage segments to be added while still maintaining the same overall device density.

The device also contains a specialized OTP (One-Time Programmable) Security Register that can be used for purposes such as unique device serialization, system-level Electronic Serial Number (ESN) storage, locked key storage, etc.

Specifically designed for use in many different systems, the AT25XE021A supports read, program, and erase operations with a wide supply voltage range of 1.65V to 3.6V. No separate voltage is required for programming and erasing.

2. Pin Descriptions and Pinouts

Table 2-1. Pin Descriptions

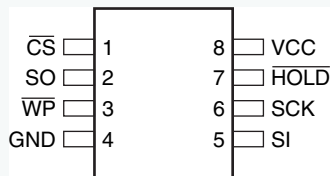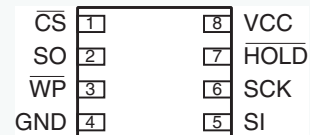| Symbol	Name and Function	Asserted State	Type
$\overline{CS}$	**CHIP SELECT:** Asserting the $\overline{CS}$ pin selects the device. When the $\overline{CS}$ pin is deasserted, the device will be deselected and normally be placed in standby mode (not Deep Power-Down mode), and the SO pin will be in a high-impedance state. When the device is deselected, data will not be accepted on the SI pin. A high-to-low transition on the $\overline{CS}$ pin is required to start an operation, and a low-to-high transition is required to end an operation. When ending an internally self-timed operation such as a program or erase cycle, the device will not enter the standby mode until the completion of the operation.	Low	Input
SCK	**SERIAL CLOCK:** This pin is used to provide a clock to the device and is used to control the flow of data to and from the device. Command, address, and input data present on the SI pin is always latched in on the rising edge of SCK, while output data on the SO pin is always clocked out on the falling edge of SCK.	-	Input
SI (I/O$_0$)	**SERIAL INPUT:** The SI pin is used to shift data into the device. The SI pin is used for all data input including command and address sequences. Data on the SI pin is always latched in on the rising edge of SCK. With the Dual-Output Read commands, the SI Pin becomes an output pin (I/O$_0$) in conjunction with other pins to allow two bits of data on (I/O$_{1-0}$) to be clocked out on every falling edge of SCK. To maintain consistency with the SPI nomenclature, the SI (I/O$_0$) pin will be referenced as the SI pin unless specifically addressing the Dual-I/O modes in which case it will be referenced as I/O$_0$. Data present on the SI pin will be ignored whenever the device is deselected ($\overline{CS}$ is deasserted).	-	Input/ Output

Table 2-1. Pin Descriptions (Continued)

| Symbol	Name and Function	Asserted State	Type
SO (I/O_1)	**SERIAL OUTPUT:** The SO pin is used to shift data out from the device. Data on the SO pin is always clocked out on the falling edge of SCK. With the Dual-Output Read commands, the SO Pin remains an output pin (I/O_1) in conjunction with other pins to allow two bits of data on (I/O_{1-0}) to be clocked out on every falling edge of SCK. To maintain consistency with the SPI nomenclature, the SO (I/O_1) pin will be referenced as the SO pin unless specifically addressing the Dual-I/O modes in which case it ise referenced as $I/O_{1.}$ The SO pin will be in a high-impedance state whenever the device is deselected ($\overline{CS}$ is deasserted).	-	Input/Output
$\overline{WP}$	**WRITE PROTECT:** The $\overline{WP}$ pin controls the hardware locking feature of the device. Please refer to "Protection Commands and Features" on page 17 for more details on protection features and the $\overline{WP}$ pin. The $\overline{WP}$ pin is internally pulled-high and may be left floating if hardware controlled protection will not be used. However, it is recommended that the $\overline{WP}$ pin also be externally connected to V_{CC} whenever possible.	Low	Input
$\overline{HOLD}$	**HOLD:** The $\overline{HOLD}$ pin is used to temporarily pause serial communication without deselecting or resetting the device. While the $\overline{HOLD}$ pin is asserted, transitions on the SCK pin and data on the SI pin will be ignored, and the SO pin will be in a high-impedance state. The $\overline{CS}$ pin must be asserted, and the SCK pin must be in the low state in order for a Hold condition to start. A Hold condition pauses serial communication only and does not have an effect on internally self-timed operations such as a program or erase cycle. Please refer to "Hold" on page 35 for additional details on the Hold operation.The $\overline{HOLD}$ pin is internally pulled-high and may be left floating if the Hold function will not be used. However, it is recommended that the $\overline{HOLD}$ pin also be externally connected to V_{CC} whenever possible.	Low	Input
V_{CC}	**DEVICE POWER SUPPLY:** The V_{CC} pin is used to supply the source voltage to the device. Operations at invalid V_{CC} voltages may produce spurious results and should not be attempted.	-	Power
GND	**GROUND:** The ground reference for the power supply. GND should be connected to the system ground.	-	Power

Table 2-2. Pinouts

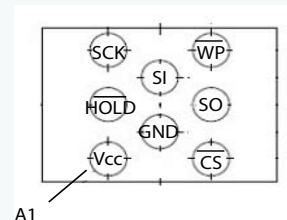**Figure 2-1.** 8-SOIC Top View

Figure 2-3. 8-UDFN (Top View)
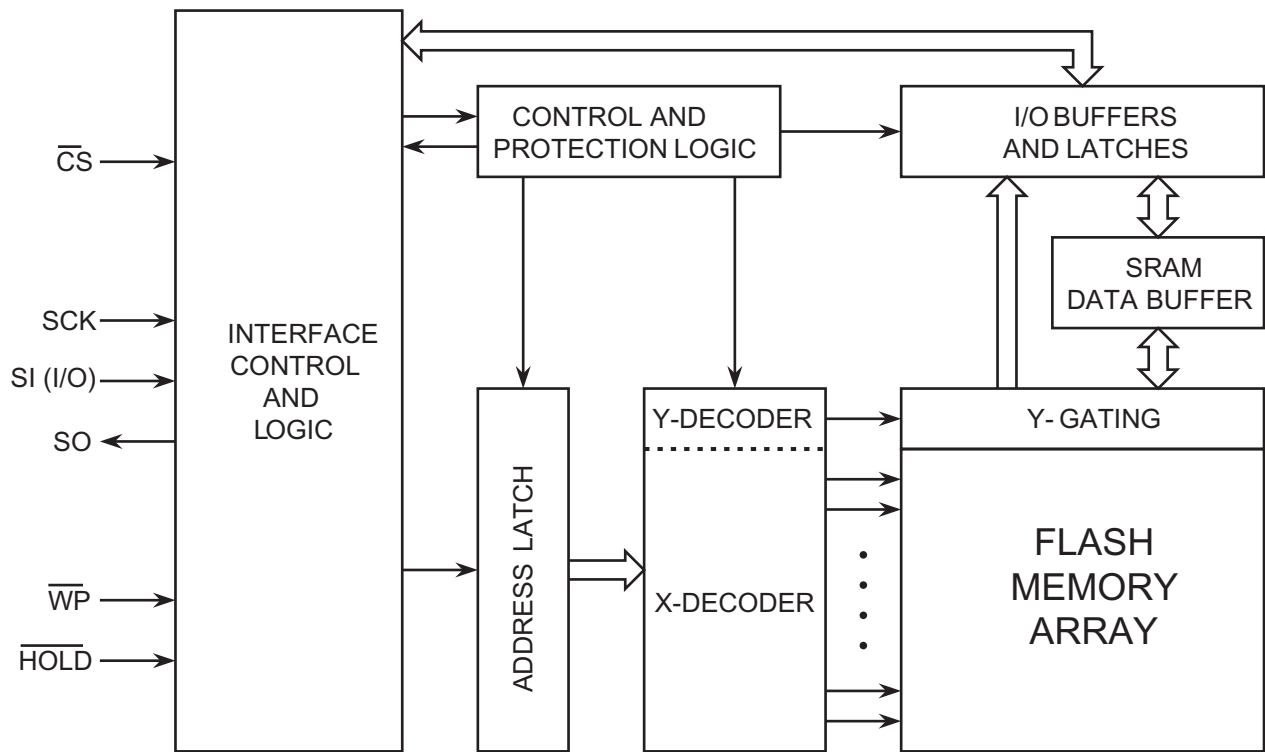

Figure 2-2. 8-TSSOP Top View
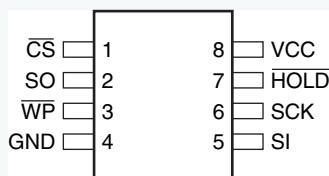
Figure 2-4. WLCSP Bottom View

3. Block Diagram

Figure 3-1. Block Diagram

4. Memory Array

To provide the greatest flexibility, the memory array of the AT25XE021A can be erased in three levels of granularity including a full chip erase. The size of the erase blocks is optimized for both code and data storage applications, allowing both code and data segments to reside in their own erase regions. The Memory Architecture Diagram illustrates the breakdown of each erase level.

**Figure 4-1. Memory Architecture Diagram**

Block Erase Detail

Internal Sectoring for Sector Protection Function	64KB Block Erase (D8h Command)	32KB Block Erase (52h Command)	4KB Block Erase (20h Command)	Block Address Range
64KB (Sector 3)	64KB	32KB	4KB	03FFFFh − 03F000h
			4KB	03EFFFh − 03E000h
			4KB	03DFFFh − 03D000h
			4KB	03CFFFh − 03C000h
			4KB	03BFFFh − 03B000h
			4KB	03AFFFh − 03A000h
			4KB	039FFFh − 039000h
			4KB	038FFFh − 038000h
		32KB	4KB	037FFFh − 037000h
			4KB	036FFFh − 036000h
			4KB	035FFFh − 035000h
			4KB	034FFFh − 034000h
			4KB	033FFFh − 033000h
			4KB	032FFFh − 032000h
			4KB	031FFFh − 031000h
			4KB	030FFFh − 030000h
64KB (Sector 2)	64KB	32KB	4KB	02FFFFh − 02F000h
			4KB	02EFFFh − 02E000h
			4KB	02DFFFh − 02D000h
			4KB	02CFFFh − 02C000h
			4KB	02BFFFh − 02B000h
			4KB	02AFFFh − 02A000h
			4KB	029FFFh − 029000h
			4KB	028FFFh − 028000h
		32KB	4KB	027FFFh − 027000h
			4KB	026FFFh − 026000h
			4KB	025FFFh − 025000h
			4KB	024FFFh − 024000h
			4KB	023FFFh − 023000h
			4KB	022FFFh − 022000h
			4KB	021FFFh − 021000h
			4KB	020FFFh − 020000h
⋮	⋮	⋮	⋮	
64KB (Sector 0)	64KB	32KB	4KB	00FFFFh − 00F000h
			4KB	00EFFFh − 00E000h
			4KB	00DFFFh − 00D000h
			4KB	00CFFFh − 00C000h
			4KB	00BFFFh − 00B000h
			4KB	00AFFFh − 00A000h
			4KB	009FFFh − 009000h
			4KB	008FFFh − 008000h
		32KB	4KB	007FFFh − 007000h
			4KB	006FFFh − 006000h
			4KB	005FFFh − 005000h
			4KB	004FFFh − 004000h
			4KB	003FFFh − 003000h
			4KB	002FFFh − 002000h
			4KB	001FFFh − 001000h
			4KB	000FFFh − 000000h

Page Program Detail

1-256 Byte Page Program (02h Command)	Page Address Range
256 Bytes	03FFFFh − 03FF00h
256 Bytes	03FEFFh − 03FE00h
256 Bytes	03FDFFh − 03FD00h
256 Bytes	03FCFFh − 03FC00h
256 Bytes	03FBFFh − 03FB00h
256 Bytes	03FAFFh − 03FA00h
256 Bytes	03F9FFh − 03F900h
256 Bytes	03F8FFh − 03F800h
256 Bytes	03F7FFh − 03F700h
256 Bytes	03F6FFh − 03F600h
256 Bytes	03F5FFh − 03F500h
256 Bytes	03F4FFh − 03F400h
256 Bytes	03F3FFh − 03F300h
256 Bytes	03F2FFh − 03F200h
256 Bytes	03F1FFh − 03F100h
256 Bytes	03F0FFh − 03F000h
256 Bytes	03EFFFh − 03EF00h
256 Bytes	03EEFFh − 03EE00h
256 Bytes	03EDFFh − 03ED00h
256 Bytes	03ECFFh − 03EC00h
256 Bytes	03EBFFh − 03EB00h
256 Bytes	03EAFFh − 03EA00h
256 Bytes	03E9FFh − 03E900h
256 Bytes	03E8FFh − 03E800h
⋮	
256 Bytes	0017FFh − 001700h
256 Bytes	0016FFh − 001600h
256 Bytes	0015FFh − 001500h
256 Bytes	0014FFh − 001400h
256 Bytes	0013FFh − 001300h
256 Bytes	0012FFh − 001200h
256 Bytes	0011FFh − 001100h
256 Bytes	0010FFh − 001000h
256 Bytes	000FFFh − 000F00h
256 Bytes	000EFFh − 000E00h
256 Bytes	000DFFh − 000D00h
256 Bytes	000CFFh − 000C00h
256 Bytes	000BFFh − 000B00h
256 Bytes	000AFFh − 000A00h
256 Bytes	0009FFh − 000900h
256 Bytes	0008FFh − 000800h
256 Bytes	0007FFh − 000700h
256 Bytes	0006FFh − 000600h
256 Bytes	0005FFh − 000500h
256 Bytes	0004FFh − 000400h
256 Bytes	0003FFh − 000300h
256 Bytes	0002FFh − 000200h
256 Bytes	0001FFh − 000100h
256 Bytes	0000FFh − 000000h

5. Device Operation

The AT25XE021A is controlled by a set of instructions that are sent from a host controller, commonly referred to as the SPI Master. The SPI Master communicates with the AT25XE021A via the SPI bus which is comprised of four signal lines: Chip Select ($\overline{CS}$), Serial Clock (SCK), Serial Input (SI), and Serial Output (SO).

The SPI protocol defines a total of four modes of operation (mode 0, 1, 2, or 3) with each mode differing in respect to the SCK polarity and phase and how the polarity and phase control the flow of data on the SPI bus. The AT25XE021A supports the two most common modes, SPI Modes 0 and 3. The only difference between SPI Modes 0 and 3 is the polarity of the SCK signal when in the inactive state (when the SPI Master is in standby mode and not transferring any data). With SPI Modes 0 and 3, data is always latched in on the rising edge of SCK and always output on the falling edge of SCK.

Figure 5-1. SPI Mode 0 and 3

$\overline{CS}$

SCK

SI   MSB   LSB

SO   MSB   LSB
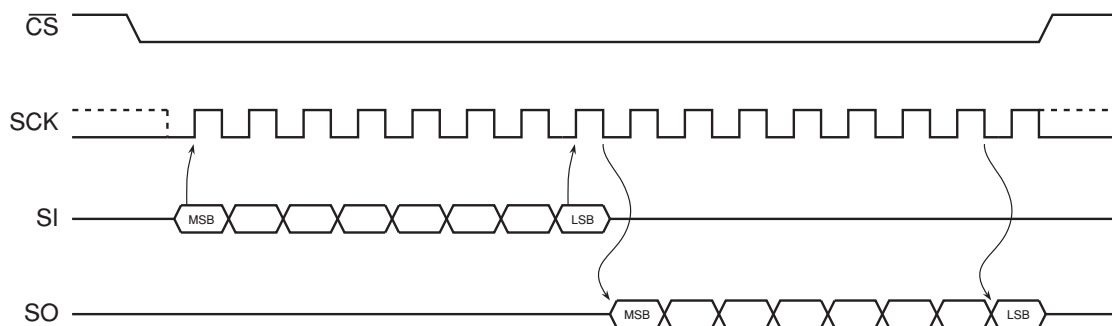
5.1 Dual Output Read

The AT25XE021A features a Dual-Output Read mode that allow two bits of data to be clocked out of the device every clock cycle to improve throughput. To accomplish this, both the SI and SO pins are utilized as outputs for the transfer of data bytes. With the Dual-Output Read Array command, the SI pin becomes an output along with the SO pin.

6. Commands and Addressing

A valid instruction or operation must always be started by first asserting the $\overline{CS}$ pin. After the $\overline{CS}$ pin has been asserted, the host controller must then clock out a valid 8-bit opcode on the SPI bus. Following the opcode, instruction dependent information such as address and data bytes would then be clocked out by the host controller. All opcode, address, and data bytes are transferred with the most-significant bit (MSB) first. An operation is ended by deasserting the $\overline{CS}$ pin.

Opcodes not supported by the AT25XE021A will be ignored by the device and no operation will be started. The device will continue to ignore any data presented on the SI pin until the start of the next operation ($\overline{CS}$ pin being deasserted and then reasserted). In addition, if the $\overline{CS}$ pin is deasserted before complete opcode and address information is sent to the device, then no operation will be performed and the device will simply return to the idle state and wait for the next operation.

Addressing of the device requires a total of three bytes of information to be sent, representing address bits A23-A0. Since the upper address limit of the AT25XE021A memory array is 03FFFFh, address bits A23-A18 are always ignored by the device.

Table 6-1.   Command Listing

Command		Opcode		Clock Frequency	Address Bytes	Dummy Bytes	Data Bytes
Read Commands							
Read Array		0Bh	0000 1011	Up to 70MHz	3	1	1+
		03h	0000 0011	Up to 25MHz	3	0	1+
Dual Output Read		3Bh	0011 1011	Up to 40MHz	3	1	1+
Program and Erase Commands							
Page Erase		81h	1000 0001	Up to 70MHz	3	0	0
Block Erase (4 Kbytes)		20h	0010 0000	Up to 70MHz	3	0	0
Block Erase (32 Kbytes)		52h	0101 0010	Up to 70MHz	3	0	0
Block Erase (64 Kbytes)		D8h	1101 1000	Up to 70MHz	3	0	0
Chip Erase		60h	0110 0000	Up to 70MHz	0	0	0
		C7h	1100 0111	Up to 70MHz	0	0	0
Byte/Page Program (1 to 256 Bytes)		02h	0000 0010	Up to 70MHz	3	0	1+
Sequential Program Mode		ADh	1010 1101	Up to 70MHz	3, 0 [1]	0	1
		AFh	1010 1111	Up to 70MHz	3, 0 [1]	0	1
Dual-Input Byte/Page Program (1 to 256 bytes)		A2h	1010 0010	Up to 70MHz	3	0	1+
Protection Commands							
Write Enable		06h	0000 0110	Up to 70MHz	0	0	0
Write Disable		04h	0000 0100	Up to 70MHz	0	0	0
Protect Sector		36h	0011 0110	Up to 70MHz	3	0	0
Unprotect Sector		39h	0011 1001	Up to 70MHz	3	0	0
Read Sector Protection Registers		3Ch	0011 1100	Up to 70MHz	3	0	1+
Security Commands							
Program OTP Security Register		9Bh	1001 1011	Up to 70MHz	3	0	1+
Read OTP Security Register		77h	0111 0111	Up to 70MHz	3	2	1+
Status Register Commands							
Read Status Register		05h	0000 0101	Up to 70MHz	0	0	1+
Active Status Interrupt		25h	0010 0101	Up to 70MHz	0	1	0
Write Status Register Byte 1		01h	0000 0001	Up to 70MHz	0	0	1
Write Status Register Byte 2		31h	0011 0001	Up to 70MHz	0	0	1
Miscellaneous Commands							
Reset		F0h	1111 0000	Up to 70MHz	0	0	1(D0h)

Table 6-1.   Command Listing

Command	Opcode		Clock Frequency	Address Bytes	Dummy Bytes	Data Bytes
Read Manufacturer and Device ID	9Fh	1001 1111	Up to 70MHz	0	0	1 to 4
Deep Power-Down	B9h	1011 1001	Up to 70MHz	0	0	0
Resume from Deep Power-Down	ABh	1010 1011	Up to 70MHz	0	0	0
Ultra Deep Power-Down	79h	0111 1001	Up to 70MHz	0	0	0

1.   Three address bytes are required for the first operation to designate the address to start programming. Afterwards, the internal address counter automatically increments, so subsequent Sequential Program Mode operations only require clocking in of the opcode and the data byte until the Sequential Program Mode has been exited.

7.   Read Commands

7.1   Read Array

The Read Array command can be used to sequentially read a continuous stream of data from the device by simply providing the clock signal once the initial starting address is specified. The device incorporates an internal address counter that automatically increments every clock cycle.

Two opcodes (0Bh and 03h) can be used for the Read Array command. The use of each opcode depends on the maximum clock frequency that will be used to read data from the device. The 0Bh opcode can be used at any clock frequency up to the maximum specified by f_{CLK}, and the 03h opcode can be used for lower frequency read operations up to the maximum specified by f_{RDLF}.

To perform the Read Array operation, the $\overline{CS}$ pin must first be asserted and the appropriate opcode (0Bh or 03h) must be clocked into the device. After the opcode has been clocked in, the three address bytes must be clocked in to specify the starting address location of the first byte to read within the memory array. Following the three address bytes, an additional dummy byte needs to be clocked into the device if the 0Bh opcode is used for the Read Array operation.

After the three address bytes (and the dummy byte if using opcode 0Bh) have been clocked in, additional clock cycles will result in data being output on the SO pin. The data is always output with the MSB of a byte first. When the last byte (03FFFFh) of the memory array has been read, the device will continue reading back at the beginning of the array (000000h). No delays will be incurred when wrapping around from the end of the array to the beginning of the array.

Deasserting the $\overline{CS}$ pin will terminate the read operation and put the SO pin into high-impedance state. The $\overline{CS}$ pin can be deasserted at any time and does not require a full byte of data be read.

Figure 7-1.   Read Array - 03h Opcode
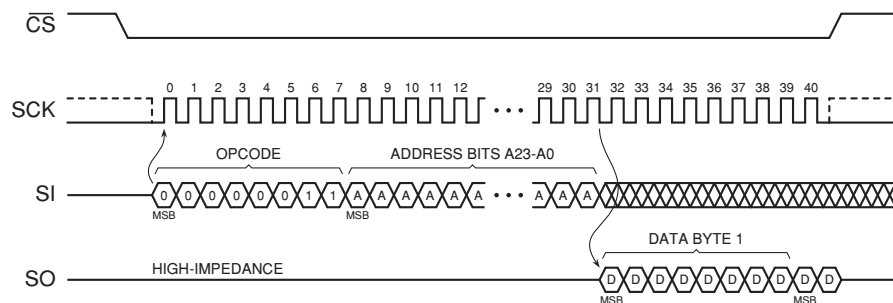
**Figure 7-2. Read Array - 0Bh Opcode**
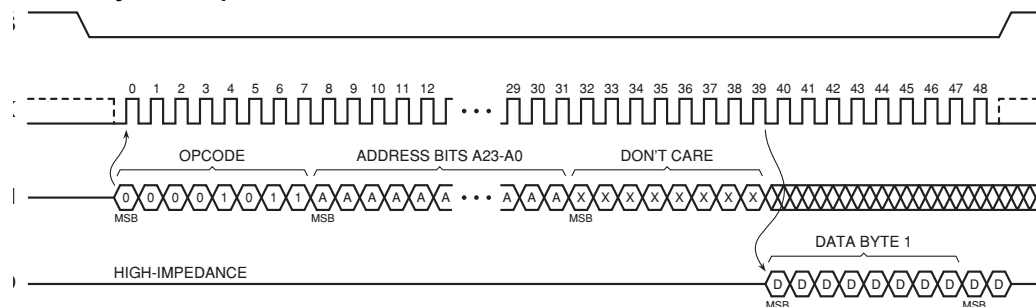
7.2 Dual-Output Read Array

The Dual-Output Read Array command is similar to the standard Read Array command and can be used to sequentially read a continuous stream of data from the device by simply providing the clock signal once the initial starting address has been specified. Unlike the standard Read Array command, however, the Dual-Output Read Array command allows two bits of data to be clocked out of the device on every clock cycle, rather than just one.

The Dual-Output Read Array command can be used at any clock frequency, up to the maximum specified by f_{RDDO}. To perform the Dual-Output Read Array operation, the $\overline{CS}$ pin must first be asserted and then the opcode 3Bh must be clocked into the device. After the opcode has been clocked in, the three address bytes must be clocked in to specify the location of the first byte to read within the memory array. Following the three address bytes, a single dummy byte must also be clocked into the device.

After the three address bytes and the dummy byte have been clocked in, additional clock cycles will result in data being output on both the SO and SI pins. The data is always output with the MSB of a byte first and the MSB is always output on the SO pin. During the first clock cycle, bit seven of the first data byte is output on the SO pin, while bit six of the same data byte is output on the SIO pin. During the next clock cycle, bits five and four of the first data byte are output on the SO and SIO pins, respectively. The sequence continues with each byte of data being output after every four clock cycles. When the last byte (03FFFFh) of the memory array has been read, the device will continue reading from the beginning of the array (000000h). No delays will be incurred when wrapping around from the end of the array to the beginning of the array.Deasserting the $\overline{CS}$ pin will terminate the read operation and put the SO and SI pins into a high-impedance state. The $\overline{CS}$ pin can be deasserted at any time and does not require that a full byte of data be read.

Figure 7-3. Dual-Output Read Array
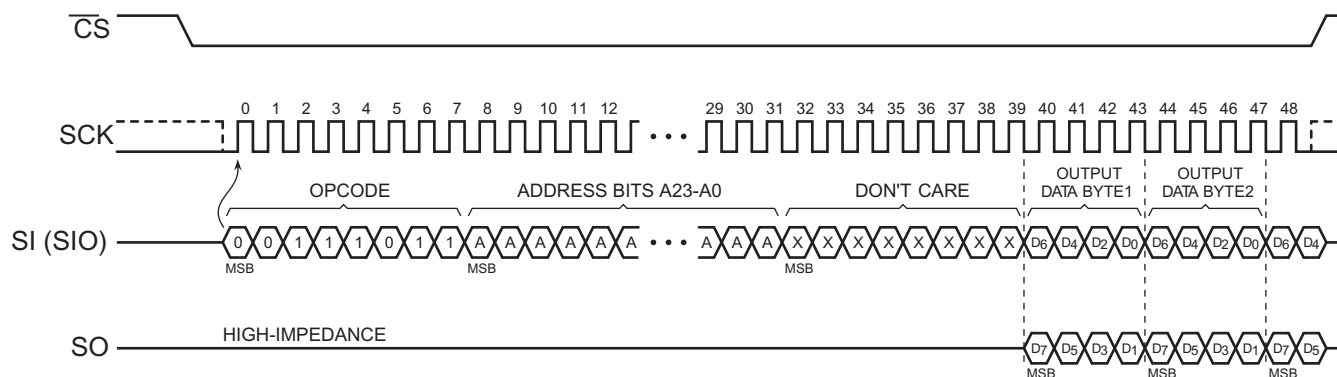
8.   Program and Erase Commands

8.1   Byte/Page Program

The Byte/Page Program command allows anywhere from a single byte of data to 256 bytes of data to be programmed into previously erased memory locations. An erased memory location is one that has all eight bits set to the logical "1" state (a byte value of FFh). Before a Byte/Page Program command can be started, the Write Enable command must have been previously issued to the device (see "Write Enable" on page 17) to set the Write Enable Latch (WEL) bit of the Status Register to a logical "1" state.

To perform a Byte/Page Program command, an opcode of 02h must be clocked into the device followed by the three address bytes denoting the first byte location of the memory array to begin programming at. After the address bytes have been clocked in, data can then be clocked into the device and will be stored in an internal buffer.

If the starting memory address denoted by A23-A0 does not fall on an even 256-byte page boundary (A7-A0 are not all 0), then special circumstances regarding which memory locations to be programmed will apply. In this situation, any data that is sent to the device that goes beyond the end of the page will wrap around back to the beginning of the same page. For example, if the starting address denoted by A23-A0 is 0000FEh, and three bytes of data are sent to the device, then the first two bytes of data will be programmed at addresses 0000FEh and 0000FFh while the last byte of data will be programmed at address 000000h. The remaining bytes in the page (addresses 000001h through 0000FDh) will not be programmed and will remain in the erased state (FFh). In addition, if more than 256 bytes of data are sent to the device, then only the last 256 bytes sent will be latched into the internal buffer.

When the $\overline{CS}$ pin is deasserted, the device will take the data stored in the internal buffer and program it into the appropriate memory array locations based on the starting address specified by A23-A0 and the number of data bytes sent to the device. If less than 256 bytes of data were sent to the device, then the remaining bytes within the page will not be programmed and will remain in the erased state (FFh). The programming of the data bytes is internally self-timed and should take place in a time of t_{PP} or t_{BP} if only programming a single byte.

The three address bytes and at least one complete byte of data must be clocked into the device before the $\overline{CS}$ pin is deasserted, and the $\overline{CS}$ pin must be deasserted on even byte boundaries (multiples of eight bits); otherwise, the device will abort the operation and no data will be programmed into the memory array. In addition, if the memory is in the protected state (see "Protect Sector" on page 19), then the Byte/Page Program command will not be executed, and the device will return to the idle state once the $\overline{CS}$ pin has been deasserted. The WEL bit in the Status Register will be reset back to the logical "0" state if the program cycle aborts due to an incomplete address being sent, an incomplete byte of data being sent, the $\overline{CS}$ pin being deasserted on uneven byte boundaries, or because the memory location to be programmed is protected.

While the device is programming, the Status Register can be read and will indicate that the device is busy. For faster throughput, it is recommended that the Status Register be polled rather than waiting the t_{BP} or t_{PP} time to determine if the data bytes have finished programming. For fastest throughput and least power consumption, it is recommended that the Active Status Interrupt command 25h be used. After the initial 16 clks, no more clocks are required. Once the BUSY cycle is done, SO will be driven low immediately to signal the device has finished programming.At some point before the program cycle completes, the WEL bit in the Status Register will be reset back to the logical "0" state.

The device also incorporates an intelligent programming algorithm that can detect when a byte location fails to program properly. If a programming error arises, it will be indicated by the EPE bit in the Status Register.

Figure 8-1. Byte Program
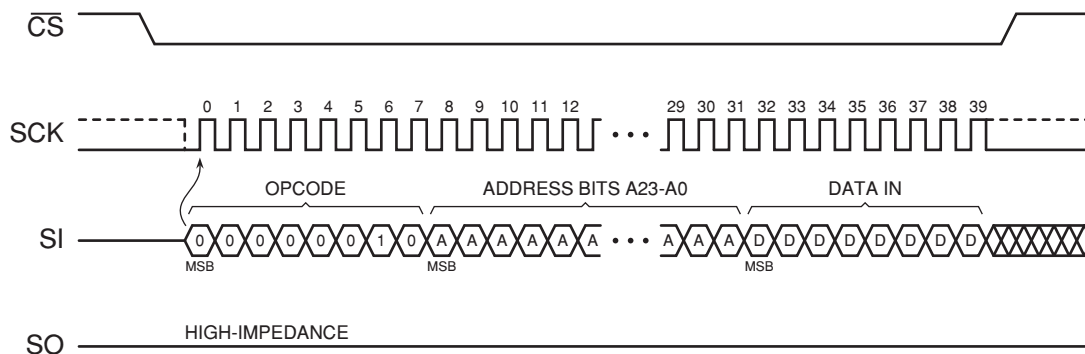
Figure 8-2.   Page Program
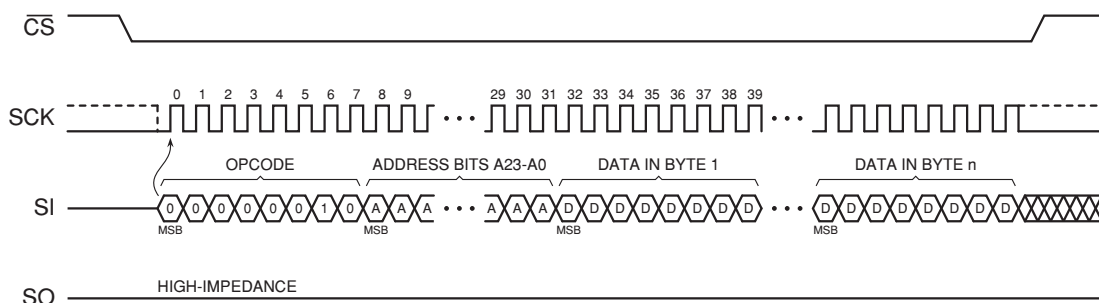
8.2   Dual-Input Byte/Page Program

The Dual-Input Byte/Page Program command is similar to the standard Byte/Page Program command and can be used to program anywhere from a single byte of data up to 256 bytes of data into previously erased memory locations. Unlike the standard Byte/Page Program command, however, the Dual-Input Byte/Page Program command allows two bits of data to be clocked into the device on every clock cycle rather than just one.

Before the Dual-Input Byte/Page Program command can be started, the Write Enable command must have been previously issued to the device (see "Write Enable" on page 17) to set the Write Enable Latch (WEL) bit of the Status Register to a Logical 1 state. To perform a Dual-Input Byte/Page Program command, an A2h opcode must be clocked into the device followed by the three address bytes denoting the first location of the memory array to begin programming at. After the address bytes have been clocked in, data can then be clocked into the device two bits at a time on both the SO and SI pins.

The data is always input with the MSB of a byte first, and the MSB is always input on the SO pin. During the first clock cycle, bit seven of the first data byte is input on the SO pin while bit six of the same data byte is input on the SI pin. During the next clock cycle, bits five and four of the first data byte are input on the SO and SI pins, respectively. The sequence continues with each byte of data being input after every four clock cycles. Like the standard Byte/Page Program command, all data clocked into the device are stored in an internal buffer.

If the starting memory address denoted by A23-A0 does not fall on an even 256-byte page boundary (A7-A0 are not all 0), then special circumstances regarding which memory locations are to be programmed will apply. In this situation, any data that are sent to the device that go beyond the end of the page will wrap around to the beginning of the same page. In addition, if more than 256 bytes of data is sent to the device, then only the last 256 bytes sent will be latched into the internal buffer.

Example: If the starting address denoted by A23-A0 is 0000FEh and three bytes of data are sent to the device, then the first two bytes of data will be programmed at addresses 0000FEh and 0000FFh, while the last byte of

data will be programmed at address 000000h. The remaining bytes in the page (addresses 000001h through 0000FDh) will not be programmed and will remain in the erased state (FFh).

When the $\overline{CS}$ pin is deasserted, the device will program the data stored in the internal buffer into the appropriate memory array locations based on the starting address specified by A23-A0 and the number of data bytes sent to the device. If fewer than 256 bytes of data is sent to the device, then the remaining bytes within the page will not be programmed and will remain in the erased state (FFh). The programming of the data bytes is internally self-timed and should take place in a time of t_{PP} or t_{BP} if only programming a page ($t_{PP)}$ or a single byte ($t_{BP)}$.

The three address bytes and at least one complete byte of data must be clocked into the device before the $\overline{CS}$ pin is deasserted, and the $\overline{CS}$ pin must be deasserted on even byte boundaries (multiples of eight bits); otherwise, the device will abort the operation and no data will be programmed into the memory array. In addition, if the address specified by A23-A0 points to a memory location within a sector that is in the protected state (see "Protect Sector" on page 19), then the Byte/Page Program command will not be executed and the device will return to the idle state once the $\overline{CS}$ pin has been deasserted. The WEL bit in the Status Register will be reset back to the Logical 0 state if the program cycle aborts due to an incomplete address being sent, an incomplete byte of data being sent, the $\overline{CS}$ pin being deasserted on uneven byte boundaries, or because the memory location to be programmed is protected or locked down.

While the device is programming, the Status Register can be read and will indicate that the device is busy. For faster throughput, it is recommended that the Status Register be polled rather than waiting the t_{BP} or t_{PP} time to determine if the data bytes have finished programming. For fastest throughput and least power consumption, it is recommended that the Active Status Interrupt command 25h be used. At some point before the program cycle completes, the WEL bit in the Status Register will be reset back to the Logical 0 state.
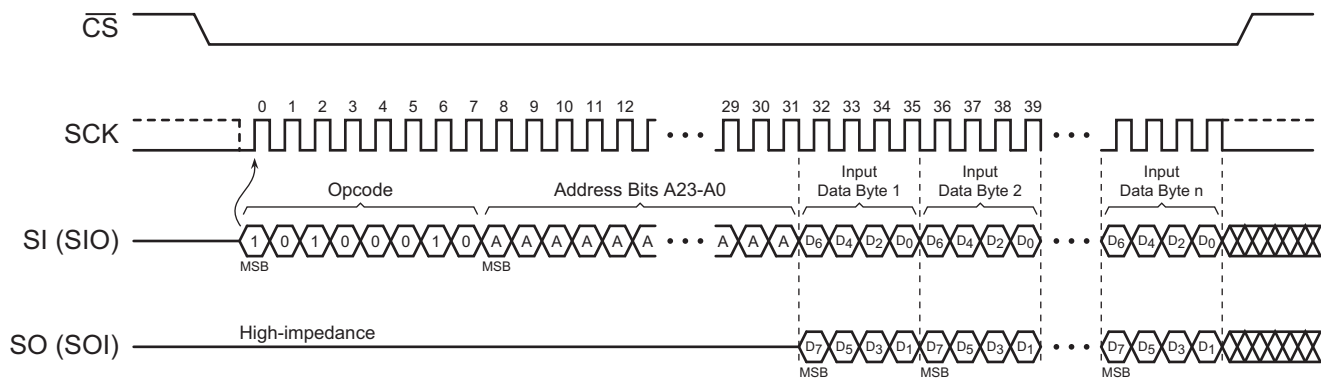
The device also incorporates an intelligent programming algorithm that can detect when a byte location fails to program properly. If a programming error arises, it will be indicated by the EPE bit in the Status Register.

Figure 8-3.   Dual-Input Byte Program
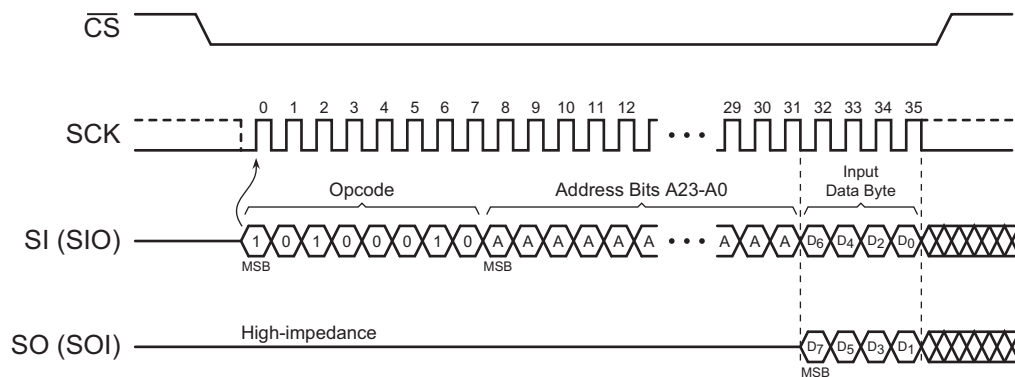
Figure 8-4.   Dual-Input Page Program

8.3   Sequential Program Mode

The Sequential Program Mode improves throughput over the Byte/Page Program command when the Byte/Page Program command is used to program single bytes only into consecutive address locations. For example, some systems may be designed to program only a single byte of information at a time and cannot utilize a buffered Page Program operation due to design restrictions. In such a case, the system would normally have to perform multiple Byte Program operations in order to program data into sequential memory locations. This approach can add considerable system overhead and SPI bus traffic.

The Sequential Programming Mode helps reduce system overhead and bus traffic by incorporating an internal address counter that keeps track of the byte location to program, thereby eliminating the need to supply an address sequence to the device for every byte to program. When using the Sequential Program mode, all address locations to be programmed must be in the erased state. Before the Sequential Program mode can first be entered, the Write Enable command must have been previously issued to the device to set the WEL bit of the Status Register to a logical "1" state.

To start the Sequential Program Mode, the $\overline{CS}$ pin must first be asserted, and either an opcode of ADh or AFh must be clocked into the device. For the first program cycle, three address bytes must be clocked in after the opcode to designate the first byte location to program. After the address bytes have been clocked in, the byte of data to be programmed can be sent to the device. Deasserting the $\overline{CS}$ pin will start the internally self-timed program operation, and the byte of data will be programmed into the memory location specified by A23 - A0.

After the first byte has been successfully programmed, a second byte can be programmed by simply reasserting the $\overline{CS}$ pin, clocking in the ADh or AFh opcode, and then clocking in the next byte of data. When the $\overline{CS}$ pin is deasserted, the second byte of data will be programmed into the next sequential memory location. The process would be repeated for any additional bytes. There is no need to reissue the Write Enable command once the Sequential Program Mode has been entered.

When the last desired byte has been programmed into the memory array, the Sequential Program Mode operation can be terminated by reasserting the $\overline{CS}$ pin and sending the Write Disable command to the device to reset the WEL bit in the Status Register back to the logical "0" state.

If more than one byte of data is ever clocked in during each program cycle, then only the last byte of data sent on the SI pin will be stored in the internal latches. The programming of each byte is internally self-timed and should take place in a time of t_{BP}. For each program cycle, a complete byte of data must be clocked into the device before the $\overline{CS}$ pin is deasserted, and the $\overline{CS}$ pin must be deasserted on even byte boundaries (multiples of eight bits); otherwise, the device will abort the operation, the byte of data will not be programmed into the memory array, and the WEL bit in the Status Register will be reset back to the logical "0" state.

If the address initially specified by A23 - A0 points to a memory location within a sector that is in the protected state, then the Sequential Program Mode command will not be executed, and the device will return to the idle state once the $\overline{CS}$ pin has been deasserted. The WEL bit in the Status Register will also be reset back to the logical "0" state.

There is no address wrapping when using the Sequential Program Mode. Therefore, when the last byte (03FFFFh) of the memory array has been programmed, the device will automatically exit the Sequential Program mode and reset the WEL bit in the Status Register back to the logical "0" state. In addition, the Sequential Program mode will not automatically skip over protected sectors; therefore, once the highest unprotected memory location in a programming sequence has been programmed, the device will automatically exit the Sequential Program mode and reset the WEL bit in the Status Register. For example, if Sector 1 was protected and Sector 0 was currently being programmed, once the last byte of Sector 0 was programmed, the Sequential Program mode would automatically end. To continue programming with Sector 2, the Sequential Program mode would have to be restarted by supplying the ADh or AFh opcode, the three address bytes, and the first byte of Sector 2 to program.

While the device is programming a byte, the Status Register can be read and will indicate that the device is busy. For faster throughput, it is recommended that the Status Register be polled at the end of each program cycle rather than waiting the t_{BP} time to determine if the byte has finished programming before starting the next Sequential Program mode cycle.

The device also incorporates an intelligent programming algorithm that can detect when a byte location fails to program properly. If a programming error arises, it will be indicated by the EPE bit in the Status Register.

Figure 8-5. Sequential Program Mode – Status Register Polling
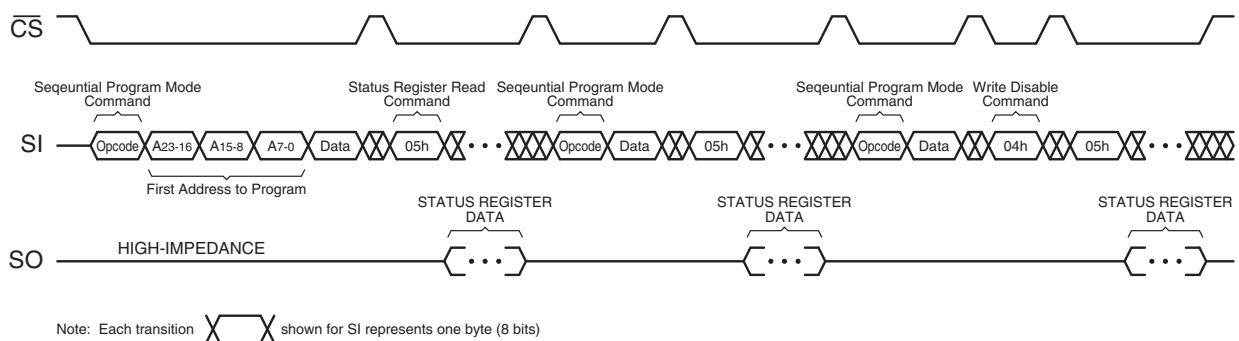
Figure 8-6. Sequential Program Mode – Waiting Maximum Byte Program Time
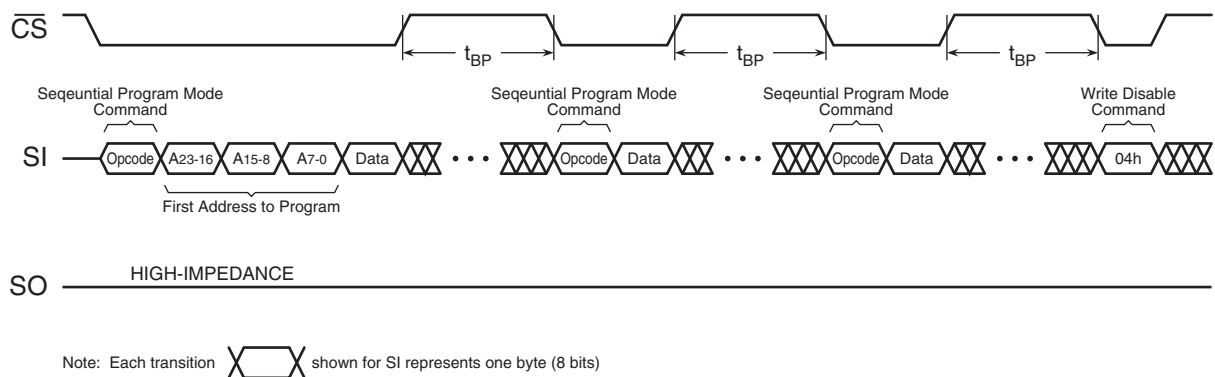
8.4   Page Erase

Page Erase for 2Mbit, 1024 Pages [ten (10) page address bits, PA<9:0>] of 256Bytes each.

The Page Erase command can be used to individually erase any page in the main memory array. The Main Memory Byte/Page Program command can be utilized at a later time.

To perform a Page Erase with the standard page size (256 bytes), an opcode of 81h must be clocked into the device followed by three address bytes comprised of:

Byte 0: 81h the page erase command code

Byte 1: XXXX XX, PA9, PA8; which is six (6) dummy bits and two (2) page address bits

Byte 2: PA<7:0>; which is eight (8) page address bits

Byte 3: XXXX XXXX; which is eight (8) dummy bits

When a low-to-high transition occurs on the $\overline{CS}$ pin, the device will erase the selected page (the erased state is a Logic 1). The erase operation is internally self-timed and should take place in a maximum time of t_{PE}. During this time, the $\overline{RDY}$/BUSY bit in the Status Register will indicate that the device is busy.

The device also incorporates an intelligent erase algorithm that can detect when a byte location fails to erase properly. If an erase error arises, it will be indicated by the EPE bit in the Status Register.

8.5   Block Erase

A block of 4, 32, or 64Kbytes can be erased (all bits set to the logical "1" state) in a single operation by using one of three different opcodes for the Block Erase command. An opcode of 20h is used for a 4-Kbyte erase, an opcode of 52h for a 32-Kbyte erase, and an opcode of D8h is used for a 64-Kbyte erase. Before a Block Erase command can be started, the Write Enable command must have been previously issued to the device to set the WEL bit of the Status Register to a logical "1" state.

To perform a Block Erase, the $\overline{CS}$ pin must first be asserted and the appropriate opcode (20h, 52h, or D8h) must be clocked into the device. After the opcode has been clocked in, the three address bytes specifying an address within the 4-, 32-, or 64-Kbyte block to be erased must be clocked in. Any additional data clocked into the device will be ignored. When the $\overline{CS}$ pin is deasserted, the device will erase the appropriate block. The erasing of the block is internally self-timed and should take place in a time of t_{BLKE}.

Since the Block Erase command erases a region of bytes, the lower order address bits do not need to be decoded by the device. Therefore, for a 4-Kbyte erase, address bits A11-A0 will be ignored by the device and their values can be either a logical "1" or "0". For a 32-Kbyte erase, address bits A14-A0 will be ignored by the device. For a 64-Kbyte erase, address bits A15-A0 will be ignored by the device. Despite the lower order address bits not being decoded by the device, the complete three address bytes must still be clocked into the device before the $\overline{CS}$ pin is deasserted, and the $\overline{CS}$ pin must be deasserted on an even byte boundary (multiples of eight bits); otherwise, the device will abort the operation and no erase operation will be performed.

If the memory is in the protected state, then the Block Erase command will not be executed, and the device will return to the idle state once the $\overline{CS}$ pin has been deasserted.

The WEL bit in the Status Register will be reset back to the logical "0" state if the erase cycle aborts due to an incomplete address being sent, the $\overline{CS}$ pin being deasserted on uneven byte boundaries, or because a memory location within the region to be erased is protected.

While the device is executing a successful erase cycle, the Status Register can be read and will indicate that the device is busy. For faster throughput, it is recommended that the Status Register be polled rather than waiting the t_{BLKE} time to determine if the device has finished erasing. At some point before the erase cycle completes, the WEL bit in the Status Register will be reset back to the logical "0" state.

For fastest throughput and least power consumption, it is recommended that the Active Status Interrupt command 25h be used. After the initial 16 clks, no more clocks are required. Once the BUSY cycle is done, SO will be driven low immediately to signal the device has finished erasing.

The device also incorporates an intelligent erase algorithm that can detect when a byte location fails to erase properly. If an erase error occurs, it will be indicated by the EPE bit in the Status Register.

Figure 8-7.   Block Erase
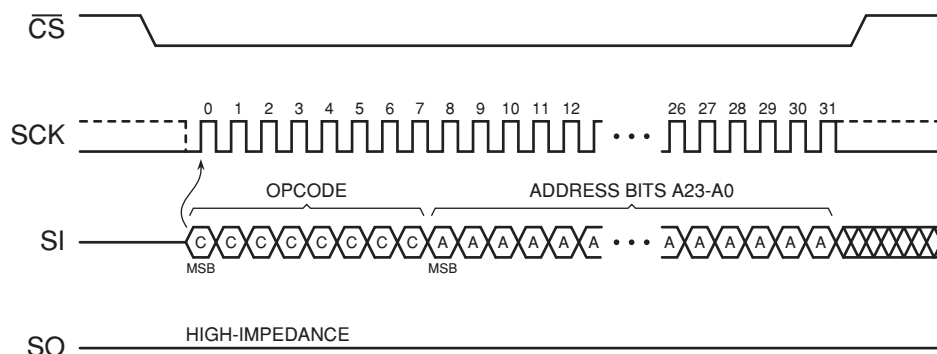
8.6   Chip Erase

The entire memory array can be erased in a single operation by using the Chip Erase command. Before a Chip Erase command can be started, the Write Enable command must have been previously issued to the device to set the WEL bit of the Status Register to a logical "1" state.

Two opcodes (60h and C7h) can be used for the Chip Erase command. There is no difference in device functionality when utilizing the two opcodes, so they can be used interchangeably. To perform a Chip Erase, one of the two opcodes must be clocked into the device. Since the entire memory array is to be erased, no address bytes need to be clocked into the device, and any data clocked in after the opcode will be ignored. When the $\overline{CS}$ pin is deasserted, the device will erase the entire memory array. The erasing of the device is internally self-timed and should take place in a time of t_{CHPE}.

The complete opcode must be clocked into the device before the $\overline{CS}$ pin is deasserted, and the $\overline{CS}$ pin must be deasserted on an even byte boundary (multiples of eight bits); otherwise, no erase will be performed. In addition, if any sector in the memory array is in the protected state, then the Chip Erase command will not be executed, and the device will return to the idle state once the $\overline{CS}$ pin has been deasserted. The WEL bit in the Status Register will be reset back to the logical "0" state if the $\overline{CS}$ pin is deasserted on uneven byte boundaries or if the memory is in the protected state.

While the device is executing a successful erase cycle, the Status Register can be read and will indicate that the device is busy. For faster throughput, it is recommended that the Status Register be polled rather than waiting the t_{CHPE} time to determine if the device has finished erasing. At some point before the erase cycle completes, the WEL bit in the Status Register will be reset back to the logical "0" state.

The device also incorporates an intelligent erase algorithm that can detect when a byte location fails to erase properly. If an erase error occurs, it will be indicated by the EPE bit in the Status Register.

Figure 8-8.   Chip Erase
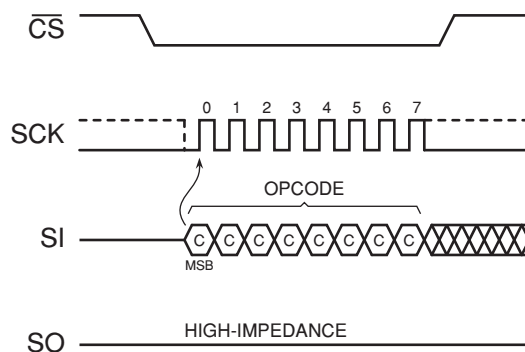
9. Protection Commands and Features

9.1 Write Enable

The Write Enable command is used to set the Write Enable Latch (WEL) bit in the Status Register to a logical "1" state. The WEL bit must be set before a Byte/Page Program, Erase, Program OTP Security Register, or Write Status Register command can be executed. This makes the issuance of these commands a two step process, thereby reducing the chances of a command being accidentally or erroneously executed. If the WEL bit in the Status Register is not set prior to the issuance of one of these commands, then the command will not be executed.

To issue the Write Enable command, the $\overline{CS}$ pin must first be asserted and the opcode of 06h must be clocked into the device. No address bytes need to be clocked into the device, and any data clocked in after the opcode will be ignored. When the $\overline{CS}$ pin is deasserted, the WEL bit in the Status Register will be set to a logical "1". The complete opcode must be clocked into the device before the $\overline{CS}$ pin is deasserted, and the $\overline{CS}$ pin must be deasserted on an even byte boundary (multiples of eight bits); otherwise, the device will abort the operation and the state of the WEL bit will not change.

Figure 9-1.   Write Enable
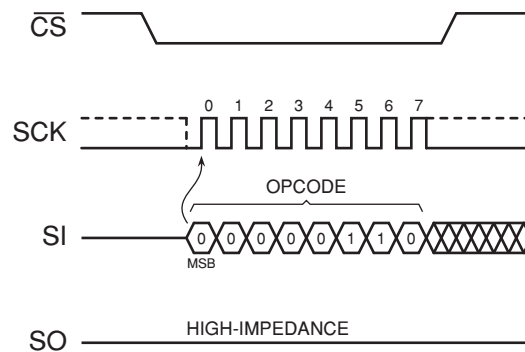
9.2 Write Disable

The Write Disable command is used to reset the Write Enable Latch (WEL) bit in the Status Register to the logical "0" state. With the WEL bit reset, all Byte/Page Program, Erase, Program OTP Security Register, and Write Status Register commands will not be executed. Other conditions can also cause the WEL bit to be reset; for more details, refer to the WEL bit section of the Status Register description.

To issue the Write Disable command, the $\overline{CS}$ pin must first be asserted and the opcode of 04h must be clocked into the device. No address bytes need to be clocked into the device, and any data clocked in after the opcode will be ignored. When the $\overline{CS}$ pin is deasserted, the WEL bit in the Status Register will be reset to a logical "0". The complete opcode must be clocked into the device before the $\overline{CS}$ pin is deasserted, and the $\overline{CS}$ pin must be deasserted on an even byte boundary (multiples of eight bits); otherwise, the device will abort the operation and the state of the WEL bit will not change.
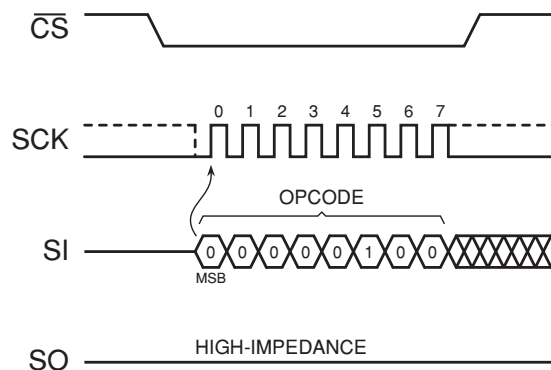
Figure 9-2. Write Disable

9.3 Protect Sector

Every physical sector of the device has a corresponding single-bit Sector Protection Register that is used to control the software protection of a sector. Upon device power-up or after a device reset, each Sector Protection Register will default to the logical "1" state indicating that all sectors are protected and cannot be programmed or erased.

Issuing the Protect Sector command to a particular sector address will set the corresponding Sector Protection Register to the logical "1" state. The following table outlines the two states of the Sector Protection Registers.
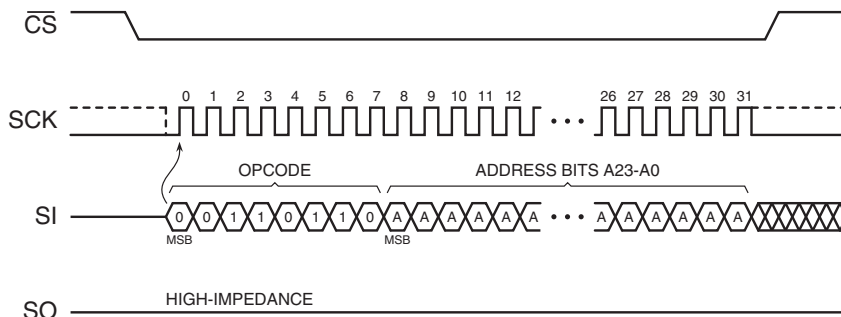
Table 9-1. Sector Protection Register Values

Value	Sector Protection Status
0	Sector is unprotected and can be programmed and erased.
1	Sector is protected and cannot be programmed or erased. This is the default state.

Before the Protect Sector command can be issued, the Write Enable command must have been previously issued to set the WEL bit in the Status Register to a logical "1". To issue the Protect Sector command, the $\overline{CS}$ pin must first be asserted and the opcode of 36h must be clocked into the device followed by three address bytes designating any address within the sector to be protected. Any additional data clocked into the device will be ignored. When the $\overline{CS}$ pin is deasserted, the Sector Protection Register corresponding to the physical sector addressed by A23 - A0 will be set to the logical "1" state, and the sector itself will then be protected from program and erase operations. In addition, the WEL bit in the Status Register will be reset back to the logical "0" state.

The complete three address bytes must be clocked into the device before the $\overline{CS}$ pin is deasserted, and the $\overline{CS}$ pin must be deasserted on an even byte boundary (multiples of eight bits); otherwise, the device will abort the operation, the state of the Sector Protection Register will be unchanged, and the WEL bit in the Status Register will be reset to a logical "0".

As a safeguard against accidental or erroneous protecting or unprotecting of sectors, the Sector Protection Registers can themselves be locked from updates by using the SPRL (Sector Protection Registers Locked) bit of the Status Register (please refer to the Status Register description for more details). If the Sector Protection Registers are locked, then any attempts to issue the Protect Sector command will be ignored, and the device will reset the WEL bit in the Status Register back to a logical "0" and return to the idle state once the $\overline{CS}$ pin has been deasserted.

Figure 9-3.   Protect Sector

CS

SCK   0 1 2 3 4 5 6 7 8 9 10 11 12   26 27 28 29 30 31

OPCODE   ADDRESS BITS A23-A0

SI   0 0 1 1 0 1 1 0 A A A A A A A • • • A A A A A A A
      MSB   MSB

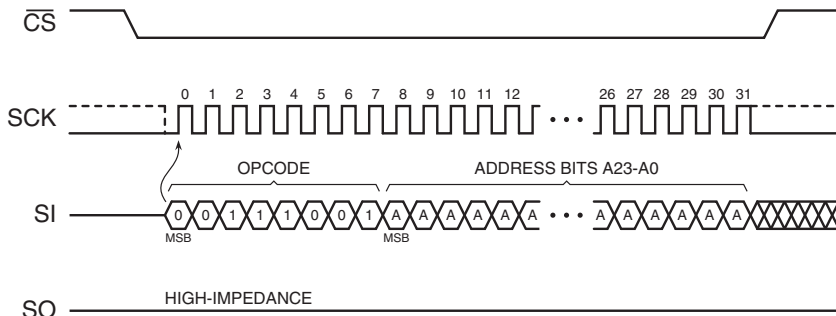SO   HIGH-IMPEDANCE

9.4   Unprotect Sector

Issuing the Unprotect Sector command to a particular sector address will reset the corresponding Sector Protection Register to the logical "0" state (see Table 9-1 for Sector Protection Register values). Every physical sector of the device has a corresponding single-bit Sector Protection Register that is used to control the software protection of a sector.

Before the Unprotect Sector command can be issued, the Write Enable command must have been previously issued to set the WEL bit in the Status Register to a logical "1". To issue the Unprotect Sector command, the CS pin must first be asserted and the opcode of 39h must be clocked into the device. After the opcode has been clocked in, the three address bytes designating any address within the sector to be unlocked must be clocked in. Any additional data clocked into the device after the address bytes will be ignored. When the CS pin is deasserted, the Sector Protection Register corresponding to the sector addressed by A23 - A0 will be reset to the logical "0" state, and the sector itself will be unprotected. In addition, the WEL bit in the Status Register will be reset back to the logical "0" state.

The complete three address bytes must be clocked into the device before the CS pin is deasserted, and the CS pin must be deasserted on an even byte boundary (multiples of eight bits); otherwise, the device will abort the operation, the state of the Sector Protection Register will be unchanged, and the WEL bit in the Status Register will be reset to a logical "0".

As a safeguard against accidental or erroneous locking or unlocking of sectors, the Sector Protection Registers can themselves be locked from updates by using the SPRL (Sector Protection Registers Locked) bit of the Status Register (please refer to the Status Register description for more details). If the Sector Protection Registers are locked, then any attempts to issue the Unprotect Sector command will be ignored, and the device will reset the WEL bit in the Status Register back to a logical "0" and return to the idle state once the CS pin has been deasserted.

Figure 9-4.   Unprotect Sector

CS

SCK   0 1 2 3 4 5 6 7 8 9 10 11 12   26 27 28 29 30 31

OPCODE   ADDRESS BITS A23-A0

SI   0 0 1 1 1 0 0 1 A A A A A A A • • • A A A A A A A
      MSB   MSB

SO   HIGH-IMPEDANCE

9.5   Global Protect/Unprotect

The Global Protect and Global Unprotect features can work in conjunction with the Protect Sector and Unprotect Sector functions. For example, a system can globally protect the entire memory array and then use the Unprotect Sector command to individually unprotect certain sectors and individually reprotect them later by using the Protect Sector command. Likewise, a system can globally unprotect the entire memory array and then individually protect certain sectors as needed.

Performing a Global Protect or Global Unprotect is accomplished by writing a certain combination of data to the Status Register using the Write Status Register command (see "Write Status Register" section on for command execution details). The Write Status Register command is also used to modify the SPRL (Sector Protection Registers Locked) bit to control hardware and software locking.

To perform a Global Protect, the appropriate $\overline{WP}$ pin and SPRL conditions must be met, and the system must write a logical "1" to bits 5, 4, 3, and 2 of the Status Register. Conversely, to perform a Global Unprotect, the same $\overline{WP}$ and SPRL conditions must be met but the system must write a logical "0" to bits 5, 4, 3, and 2 of the Status Register. Table 9-2 details the conditions necessary for a Global Protect or Global Unprotect to be performed.

Table 9-2.   Valid SPRL and Global Protect/Unprotect Conditions

$\overline{WP}$ State	Current SPRL Value	New Write Status Register Data Bit 7 6 5 4 3 2 1 0	Protection Operation	New SPRL Value
0	0	0 x 0 0 0 0 x x 0 x 0 0 0 1 x x ? 0 x 1 1 1 0 x x 0 x 1 1 1 1 x x 1 x 0 0 0 0 x x 1 x 0 0 0 1 x x ? 1 x 1 1 1 0 x x 1 x 1 1 1 1 x x	Global Unprotect – all Sector Protection Registers reset to 0 No change to current protection. No change to current protection. No change to current protection. Global Protect – all Sector Protection Registers set to 1 Global Unprotect – all Sector Protection Registers reset to 0 No change to current protection. No change to current protection. No change to current protection. Global Protect – all Sector Protection Registers set to 1	0 0 0 0 0 1 1 1 1 1
0	1	x x x x x x x x	No change to the current protection level. All sectors currently protected will remain protected and all sectors currently unprotected will remain unprotected. The Sector Protection Registers are hard-locked and cannot be changed when the $\overline{WP}$ pin is LOW and the current state of SPRL is 1. Therefore, a Global Protect/Unprotect will not occur. In addition, the SPRL bit cannot be changed (the $\overline{WP}$ pin must be HIGH in order to change SPRL back to a 0).	
1	0	0 x 0 0 0 0 x x 0 x 0 0 0 1 x x ? 0 x 1 1 1 0 x x 0 x 1 1 1 1 x x 1 x 0 0 0 0 x x 1 x 0 0 0 1 x x ? 1 x 1 1 1 0 x x 1 x 1 1 1 1 x x	Global Unprotect – all Sector Protection Registers reset to 0 No change to current protection. No change to current protection. No change to current protection. Global Protect – all Sector Protection Registers set to 1 Global Unprotect – all Sector Protection Registers reset to 0 No change to current protection. No change to current protection. No change to current protection. Global Protect – all Sector Protection Registers set to 1	0 0 0 0 0 1 1 1 1 1
1	1	0 x 0 0 0 0 x x 0 x 0 0 0 1 x x ? 0 x 1 1 1 0 x x 0 x 1 1 1 1 x x 1 x 0 0 0 0 x x 1 x 0 0 0 1 x x ? 1 x 1 1 1 0 x x 1 x 1 1 1 1 x x	No change to the current protection level. All sectors currently protected will remain protected, and all sectors currently unprotected will remain unprotected. The Sector Protection Registers are soft-locked and cannot be changed when the current state of SPRL is 1. Therefore, a Global Protect/Unprotect will not occur. However, the SPRL bit can be changed back to a 0 from a 1 since the $\overline{WP}$ pin is HIGH. To perform a Global Protect/Unprotect, the Write Status Register command must be issued again after the SPRL bit has been changed from a 1 to a 0.	0 0 0 0 0 1 1 1 1 1

Essentially, if the SPRL bit of the Status Register is in the logical "0" state (Sector Protection Registers are not locked), then writing a 00h to the Status Register will perform a Global Unprotect without changing the state of the SPRL bit. Similarly, writing a 7Fh to the Status Register will perform a Global Protect and keep the SPRL bit in the logical "0" state. The SPRL bit can, of course, be changed to a logical "1" by writing an FFh if software-locking or hardware-locking is desired along with the Global Protect.

If the desire is to only change the SPRL bit without performing a Global Protect or Global Unprotect, then the system can simply write a 0Fh to the Status Register to change the SPRL bit from a logical "1" to a logical "0" provided the WP pin is deasserted. Likewise, the system can write an F0h to change the SPRL bit from a logical "0" to a logical "1" without affecting the current sector protection status (no changes will be made to the Sector Protection Registers).

When writing to the Status Register, bits 5, 4, 3, and 2 will not actually be modified but will be decoded by the device for the purposes of the Global Protect and Global Unprotect functions. Only bit 7, the SPRL bit, will actually be modified. Therefore, when reading the Status Register, bits 5, 4, 3, and 2 will not reflect the values written to them but will instead indicate the status of the WP pin and the sector protection status. Please refer to the "Read Status Register" section and Table 11-1 on page 25 for details on the Status Register format and what values can be read for bits 5, 4, 3, and 2.

9.6   Read Sector Protection Registers

The Sector Protection Registers can be read to determine the current software protection status of each sector. Reading the Sector Protection Registers, however, will not determine the status of the WP pin.

To read the Sector Protection Register for a particular sector, the CS pin must first be asserted and the opcode of 3Ch must be clocked in. Once the opcode has been clocked in, three address bytes designating any address within the sector must be clocked in. After the last address byte has been clocked in, the device will begin outputting data on the SO pin during every subsequent clock cycle. The data being output will be a repeating byte of either FFh or 00h to denote the value of the appropriate Sector Protection Register.

Table 9-3.   Read Sector Protection Register – Output Data

Output Data	Sector Protection Register Value
00h	Sector Protection Register value is 0 (sector is unprotected).
FFh	Sector Protection Register value is 1 (sector is protected).

Deasserting the CS pin will terminate the read operation and put the SO pin into a high-impedance state. The CS pin can be deasserted at any time and does not require that a full byte of data be read.

In addition to reading the individual Sector Protection Registers, the Software Protection Status (SWP) bit in the Status Register can be read to determine if all, some, or none of the sectors are software protected (refer to the "Status Register Commands" on page 28 for more details).

Figure 9-5.   Read Sector Protection Register
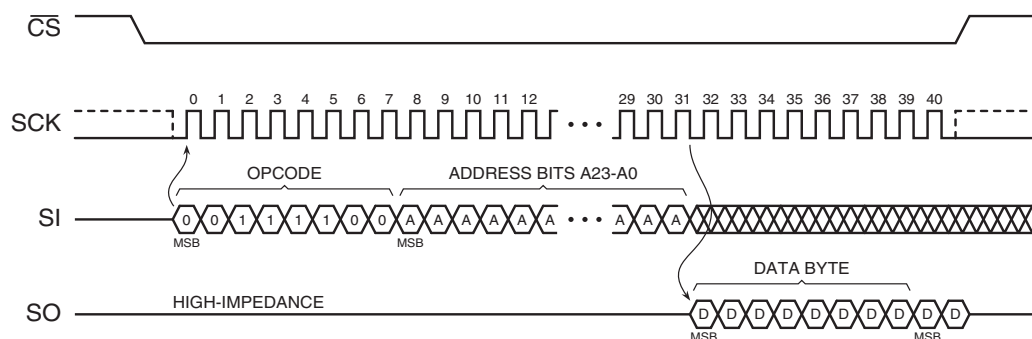
9.7 Protected States and the Write Protect ($\overline{WP}$) Pin

The $\overline{WP}$ pin is not linked to the memory array itself and has no direct effect on the protection status of the memory array. Instead, the $\overline{WP}$ pin, in conjunction with the SPRL (Sector Protection Registers Locked) bit in the Status Register, is used to control the hardware locking mechanism of the device. For hardware locking to be active, two conditions must be met – the $\overline{WP}$ pin must be asserted and the SPRL bit must be in the logical "1" state.

When hardware locking is active, the Sector Protection Registers are locked and the SPRL bit itself is also locked. Therefore, sectors that are protected will be locked in the protected state, and sectors that are unprotected will be locked in the unprotected state. These states cannot be changed as long as hardware locking is active, so the Protect Sector, Unprotect Sector, and Write Status Register commands will be ignored. In order to modify the protection status of a sector, the $\overline{WP}$ pin must first be deasserted, and the SPRL bit in the Status Register must be reset back to the logical "0" state using the Write Status Register command. When resetting the SPRL bit back to a logical "0", it is not possible to perform a Global Protect or Global Unprotect at the same time since the Sector Protection Registers remain soft-locked until after the Write Status Register command has been executed.

If the $\overline{WP}$ pin is permanently connected to GND, then once the SPRL bit is set to a logical "1", the only way to reset the bit back to the logical "0" state is to power-cycle or reset the device. This allows a system to power-up with all sectors software protected but not hardware locked. Therefore, sectors can be unprotected and protected as needed and then hardware locked at a later time by simply setting the SPRL bit in the Status Register.

When the $\overline{WP}$ pin is deasserted, or if the $\overline{WP}$ pin is permanently connected to VCC, the SPRL bit in the Status Register can still be set to a logical "1" to lock the Sector Protection Registers. This provides a software locking ability to prevent erroneous Protect Sector or Unprotect Sector commands from being processed. When changing the SPRL bit to a logical "1" from a logical "0", it is also possible to perform a Global Protect or Global Unprotect at the same time by writing the appropriate values into bits 5, 4, 3, and 2 of the Status Register.

Tables 9-4 and 9-5 detail the various protection and locking states of the device.
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Table 9-4. Sector Protection Register States

$\overline{WP}$	Sector Protection Register n [1]	Sector n[1]
X (Don't Care)	0	Unprotected
	1	Protected

1. "n" represents a sector number

Table 9-5. Hardware and Software Locking

$\overline{WP}$	SPRL	Locking	SPRL Change Allowed	Sector Protection Registers
0	0		Can be modified from 0 to 1	Unlocked and modifiable using the Protect and Unprotect Sector commands. Global Protect and Unprotect can also be performed.
0	1	Hardware Locked	Locked	Locked in current state. Protect and Unprotect Sector commands will be ignored. Global Protect and Unprotect cannot be performed.
1	0		Can be modified from 0 to 1	Unlocked and modifiable using the Protect and Unprotect Sector commands. Global Protect and Unprotect can also be performed.
1	1	Software Locked	Can be modified from 1 to 0	Locked in current state. Protect and Unprotect Sector commands will be ignored. Global Protect and Unprotect cannot be performed.

10.   Security Commands

10.1   Program OTP Security Register

The device contains a specialized OTP (One-Time Programmable) Security Register that can be used for purposes such as unique device serialization, system-level Electronic Serial Number (ESN) storage, locked key storage, etc. The OTP Security Register is independent of the main Flash memory array and is comprised of a total of 128 bytes of memory divided into two portions. The first 64 bytes (byte locations 0 through 63) of the OTP Security Register are allocated as a one-time user-programmable space. Once these 64 bytes have been programmed, they cannot be erased or reprogrammed. The remaining 64 bytes of the OTP Security Register (byte locations 64 through 127) are factory programmed by Adesto and will contain a unique value for each device. The factory programmed data is fixed and cannot be changed

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Table 10-1.   OTP Security Register

Security Register Byte Number									
0	1	…	62	63	64	65	…	126	127
One-Time User Programmable					Factory Programmed by Adesto				

The user-programmable portion of the OTP Security Register does not need to be erased before it is programmed. In addition, the Program OTP Security Register command operates on the entire 64-byte user-programmable portion of the OTP Security Register at one time. Once the user-programmable space has been programmed with any number of bytes, the user-programmable space cannot be programmed again; therefore, it is not possible to only program the first two bytes of the register and then program the remaining 62 bytes at a later time.

Before the Program OTP Security Register command can be issued, the Write Enable command must have been previously issued to set the WEL bit in the Status Register to a logical "1". To program the OTP Security Register, the $\overline{CS}$ pin must first be asserted and an opcode of 9Bh must be clocked into the device followed by the three address bytes denoting the first byte location of the OTP Security Register to begin programming at. Since the size of the user-programmable portion of the OTP Security Register is 64 bytes, the upper order address bits do not need to be decoded by the device. Therefore, address bits A23-A6 will be ignored by the device and their values can be either a logical "1" or "0". After the address bytes have been clocked in, data can then be clocked into the device and will be stored in the internal buffer.

If the starting memory address denoted by A23-A0 does not start at the beginning of the OTP Security Register memory space (A5-A0 are not all 0), then special circumstances regarding which OTP Security Register locations to be programmed will apply. In this situation, any data that is sent to the device that goes beyond the end of the 64-byte user-programmable space will wrap around back to the beginning of the OTP Security Register. For example, if the starting address denoted by A23-A0 is 00003Eh, and three bytes of data are sent to the device, then the first two bytes of data will be programmed at OTP Security Register addresses 00003Eh and 00003Fh while the last byte of data will be programmed at address 000000h. The remaining bytes in the OTP Security Register (addresses 000001h through 00003Dh) will not be programmed and will remain in the erased state (FFh). In addition, if more than 64 bytes of data are sent to the device, then only the last 64 bytes sent will be latched into the internal buffer.

When the $\overline{CS}$ pin is deasserted, the device will take the data stored in the internal buffer and program it into the appropriate OTP Security Register locations based on the starting address specified by A23-A0 and the number of data bytes sent to the device. If less than 64 bytes of data were sent to the device, then the remaining bytes within the OTP Security Register will not be programmed and will remain in the erased state (FFh). The programming of the data bytes is internally self-timed and should take place in a time of t_{OTPP}.

The three address bytes and at least one complete byte of data must be clocked into the device before the $\overline{CS}$ pin is deasserted, and the $\overline{CS}$ pin must be deasserted on even byte boundaries (multiples of eight bits); otherwise, the device will abort the operation and the user-programmable portion of the OTP Security Register will not be programmed. The WEL bit in the Status Register will be reset back to the logical "0" state if the OTP Security Register program cycle aborts due to an incomplete address being sent, an incomplete byte of data being sent, the $\overline{CS}$ pin being deasserted on uneven byte boundaries, or because the user-programmable portion of the OTP Security Register was previously programmed.

While the device is programming the OTP Security Register, the Status Register can be read and will indicate that the device is busy. For faster throughput, it is recommended that the Status Register be polled rather than waiting the t_{OTPP} time to determine if the data bytes have finished programming. At some point before the OTP Security Register programming completes, the WEL bit in the Status Register will be reset back to the logical "0" state.

If the device is powered-down during the OTP Security Register program cycle, then the contents of the 64-byte user programmable portion of the OTP Security Register cannot be guaranteed and cannot be programmed again.

The Program OTP Security Register command utilizes the internal 256-buffer for processing. Therefore, the contents of the buffer will be altered from its previous state when this command is issued.

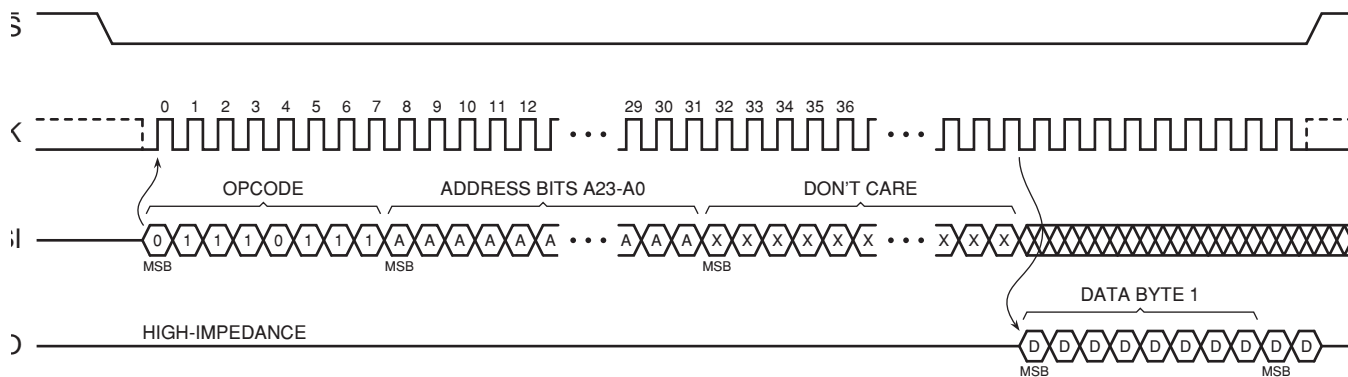**Figure 10-1. Program OTP Security Register**
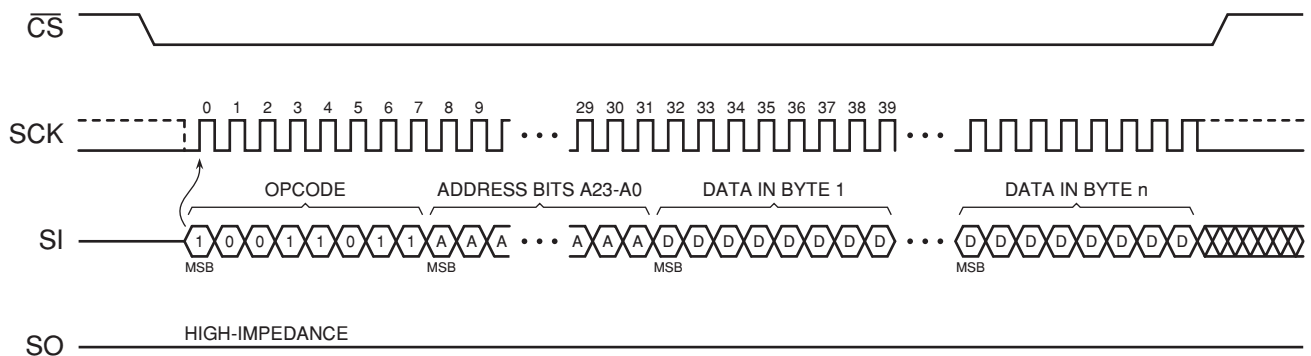
10.2 Read OTP Security Register

The OTP Security Register can be sequentially read in a similar fashion to the Read Array operation up to the maximum clock frequency specified by f_{CLK}. To read the OTP Security Register, the $\overline{CS}$ pin must first be asserted and the opcode of 77h must be clocked into the device. After the opcode has been clocked in, the three address bytes must be clocked in to specify the starting address location of the first byte to read within the OTP Security Register. Following the three address bytes, two dummy bytes must be clocked into the device before data can be output.

After the three address bytes and the dummy bytes have been clocked in, additional clock cycles will result in OTP Security Register data being output on the SO pin. When the last byte (00007Fh) of the OTP Security Register has been read, the device will continue reading back at the beginning of the register (000000h). No delays will be incurred when wrapping around from the end of the register to the beginning of the register.

Deasserting the $\overline{CS}$ pin will terminate the read operation and put the SO pin into a high-impedance state. The $\overline{CS}$ pin can be deasserted at any time and does not require that a full byte of data be read.

Figure 10-2. Read OTP Security Register


```
                    0  1  2  3  4  5  6  7  8  9  10 11 12      29 30 31 32 33 34 35 36

                         OPCODE              ADDRESS BITS A23-A0           DON'T CARE

                    0  1  1  1  0  1  1  1  A  A  A  A  A  A ... A  A  A  X  X  X  X  X  X  X ... X  X  X
                    MSB                MSB                    MSB

                                                                               DATA BYTE 1

    HIGH-IMPEDANCE                                                          D  D  D  D  D  D  D  D  D  D
                                                                           MSB                      MSB
```

11. Status Register Commands

11.1 Read Status Register

The Status Register can be read to determine the device's ready/busy status, as well as the status of many other functions such as Hardware Locking and Software Protection. The Status Register can be read at any time, including during an internally self-timed program or erase operation.The Status Register consists of two bytes.

To read the Status Register, the $\overline{CS}$ pin must first be asserted and the opcode of 05h must be clocked into the device. After the opcode has been clocked in, the device will begin outputting Status Register data on the SO pin during every subsequent clock cycle. After the last bit (bit 0) of Status Register Byte 2 has been clocked out, the sequence will repeat itself, starting again with bit 7 of Status Register Byte 1, as long as the $\overline{CS}$ pin remains asserted and the clock pin is being pulsed. The data in the Status Register is constantly being updated, so each repeating sequence will output new data.

Deasserting the $\overline{CS}$ pin will terminate the Read Status Register operation and put the SO pin into a high-impedance state. The $\overline{CS}$ pin can be deasserted at any time and does not require that a full byte of data be read.

Table 11-1.   Status Register Format

Bit [1]	Name		Type [2]	Description	
7	SPRL	Sector Protection Registers Locked	R/W	0	Sector Protection Registers are unlocked (default).
				1	Sector Protection Registers are locked.
6	SPM	Sequential Program Mode Status	R	0	Byte/Page Programming Mode (default).
				1	Sequential Programming Mode entered.
5	EPE	Erase/Program Error	R	0	Erase or program operation was successful.
				1	Erase or program error detected.
4	WPP	Write Protect ($\overline{WP}$) Pin Status	R	0	$\overline{WP}$ is asserted.
				1	$\overline{WP}$ is deasserted.