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Features

- **Fast Read Access Time – 70 ns**
- **5-volt Only Reprogramming**
- **Page Program Operation**
  - **Single Cycle Reprogram (Erase and Program)**
  - **Internal Address and Data Latches for 64 Bytes**
- **Internal Program Control and Timer**
- **Hardware and Software Data Protection**
- **Fast Program Cycle Times**
  - **Page (64 Byte) Program Time – 10 ms**
  - **Chip Erase Time– 10 ms**
- **$\overline{\text{DATA}}$ Polling for End of Program Detection**
- **Low-power Dissipation**
  - **50 mA Active Current**
  - **300 µA CMOS Standby Current**
- **Typical Endurance > 10,000 Cycles**
- **Single 5V ± 10% Supply**
- **CMOS and TTL Compatible Inputs and Outputs**
- **Commercial and Industrial Temperature Ranges**

256K (32K x 8) 5-volt Only Flash Memory

AT29C256

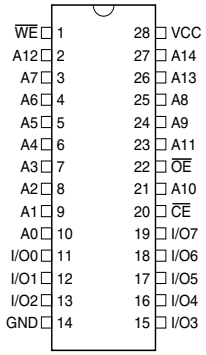
Description

The AT29C256 is a five-volt-only in-system Flash programmable and erasable read only memory (PEROM). Its 256K of memory is organized as 32,768 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 70 ns with power dissipation of just 275 mW. When the device is deselected, the CMOS standby current is less than 300 µA. The device endurance is such that any sector can typically be written to in excess of 10,000 times.

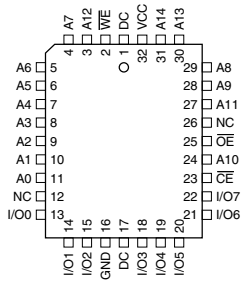
Pin Configurations

Pin Name	Function
A0 - A14	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect
DC	Don't Connect

DIP Top View

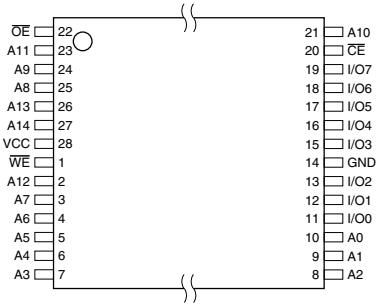


PLCC and LCC Top View



Note: PLCC package pins 1 and 17 are DON'T CONNECT.

TSOP Top View
Type 1

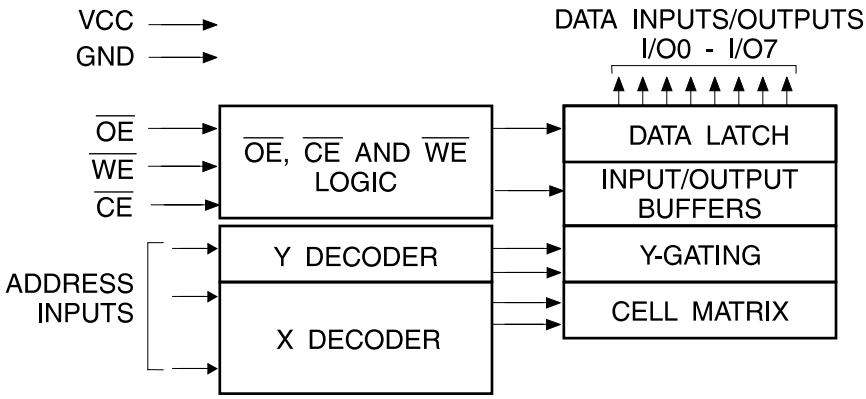


Rev. 0046O–FLASH–06/02

To allow for simple in-system reprogrammability, the AT29C256 does not require high input voltages for programming. Five-volt-only commands determine the operation of the device. Reading data out of the device is similar to reading from a static RAM. Reprogramming the AT29C256 is performed on a page basis; 64 bytes of data are loaded into the device and then simultaneously programmed. The contents of the entire device may be erased by using a six-byte software code (although erasure before programming is not needed).

During a reprogram cycle, the address locations and 64 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a program cycle, the device will automatically erase the page and then program the latched data using an internal control timer. The end of a program cycle can be detected by $\overline{\text{DATA}}$ polling of I/O7. Once the end of a program cycle has been detected a new access for a read, program or chip erase can begin.

Block Diagram



Device Operation

READ: The AT29C256 is accessed like a static RAM. When $\overline{\text{CE}}$ and $\overline{\text{OE}}$ are low and $\overline{\text{WE}}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{\text{CE}}$ or $\overline{\text{OE}}$ is high. This dual-line control gives designers flexibility in preventing bus contention.

BYTE LOAD: A byte load is performed by applying a low pulse on the $\overline{\text{WE}}$ or $\overline{\text{CE}}$ input with $\overline{\text{CE}}$ or $\overline{\text{WE}}$ low (respectively) and $\overline{\text{OE}}$ high. The address is latched on the falling edge of $\overline{\text{CE}}$ or $\overline{\text{WE}}$, whichever occurs last. The data is latched by the first rising edge of $\overline{\text{CE}}$ or $\overline{\text{WE}}$. Byte loads are used to enter the 64 bytes of a page to be programmed or the software codes for data protection and chip erasure.

PROGRAM: The device is reprogrammed on a page basis. If a byte of data within a page is to be changed, data for the entire page must be loaded into the device. Any byte that is not loaded during the programming of its page will be indeterminate. Once the bytes of a page are loaded into the device, they are simultaneously programmed during the internal programming period. After the first data byte has been loaded into the device, successive bytes are entered in the same manner. Each new byte to be programmed must have its high-to-low transition on $\overline{WE}$ (or $\overline{CE}$) within 150 µs of the low-to-high transition of $\overline{WE}$ (or $\overline{CE}$) of the preceding byte. If a high-to-low transition is not detected within 150 µs of the last low-to-high transition, the load period will end and the internal programming period will start. A6 to A14 specify the page address. The page address must be valid during each high-to-low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A5 specify the byte address within the page. The bytes may be loaded in any order; sequential loading is not required. Once a programming operation has been initiated, and for the duration of t_{WC}, a read operation will effectively be a polling operation.

SOFTWARE DATA PROTECTION: A software controlled data protection feature is available on the AT29C256. Once the software protection is enabled a software algorithm must be issued to the device before a program may be performed. The software protection feature may be enabled or disabled by the user; when shipped from Atmel, the software data protection feature is disabled. To enable the software data protection, a series of three program commands to specific addresses with specific data must be performed. After the software data protection is enabled the same three program commands must begin each program cycle in order for the programs to occur. All software program commands must obey the page program timing specifications. Once set, the software data protection feature remains active unless its disable command is issued. Power transitions will not reset the software data protection feature, however the software feature will guard against inadvertent program cycles during power transitions.

Once set, software data protection will remain active unless the disable command sequence is issued.

After setting SDP, any attempt to write to the device without the three-byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, a read operation will effectively be a polling operation.

After the software data protection's three-byte command code is given, a byte load is performed by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. The 64 bytes of data must be loaded into each sector by the same procedure as outlined in the program section under device operation.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT29C256 in the following ways: (a) V_{CC} sense – if V_{CC} is below 3.8V (typical), the program function is inhibited; (b) V_{CC} power on delay – once V_{CC} has reached the V_{CC} sense level, the device will automatically time out 5 ms (typical) before programming; (c) Program inhibit – holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits program cycles; and (d) Noise filter – pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a program cycle.

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer and may be accessed by a hardware operation. For details, see Operating Modes or Product Identification.

DATA POLLING: The AT29C256 features $\overline{\text{DATA}}$ polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{\text{DATA}}$ polling may begin at any time during the program cycle.

TOGGLE BIT: In addition to $\overline{\text{DATA}}$ polling the AT29C256 provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

OPTIONAL CHIP ERASE MODE: The entire device can be erased by using a six-byte software code. Please see Software Chip Erase application note for details.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{\text{OE}}$ with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range

		AT29C256-70	AT29C256-90	AT29C256-12	AT29C256-15
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		5V ± 5%	5V± 10%	5V± 10%	5V± 10%

Note: Not recommended for New Designs.

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	Ai	D_{OUT}
Program(2)	V_{IL}	V_{IH}	V_{IL}	Ai	D_{IN}
5V Chip Erase	V_{IL}	V_{IH}	V_{IL}	Ai	
Standby/Write Inhibit	V_{IH}	X(1)	X	X	High Z
Write Inhibit	X	X	V_{IH}		
Write Inhibit	X	V_{IL}	X		
Output Disable	X	V_{IH}	X		High Z
High Voltage Chip Erase	V_{IL}	V_H(3)	V_{IL}	X	High Z
Product Identification					
Hardware	V_{IL}	V_{IL}	V_{IH}	A1-A14 = V_{IL}, A9 = V_H, A0 = V_{IL}	Manufacturer Code(4)
				A1-A14 = V_{IL}, A9 = V_H, A0 = V_{IH}	Device Code(4)
Software(5)				A0 = V_{IL}	Manufacturer Code(4)
				A0 = V_{IH}	Device Code(4)

Notes:
1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. V_H = 12.0V ± 0.5V.
4. Manufacturer Code: 1F, Device Code: DC.
5. See details under Software Product Identification Entry/Exit.

DC Characteristics

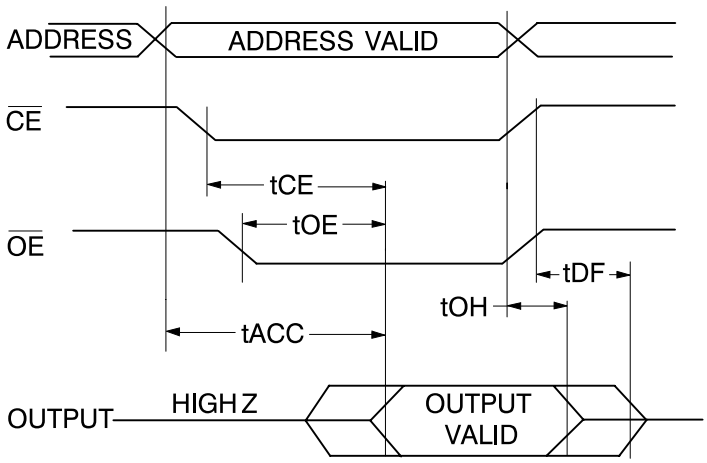
Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}		10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC}		300	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC}		3	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA		50	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA	2.4		V
V_{OH2}	Output High Voltage CMOS	I_{OH} = -100 µA; V_{CC} = 4.5V	4.2		V

AC Read Characteristics

Symbol	Parameter	AT29C256-70		AT29C256-90		AT29C256-12		AT29C256-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		70		90		120		150	ns
t_{CE}[1]	$\overline{CE}$ to Output Delay		70		90		120		150	ns
t_{OE}[2]	$\overline{OE}$ to Output Delay	0	40	0	40	0	50	0	70	ns
t_{DF}[3][4]	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	25	0	25	0	30	0	40	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		0		ns

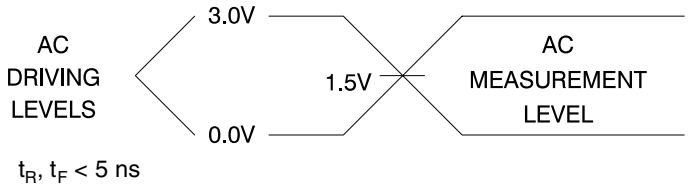
Note: Not recommended for New Designs.

AC Read Waveforms[1][2][3][4]



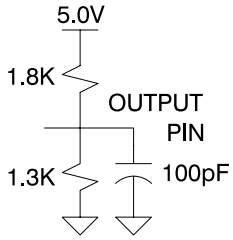
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (CL = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

Output Test Load



Pin Capacitance

f = 1 MHz, T = 25°C[1]

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

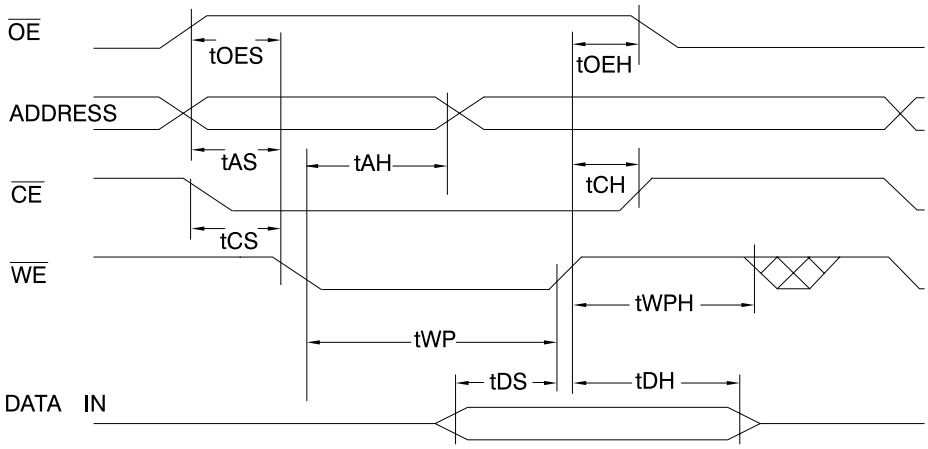
Note: 1. This parameter is characterized and is not 100% tested.

AC Byte Load Characteristics

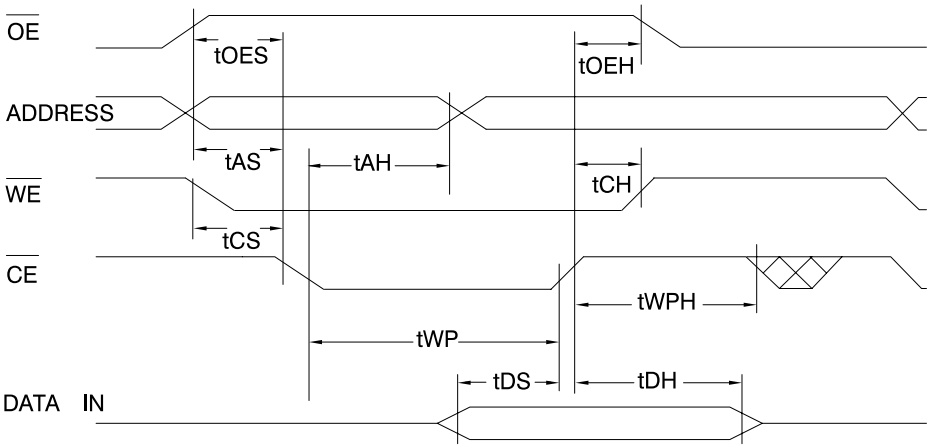
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	90		ns
t_{DS}	Data Set-up Time	35		ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns
t_{WPH}	Write Pulse Width High	100		ns

AC Byte Load Waveforms

$\overline{WE}$ Controlled



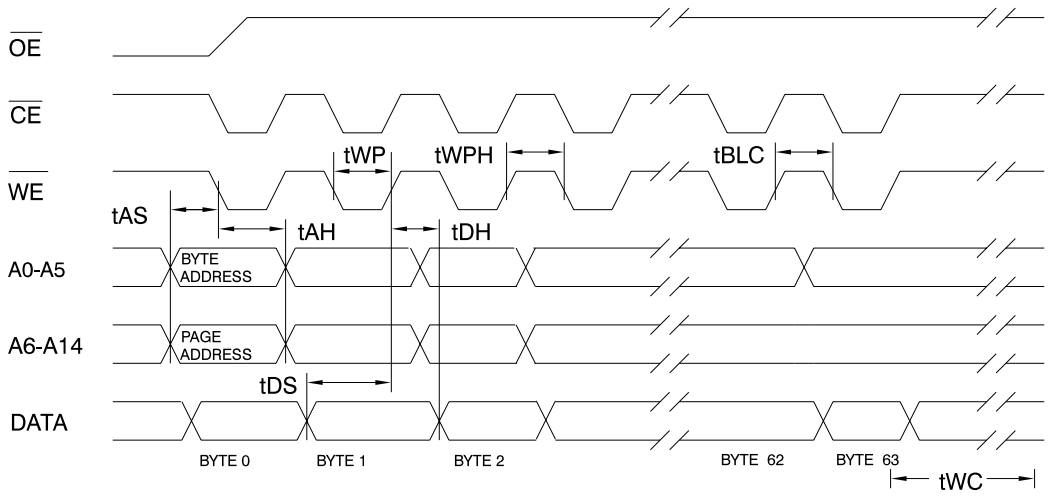
$\overline{CE}$ Controlled



Program Cycle Characteristics

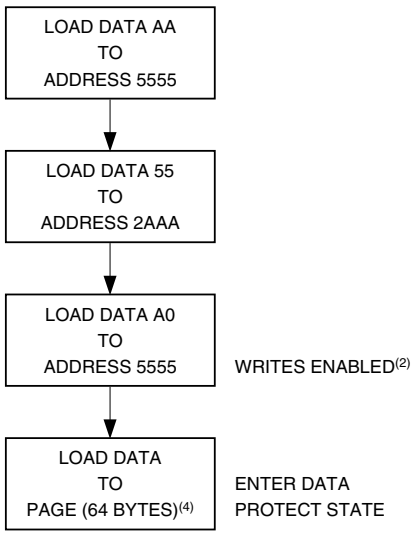
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	35		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	90		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	100		ns

Program Cycle Waveforms(1)(2)(3)



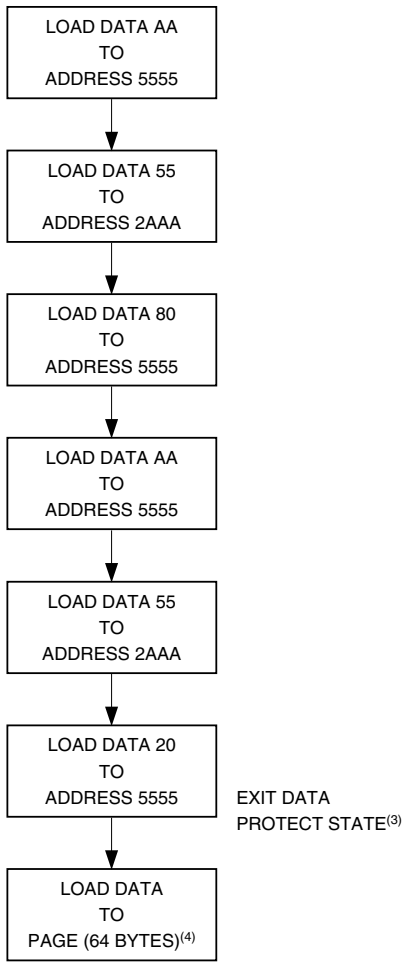
Notes: 1. A6 through A14 must specify the page address during each high-to-low transition of $\overline{WE}$ (or $\overline{CE}$).
2. $\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
3. All bytes that are not loaded within the page being programmed will be indeterminate.

Software Data Protection Enable Algorithm[1]

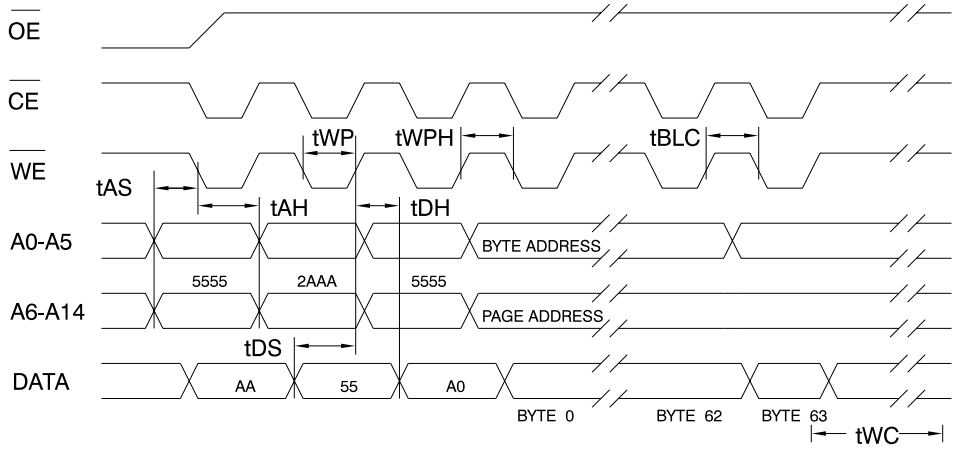


Notes:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Data Protect state will be re-activated at end of program cycle.
3. Data Protect state will be deactivated at end of program period.
4. 64 bytes of data **MUST BE** loaded.

Software Data Protection Disable Algorithm[1]



Software Protected Program Cycle Waveform[1][2][3]



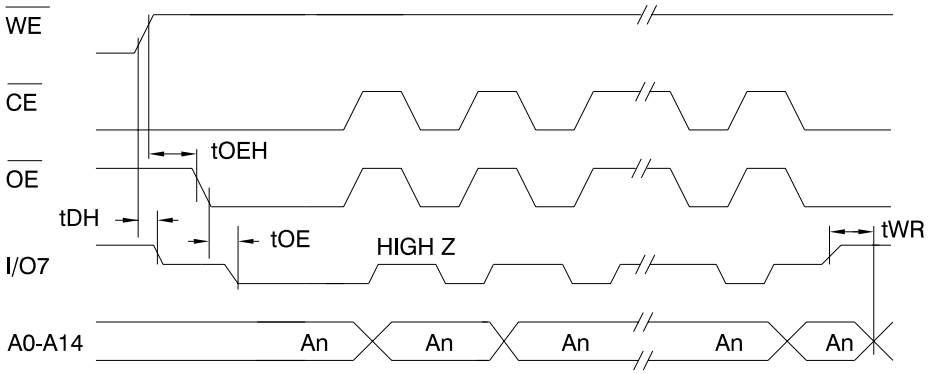
Notes:
1. A6 through A14 must specify the page address during each high-to-low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
2. $\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
3. All bytes that are not loaded within the page being programmed will be indeterminate.

$\overline{\text{Data}}$ Polling Characteristics(1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay(2)				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

$\overline{\text{Data}}$ Polling Waveforms

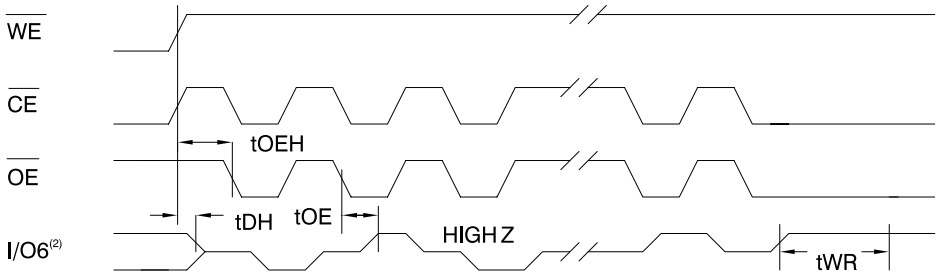


Toggle Bit Characteristics(1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay(2)				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

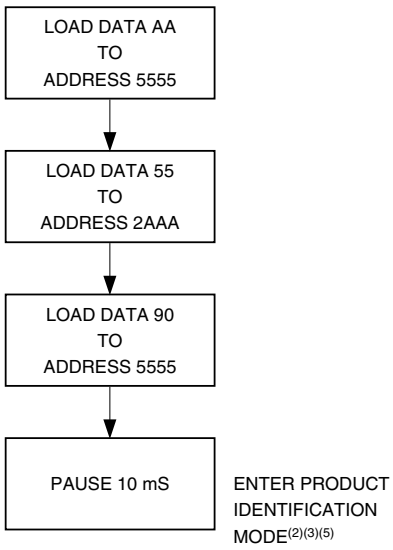
Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

Toggle Bit Waveforms(1)(2)(3)

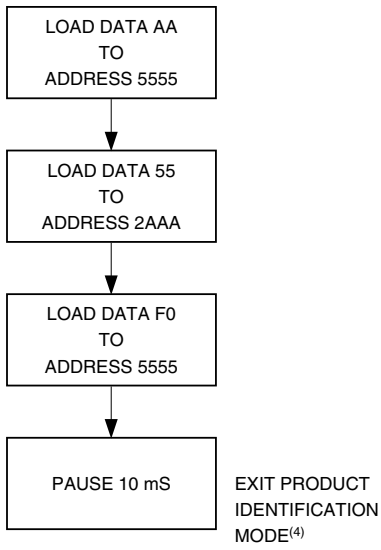


Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Software Product Identification Entry[1]

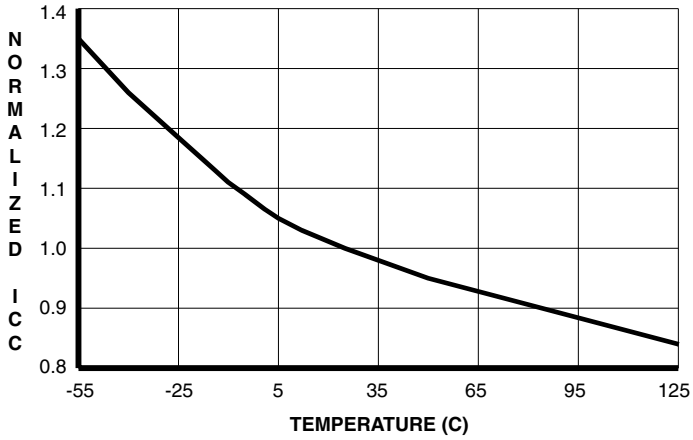


Software Product Identification Exit[1]

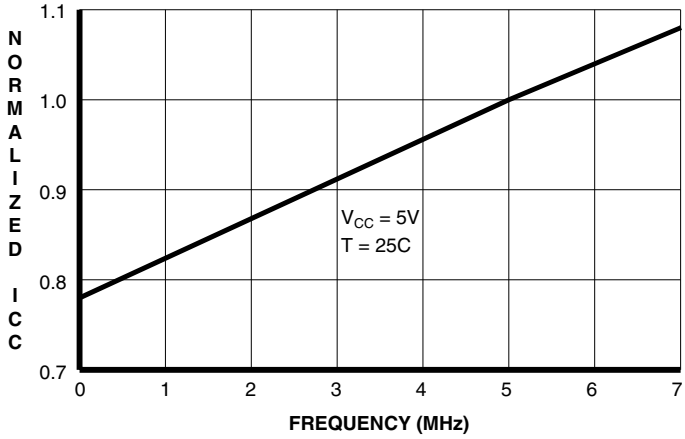


Notes:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. A1 - A14 = V_{IL}.
   Manufacturer Code is read for A0 = V_{IL};
   Device Code is read for A0 = V_{IH}.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.
5. Manufacturer Code is 1F. The Device Code is DC.

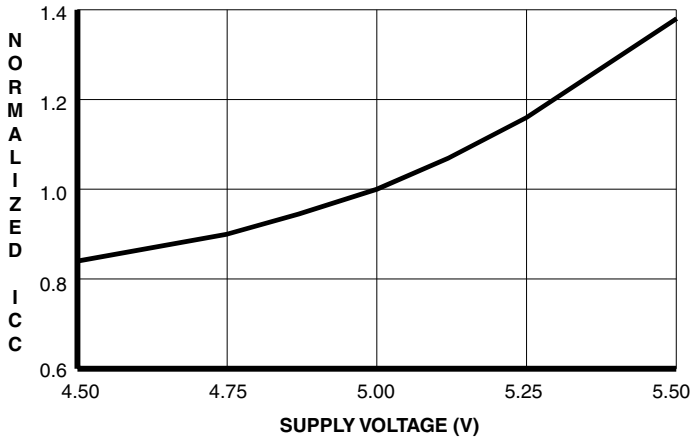
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



Ordering Information

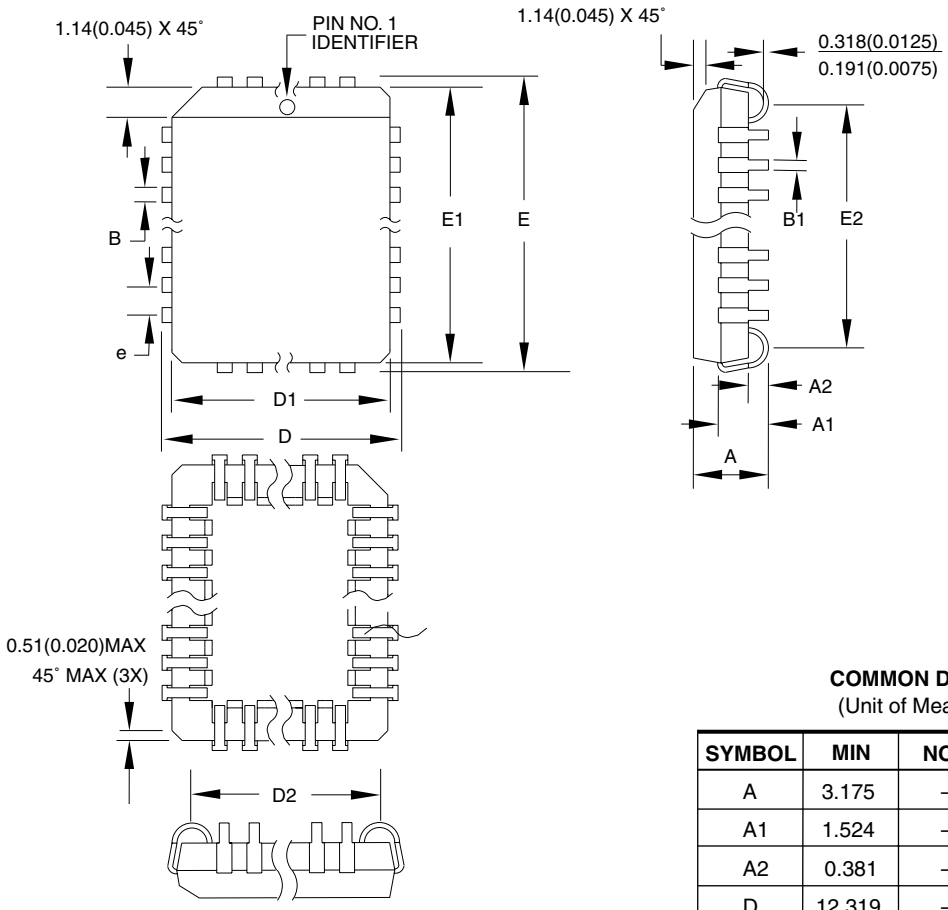
t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	50	0.3	AT29C256-70JC AT29C256-70PC AT29C256-70TC	32J 28P6 28T	Commercial (0° to 70°C)
			AT29C256-70JI AT29C256-70TI	32J 28T	Industrial (-40° to 85°C)
90	50	0.3	AT29C256-90JC AT29C256-90PC AT29C256-90TC	32J 28P6 28T	Commercial (0° to 70°C)
			AT29C256-90JI AT29C256-90PI AT29C256-90TI	32J 28P6 28T	Industrial (-40° to 85°C)
120	50	0.3	AT29C256-12JC AT29C256-12PC AT29C256-12TC	32J 28P6 28T	Commercial (0° to 70°C)
			AT29C256-12JI AT29C256-12PI AT29C256-12TI	32J 28P6 28T	Industrial (-40° to 85°C)
150	50	0.3	AT29C256-15JC AT29C256-15PC AT29C256-15TC	32J 28P6 28T	Commercial (0° to 70°C)
			AT29C256-15JI AT29C256-15PI AT29C256-15TI	32J 28P6 28T	Industrial (-40° to 85°C)

Note: Not recommended for New Designs.

Package Type	
32J	32-lead, Plastic J-leaded Chip Carrier (PLCC)
28P6	28-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28T	28-lead, Plastic Thin Small Outline Package (TSOP)

Packaging Information

32J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

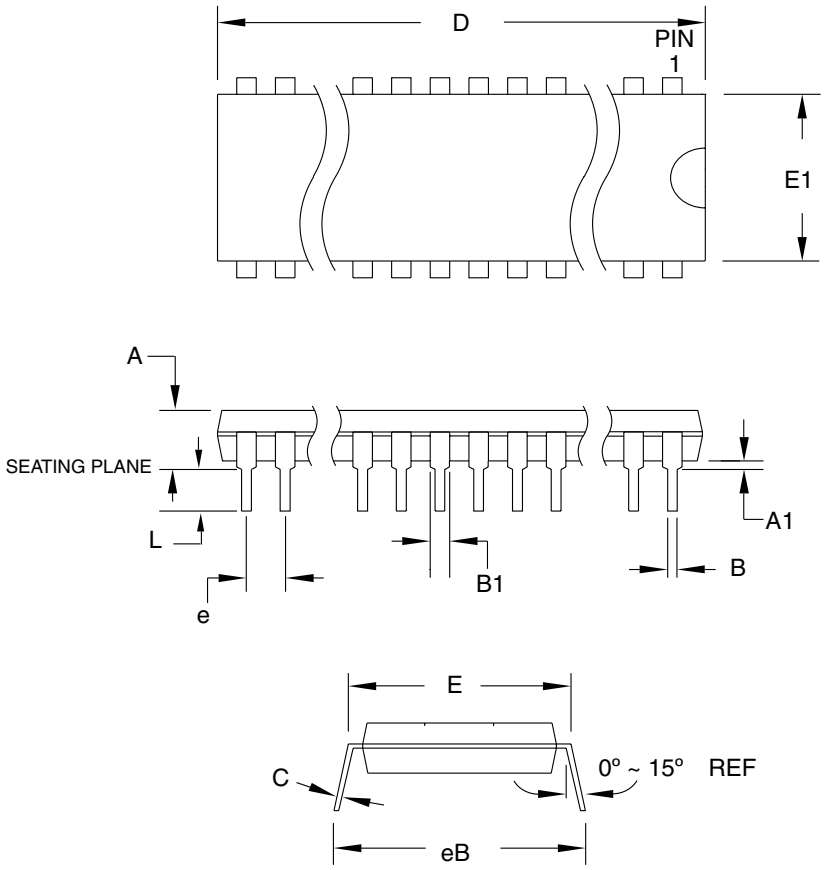
SYMBOL	MIN	NOM	MAX	NOTE
A	3.175	–	3.556	
A1	1.524	–	2.413	
A2	0.381	–	–	
D	12.319	–	12.573	
D1	11.354	–	11.506	Note 2
D2	9.906	–	10.922	
E	14.859	–	15.113	
E1	13.894	–	14.046	Note 2
E2	12.471	–	13.487	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-016, Variation AE.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**32J**, 32-lead, Plastic J-leaded Chip Carrier (PLCC)	32J	B

28P6 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

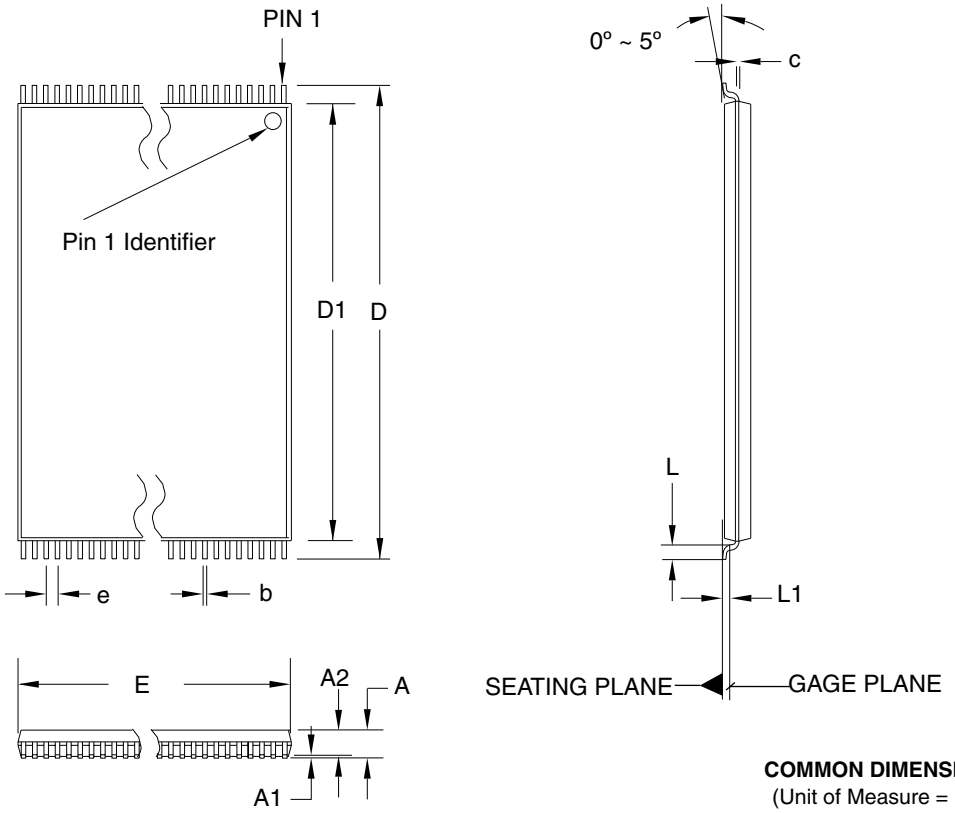
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.826	
A1	0.381	–	–	
D	36.703	–	37.338	Note 2
E	15.240	–	15.875	
E1	13.462	–	13.970	Note 2
B	0.356	–	0.559	
B1	1.041	–	1.651	
L	3.048	–	3.556	
C	0.203	–	0.381	
eB	15.494	–	17.526	
e	2.540 TYP			

Notes:
1. This package conforms to JEDEC reference MS-011, Variation AB.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

09/28/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**28P6**, 28-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP)	28P6	B

28T – TSOP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.90	1.00	1.05	
D	13.20	13.40	13.60	
D1	11.70	11.80	11.90	Note 2
E	7.90	8.00	8.10	Note 2
L	0.50	0.60	0.70	
L1	0.25 BASIC			
b	0.17	0.22	0.27	
c	0.10	–	0.21	
e	0.55 BASIC			

Notes:
1. This package conforms to JEDEC reference MO-183.
2. Dimensions D1 and E do not include mold protrusion. Allowable protrusion on E is 0.15 mm per side and on D1 is 0.25 mm per side.
3. Lead coplanarity is 0.10 mm maximum.

10/18/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**28T**, 28-lead (8 x 13.4 mm Package) Plastic Thin Small Outline Package, Type I (TSOP)	28T	B

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