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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



Features

- Fast Read Access Time - 90 ns
- Five-Volt-Only Reprogramming
- Page Program Operation
 - Single Cycle Reprogram (Erase and Program)
 - Internal Address and Data Latches for 64 Bytes
- Internal Program Control and Timer
- Hardware and Software Data Protection
- Fast Program Cycle Times
 - Page (64 Byte) Program Time - 10 ms
 - Chip Erase Time - 10 ms
- DATA Polling for End of Program Detection
- Low Power Dissipation
 - 50 mA Active Current
 - 300 μ A CMOS Standby Current
- Typical Endurance > 10,000 Cycles
- Single 5 V $\pm$ 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- Commercial and Industrial Temperature Ranges

256K (32K x 8)
5-Volt Only
CMOS Flash
PEROM

5

Description

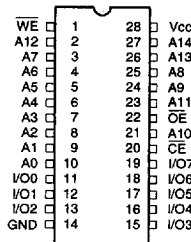
The AT29C256 is a five-volt-only in-system Flash programmable and erasable read only memory (PEROM). Its 256K of memory is organized as 32,768 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 90 ns with power dissipation of just 275 mW. When the device is deselected, the CMOS standby current is less than 300 μ A. The device endurance is such that any sector can typically be written to in excess of 10,000 times.

(continued)

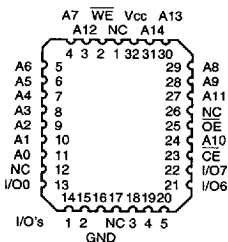
Pin Configurations

Pin Name	Function
A0 - A14	Addresses
CE	Chip Enable
OE	Output Enable
WE	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

DIP Top View



PLCC and LCC Top View



TSOP Top View
Type 1



Note: PLCC package pins 1 and 17 are DON'T CONNECT.

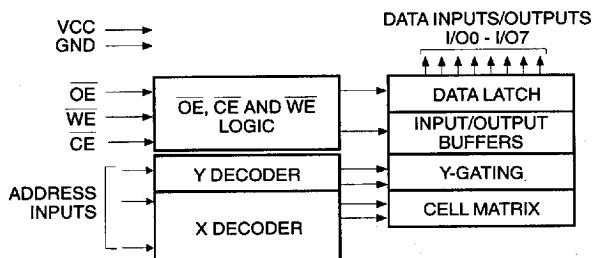


Description (Continued)

To allow for simple in-system reprogrammability, the AT29C256 does not require high input voltages for programming. Five-volt-only commands determine the operation of the device. Reading data out of the device is similar to reading from a static RAM. Reprogramming the AT29C256 is performed on a page basis; 64 bytes of data are loaded into the device and then simultaneously programmed. The contents of the entire device may be erased by using a six-byte software code (although erase before programming is not needed).

During a reprogram cycle, the address locations and 64 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a program cycle, the device will automatically erase the page and then program the latched data using an internal control timer. The end of a program cycle can be detected by $\overline{\text{DATA}}$ polling of I/O7. Once the end of a program cycle has been detected a new access for a read, program or chip erase can begin.

Block Diagram



Device Operation

READ: The AT29C256 is accessed like a static RAM. When $\overline{\text{CE}}$ and $\overline{\text{OE}}$ are low and $\overline{\text{WE}}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{\text{CE}}$ or $\overline{\text{OE}}$ is high. This dual-line control gives designers flexibility in preventing bus contention.

BYTE LOAD: A byte load is performed by applying a low pulse on the $\overline{\text{WE}}$ or $\overline{\text{CE}}$ input with $\overline{\text{CE}}$ or $\overline{\text{WE}}$ low (respectively) and $\overline{\text{OE}}$ high. The address is latched on the falling edge of $\overline{\text{CE}}$ or $\overline{\text{WE}}$, whichever occurs last. The data is latched by the first rising edge of $\overline{\text{CE}}$ or $\overline{\text{WE}}$. Byte loads are used to enter the 64 bytes of a page to be programmed or the software codes for data protection and chip erasure.

PROGRAM: The device is reprogrammed on a page basis. If a byte of data within a page is to be changed, data for the entire page must be loaded into the device. Any byte that is not loaded during the programming of its page will be erased to read FFh. Once the bytes of a page are loaded into the device, they are simultaneously programmed during the internal programming period. After the first data byte has been loaded into the device, successive bytes are entered in the same manner. Each new byte to be programmed must have its high to low transition on $\overline{\text{WE}}$ (or $\overline{\text{CE}}$) within 150 μs of the low to high transition of $\overline{\text{WE}}$ (or $\overline{\text{CE}}$) of the preceding byte. If a high to low transition is not detected within 150 μs of the last low to high transition, the load period will end and the internal programming period will start. A6 to A14 specify the page address. The page address must be valid during each high to low transition of $\overline{\text{WE}}$ (or $\overline{\text{CE}}$). A0 to A5 specify the byte address within the page. The bytes may be loaded in any order; sequential loading is not required. Once a

programming operation has been initiated, and for the duration of t_{WC}, a read operation will effectively be a polling operation.

SOFTWARE DATA PROTECTION: A software controlled data protection feature is available on the AT29C256. Once the software protection is enabled a software algorithm must be issued to the device before a program may be performed. The software protection feature may be enabled or disabled by the user; when shipped from Atmel, the software data protection feature is disabled. To enable the software data protection, a series of three program commands to specific addresses with specific data must be performed. After the software data protection is enabled the same three program commands must begin each program cycle in order for the programs to occur. All software program commands must obey the page program timing specifications. Once set, the software data protection feature remains active unless its disable command is issued. Power transitions will not reset the software data protection feature, however the software feature will guard against inadvertent program cycles during power transitions.

Once set, software data protection will remain active unless the disable command sequence is issued.

After setting SDP, any attempt to write to the device without the three-byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, a read operation will effectively be a polling operation.

After the software data protection's three-byte command code is given, a byte load is performed by applying a low pulse on the $\overline{\text{WE}}$ or $\overline{\text{CE}}$ input with $\overline{\text{CE}}$ or $\overline{\text{WE}}$ low (respectively) and $\overline{\text{OE}}$ high.

(continued)

Device Operation (Continued)

The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. The 64 bytes of data must be loaded into each sector by the same procedure as outlined in the program section under device operation.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT29C256 in the following ways: (a) VCC sense— if VCC is below 3.8 V (typical), the program function is inhibited. (b) VCC power on delay— once VCC has reached the VCC sense level, the device will automatically time out 5 ms (typical) before programming. (c) Program inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits program cycles. (d) Noise filter— pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a program cycle.

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer and may be accessed by a hardware operation. For details, see Operating Modes or Product Identification.

DATA POLLING: The AT29C256 features $\overline{DATA}$ polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{DATA}$ polling may begin at any time during the program cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ polling the AT29C256 provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

OPTIONAL CHIP ERASE MODE: The entire device can be erased by using a six-byte software code. Please see Software Chip Erase application note for details.

Absolute Maximum Ratings*

Temperature Under Bias.....	-55°C to +125°C
Storage Temperature.....	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6 V to +6.25 V
All Output Voltages with Respect to Ground	-0.6 V to V _{CC} +0.6 V
Voltage on $\overline{OE}$ with Respect to Ground	-0.6 V to +13.5 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Capacitance (f = 1 MHz, T = 25°C) ⁽¹⁾

	Typ	Max	Units	Conditions
C _{IN}	4	6	pF	V _{IN} = 0 V
C _{OUT}	8	12	pF	V _{OUT} = 0 V

Note: 1. This parameter is characterized and is not 100% tested.



D.C. and A.C. Operating Range

		AT29C256-90	AT29C256-12	AT29C256-15	AT29C256-20	AT29C256-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V _{CC} Power Supply		5 V ± 10%	5 V ± 10%	5 V ± 10%	5 V ± 10%	5 V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Ai	I/O
Read	V _{IL}	V _{IL}	V _{IH}	Ai	DOUT
Program ⁽²⁾	V _{IL}	V _{IH}	V _{IL}	Ai	DIN
5V Chip Erase	V _{IL}	V _{IH}	V _{IL}	Ai	
Standby/Write Inhibit	V _{IH}	X ⁽¹⁾	X	X	High Z
Write Inhibit	X	X	V _{IH}		
Write Inhibit	X	V _{IL}	X		
Output Disable	X	V _{IH}	X		High Z
High Voltage Chip Erase	V _{IL}	V _H ⁽³⁾	V _{IL}	X	High Z
Product Identification					
Hardware	V _{IL}	V _{IL}	V _{IH}	A1-A14 = V _{IL} , A9 = V _H , A0 = V _{IL}	Manufacturer Code ⁽⁴⁾
				A1-A14 = V _{IL} , A9 = V _H , A0 = V _{IH}	Device Code ⁽⁴⁾
Software ⁽⁵⁾				A0 = V _{IL}	Manufacturer Code ⁽⁴⁾
				A0 = V _{IH}	Device Code ⁽⁴⁾

- Notes: 1. X can be V_{IL} or V_{IH}.
 2. Refer to A.C. Programming Waveforms.
 3. V_H = 12.0 V ± 0.5 V.

4. Manufacturer Code: 1F, Device Code: DC
 5. See details under Software Product Identification Entry/Exit.

D.C. Characteristics

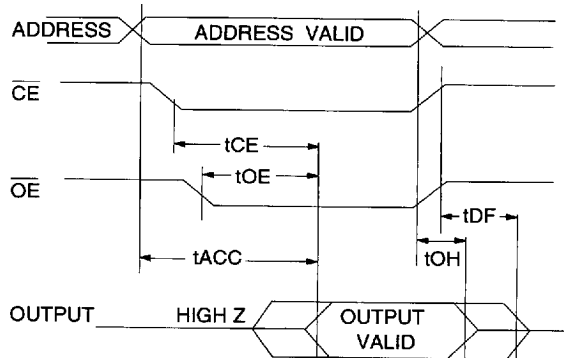
Symbol	Parameter	Condition	Min	Max	Units
I _{LI}	Input Load Current	V _{IN} = 0 V to V _{CC}		10	μA
I _{LO}	Output Leakage Current	V _{IO} = 0 V to V _{CC}		10	μA
I _{SB1}	V _{CC} Standby Current CMOS	$\overline{CE}$ = V _{CC} - 0.3 V to V _{CC}		300	μA
I _{SB2}	V _{CC} Standby Current TTL	$\overline{CE}$ = 2.0 V to V _{CC}		3	mA
I _{CC}	V _{CC} Active Current	f = 5 MHz; I _{OUT} = 0 mA		50	mA
V _{IL}	Input Low Voltage			0.8	V
V _{IH}	Input High Voltage		2.0		V
V _{OL}	Output Low Voltage	I _{OL} = 2.1 mA		.45	V
V _{OH1}	Output High Voltage	I _{OH} = -400 μA	2.4		V
V _{OH2}	Output High Voltage CMOS	I _{OH} = -100 μA; V _{CC} = 4.5 V	4.2		V

A.C. Read Characteristics

Symbol	Parameter	AT29C256-90		AT29C256-12		AT29C256-15		AT29C256-20		AT29C256-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		90		120		150		200		250	ns
$t_{CE}^{(1)}$	$\overline{CE}$ to Output Delay		90		120		150		200		250	ns
$t_{OE}^{(2)}$	$\overline{OE}$ to Output Delay	0	40	0	50	0	70	0	80	0	100	ns
$t_{DF}^{(3,4)}$	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	25	0	30	0	40	0	50	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		0		0		ns

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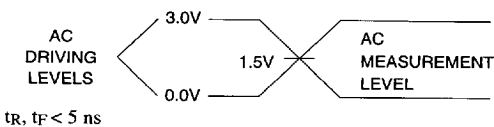
A.C. Read Waveforms (1,2,3,4)



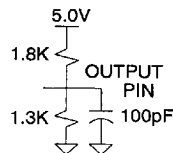
Notes:

- $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC} .
- $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC} .
- t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first ($C_L = 5pF$).
- This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



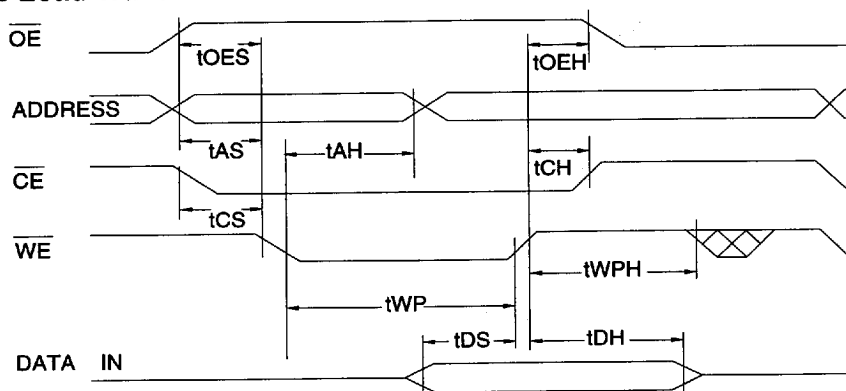
Output Test Load



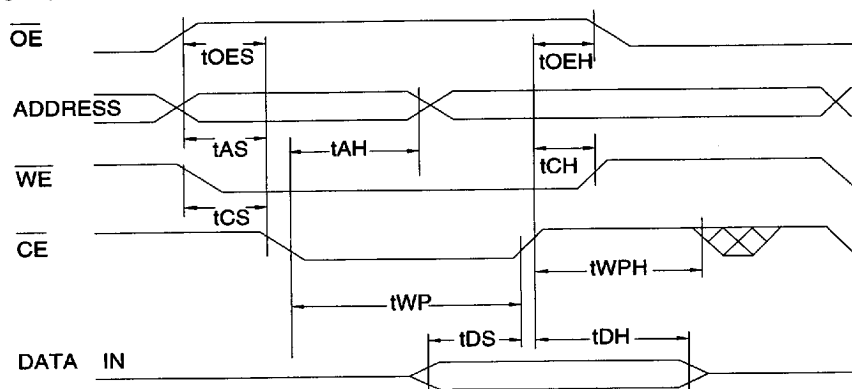
A.C. Byte Load Characteristics

Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	90		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns
t_{WPH}	Write Pulse Width High	100		ns

A.C. Byte Load Waveforms- $\overline{WE}$ Controlled



A.C. Byte Load Waveforms- $\overline{CE}$ Controlled

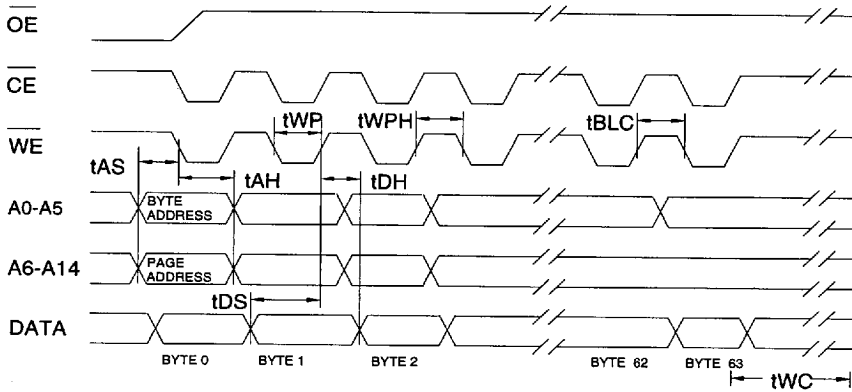


Program Cycle Characteristics

Symbol	Parameter	Min	Max	Units
t _{WC}	Write Cycle Time		10	ms
t _{AS}	Address Set-up Time	0		ns
t _{AH}	Address Hold Time	50		ns
t _{DS}	Data Set-up Time	50		ns
t _{DH}	Data Hold Time	0		ns
t _{WP}	Write Pulse Width	90		ns
t _{BLC}	Byte Load Cycle Time		150	μs
t _{WPH}	Write Pulse Width High	100		ns

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Program Cycle Waveforms ^(1,2,3)

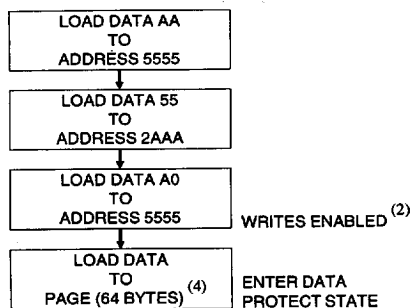


- Notes:
1. A6 through A14 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
 2. OE must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
 3. All bytes that are not loaded within the page being programmed will be erased to FF.

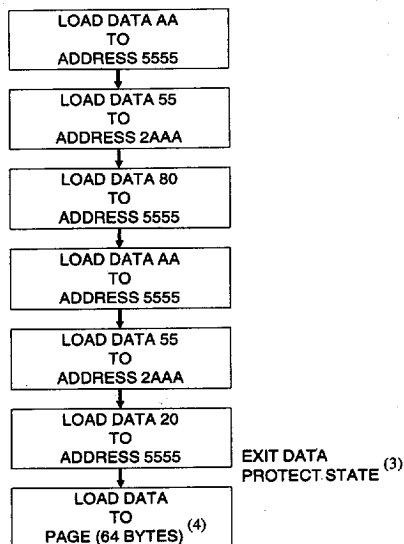


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Software Data Protection Enable Algorithm ⁽¹⁾



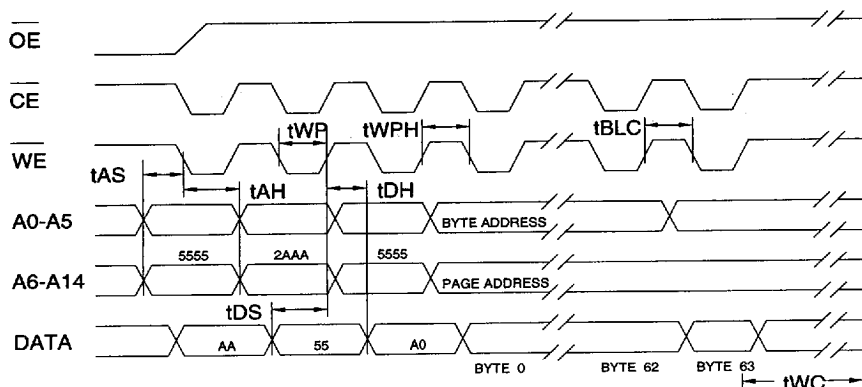
Software Data Protection Disable Algorithm ⁽¹⁾



Notes for software program code:

1. Data Format: I/O7 - I/O0 (Hex);
Address Format: A14 - A0 (Hex).
2. Data Protect state will be activated at end of program cycle.
3. Data Protect state will be deactivated at end of program period.
4. 64 bytes of data **must** be loaded.

Software Protected Program Cycle Waveform ^(1,2,3)



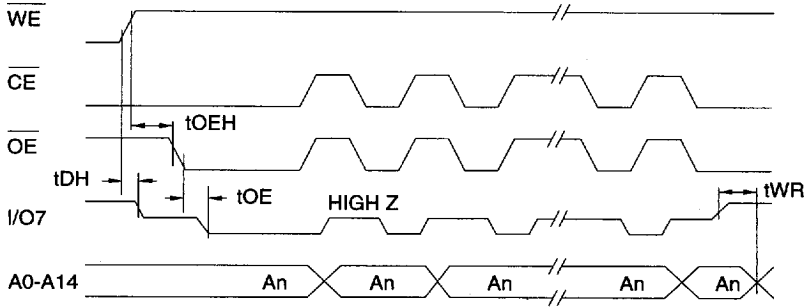
- Notes:
1. A6 through A14 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
 2. $\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
 3. All bytes that are not loaded within the page being programmed will be erased to FF.

Data Polling Characteristics⁽¹⁾

Symbol	Parameter	Min	Typ	Max	Units
t _{DH}	Data Hold Time	0			ns
t _{OE}	$\overline{\text{OE}}$ Hold Time	10			ns
t _{OE}	$\overline{\text{OE}}$ to Output Delay ⁽²⁾				ns
t _{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in A.C. Read Characteristics.

Data Polling Waveforms



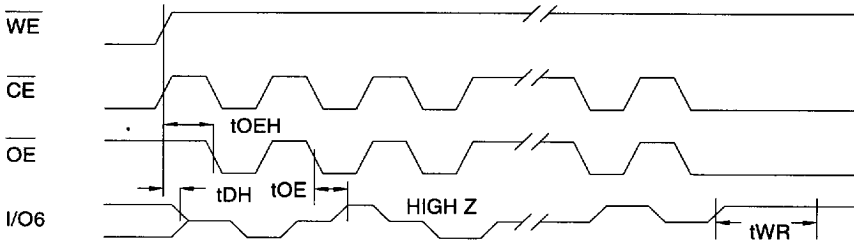
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Toggle Bit Characteristics⁽¹⁾

Symbol	Parameter	Min	Typ	Max	Units
t _{DH}	Data Hold Time	0			ns
t _{OE}	$\overline{\text{OE}}$ Hold Time	10			ns
t _{OE}	$\overline{\text{OE}}$ to Output Delay ⁽²⁾				ns
t _{OEHP}	$\overline{\text{OE}}$ High Pulse	150			ns
t _{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in A.C. Read Characteristics.

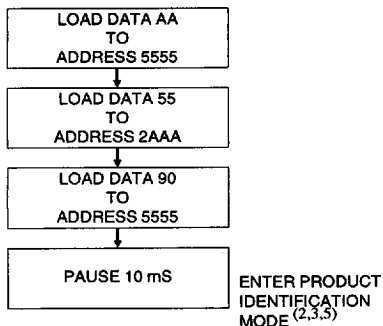
Toggle Bit Waveforms^(1,2,3)



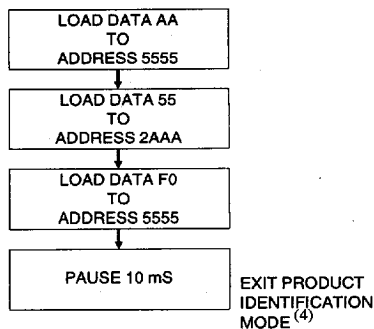
Notes:
1. Toggling either $\overline{\text{OE}}$ or $\overline{\text{CE}}$ or both $\overline{\text{OE}}$ and $\overline{\text{CE}}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.



Software Product Identification Entry ⁽¹⁾



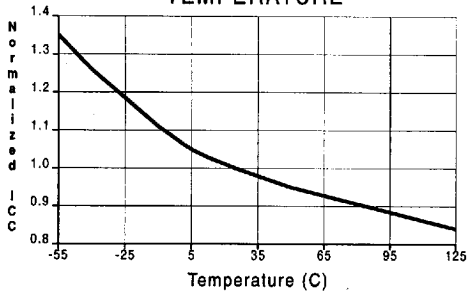
Software Product Identification Exit ⁽¹⁾



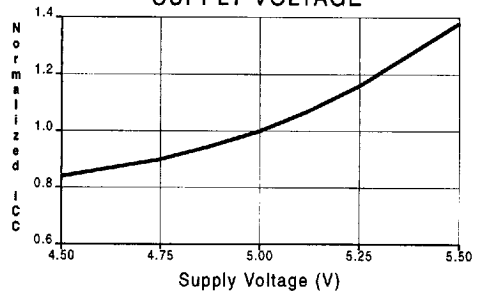
Notes for software product identification:

1. Data Format: I/O7 - I/O0 (Hex);
Address Format: A14 - A0 (Hex).
2. A1 - A14 = V_{IL}.
Manufacture Code is read for A0 = V_{IL};
Device Code is read for A0 = V_{IH}.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.
5. Manufacturer Code: 1F
Device Code: DC

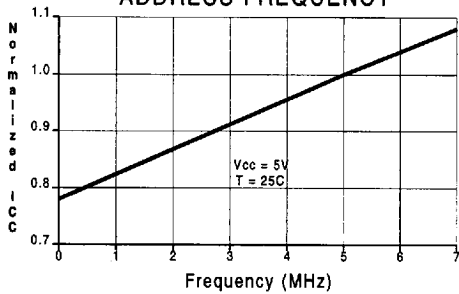
NORMALIZED SUPPLY CURRENT vs.
TEMPERATURE



NORMALIZED SUPPLY CURRENT vs.
SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT vs.
ADDRESS FREQUENCY





Ordering Information

t _{ACC} (ns)	I _{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	50	0.3	AT29C256-90DC AT29C256-90JC AT29C256-90PC	28D6 32J 28P6	Commercial (0° to 70°C)
90	50	0.3	AT29C256-90TC	28T	Commercial (0° to 70°C)
			AT29C256-90JI AT29C256-90TI	32J 28T	Industrial (-40° to 85°C)
120	50	0.3	AT29C256-12DC AT29C256-12JC AT29C256-12LC AT29C256-12PC AT29C256-12TC	28D6 32J 32L 28P6 28T	Commercial (0° to 70°C)
			AT29C256-12DI AT29C256-12JI AT29C256-12LI AT29C256-12PI	28D6 32J 32L 28P6	Industrial (-40° to 85°C)
150	50	0.3	AT29C256-15DC AT29C256-15JC AT29C256-15LC	28D6 32J 32L	Commercial (0° to 70°C)
			AT29C256-15DI AT29C256-15JI AT29C256-15LI AT29C256-15PI AT29C256-15TI	28D6 32J 32L 28P6 28T	Industrial (-40° to 85°C)
200	50	0.3	AT29C256-20DC AT29C256-20JC AT29C256-20LC AT29C256-20PC	28D6 32J 32L 28P6	Commercial (0° to 70°C)
			AT29C256-20DI AT29C256-20JI AT29C256-20LI AT29C256-20PI	28D6 32J 32L 28P6	Industrial (-40° to 85°C)
250	50	0.3	AT29C256-25DC AT29C256-25JC AT29C256-25LC AT29C256-25PC	28D6 32J 32L 28P6	Commercial (0° to 70°C)
250	50	0.3	AT29C256-25DI AT29C256-25JI AT29C256-25LI AT29C256-25PI	28D6 32J 32L 28P6	Industrial (-40° to 85°C)

Package Type

28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28T	28 Lead, Thin Small Outline Package (TSOP)

5-14

AT29C256

■ 1074177 0008241 25T ■