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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



**9- to 12-bit Selectable, $\pm 0.5^{\circ}\text{C}$ Accurate
Digital Temperature Sensor with Nonvolatile Registers**

DATASHEET

[See Applicable Errata in Section 15.](#)

Features

- Single 2.7V - 5.5V supply
- Measures temperature from -55°C to $+125^{\circ}\text{C}$
- Highly accurate temperature measurements requiring no external components
 - $\pm 0.5^{\circ}\text{C}$ accuracy (typical) over the 0°C to $+85^{\circ}\text{C}$ range
 - $\pm 1.0^{\circ}\text{C}$ accuracy (typical) over the -25°C to $+105^{\circ}\text{C}$ range
 - $\pm 2.0^{\circ}\text{C}$ accuracy (typical) over the -40°C to $+125^{\circ}\text{C}$ range
- User-configurable resolution
 - 9 to 12 bits (0.5°C to 0.0625°C)
- User-configurable high and low temperature limits
- Nonvolatile registers to retain user-configured or pre-defined power-up defaults
- Register locking to prevent erroneous misconfiguration
- Register lockdown for permanent, non-changeable device configuration
- ALERT output pin for indicating temperature alarms
- 2-wire I²C and SMBus™ compatible serial interface
 - Supports SMBus Timeout
 - Supports SMBus Alert and Alert Response Address (ARA)
 - Selectable addressing allows up to eight devices on the same bus
- Built-in noise suppression filtering for clock and data input signals
- Low power dissipation
 - $75\mu\text{A}$ active current (typical) during temperature measurements
- Shutdown mode to minimize power consumption
 - $1\mu\text{A}$ shutdown current (typical)
- One-shot mode for single temperature measurement while in Shutdown mode
- Pin and software compatible to industry-standard LM75-type devices
- Industry standard green (Pb/Halide-free/RoHS compliant) package options
 - 8-lead SOIC (150-mil)
 - 8-lead MSOP (3 x 3mm)
 - 8-pad Ultra Thin DFN (UDFN - 2 x 3 x 0.6mm)

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1. Description

The Atmel® AT30TS750 is a complete, precise temperature monitoring device designed for use in a variety of applications that require the measuring of local temperatures as an integral part of the system's function and/or reliability. The AT30TS750 device combines a high-precision digital temperature sensor, programmable high and low temperature alarms, and a 2-wire I²C and SMBus (System Management Bus) compatible serial interface into a single, compact package.

The temperature sensor can measure temperatures over the full -55°C to +125°C temperature range and has a typical accuracy as precise as ±0.5°C from 0°C to +85°C. The result of the digitized temperature measurements are stored in one of the AT30TS750's internal registers, which is readable at any time through the device's serial interface.

The AT30TS750 utilizes flexible, user-programmable internal registers to configure the temperature sensor's performance and response to high and low temperature conditions. The device also contains a set of Nonvolatile Registers to retain the configuration and temperature limit settings even after the device has been power cycled, thereby eliminating the need for the device to be reconfigured after each Power-up operation. This additional flexibility permits the device to run self-contained and not rely upon a host controller for device configuration.

A dedicated alarm output activates if the temperature measurement exceeds the user-defined temperature and fault count limits. To reduce current consumption and save power, the AT30TS750 features a Shutdown mode that turns off all internal circuitry except for the internal power-on reset (POR) and serial interface circuits. The device can also be configured to power-up in the Shutdown mode to ensure that the device remains in a low-power state until the user wishes to perform temperature measurements.

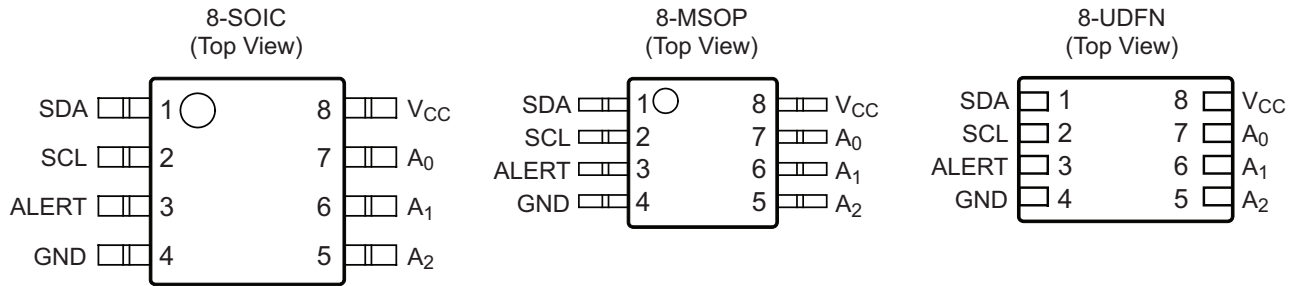
The AT30TS750 is factory-calibrated and requires no external components to measure temperature. With its flexibility and high-degree of accuracy, the AT30TS750 is ideal for extended temperature measurements in a wide variety of communication, computer, consumer, environmental, industrial, and instrumentation applications.

2. Pin Descriptions and Pinouts

Table 1. Pin Description

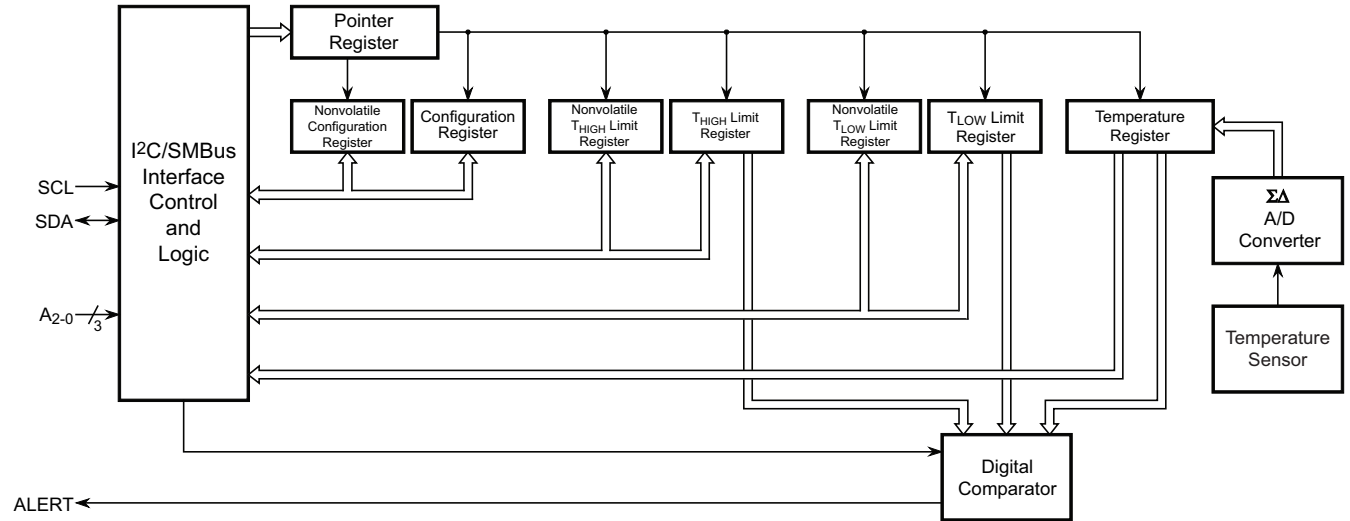
Symbol	Name and Function	Asserted State	Type
SCL	<p>Serial Clock: This pin is used to provide a clock to the device and is used to control the flow of data to and from the device. Command and input data present on the SDA pin is always latched in on the rising edge of SCL, while output data on the SDA pin is always clocked out on the falling edge of SCL.</p> <p>The SCL pin must either be forced high when the serial bus is idle or pulled-high using an external pull-up resistor.</p>	—	Input
SDA	<p>Serial Data: The SDA pin is an open-drain bidirectional input/output pin used to serially transfer data to and from the device.</p> <p>The SDA pin must be pulled-high using an external pull-up resistor and may be wire-ANDed with any number of other open-drain or open-collector pins from other devices on the same bus.</p>	—	Input/Output
ALERT	<p>Alert: The ALERT pin is an open-drain output pin used to indicate when the temperature goes beyond the user-programmed temperature limits. The ALERT pin can be operated in one of two different modes (Interrupt or Comparator mode) as defined by the CMP/INT bit in the Configuration Register. The ALERT pin defaults to an active-low output upon device power-up or reset but can be reconfigured as an active-high output by setting the POL bit in the Configuration Register.</p> <p>This pin can be wire-ANDed together with ALERT pins from other devices on the same bus. When wire-ANDing pins together, the ALERT pin should be configured as an active-low output so that when a single ALERT pin on the common alert bus goes active, the entire common alert bus will go low and the host controller will be properly notified since other ALERT pins that may be in the inactive-high state will not mask the true alert signal. In an SMBus environment, the SMBus host can respond by sending an SMBus ARA (Alert Response Address) command to determine which device on the SMBus generated the alert signal.</p> <p>The ALERT pin must be pulled-high using an external pull-up resistor even when it is not used. Care must also be taken to prevent this pin from being shorted directly to ground without a resistor at any time whether during testing or normal operation.</p>	—	Output
A ₂₋₀	<p>Address Inputs: The A₂₋₀ pins are used to select the device address and correspond to the three least-significant bits (LSBs) of the I²C/SMBus 7-bit slave address. These pins can be directly connected in any combination to V_{CC} or GND, and by utilizing the A₂₋₀ pins, up to eight devices may be addressed on a single bus.</p> <p>The A₂₋₀ pins are internally pulled to GND and may be left floating. However, it is highly recommended that the A₂₋₀ pins always be directly connected to V_{CC} or GND to ensure a known address state.</p>	—	Input
V _{CC}	<p>Device Power Supply: The V_{CC} pin is used to supply the source voltage to the device. Operations at invalid V_{CC} voltages may produce spurious results and should not be attempted.</p>	—	Power
GND	<p>Ground: The ground reference for the power supply. GND should be connected to the system ground.</p>	—	Power

Figure 1. Pin Configurations



3. Block Diagram

Figure 3-1. Block Diagram



4. Device Communication

The AT30TS750 operates as a slave device and utilizes a simple 2-wire I²C and SMBus compatible digital serial interface to communicate with a host controller, commonly referred to as the bus Master. The Master initiates and controls all Read and Write operations to the slave devices on the serial bus, and both the Master and the slave devices can transmit and receive data on the bus.

The serial interface is comprised of just two signal lines: Serial Clock (SCL) and Serial Data (SDA). The SCL pin is used to receive the clock signal from the Master, while the bidirectional SDA pin is used to receive command and data information from the Master as well as to send data back to the Master. Data is always latched into the AT30TS750 on the rising edge of SCL and always output from the device on the falling edge of SCL. Both the SCL and SDA pin incorporate integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise.

All command and data information is transferred with the Most-Significant Bit (MSB) first. During bus communication, one data bit is transmitted every clock cycle, and after eight bits (one byte) of data has been transferred, the receiving device must respond with either an acknowledge (ACK) or a no-acknowledge (NACK) response bit during a ninth clock cycle (ACK/NACK clock cycle) generated by the Master. Therefore, nine clock cycles are required for every one byte of data transferred. There are no unused clock cycles during any Read or Write operation, so there must not be any interruptions or breaks in the data stream during each data byte transfer and ACK or NACK clock cycle.

During data transfers, data on the SDA pin must only change while SCL is low, and the data must remain stable while SCL is high. If data on the SDA pin changes while SCL is high, then either a Start or a Stop condition will occur. Start and Stop conditions are used to initiate and end all serial bus communication between the Master and the slave devices. The number of data bytes transferred between a Start and a Stop condition is not limited and is determined by the Master.

In order for the serial bus to be idle, both the SCL and SDA pins must be in the logic-high state at the same time.

4.1 Start Condition

A Start condition occurs when there is a high-to-low transition on the SDA pin while the SCL pin is stable in the logic-high state. The Master uses a Start condition to initiate any data transfer sequence, and the Start condition must precede any command. The AT30TS750 will continuously monitor the SDA and SCL pins for a Start condition, and the device will not respond unless one is given.

4.2 Stop Condition

A Stop condition occurs when there is a low-to-high transition on the SDA pin while the SCL pin is stable in the logic-high state. The Master uses the Stop condition to end a data transfer sequence to the AT30TS750 which will subsequently return to the idle state. The Master can also utilize a repeated Start condition instead of a Stop condition to end the current data transfer if the Master will perform another operation.

4.3 Acknowledge (ACK)

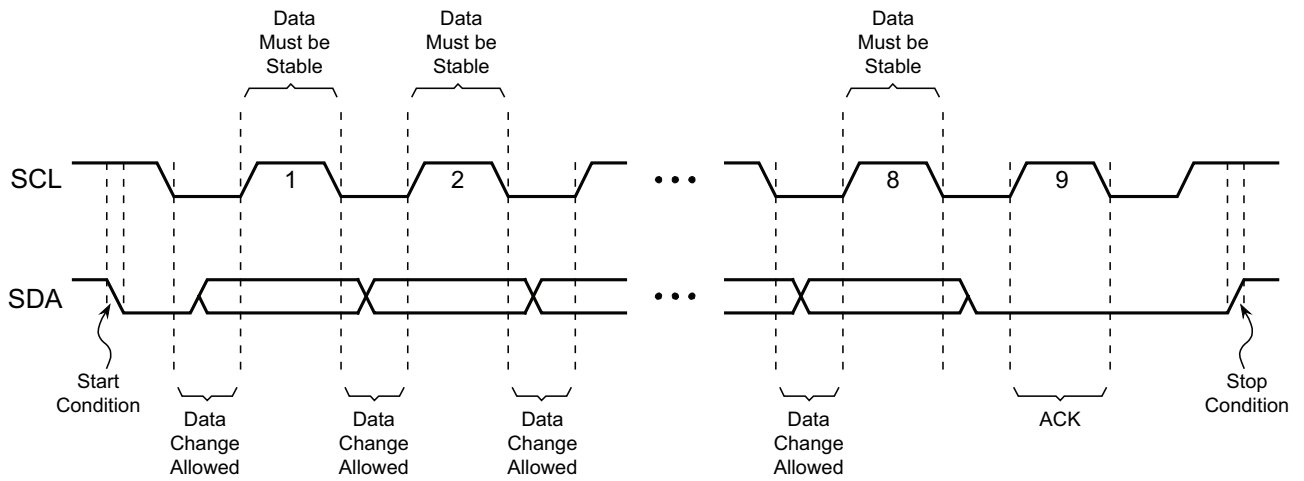
After every byte of data received, the AT30TS750 must acknowledge to the Master that it has successfully received the data byte by responding with an ACK. This is accomplished by the Master first releasing the SDA line and providing the ACK/NACK clock cycle (a ninth clock cycle for every byte). During the ACK/NACK clock cycle, the AT30TS750 must output a Logic 0 (ACK) for the entire clock cycle such that the SDA line must be stable in the logic-low state during the entire high period of the clock cycle.

4.4 No-Acknowledge (NACK)

When the AT30TS750 is transmitting data to the Master, the Master can indicate that it is done receiving data and wants to end the operation by sending a NACK response to the AT30TS750 instead of an ACK response. This is accomplished by the Master outputting a Logic 1 during the ACK/NACK clock cycle, at which point the AT30TS750 will release the SDA line so that the Master can then generate a Stop condition.

In addition, the AT30TS750 can use a NACK to respond to the Master instead of an ACK for certain invalid operation cases such as an attempt to write to a Read-only Register (e.g. an attempt to write to the Temperature Register).

Figure 4-1. Start, Stop, and ACK



5. Device Operation

Commands used to configure and control the operation of the AT30TS750 are sent to the device from the Master via the serial interface. Likewise, the Master can read the temperature data from the AT30TS750 via the serial interface. However, since multiple slave devices can reside on the serial bus, each slave device must have its own unique 7-bit address so that the Master can access each device independently.

For the AT30TS750, the first four MSBs of its 7-bit address are the device type identifier and are fixed at 1001. The remaining three LSBs correspond to the states of the hard-wired $A_{2:0}$ address pins.

Example: If the $A_{2:0}$ pins are connected to GND, then the 7-bit device address would be 1001000.

In order for the Master to select and access the AT30TS750, the Master must first initiate a Start condition. Following the Start condition, the Master must output the device address byte. The device address byte consists of the 7-bit device address plus a Read/Write (R/\overline{W}) control bit, which indicates whether the Master will be performing a Read or a Write to the AT30TS750. If the R/\overline{W} control bit is a Logic 1, then the Master will be reading data from the AT30TS750. Alternatively, if the R/\overline{W} control bit is a Logic 0, then the Master will be writing data to the AT30TS750.

Table 5-1. Atmel AT30TS750 Address Byte

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Device Type Identifier				Device Address			Read/Write
1	0	0	1	A2	A1	A0	R/\overline{W}

If the 7-bit address sent by the Master matches that of the AT30TS750, then the device will respond with an ACK after it has received the full address byte. If there is an address mismatch, then the AT30TS750 will respond with a NACK and return to the idle state.

5.1 Temperature Measurements

The AT30TS750 utilizes a band-gap type temperature sensor with an internal sigma-delta Analog-to-Digital Converter (ADC) to measure and convert the temperature reading into a digital value with a selectable resolution as high as 0.0625°C. The measured temperature is calibrated in degrees Celsius; therefore, a lookup table or conversion routine is necessary for applications that wish to deal in degrees Fahrenheit.

The result of the digitized temperature measurements are stored in the internal Temperature Register of the AT30TS750, which is readable at any time through the device's serial interface. When in the normal operating mode, the device performs continuous temperature measurements and updates the contents of the Temperature Register (see [Section 6.2 "Temperature Register" on page 16](#)) after each analog-to-digital conversion.

The resolution of the temperature measurement data can be configured to 9, 10, 11, or 12 bits which corresponds to temperature increments of 0.5°C, 0.25°C, 0.125°C, and 0.0625°C, respectively. Selecting the temperature resolution is done by setting the R1 and R0 bits in the Configuration Register (see [Section 6.3 "Configuration Register" on page 18](#)). The ADC conversion time does increase with each bit of higher resolution, so careful consideration should be given to the resolution versus conversion time relationship. The resolution after device power-up or reset will revert to what was previously selected using the NVR1 and NVR0 bits of the Nonvolatile Configuration Register bits prior to when the device was powered-down or reset.

With 12 bits of resolution, the AT30TS750 can theoretically measure a temperature range of 255°C (-128°C to +127°C); however, the device is only designed to measure temperatures over a range of -55°C to +125°C.

5.2 Temperature Alarm

After the measured temperature value has been stored into the Temperature Register, the data will be compared with both the high and low temperature limits defined by the values stored in the T_{HIGH} Limit Register and T_{LOW} Limit Register. If the comparison results in a valid fault condition (see Section 5.2.1 “Fault Tolerance Limits” on page 10), then the device will activate the ALERT output pin.

The polarity and function of the ALERT pin can be configured by using specific bits in the Configuration Register. The polarity of the ALERT pin is controlled by the POL bit in the Configuration Register while the function of the ALERT pin changes based on the Alarm Thermostat mode, which can be configured to either Comparator mode (see Section 5.2.2 “Comparator Mode” on page 11) or Interrupt mode (see Section 5.2.3 “Interrupt Mode” on page 12) by using the CMP/INT bit in the Configuration Register. After the device powers up or resets, the NVPOL and NVCMP/INT bits of the Nonvolatile Configuration Register are automatically copied into the POL and CMP/INT bits of the Configuration Register; therefore, the ALERT pin polarity and function will revert back to the settings defined by the NVPOL and NVCMP/INT bits prior to when the device was powered-down or reset.

The value of the high temperature limit stored in the T_{HIGH} Limit Register must be greater than the value of the low temperature limit stored in the T_{LOW} Limit Register in order for the ALERT function to work properly; otherwise, the ALERT pin will output erroneous results and will falsely signal temperature alarms.

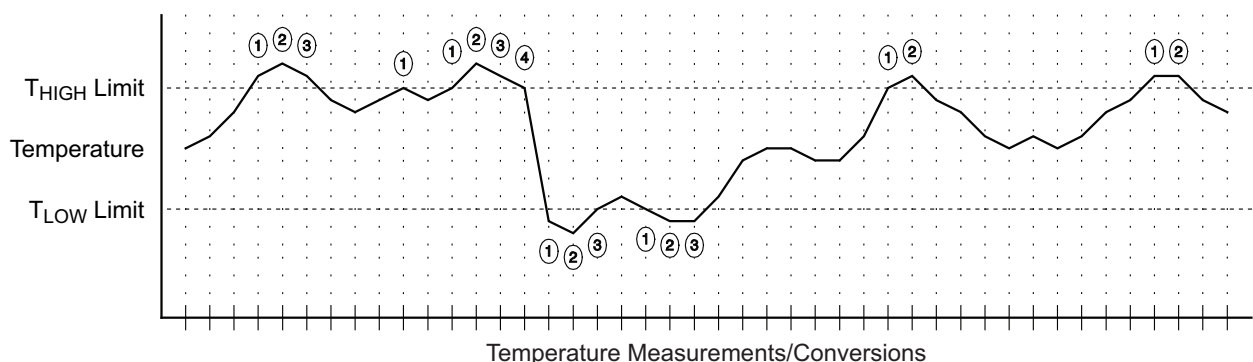
5.2.1 Fault Tolerance Limits

A temperature fault occurs if the measured temperature meets or exceeds either the high temperature limit set by the T_{HIGH} Limit Register or the low temperature limit set by the T_{LOW} Limit Register. To prevent false alarms due to environmental or temperature noise, the device incorporates a fault tolerance queue that requires consecutive temperature faults to occur before resulting in a valid fault condition. The fault tolerance queue value is controlled by the FT1 and FT0 bits in the Configuration Register and can be set to a single fault count of 1 or a count of 2, 4, or 6 consecutive faults.

An internal counter that automatically increments after a temperature fault is used to determine if the fault tolerance queue setting has been met. After incrementing the fault counter, the device will compare the count to the fault tolerance queue setting to see if a valid fault condition should be triggered. Once a valid fault condition occurs, the device will activate the ALERT output pin. If the most recent measured temperature does not meet or exceed the high or low temperature limit, then the internal fault counter will be reset back to zero.

Figure 5-1 shows a sample temperature profile and how each temperature fault would impact the internal fault counter.

Figure 5-1. Fault Count Example



After the device powers up or resets, the NVFT1 and NVFT0 bits of the Nonvolatile Configuration Register are automatically copied into the FT1 and FT0 bits of the Configuration Register; therefore, the Fault Tolerance Queue setting will revert back to the settings defined by the NVFT1 and NVFT0 bits prior to when the device was powered down or reset.

5.2.2 Comparator Mode

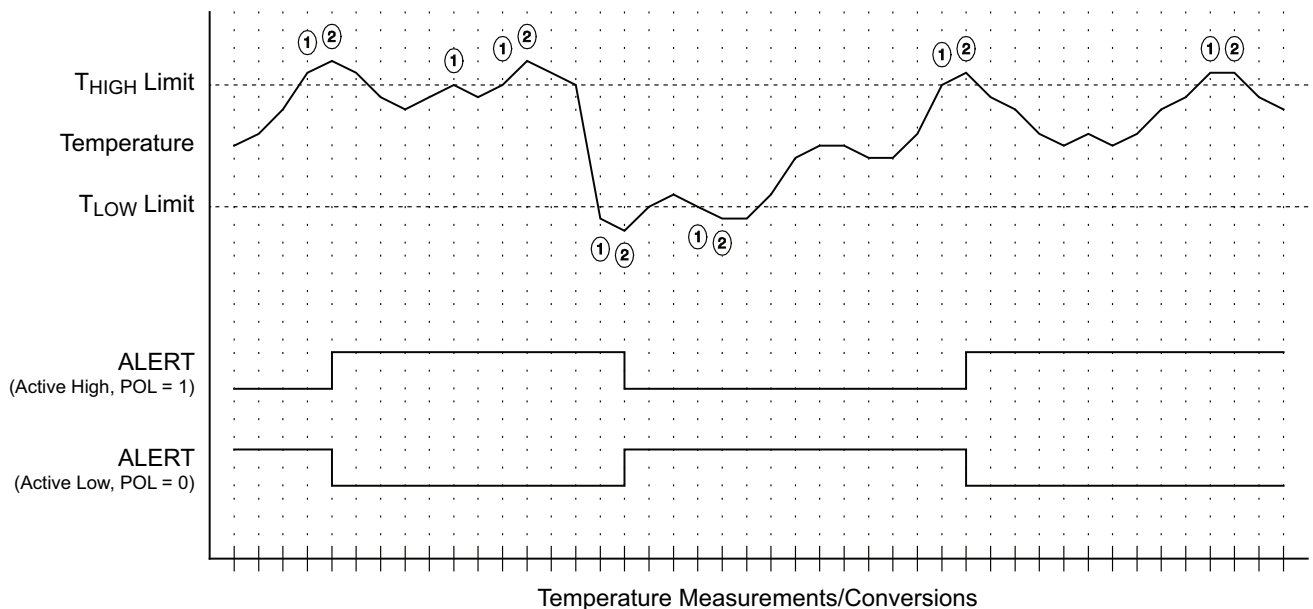
When the device operates in the Comparator mode, then the ALERT pin goes active if the measured temperature meets or exceeds the high temperature limit set by the T_{HIGH} Limit Register and a valid fault condition exists (the consecutive number of temperature faults has been reached). The ALERT pin will return to the inactive state after the measured temperature drops below the T_{LOW} Limit Register value the appropriate number of times to create a subsequent valid fault condition. The ALERT pin only changes state based on the high and low temperature limits and fault conditions; reading from or writing to any register or putting the device into Shutdown mode will not affect the state of the ALERT pin. The high temperature limit set by the T_{HIGH} Limit Register must be greater than the low temperature limit set by the T_{LOW} Limit Register in order for the ALERT pin to activate correctly.

If switching from Interrupt mode to Comparator mode while the ALERT pin is already active, then the ALERT pin will remain active until the measured temperature is below the T_{LOW} Limit Register value the appropriate number of times to create a valid fault condition.

The ALERT pin will return to the inactive state if the device receives the General Call Reset command. When reset, the contents of the Nonvolatile Configuration Register will be copied into the Configuration Register; therefore, the device may or may not return to the Comparator mode depending on the setting of the NVCMP/INT bit in the Nonvolatile Configuration Register.

Figure 5-2 illustrates both the active high and active low ALERT pin response for a sample temperature profile with the device configured for the Comparator mode and a fault tolerance queue setting of two.

Figure 5-2. Comparator Mode (Fault Tolerance Queue = 2)



5.2.3 Interrupt Mode

Similar to the Comparator mode, when the device operates in the Interrupt mode, the ALERT pin will go active if the measured temperature meets or exceeds the high temperature limit set by the T_{HIGH} Limit Register and a valid fault condition exists (the consecutive number of temperature faults has been reached). Unlike the Comparator mode, however, the ALERT pin will remain active until one of three normal operation events takes place: any one of the device's registers is read, the device responds to an SMBus Alert Response Address (ARA), or the device is put into Shutdown mode.

Once the ALERT pin returns to the inactive state, it will not go active again until the measured temperature drops below the low temperature limit set by the T_{LOW} Limit Register for the appropriate number of consecutive faults. Again, the ALERT pin will remain active until one of the device's registers is read, the device responds to an SMBus ARA, or the device is placed into the Shutdown mode.

After the ALERT pin becomes inactive again, the cycle will repeat itself with the ALERT pin going active after the measured temperature meets or exceeds the T_{HIGH} Limit Register value for the proper number of consecutive faults. This process is cyclical between T_{HIGH} and T_{LOW} temperature alarms (e.g. T_{HIGH} event, ALERT clear, T_{LOW} event, ALERT clear, T_{HIGH} event, ALERT clear, T_{LOW} event, etc.).

In order for the ALERT pin to normally become active for the first time in the Interrupt Mode, the first event must be a T_{HIGH} temperature alarm event. Therefore, even if the measured temperature initially starts off between the T_{HIGH} and T_{LOW} limits and then drops below the T_{LOW} temperature limit and has met valid fault conditions, the ALERT pin will still not go active. The high temperature limit set by the T_{HIGH} Limit Register must be greater than the low temperature limit set by the T_{LOW} Limit Register in order for the ALERT pin to activate correctly.

If switching from Comparator mode to Interrupt Mode while the ALERT pin is already active, then the ALERT pin will remain active until it is cleared by one of the events already detailed: any one of the device's registers is read, the device responds to an SMBus Alert Response Address (ARA), or the device is put into Shutdown Mode. The ALERT pin will also return to the inactive state if the device receives the General Call Reset command. When reset, the contents of the Nonvolatile Configuration Register will be copied into the Configuration Register; therefore, the device may or may not return to the Interrupt mode depending on the setting of the NVCMP/INT bit in the Nonvolatile Configuration Register.

Figures 5-3 and Figure 5-4 show both the active high and active low ALERT pin response for a sample temperature profile with the device configured for the Interrupt mode and a fault tolerance queue setting of two. Figure 5-4 illustrates how the ALERT pin output would look if there was a longer delay between the ALERT trigger and the reading of a register.

Figure 5-3. Interrupt Mode (Fault Tolerance Queue = 2)

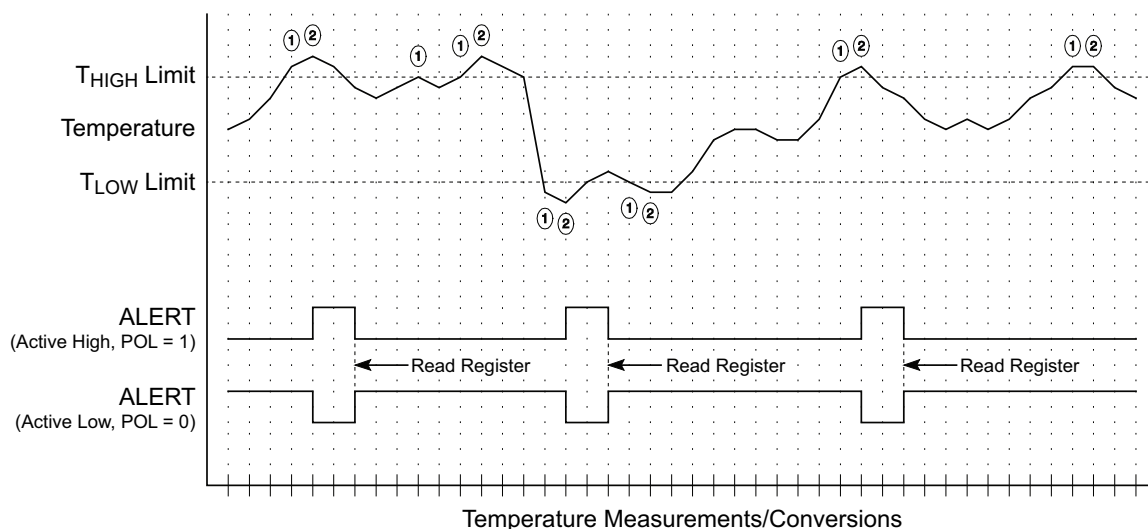
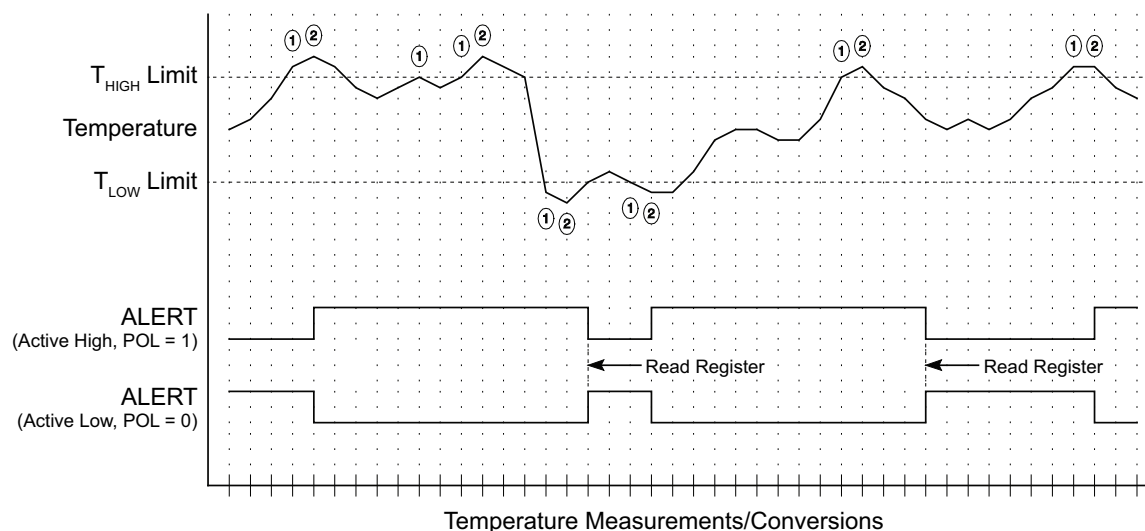


Figure 5-4. Interrupt Mode (Fault Tolerance Queue = 2) Delay Before Reading Register



5.3 Shutdown Mode

To reduce current consumption and save power, the device features a Shutdown mode that disables all internal device circuitry except for the serial interface and POR circuits. While in the Shutdown mode, the internal temperature sensor is not active, so no temperature measurements will be made. Entering and exiting the Shutdown mode is controlled by the SD bit in the Configuration Register.

Entering the Shutdown mode can affect the ALERT pin depending on the Alarm Thermostat mode. If the device is configured to operate in the Interrupt mode, then the ALERT pin will go inactive when the device enters the Shutdown mode. However, the ALERT pin will not change states if the device is operating in the Comparator mode.

The fault count information will not change when the device enters or exits the Shutdown mode. Therefore, the number of previous temperature faults recorded by the internal fault counter will be retained unless the device is power-cycled or reset. When exiting the Shutdown mode, the ALERT pin will go active if operating in Interrupt mode, a valid fault condition exists, and the T_{HIGH} and T_{LOW} event cycles are maintained (i.e. T_{HIGH} event before entering Shutdown mode followed by a T_{LOW} event when exiting Shutdown mode).

The device can be powered-down while in the Shutdown mode so that it will remain in the Shutdown mode after the subsequent Power-up operation. This is accomplished by setting the NVSD bit in the Nonvolatile Configuration Register to the Logic 1 state prior to power-down. Upon power-up or reset, the device will first copy the contents of the Nonvolatile Data Registers into the Volatile Data Registers, after which the device will perform a single temperature measurement and store the result in the Temperature Register. After this process is complete, the device will re-enter the Shutdown mode.

5.3.1 One-shot Mode

The AT30TS750 features a One-shot Temperature mode that allows the device to perform a single temperature measurement while in the Shutdown mode. By keeping the device in the Shutdown mode and utilizing the One-shot mode, the AT30TS750 can remain in a lower power state and only go active to take temperature measurements on an as-needed basis. The internal fault counter will be updated when taking a temperature measurement using the One-shot mode; therefore, a valid fault condition can be generated by the One-shot temperature measurements. If operating in Comparator mode, then the fault condition will cause the ALERT pin to go either active or inactive depending on if the fault condition is a result of a T_{HIGH} or T_{LOW} event. If operating in Interrupt mode, the fault condition will cause the ALERT pin to pulse active for a short duration of time to indicate a T_{HIGH} or T_{LOW} event has occurred. The ALERT pin will then return to the inactive state.

The One-shot mode is controlled using the OS bit in the Configuration Register (see [Section 6.3.1 "OS Bit" on page 19](#)).

6. Registers

The AT30TS750 contains eight registers (a Pointer Register and seven data registers) that are used to control the operational mode and performance of the temperature sensor, store the user-defined high and low temperature limits, and store the digitized temperature measurements. All accesses to the device are performed using these eight registers. In order to read from and write to one of the device's seven data registers, the user must first select a desired data register by utilizing the Pointer Register.

The device incorporates both volatile and nonvolatile versions of the Configuration Register, the T_{LOW} Limit Register, and the T_{HIGH} Limit Register. Upon device power-up or reset, the AT30TS750 will copy the contents of the Nonvolatile Data Registers into the Volatile Data Registers. Both the volatile and Nonvolatile Data Registers can be modified separately provided that the registers are not locked or locked down; however, all temperature sensor related operations, such as responses to high and low temperature conditions, are based on the settings stored in the volatile versions of the registers only. Therefore, if the Nonvolatile Data Registers are updated with new values, then the contents of the Nonvolatile Data Registers should be copied to the Volatile Data Registers (see [Section 9.1 “Copy Nonvolatile Registers to Volatile Registers”](#) on page 32)

Table 6-1. Registers

Register	Address	Read/Write	Size	Power-on Default	Factory Default
Pointer Register	n/a	W	8-bit	00h	n/a
Temperature Register	00h	R	16-bit	0000h	n/a
Configuration Register	01h	R/W	16-bit	Copy of Nonvolatile Configuration Register	n/a
T_{LOW} Limit Register	02h	R/W	16-bit	Copy of Nonvolatile T_{LOW} Limit Register	n/a
T_{HIGH} Limit Register	03h	R/W	16-bit	Copy of Nonvolatile T_{HIGH} Limit Register	n/a
Nonvolatile Configuration Register	11h	R/W	16-bit	Last Programmed State	0000h
Nonvolatile T_{LOW} Limit Register	12h	R/W	16-bit	Last Programmed State	4B00h (75°C)
Nonvolatile T_{HIGH} Limit Register	13h	R/W	16-bit	Last Programmed State	5000h (80°C)

The Configuration Register, despite being 16-bits wide, is compatible to industry standard LM75-type temperature sensors that use an 8-bit wide register in that only the first 8-bits of the Configuration Register need to be written to or read from.

6.1 Pointer Register

The 8-bit Write-only Pointer Register is used to address and select which one of the device's seven data registers (Temperature Register, Configuration Register, T_{LOW} Limit Register, T_{HIGH} Limit Register, Nonvolatile Configuration Register, Nonvolatile T_{LOW} Limit Register, or Nonvolatile T_{HIGH} Limit Register) will be read from or written to.

For Read operations from the AT30TS750, once the Pointer Register is set to point to a particular data register, it remains pointed to that same data register until the Pointer Register value is changed.

Example: If the user sets the Pointer Register to point to the Temperature Register, then all subsequent reads from the device will output data from the Temperature Register until the Pointer Register value is changed.

For Write operations to the AT30TS750, the Pointer Register value must be refreshed each time a write to the device is to be performed, even if the same data register is going to be written to a second time in a row.

Example: If the Pointer Register is set to point to the Configuration Register, once the subsequent Write operation to the Configuration Register has completed, the user cannot write again into the Configuration Register without first setting the Pointer Register value again. As long as a Write operation is to be performed, the device will assume that the Pointer Register value is the first data byte received after the address byte.

Since only seven data registers are available for access, only the five LSBs (P4-P0) of the Pointer Register are used; the remaining three bits (P7-P5) of the Pointer Register should always be set to zero to allow for future migration paths to other temperature sensor devices that have more than seven data registers. In addition, the device incorporates additional commands that are decoded in lieu of the Pointer Register byte. Therefore, if bits P7-P5 are not set as zero when setting the value of the Pointer Register byte, the device may interpret the data as one of the additional commands. Table 6-2 shows the bit assignments of the Pointer Register and the associated pointer addresses of the data registers available. Attempts to write any values other than those listed in Table 6-2 into the Pointer Register will be ignored by the device, and the contents of the Pointer Register will not be changed. The device will respond back to the Master with a NACK to indicate that the device received an invalid Pointer Register byte.

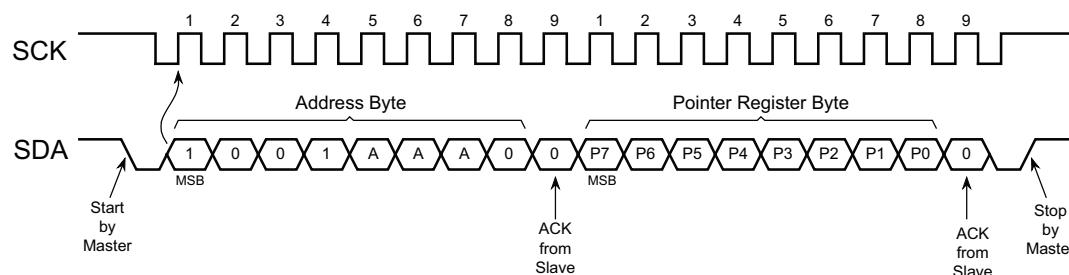
Table 6-2. Pointer Register and Address Assignments

Pointer Register Value								Associated Address	Register Selected
P7	P6	P5	P4	P3	P2	P1	P0		
0	0	0	0	0	0	0	0	00h	Temperature Register
0	0	0	0	0	0	0	1	01h	Configuration Register
0	0	0	0	0	0	1	0	02h	T _{LOW} Limit Register
0	0	0	0	0	0	1	1	03h	T _{HIGH} Limit Register
0	0	0	1	0	0	0	1	11h	Nonvolatile Configuration Register
0	0	0	1	0	0	1	0	12h	Nonvolatile T _{LOW} Limit Register
0	0	0	1	0	0	1	1	13h	Nonvolatile T _{HIGH} Limit Register

To set the value of the Pointer Register, the Master must first initiate a Start condition followed by the AT30TS750 device address byte (1001AAA0 where "AAA" corresponds to the hard-wired A₂₋₀ address pins). After the AT30TS750 has received the proper address byte, the device will send an ACK to the Master. The Master must then send the appropriate data byte to the AT30TS750 to set the value of the Pointer Register.

After device power-up or reset, the Pointer Register defaults to 00h which is the Temperature Register location; therefore, the Temperature Register can be read from immediately after device power-up or reset without having to set the Pointer Register. If the device is configured to power-up in the Shutdown mode, then the device will make a single temperature measurement immediately after power-up so that valid temperature data can be output from the Temperature Register.

Figure 6-1. Write Pointer Register



6.2 Temperature Register

The Temperature Register is a 16-bit Read-only Register that stores the digitized value of the most recent temperature measurement. The temperature data value is represented in the two's complement format, and, depending on the resolution selected, up to 12 bits of data will be available for output with the remaining LSBs being fixed in the Logic 0 state. The Temperature Register can be read at any time, and since temperature measurements are performed in the background, reading the Temperature Register does not affect any other operation that may be in progress.

The MSB (bit 15) of the Temperature Register contains the sign bit of the measured temperature value with a zero indicating a positive number and a one indicating a negative number. The remaining MSBs of the Temperature Register contain the temperature value in the two's complement format. [Table 6-3](#) details the Temperature Register format for the different selectable resolutions, and [Table 6-4](#) shows some examples for 12-bit resolution Temperature Register data values and the associated temperature readings.

Table 6-3. Temperature Register Format

Resolution	Upper Byte								Lower Byte							
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
12 bits	Sign	TD	TD	TD	TD	TD	TD	TD	TD	TD	TD	TD	0	0	0	0
11 bits	Sign	TD	TD	TD	TD	TD	TD	TD	TD	TD	TD	0	0	0	0	0
10 bits	Sign	TD	TD	TD	TD	TD	TD	TD	TD	TD	0	0	0	0	0	0
9 bits	Sign	TD	TD	TD	TD	TD	TD	TD	TD	0	0	0	0	0	0	0

Note: TD = Temperature Data

Table 6-4. 12-bit Resolution Temperature Data/Values Examples

Temperature	Temperature Register Data	
	Binary Value	Hex Value
+125°C	0111 1101 0000 0000	7D00h
+100°C	0110 0100 0000 0000	6400h
+75°C	0100 1011 0000 0000	4B00h
+50.5°C	0011 0010 1000 0000	3200h
+25.25°C	0001 1001 0100 0000	1940h
+10.125°C	0000 1010 0010 0000	0A20h
+0.0625°C	0000 0000 0001 0000	0010h
0°C	0000 0000 0000 0000	0000h
-0.0625°C	1111 1111 1111 0000	FFF0h
-10.125°C	1111 0101 1110 0000	F5E0h
-25.25°C	1110 0111 1100 0000	E7C0h
-50.5°C	1100 1110 1000 0000	CE80h
-55°C	1100 1001 0000 0000	C900h

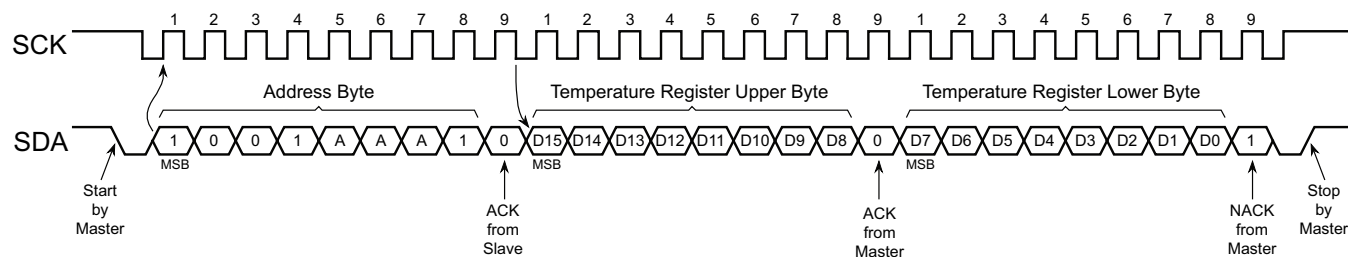
After each temperature measurement and digital conversion is complete, the new temperature data is loaded into the Temperature Register if the register is not currently being read. If a read is in progress, then the previous temperature data will be output.

In order to read the most recent temperature measurement data, the Pointer Register must be set or have been previously set to 00h. If the Pointer Register has already been set to 00h, the Temperature Register can be read by having the Master first initiate a Start condition followed by the AT30TS750 device address byte (1001AAA1 where "AAA" corresponds to the hard-wired A₂₋₀ address pins). After the AT30TS750 has received the proper address byte, the device will send an ACK to the Master. The Master can then read the upper byte of the Temperature Register. After the upper byte of the Temperature Register has been clocked out of the AT30TS750, the Master must send an ACK to indicate that it is ready for the lower byte of the temperature data. The AT30TS750 will then clock out the lower byte of the Temperature Register, after which the Master must send a NACK to end the operation. When the AT30TS750 receives the NACK, it will release the SDA line so that the Master can send a Stop or repeated Start condition. If the Master does not send a NACK but instead sends an ACK after the lower byte of the Temperature Register has been clocked out, then the device will repeat the sequence by outputting new temperature data starting with the upper byte of the Temperature Register.

If 8-bit temperature resolution is satisfactory, then the lower byte of the Temperature Register does not need to be read. In this case, the Master would send a NACK instead of an ACK after the upper byte of the Temperature Register has been clocked out of the AT30TS750. When the AT30TS750 receives the NACK, the device will know that it should not send out the lower byte of the Temperature Register and will instead release the SDA line so the Master can send a Stop or repeated Start condition.

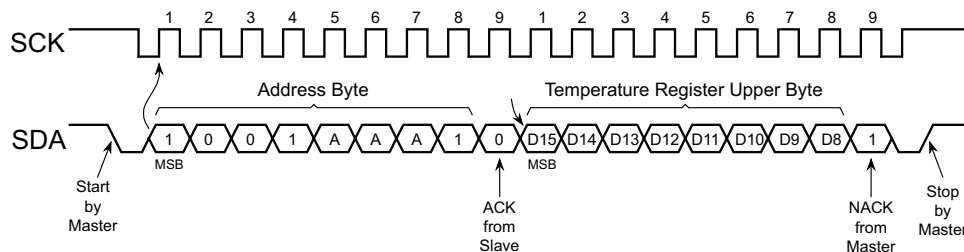
The Temperature Register defaults to 0000h after device power-up or reset; therefore, the system should wait the maximum conversion time (t_{CONV}) for the selected resolution before attempting to read valid temperature data. If the device is configured to power-up in the Shutdown mode, then the device will make a single temperature measurement immediately after power-up so that valid temperature data can be output from the Temperature Register after the maximum t_{CONV} time. Since the Temperature Register is a Read-only register, any attempts to write to the register will be ignored, and the device will subsequently respond by sending a NACK back to the Master for any data bytes that are sent.

Figure 6-2. Read Temperature Register – 16 Bits



Note: Assumes the Pointer Register was previously set to point to the Temperature Register.

Figure 6-3. Read Temperature Register – 8 Bits



Note: Assumes the Pointer Register was previously set to point to the Temperature Register.

6.3 Configuration Register

The Configuration Register is used to control key operational modes and settings of the device such as the One-shot mode, the temperature conversion resolution, the fault tolerance queue, the ALERT pin polarity, the Alarm Thermostat mode, and the Shutdown mode. The Configuration Register is a 16-bit wide Read/Write Register; however, only the first 8-bits of the register are actually used while the least-significant 8-bits are reserved for future use to provide an upward migration path to other temperature sensor devices that have enhanced features. Since only the most-significant 8-bits of the Configuration Register are used, the device is backwards compatible to industry standard LM75-type temperature sensors that use 8-bit wide registers.

After device power-up or reset, the contents of the most-significant byte (bits 15 through 8) of the Nonvolatile Configuration Register will always be automatically copied into the Configuration Register. Therefore, the Configuration Register settings will match the settings of the Nonvolatile Configuration Register prior to when the device was powered-down or reset. Since the Configuration Register value will always be copied from the Nonvolatile Configuration Register, the Configuration Register can be temporarily changed without affecting subsequent power-up/reset settings. If it is desired for the new Configuration Register settings to become the new power-up/reset settings, then the contents of the Configuration Register can be copied into the most-significant byte of the Nonvolatile Configuration Register by using the copy Volatile Registers to Nonvolatile Registers command (see [Section 9.2 “Copy Volatile Registers to Nonvolatile Registers” on page 33](#)). Please note that when using the copy Volatile Registers to Nonvolatile Registers command, the contents of the T_{HIGH} and T_{LOW} Limit Registers will also be copied into the nonvolatile T_{HIGH} and T_{LOW} Limit Registers.

Table 6-5. Configuration Register

Bit	Name		Type	Description	
15	OS	One-shot Mode	R/W	0	Normal Operation (Default)
				1	Perform One-shot Measurement (Valid in Shutdown Mode Only)
14:13	R1:R0	Conversion Resolution	R/W	00	9-bits (Default)
				01	10-bits
				10	11-bits
				11	12-bits
12:11	FT1:FT0	Fault Tolerance Queue	R/W	00	Alarm after 1 Fault (Default)
				01	Alarm after 2 Consecutive Faults
				10	Alarm after 4 Consecutive Faults
				11	Alarm after 6 Consecutive Faults
10	POL	ALERT Pin Polarity	R/W	0	ALERT Pin is Active Low (Default)
				1	ALERT Pin is Active High
9	CMP/INT	Alarm Thermostat Mode	R/W	0	Comparator Mode (Default)
				1	Interrupt Mode
8	SD	Shutdown Mode	R/W	0	Temperature Sensor Performing Active Measurements (Default)
				1	Temperature Sensor Disabled and Device In Shutdown Mode
7:1	<i>RFU</i>	<i>Reserved for Future Use</i>	R	0	<i>Reserved for Future Use</i>
0	NVRBSY	Nonvolatile Registers Busy	R	0	Nonvolatile Registers are ready for access.
				1	Nonvolatile Registers are busy and cannot be read from or written to.

To set the value of the Configuration Register, the Master must first initiate a Start condition followed by the AT30TS750's device address byte (1001AAA0 where "AAA" corresponds to the hard-wired A₂₋₀ address pins). After the AT30TS750 has received the proper address byte, the device will send an ACK to the Master. The Master must then send the appropriate Pointer Register byte of 01h to select the Configuration Register. After the Pointer Register byte of 01h has been sent, the AT30TS750 will send another ACK to the Master. After receiving the ACK from the AT30TS750, the Master must then send the appropriate data byte to the AT30TS750 to set the value of the Configuration Register. Only the first data byte sent to the AT30TS750 will be recognized as valid data; any subsequent bytes received by the device will simply be ignored. If the Master does not send a complete byte of Configuration Register data prior to issuing a Stop or repeated Start condition, then the AT30TS750 will ignore the data and the contents of the Configuration Register will be unchanged.

In addition to the Master not sending a complete byte of Configuration Register data, writing to the Configuration Register will be ignored and no operation will be performed if the Volatile and Nonvolatile Registers are currently locked (the RLCK bit of the Nonvolatile Configuration Register is in the Logic 1 state) or the Volatile and Nonvolatile Registers are permanently locked down (the RLCKDWN bit of the Nonvolatile Configuration Register is in the Logic 1 state). However, the device will still respond with an ACK to indicate that it received the proper data byte even though the contents of the Configuration Register will not be changed.

6.3.1 OS Bit

The OS bit is used to enable the One-shot Temperature Measurement mode. When a Logic 1 is written to the OS bit while the AT30TS750 is in the Shutdown mode, the device will become active and perform a single temperature measurement and conversion. After the Temperature Register has been updated with the measured temperature data, the device will return to the low-power Shutdown mode and clear the OS bit.

Writing a one to the OS bit when the device is not in the Shutdown mode will have no affect. When reading the Configuration Register, the OS bit will always be read as a Logic 0.

6.3.2 R1:R0 Bits

The R1 and R0 bits are used to select the conversion resolution of the internal sigma-delta ADC. Four possible resolutions can be set to maximize for either higher resolution or faster conversion times. The R1 and R0 bits will be copied from the NVR1 and NVR0 in the Nonvolatile Configuration Register after device power-up or reset, allowing the device to retain the conversion resolution that was previously set by the Nonvolatile Configuration Register prior to power-down or reset.

Table 6-6. Conversion Resolution

R1	R0	Conversion Resolution		Conversion Time
0	0	9 bits	0.5°C	25ms
0	1	10 bits	0.25°C	50ms
1	0	11 bits	0.125°C	100ms
1	1	12 bits	0.0625°C	200ms

6.3.3 FT1:FT0 Bits

The FT1 and FT0 bits are used to set the fault tolerance queue value which defines how many consecutive faults must occur before the ALERT pin will be activated (see [Section 5.2.1 “Fault Tolerance Limits” on page 10](#)). The FT1 and FT0 bit settings provide four different fault values as detailed in [Table 6-7](#). After the device powers up or resets, the FT1 and FT0 bits will be copied from the NVFT1 and NVFT0 in the Nonvolatile Configuration Register; therefore, the fault tolerance queue value will default to whatever value was previously stored in the Nonvolatile Configuration Register prior to Configuration Register power-down or reset.

Table 6-7. Fault Tolerance Queue

FT1	FT0	Consecutive Faults Required
0	0	1
0	1	2
1	0	4
1	1	6

6.3.4 POL Bit

The ALERT pin polarity is controlled by the POL bit. When the POL bit is in the Logic 0 state, the ALERT pin will be an active low output. To configure the ALERT pin as an active high output, the POL bit must be set to the Logic 1 state.

After the device powers up or resets, the POL bit will be copied from the NVPOL bit in the Nonvolatile Configuration Register; therefore, the polarity of the ALERT pin will default to the state defined by the Nonvolatile Configuration Register prior to power-down or reset.

6.3.5 CMP/INT Bit

The CMP/INT bit controls whether the device will operate in the Comparator mode or the Interrupt mode. Setting the CMP/INT bit to the Logic 0 state will put the device into the Comparator mode. Alternatively, when the CMP/INT bit is set to the Logic 1 state, then the device will operate in the Interrupt mode. The function of the ALERT pin changes based on the CMP/INT bit setting.

The CMP/INT bit will be copied from the NVCMP/INT bit in the Nonvolatile Configuration Register after the device powers up or resets. Since the CMP/INT bit is copied from the NVCMP/INT bit, the device will default to whatever mode was selected by the Nonvolatile Configuration Register prior to power-down or reset.

6.3.6 SD Bit

The SD bit is used to enable or disable the device's Shutdown mode. When the SD bit is in the Logic 0 state, the device will be in the normal operational mode and perform continuous temperature measurements and conversions. When the SD bit is set to the Logic 1 state, the device will finish the current temperature measurement and conversion and will store the result in the Temperature Register, after which the device will then enter the Shutdown mode.

Resetting the SD bit back to a Logic 0 will return the device to the normal operating mode.

After the device powers up or resets, the SD bit will be copied from the NVSD bit in the Nonvolatile Configuration Register. Therefore, it is possible for the device to automatically enter the Shutdown mode after power-up or reset by setting the NVSD bit to the Logic 1 state prior to power-down or reset. See [Section 5.3 “Shutdown Mode” on page 13](#) for more details.

6.3.7 NVRBSY

The Ready/Busy status of the Nonvolatile Configuration Register, Nonvolatile T_{LOW} Limit Register, and Nonvolatile T_{HIGH} Limit Register can be determined by reading the NVRBSY bit. When the NVRBSY bit is in the Logic 0 state, then the Nonvolatile Configuration and Limit Registers are available to be read from or written to. When the NVRBSY bit is in the Logic 1 state, the Nonvolatile Registers are busy and cannot be accessed for reading, writing, or copying. Attempting to read the Nonvolatile Registers while the registers are busy will result in erroneous data being output. Similarly, any attempts to write to one of the Nonvolatile Registers while the NVRBSY bit is in the Logic 1 state will result in the data being ignored. Both the copy Nonvolatile Registers to Volatile Registers and the copy Volatile Registers to Nonvolatile Registers commands will also be ignored when the NVRBSY bit is in the Logic 1 state. For more details and a complete list of commands that are and are not allowed while NVRBSY is in the Logic 1 state, see [Section 8. “Operations Allowed During Nonvolatile Busy Status”](#) on page 31.

Figure 6-4. Write to Configuration Register

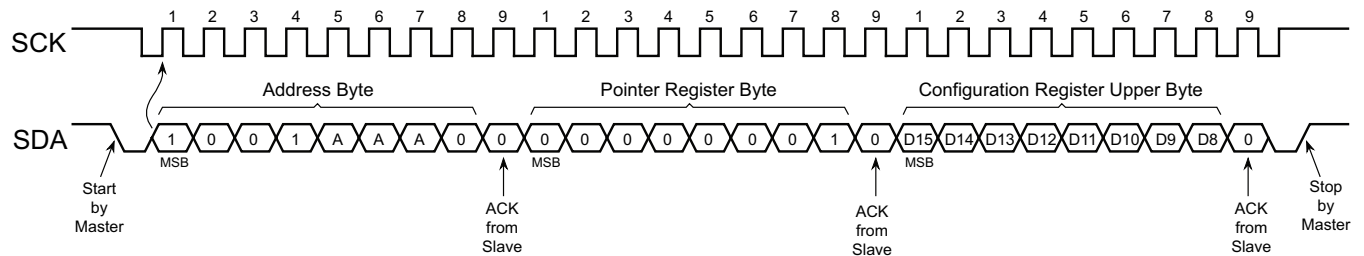
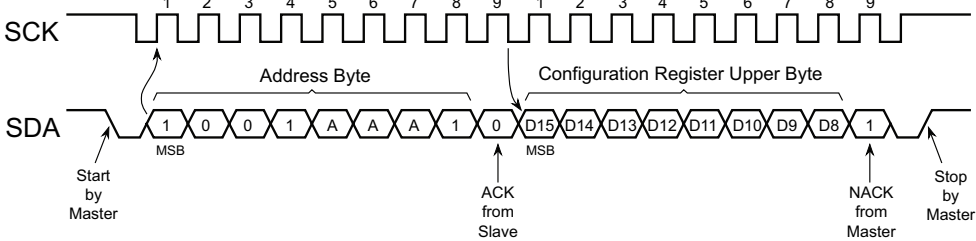


Figure 6-5. Read from Configuration Register



Note: Assumes the Pointer Register was previously set to point to the Configuration Register.

6.4 Nonvolatile Configuration Register

The Nonvolatile Configuration Register is a 16-bit wide Read/Write register used to manage key power-up/reset device settings and operational modes including the locking of the AT30TS750's various registers. The Nonvolatile Configuration Register is used in conjunction with the Configuration Register to control how the device operates. All bits in the Nonvolatile Configuration Register will retain their state even after the device has been powered down or reset. On every power up or reset sequence, the contents of the most-significant byte (bits 15 through 8) of the Nonvolatile Configuration Register will be copied into the Configuration Register, after which all device operations and settings will then be controlled by the Configuration Register. By utilizing the Nonvolatile Configuration Register, the device can power-up or reset in a pre-defined, user-selected operating mode (e.g. Comparator mode, Shutdown mode, etc.) with pre-defined settings (e.g. 12-bit resolution, ALERT pin active high, etc.). Therefore, unlike standard LM75-type temperature sensors, there is no need to update the Configuration Register settings after every power-up or reset.

Since the Nonvolatile Configuration Register utilizes nonvolatile storage cells, care must be taken when updating the register to accommodate the aspects of an associated program time and finite program endurance limit. Power must not be removed from the device during the internally self-timed programming cycle of the register. If power is removed prior to the completion of the programming cycle, then the contents of the register cannot be guaranteed. In addition, the contents of the register may become corrupt if it is programmed more than the maximum allowed number of writes.

Table 6-8. Nonvolatile Configuration Register

Bit	Name		Type	Description
15	NU	Not Used	R	0 Not Used
14:13	NVR1:NVR0	Conversion Resolution	R/W	00 9-bits (Factory Default)
				01 10-bits
				10 11-bits
				11 12-bits
12:11	NVFT1:NVFT0	Fault Tolerance Queue	R/W	00 Alarm after 1 Fault (Factory Default)
				01 Alarm after 2 Consecutive Faults
				10 Alarm after 4 Consecutive Faults
				11 Alarm after 6 Consecutive Faults
10	NVPOL	ALERT Pin Polarity	R/W	0 ALERT Pin is Active Low (Factory Default)
				1 ALERT Pin is Active High
9	NVCMP/INT	Alarm Thermostat Mode	R/W	0 Comparator Mode (Factory Default)
				1 Interrupt Mode
8	NVSD	Shutdown Mode	R/W	0 Temperature Sensor Performing Active Measurements (Factory Default)
				1 Temperature Sensor Disabled and Device in Shutdown Mode
7:3	RFU	Reserved for Future Use		0 Reserved for Future Use
2	RLCKDWN	Register Lockdown	R/W	0 All Configuration and Limit Registers are Not Locked Down (Factory Default)
				1 All Configuration and Limit Registers are permanently locked down (ROM) and can never be modified again.
1	RLCK	Register Lock	R/W	0 All Configuration and Limit Registers are unlocked and can be modified (Factory Default).
				1 all configuration and Limit Registers are locked and cannot be modified.
0	RFU	Reserved for Future Use	R	0 Reserved for Future Use

To set the value of the Nonvolatile Configuration Register, the Master must first initiate a Start condition followed by the AT30TS750 device address byte (1001AAA0 where "AAA" corresponds to the hard-wired A_{2-0} address pins). After the AT30TS750 has received the proper address byte, the device will send an ACK to the Master. The Master must then send the appropriate Pointer Register byte of 11h to select the Nonvolatile Configuration Register. After the Pointer Register byte of 11h has been sent, the AT30TS750 will send another ACK to the Master. After receiving the ACK from the AT30TS750, the Master must then send two data bytes to the AT30TS750 to set the value of the Nonvolatile Configuration Register. Any subsequent bytes sent to the AT30TS750 will simply be ignored by the device. If the Master does not send two complete bytes of Nonvolatile Configuration Register data prior to issuing a Stop or repeated Start condition, then the AT30TS750 will ignore the data and the contents of the Nonvolatile Configuration Register will not be changed.

After the Master has issued a Stop or repeated Start condition, the AT30TS750 will begin the internally self-timed program operation, and the contents of the Nonvolatile Configuration Register will be updated within a time of t_{PROG} . During this time, the NVRBSY bit in the Configuration Register will indicate that the device is busy. If the Master issues a repeated Start condition instead of a Stop condition, the AT30TS750 will abort the operation and the contents of the Nonvolatile Configuration Register will not be changed.

In addition to the Master not sending two complete bytes of data, writing to the Nonvolatile Configuration Register will be ignored and no operation will be performed under the following conditions: the Nonvolatile Registers are already busy (the NVRBSY bit of the Configuration Register is in the Logic 1 state), the Volatile and Nonvolatile Registers are currently locked (the RLCK bit of the Nonvolatile Configuration Register is in the Logic 1 state), or the Volatile and Nonvolatile Registers are permanently locked down (the RLCKDWN bit of the Nonvolatile Configuration Register is in the Logic 1 state). However, the device will still respond with an ACK, except in the case of the Nonvolatile Registers being busy, to indicate that it received the proper data bytes even though the program operation will not be performed. In the case of the Nonvolatile Registers being busy, the device will respond with an ACK to the address and pointer bytes but will then NACK when the data bytes are sent from the Master.

6.4.1 NVR1: NVR0 Bits

The nonvolatile NVR1 and NVR0 bits are used to select the power-up/reset default conversion resolution of the internal sigma-delta ADC. Four possible resolutions can be set to maximize for either higher resolution or faster conversion times. The NVR1 and NVR0 bits are set from the factory to default to the Logic 0 state to retain backwards compatibility to industry-standard LM75-type devices.

Table 6-9. Conversion Resolution

NVR1	NVR0	Conversion Resolution		Conversion Time
0	0	9 bits	0.5°C	25ms
0	1	10 bits	0.25°C	50ms
1	0	11 bits	0.125°C	100ms
1	1	12 bits	0.0625°C	200ms

6.4.2 NVFT1:NVFT0 Bits

The nonvolatile NVFT1 and NVFT0 bits are used to set the power-up/reset default Fault Tolerance Queue value which defines how many consecutive faults must occur before the ALERT pin will be activated (see [Section 5.2.1 “Fault Tolerance Limits” on page 10](#)). The NVFT1 and NVFT0 bit settings provide four different fault values as detailed in [Table 6-10](#). Both the NVFT1 and NVFT0 bits are factory-set to default to the Logic 0 state.

Table 6-10. Fault Tolerance Queue

NVFT1	NVFT0	Consecutive Faults Required
0	0	1
0	1	2
1	0	4
1	1	6

6.4.3 NVPOL Bit

The nonvolatile NVPOL bit controls the power-up/reset default ALERT pin polarity. When the NVPOL bit is set to the Logic 0 state, the ALERT pin will be an active low output after the device powers up or resets. Conversely, when the NVPOL bit is set to the Logic 1 state, the ALERT pin will be an active high output. The NVPOL bit is set from the factory to default to the Logic 0 state.

6.4.4 NVCMP/INT Bit

The nonvolatile NVCMP/INT bit controls whether the device will operate in the Comparator mode or the Interrupt mode after a power-up or reset sequence. Setting the NVCMP/INT bit to the Logic 0 state (the factory default setting) will allow the device to power-up/reset in the Comparator mode. Alternatively, when the NVCMP/INT bit is set to the Logic 1 state, the device will power-up/reset in the Interrupt mode.

6.4.5 NVSD Bit

The nonvolatile NVSD bit is used to enable the device to power-up/reset in the Shutdown mode. When the NVSD bit is in the Logic 0 state, the device will power-up/reset in the normal operational mode and perform continuous temperature measurements and conversions. When the NVSD bit is set to the Logic 1 state, the device will automatically enter the Shutdown mode after a power-up or reset sequence (see [Section 5.3 “Shutdown Mode” on page 13](#) for more details). The NVSD bit is factory-set to the Logic 0 state.

6.4.6 RLCKDWN

The one-time programmable RLCKDWN bit controls whether or not both the volatile and nonvolatile versions of the configuration and limit registers will be permanently locked down. Once the RLCKDWN bit is set to the Logic 1 state, the Configuration Register, T_{LOW} Limit Register, T_{HIGH} Limit Register, Nonvolatile Configuration Register, Nonvolatile T_{LOW} Limit Register, and Nonvolatile T_{HIGH} Limit Register will be locked down and can never be modified again. Since the RLCKDWN bit is one-time programmable, once the bit is set to the Logic 1 state, it cannot be reset again. The RLCKDWN bit takes priority over the RLCK bit (see [Section 7. “Register Locking” on page 30](#) for more details) and is factory-set to the Logic 0 state.

6.4.7 RLCK

The nonvolatile RLCK bit controls the reversible locking of both the Volatile and Nonvolatile Configuration and Limit Registers. When the RLCK bit is set to the Logic 0 state, the Configuration Register, T_{LOW} Limit Register, T_{HIGH} Limit Register, Nonvolatile Configuration Register, Nonvolatile T_{LOW} Limit Register, and Nonvolatile T_{HIGH} Limit Register will be unlocked and can be modified. Alternatively, when the RLCK bit is set to the Logic 1 state, the Volatile and Nonvolatile Configuration and Limit Registers will be locked and cannot be modified. When the registers are locked, only the RLCK bit of the Nonvolatile Configuration Register can be altered and reset back to a Logic 0. Any attempts at changing other bits in the Nonvolatile Configuration Register will be ignored. The RLCK bit is set from the factory to default to the Logic 0 state. See [Section 7. “Register Locking” on page 30](#) for more details.

Figure 6-6. Write to Nonvolatile Configuration Register

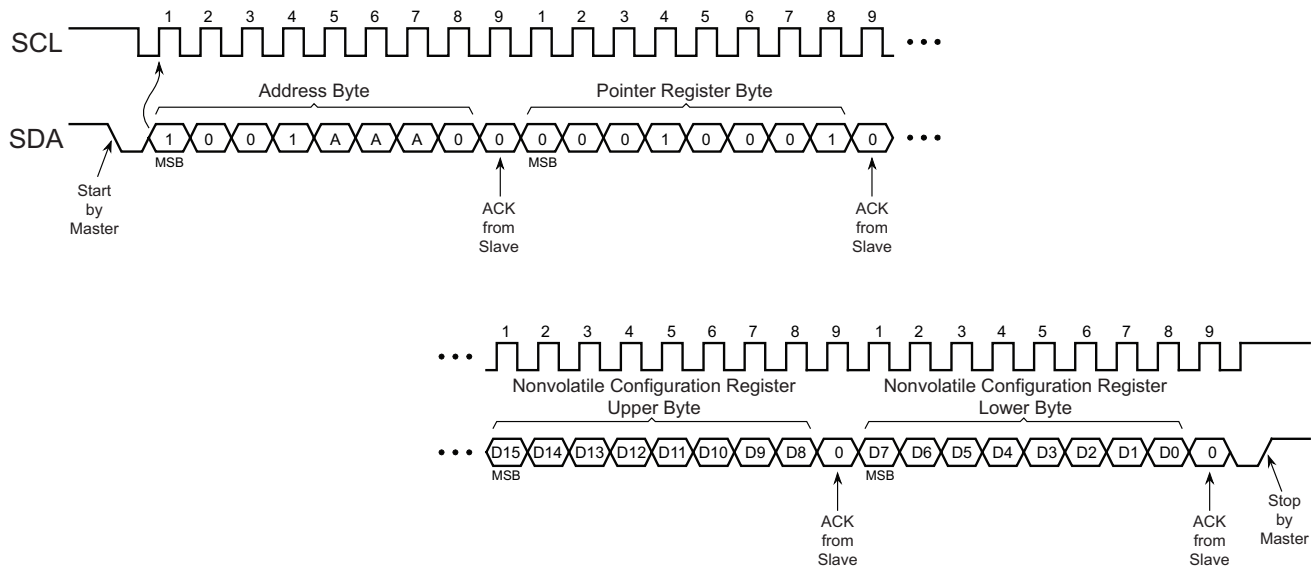
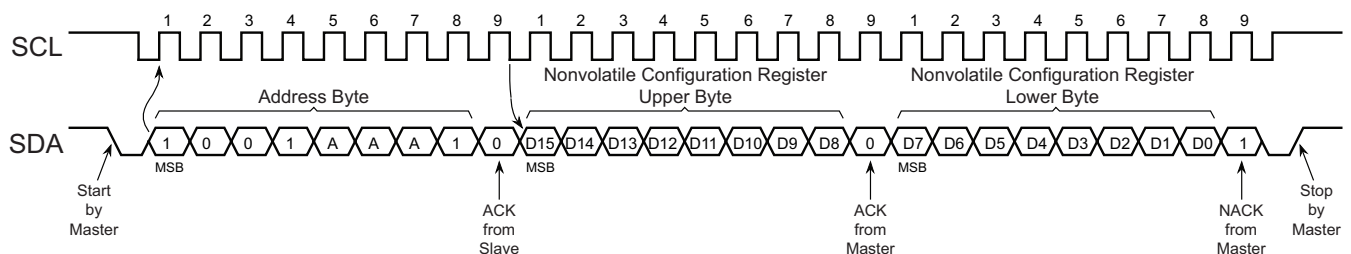


Figure 6-7. Read from Nonvolatile Configuration Register



Note: Assumes the Pointer Register was previously set to point to the Nonvolatile Configuration Register.