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Features

- High Performance, Low Power AVR[®]32 32-Bit Microcontroller
 - 210 DMIPS throughput at 150 MHz
 - 16 KB instruction cache and 16 KB data caches
 - Memory Management Unit enabling use of operating systems
 - Single-cycle RISC instruction set including SIMD and DSP instructions
 - Java Hardware Acceleration
- Pixel Co-Processor
 - Pixel Co-Processor for video acceleration through color-space conversion (YUV<->RGB), image scaling and filtering, quarter pixel motion compensation
- Multi-hierarchy bus system
 - High-performance data transfers on separate buses for increased performance
- Data Memories
 - 32KBytes SRAM
- External Memory Interface
 - SDRAM, DataFlash[™], SRAM, Multi Media Card (MMC), Secure Digital (SD), Compact Flash, Smart Media, NAND Flash
- Direct Memory Access Controller
 - External Memory access without CPU intervention
- Interrupt Controller
 - Individually maskable Interrupts
 - Each interrupt request has a programmable priority and autovector address
- System Functions
 - Power and Clock Manager
 - Crystal Oscillator with Phase-Lock-Loop (PLL)
 - Watchdog Timer
 - Real-time Clock
- 6 Multifunction timer/counters
 - Three external clock inputs, I/O pins, PWM, capture and various counting capabilities
- 4 Universal Synchronous/Asynchronous Receiver/Transmitters (USART)
 - 115.2 kbps IrDA Modulation and Demodulation
 - Hardware and software handshaking
- 3 Synchronous Serial Protocol controllers
 - Supports I2S, SPI and generic frame-based protocols
- Two-Wire Interface
 - Sequential Read/Write Operations, Philips' I2C[®] compatible
- Image Sensor Interface
 - 12-bit Data Interface for CMOS cameras
- Universal Serial Bus (USB) 2.0 High Speed (480 Mbps) Device
 - On-chip Transceivers with physical interface
- 16-bit stereo audio bitstream DAC
 - Sample rates up to 50 kHz
- On-Chip Debug System
 - Nexus Class 3
 - Full speed, non-intrusive data and program trace
 - Runtime control and JTAG interface
- Package/Pins
 - AT32AP7001: 208-pin QFP/ 90 GPIO pins
- Power supplies
 - 1.65V to 1.95V VDDCORE
 - 3.0V to 3.6V VDDIO



AVR[®]32 32-bit Microcontroller

AT32AP7001

Preliminary

Summary

32015GS-AVR32-09/09



1. Part Description

The AT32AP7001 is a complete System-on-chip application processor with an AVR32 RISC processor achieving 210 DMIPS running at 150 MHz. AVR32 is a high-performance 32-bit RISC microprocessor core, designed for cost-sensitive embedded applications, with particular emphasis on low power consumption, high code density and high application performance.

AT32AP7001 implements a Memory Management Unit (MMU) and a flexible interrupt controller supporting modern operating systems and real-time operating systems. The processor also includes a rich set of DSP and SIMD instructions, specially designed for multimedia and telecom applications.

AT32AP7001 incorporates SRAM memories on-chip for fast and secure access. For applications requiring additional memory, external 16-bit SRAM is accessible. Additionally, an SDRAM controller provides off-chip volatile memory access as well as controllers for all industry standard off-chip non-volatile memories, like Compact Flash, Multi Media Card (MMC), Secure Digital (SD)-card, SmartCard, NAND Flash and Atmel DataFlash™.

The Direct Memory Access controller for all the serial peripherals enables data transfer between memories without processor intervention. This reduces the processor overhead when transferring continuous and large data streams between modules in the MCU.

The Timer/Counters includes three identical 16-bit timer/counter channels. Each channel can be independently programmed to perform a wide range of functions including frequency measurement, event counting, interval measurement, pulse generation, delay timing and pulse width modulation.

A pixel co-processor provides color space conversions for images and video, in addition to a wide variety of hardware filter support

Synchronous Serial Controllers provide easy access to serial communication protocols, audio standards like I2S and frame-based protocols.

The Java hardware acceleration implementation in AVR32 allows for a very high-speed Java byte-code execution. AVR32 implements Java instructions in hardware, reusing the existing RISC data path, which allows for a near-zero hardware overhead and cost with a very high performance.

The Image Sensor Interface supports cameras with up to 12-bit data buses.

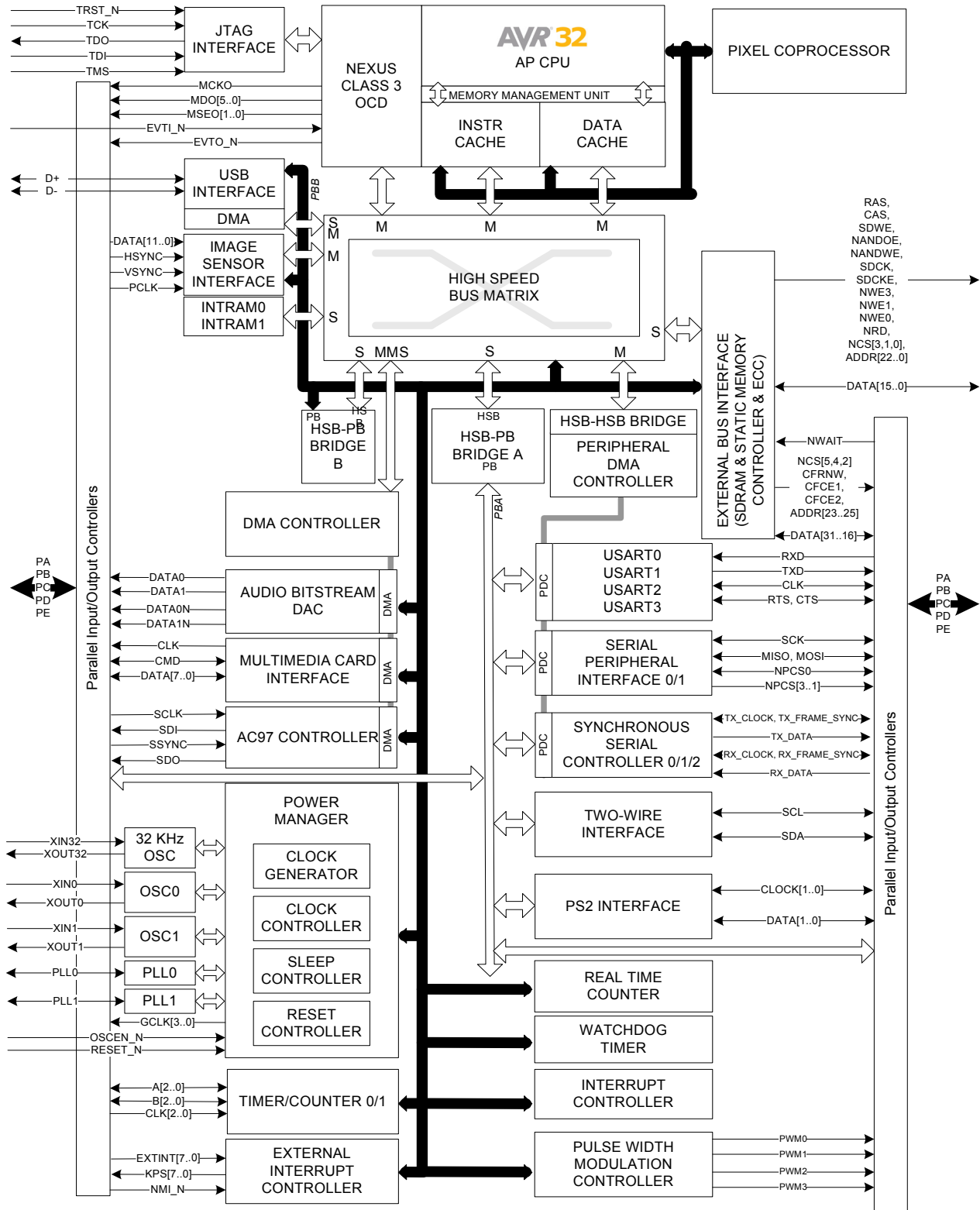
PS2 connectivity is provided for standard input devices like mice and keyboards.

AT32AP7001 integrates a class 3 Nexus 2.0 On-Chip Debug (OCD) System, with non-intrusive real-time trace, full-speed read/write memory access in addition to basic runtime control.

The C-compiler is closely linked to the architecture and is able to utilize code optimization features, both for size and speed.

2. Blockdiagram

Figure 2-1. Blockdiagram



2.0.1 AVR32AP CPU

- 32-bit load/store AVR32B RISC architecture.
 - Up to 15 general-purpose 32-bit registers.
 - 32-bit Stack Pointer, Program Counter and Link Register reside in register file.
 - Fully orthogonal instruction set.
 - Privileged and unprivileged modes enabling efficient and secure Operating Systems.
 - Innovative instruction set together with variable instruction length ensuring industry leading code density.
 - DSP extension with saturating arithmetic, and a wide variety of multiply instructions.
 - SIMD extension for media applications.
- 7 stage pipeline allows one instruction per clock cycle for most instructions.
 - Java Hardware Acceleration.
 - Byte, half-word, word and double word memory access.
 - Unaligned memory access.
 - Shadowed interrupt context for INT3 and multiple interrupt priority levels.
 - Dynamic branch prediction and return address stack for fast change-of-flow.
 - Coprocessor interface.
- Full MMU allows for operating systems with memory protection.
- 16Kbyte Instruction and 16Kbyte data caches.
 - Virtually indexed, physically tagged.
 - 4-way associative.
 - Write-through or write-back.
- Nexus Class 3 On-Chip Debug system.
 - Low-cost NanoTrace supported.

2.0.2 Pixel Coprocessor (PICO)

- Coprocessor coupled to the AVR32 CPU Core through the TCB Bus.
 - Coprocessor number one on the TCB bus.
- Three parallel Vector Multiplication Units (VMU) where each unit can:
 - Multiply three pixel components with three coefficients.
 - Add the products from the multiplications together.
 - Accumulate the result or add an offset to the sum of the products.
- Can be used for accelerating:
 - Image Color Space Conversion.
 - Configurable Conversion Coefficients.
 - Supports packed and planar input and output formats.
 - Supports subsampled input color spaces (i.e 4:2:2, 4:2:0).
 - Image filtering/scaling.
 - Configurable Filter Coefficients.
 - Throughput of one sample per cycle for a 9-tap FIR filter.
 - Can use the built-in accumulator to extend the FIR filter to more than 9-taps.
 - Can be used for bilinear/bicubic interpolations.
 - MPEG-4/H.264 Quarter Pixel Motion Compensation.
- Flexible input Pixel Selector.
 - Can operate on numerous different image storage formats.
- Flexible Output Pixel Inserter.
 - Scales and saturates the results back to 8-bit pixel values.
 - Supports packed and planar output formats.

- Configurable coefficients with flexible fixed-point representation.

2.0.3 Debug and Test system

- IEEE1149.1 compliant JTAG and boundary scan
- Direct memory access and programming capabilities through JTAG interface
- Extensive On-Chip Debug features in compliance with IEEE-ISTO 5001-2003 (Nexus 2.0) Class 3
- Auxiliary port for high-speed trace information
- Hardware support for 6 Program and 2 data breakpoints
- Unlimited number of software breakpoints supported
- Advanced Program, Data, Ownership, and Watchpoint trace supported

2.0.4 DMA Controller

- 2 HSB Master Interfaces
- 3 Channels
- Software and Hardware Handshaking Interfaces
 - 11 Hardware Handshaking Interfaces
- Memory/Non-Memory Peripherals to Memory/Non-Memory Peripherals Transfer
- Single-block DMA Transfer
- Multi-block DMA Transfer
 - Linked Lists
 - Auto-Reloading
 - Contiguous Blocks
- DMA Controller is Always the Flow Controller
- Additional Features
 - Scatter and Gather Operations
 - Channel Locking
 - Bus Locking
 - FIFO Mode
 - Pseudo Fly-by Operation

2.0.5 Peripheral DMA Controller

- Transfers from/to peripheral to/from any memory space without intervention of the processor.
- Next Pointer Support, forbids strong real-time constraints on buffer management.
- Eighteen channels
 - Two for each USART
 - Two for each Serial Synchronous Controller
 - Two for each Serial Peripheral Interface

2.0.6 Bus system

- HSB bus matrix with 10 Masters and 8 Slaves handled
 - Handles Requests from the CPU Icache, CPU Dcache, HSB bridge, HISI, USB 2.0 Controller, DMA Controller 0, DMA Controller 1, and to internal SRAM 0, internal SRAM 1, PB A, PB B, EBI and, USB.

- Round-Robin Arbitration (three modes supported: no default master, last accessed default master, fixed default master)
- Burst Breaking with Slot Cycle Limit
- One Address Decoder Provided per Master
- 2 Peripheral buses allowing each bus to run on different bus speeds.
 - PB A intended to run on low clock speeds, with peripherals connected to the PDC.
 - PB B intended to run on higher clock speeds, with peripherals connected to the DMACA.
- HSB-HSB Bridge providing a low-speed HSB bus running at the same speed as PBA
 - Allows PDC transfers between a low-speed PB bus and a bus matrix of higher clock speeds

An overview of the bus system is given in [Figure 2-1 on page 3](#). All modules connected to the same bus use the same clock, but the clock to each module can be individually shut off by the Power Manager. The figure identifies the number of master and slave interfaces of each module connected to the HSB bus, and which DMA controller is connected to which peripheral.

3. Package and Pinout

3.1 AVR32AP7001

Figure 3-1. 208 QFP Pinout.

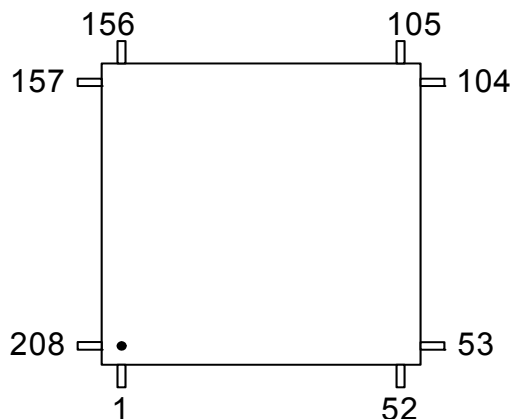


Table 3-1. QFP-208 Package Pinout

1	GND	53	GND	105	GND	157	GND
2	PE17	54	PA23	106	PX13	158	PB10
3	PE18	55	PA24	107	PX14	159	PB11
4	PX47	56	XIN1	108	PX15	160	PB12
5	PX48	57	XOUT1	109	PX16	161	PB13
6	PX49	58	AVDDUSB	110	PX17	162	PB14
7	PX50	59	AGNDUSB	111	PX34	163	PB15
8	PX51	60	VDDIO	112	PX35	164	PB16
9	VDDIO	61	FSDM	113	PX36	165	PB17
10	PX32	62	FSDP	114	PX37	166	PB18
11	PX33	63	GND	115	PX38	167	PB19
12	PX00	64	GND	116	PX18	168	PB20
13	PX01	65	HSDM	117	PX19	169	PB21
14	PX02	66	HSDP	118	PX20	170	PB22
15	PX03	67	VDDCORE	119	PX21	171	PB23
16	PX04	68	GND	120	PX22	172	VDDCORE
17	PX05	69	GND	121	PX23	173	GND
18	VDDCORE	70	VBG	122	PX24	174	GND
19	GND	71	VDDIO	123	PX25	175	PA06
20	TDO	72	PA25	124	PX26	176	PA07
21	TCK	73	PA26	125	VDDIO	177	VDDIO

Table 3-1. QFP-208 Package Pinout (Continued)

22	TMS		74	PA27		126	PX27		178	VDDIO
23	TDI		75	PA28		127	PX28		179	OSCEN_N
24	TRST_N		76	PA29		128	PX29		180	XIN32
25	EVTI_N		77	PA30		129	PX30		181	XOUT32
26	RESET_N		78	PA31		130	PX31		182	AGNDOSC
27	PA00		79	WAKE_N		131	VDDCORE		183	AVDDOSC
28	PA01		80	PB26		132	GND		184	PLL1
29	PA02		81	PB27		133	GND		185	XIN0
30	PA03		82	PB28		134	PE26		186	XOUT0
31	PA04		83	PX53		135	PX39		187	AGNDPLL
32	PA05		84	PX52		136	VDDCORE		188	AVDDPLL
33	PB24		85	PX41		137	GND		189	PLL0
34	PB25		86	GND		138	PX40		190	PE00
35	PA08		87	PE25		139	PX42		191	PE01
36	VDDIO		88	PE24		140	PX43		192	PE02
37	GND		89	PE23		141	PX44		193	PE03
38	PA09		90	PE22		142	PX45		194	PE04
39	PA10		91	PE21		143	PX46		195	PE05
40	PA11		92	PE20		144	PB00		196	PE06
41	PA12		93	PE19		145	PB01		197	PE07
42	PA13		94	PX06		146	PB02		198	PE08
43	PA14		95	PX07		147	PB03		199	PE09
44	PA15		96	PX08		148	PB04		200	PE10
45	PA16		97	PX09		149	PB05		201	PE11
46	PA17		98	PX10		150	PB06		202	PE12
47	PA18		99	PX11		151	PB07		203	PE13
48	PA19		100	PB29		152	PB08		204	PE14
49	PA20		101	PB30		153	PB09		205	PE15
50	PA21		102	PX12		154	PC16		206	PE16
51	PA22		103	PC00		155	PC17		207	No Connect
52	VDDIO		104	VDDIO		156	VDDIO		208	VDDIO

4. Signals Description

The following table gives details on the signal name classified by peripheral. The pinout multiplexing of these signals is given in the Peripheral Muxing table in the Peripherals chapter.

Table 4-1. Signal Description List

Signal Name	Function	Type	Active Level	Comments
Power				
AVDDPLL	PLL Power Supply	Power		1.65 to 1.95 V
AVDDUSB	USB Power Supply	Power		1.65 to 1.95 V
AVDDOSC	Oscillator Power Supply	Power		1.65 to 1.95 V
VDDCORE	Core Power Supply	Power		1.65 to 1.95 V
VDDIO	I/O Power Supply	Power		3.0 to 3.6V
AGNDPLL	PLL Ground	Ground		
AGNDUSB	USB Ground	Ground		
AGNDOSC	Oscillator Ground	Ground		
GND	Ground	Ground		
Clocks, Oscillators, and PLL's				
XIN0, XIN1, XIN32	Crystal 0, 1, 32 Input	Analog		
XOUT0, XOUT1, XOUT32	Crystal 0, 1, 32 Output	Analog		
PLL0, PLL1	PLL 0,1 Filter Pin	Analog		
JTAG				
TCK	Test Clock	Input		
TDI	Test Data In	Input		
TDO	Test Data Out	Output		
TMS	Test Mode Select	Input		
TRST_N	Test Reset	Input	Low	
Auxiliary Port - AUX				
MCKO	Trace Data Output Clock	Output		
MDO0 - MDO5	Trace Data Output	Output		
MSEO0 - MSEO1	Trace Frame Control	Output		
EVTI_N	Event In	Input	Low	

Table 4-1. Signal Description List

Signal Name	Function	Type	Active Level	Comments
EVTO_N	Event Out	Output	Low	
Power Manager - PM				
GCLK0 - GCLK4	Generic Clock Pins	Output		
OSCEN_N	Oscillator Enable	Input	Low	
RESET_N	Reset Pin	Input	Low	
WAKE_N	Wake Pin	Input	Low	
External Interrupt Controller - EIC				
EXTINT0 - EXTINT3	External Interrupt Pins	Input		
NMI_N	Non-Maskable Interrupt Pin	Input	Low	
AC97 Controller - AC97C				
SCLK	AC97 Clock Signal	Input		
SDI	AC97 Receive Signal	Output		
SDO	AC97 Transmit Signal	Output		
SYNC	AC97 Frame Synchronization Signal	Input		
Audio Bitstream DAC - ABDAC				
DATA0 - DATA1	D/A Data Out	Output		
DATAN0 - DATAN1	D/A Inverted Data Out	Output		
External Bus Interface - EBI				
PX0 - PX53	I/O Controlled by EBI	I/O		
ADDR0 - ADDR25	Address Bus	Output		
CAS	Column Signal	Output	Low	
CFCE1	Compact Flash 1 Chip Enable	Output	Low	
CFCE2	Compact Flash 2 Chip Enable	Output	Low	
CFRNW	Compact Flash Read Not Write	Output		
DATA0 - DATA31	Data Bus	I/O		
NANDOE	NAND Flash Output Enable	Output	Low	
NANDWE	NAND Flash Write Enable	Output	Low	
NCS0 - NCS5	Chip Select	Output	Low	

Table 4-1. Signal Description List

Signal Name	Function	Type	Active Level	Comments
NRD	Read Signal	Output	Low	
NWAIT	External Wait Signal	Input	Low	
NWE0	Write Enable 0	Output	Low	
NWE1	Write Enable 1	Output	Low	
NWE3	Write Enable 3	Output	Low	
RAS	Row Signal	Output	Low	
SDA10	SDRAM Address 10 Line	Output		
SDCK	SDRAM Clock	Output		
SDCKE	SDRAM Clock Enable	Output		
SDWE	SDRAM Write Enable	Output	Low	
Image Sensor Interface - ISI				
DATA0 - DATA11	Image Sensor Data	Input		
HSYNC	Horizontal Synchronization	Input		
PCLK	Image Sensor Data Clock	Input		
VSYSN	Vertical Synchronization	Input		
MultiMedia Card Interface - MCI				
CLK	Multimedia Card Clock	Output		
CMD0 - CMD1	Multimedia Card Command	I/O		
DATA0 - DATA7	Multimedia Card Data	I/O		
Parallel Input/Output - PIOA, PIOB, PIOC, PIOD, PIOE				
PA0 - PA31	Parallel I/O Controller PIOA	I/O		
PB0 - PB30	Parallel I/O Controller PIOB	I/O		
PD0 - PD17	Parallel I/O Controller PIOD	I/O		
PE0 - PE26	Parallel I/O Controller PIOE	I/O		
PS2 Interface - PSIF				
CLOCK0 - CLOCK1	PS2 Clock	Input		
DATA0 - DATA1	PS2 Data	I/O		
Serial Peripheral Interface - SPI0, SPI1				

Table 4-1. Signal Description List

Signal Name	Function	Type	Active Level	Comments
MISO	Master In Slave Out	I/O		
MOSI	Master Out Slave In	I/O		
NPCS0 - NPCS3	SPI Peripheral Chip Select	I/O	Low	
SCK	Clock	Output		
Synchronous Serial Controller - SSC0, SSC1, SSC2				
RX_CLOCK	SSC Receive Clock	I/O		
RX_DATA	SSC Receive Data	Input		
RX_FRAME_SYNC	SSC Receive Frame Sync	I/O		
TX_CLOCK	SSC Transmit Clock	I/O		
TX_DATA	SSC Transmit Data	Output		
TX_FRAME_SYNC	SSC Transmit Frame Sync	I/O		
DMA Controller - DMACA				
DMARQ0 - DMARQ3	DMA Requests	Input		
Timer/Counter - TIMER0, TIMER1				
A0	Channel 0 Line A	I/O		
A1	Channel 1 Line A	I/O		
A2	Channel 2 Line A	I/O		
B0	Channel 0 Line B	I/O		
B1	Channel 1 Line B	I/O		
B2	Channel 2 Line B	I/O		
CLK0	Channel 0 External Clock Input	Input		
CLK1	Channel 1 External Clock Input	Input		
CLK2	Channel 2 External Clock Input	Input		
Two-wire Interface - TWI				
SCL	Serial Clock	I/O		
SDA	Serial Data	I/O		
Universal Synchronous Asynchronous Receiver Transmitter - USART0, USART1, USART2, USART3				
CLK	Clock	I/O		

Table 4-1. Signal Description List

Signal Name	Function	Type	Active Level	Comments
CTS	Clear To Send	Input		
RTS	Request To Send	Output		
RXD	Receive Data	Input		
TXD	Transmit Data	Output		
Pulse Width Modulator - PWM				
PWM0 - PWM3	PWM Output Pins	Output		
USB Interface - USBA				
HSDM	High Speed USB Interface Data -	Analog		
FSDM	Full Speed USB Interface Data -	Analog		
HSDP	High Speed USB Interface Data +	Analog		
FSDP	Full Speed USB Interface Data +	Analog		
VBG	USB bandgap	Analog		Connected to a 6810 Ohm \pm 0.5% resistor to ground and a 10 pF capacitor to ground.

5. Power Considerations

5.1 Power Supplies

The AT32AP7001 has several types of power supply pins:

- **VDDCORE pins:** Power the core, memories, and peripherals. Voltage is 1.8V nominal.
- **VDDIO pins:** Power I/O lines. Voltage is 3.3V nominal.
- **VDDPLL pin:** Powers the PLL. Voltage is 1.8V nominal.
- **VDDUSB pin:** Powers the USB. Voltage is 1.8V nominal.
- **VDDOSC pin:** Powers the oscillators. Voltage is 1.8V nominal.

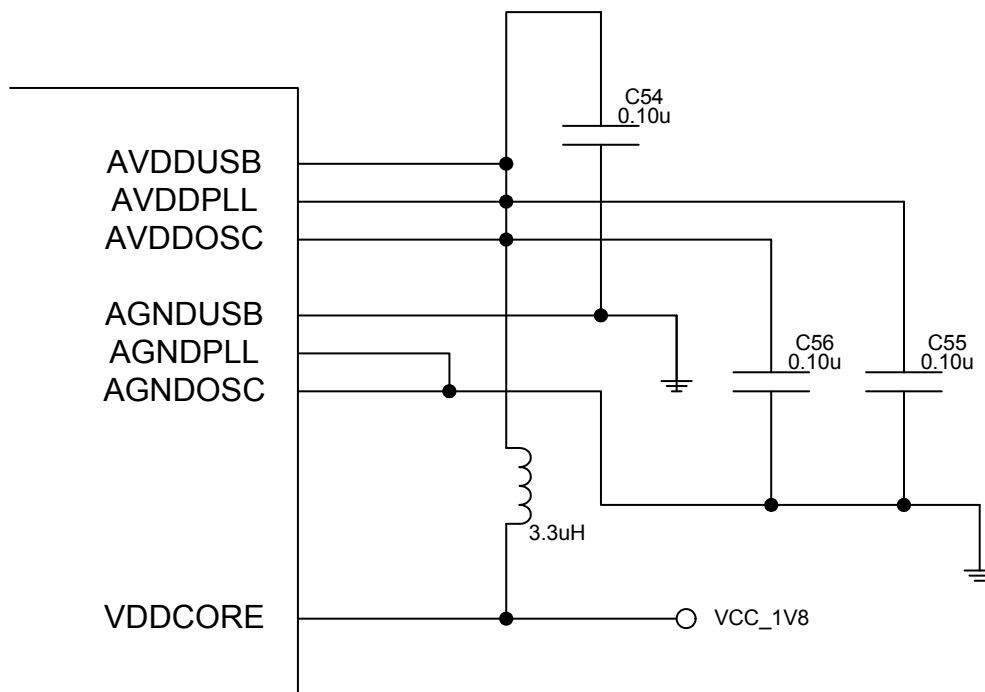
The ground pins GND are common to VDDCORE and VDDIO. The ground pin for VDDPLL is GNDPLL, and the GND pin for VDDOSC is GNDOSC.

See ["Electrical Characteristics" on page 928](#) for power consumption on the various supply pins.

5.2 Power Supply Connections

Special considerations should be made when connecting the power and ground pins on a PCB. [Figure 5-1](#) shows how this should be done.

Figure 5-1. Connecting analog power supplies



6. I/O Line Considerations

6.1 JTAG pins

The TMS, TDI and TCK pins have pull-up resistors. TDO is an output, driven at up to VDDIO, and have no pull-up resistor. The TRST_N pin is used to initialize the embedded JTAG TAP Controller when asserted at a low level. It is a schmitt input and integrates permanent pull-up resistor to VDDIO, so that it can be left unconnected for normal operations.

6.2 WAKE_N pin

The WAKE_N pin is a schmitt trigger input integrating a permanent pull-up resistor to VDDIO.

6.3 RESET_N pin

The RESET_N pin is a schmitt input and integrates a permanent pull-up resistor to VDDIO. As the product integrates a power-on reset cell, the RESET_N pin can be left unconnected in case no reset from the system needs to be applied to the product.

6.4 EVTI_N pin

The EVTI_N pin is a schmitt input and integrates a non-programmable pull-up resistor to VDDIO.

6.5 TWI pins

When these pins are used for TWI, the pins are open-drain outputs with slew-rate limitation and inputs with inputs with spike-filtering. When used as GPIO-pins or used for other peripherals, the pins have the same characteristics as PIO pins.

6.6 PIO pins

All the I/O lines integrate a programmable pull-up resistor. Programming of this pull-up resistor is performed independently for each I/O line through the PIO Controllers. After reset, I/O lines default as inputs with pull-up resistors enabled, except when indicated otherwise in the column “Reset State” of the PIO Controller multiplexing tables.

7. Memories

7.1 Embedded Memories

- **32 Kbyte SRAM**
 - Implemented as two 16Kbyte blocks
 - Single cycle access at full bus speed

7.2 Physical Memory Map

The system bus is implemented as an HSB bus matrix. All system bus addresses are fixed, and they are never remapped in any way, not even in boot. Note that AT32AP7001 by default uses segment translation, as described in the AVR32 Architecture Manual. The 32 bit physical address space is mapped as follows:

Table 7-1. AT32AP7001 Physical Memory Map

Start Address	Size	Device
0x0000_0000	64 Mbyte	EBI SRAM CS0
0x0400_0000	64 Mbyte	EBI SRAM CS4
0x0800_0000	64 Mbyte	EBI SRAM CS2
0x0C00_0000	64 Mbyte	EBI SRAM CS3
0x1000_0000	256 Mbyte	EBI SRAM/SDRAM CS1
0x2000_0000	64 Mbyte	EBI SRAM CS5
0x2400_0000	16 Kbyte	Internal SRAM 0
0x2400_4000	16 Kbyte	Internal SRAM1
0xFF20_0000	1 KByte	DMACA configuration
0xFF30_0000	1 MByte	USBA Data
0xFFE0_0000	1 MByte	PBA
0xFFFF0_0000	1 MByte	PBB

Accesses to unused areas returns an error result to the master requesting such an access.

The bus matrix has the several masters and slaves. Each master has its own bus and its own decoder, thus allowing a different memory mapping per master. The master number in the table below can be used to index the HMATRIX control registers. For example, MCFG2 is associated with the HSB-HSB bridge.

Table 7-2. HSB masters

Master 0	CPU Dcache
Master 1	CPU Icache
Master 2	HSB-HSB Bridge
Master 3	ISI DMA
Master 4	USBA DMA
Master 8	DMAC Master Interface 0
Master 9	DMAC Master Interface 1

Each slave has its own arbiter, thus allowing a different arbitration per slave. The slave number in the table below can be used to index the HMATRIX control registers. For example, SCFG3 is associated with PBB.

Table 7-3. HSB slaves

Slave 0	Internal SRAM 0
Slave 1	Internal SRAM1
Slave 2	PBA
Slave 3	PBB
Slave 4	EBI
Slave 5	USBA data
Slave 7	DMACA configuration

8. Peripherals

8.1 Peripheral address map

Table 8-1. Peripheral Address Mapping

Address		Peripheral Name	Bus
0xFF200000	DMACA	DMA Controller Slave Interface- DMACA	HSB
0xFF300000	USBA	USB Slave Interface - USBA	HSB
0xFFE00000	SPI0	Serial Peripheral Interface - SPI0	PB A
0xFFE00400	SPI1	Serial Peripheral Interface - SPI1	PB A
0xFFE00800	TWI	Two-wire Interface - TWI	PB A
0xFFE00C00	USART0	Universal Synchronous Asynchronous Receiver Transmitter - USART0	PB A
0xFFE01000	USART1	Universal Synchronous Asynchronous Receiver Transmitter - USART1	PB A
0xFFE01400	USART2	Universal Synchronous Asynchronous Receiver Transmitter - USART2	PB A
0xFFE01800	USART3	Universal Synchronous Asynchronous Receiver Transmitter - USART3	PB A
0xFFE01C00	SSC0	Synchronous Serial Controller - SSC0	PB A
0xFFE02000	SSC1	Synchronous Serial Controller - SSC1	PB A
0xFFE02400	SSC2	Synchronous Serial Controller - SSC2	PB A
0xFFE02800	PIOA	Parallel Input/Output 2 - PIOA	PB A
0xFFE02C00	PIOB	Parallel Input/Output 2 - PIOB	PB A
0xFFE03000	PIOC	Parallel Input/Output 2 - PIOC	PB A
0xFFE03400	PIOD	Parallel Input/Output 2 - PIOD	PB A
0xFFE03800	PIOE	Parallel Input/Output 2 - PIOE	PB A

Table 8-1. Peripheral Address Mapping (Continued)

Address		Peripheral Name	Bus
0xFFE03C00	PSIF	PS2 Interface - PSIF	PB A
0xFFFF00000	PM	Power Manager - PM	PB B
0xFFFF00080	RTC	Real Time Counter- RTC	PB B
0xFFFF000B0	WDT	WatchDog Timer- WDT	PB B
0xFFFF00100	EIC	External Interrupt Controller - EIC	PB B
0xFFFF00400	INTC	Interrupt Controller - INTC	PB B
0xFFFF00800	HMATRIX	HSB Matrix - HMATRIX	PB B
0xFFFF00C00	TC0	Timer/Counter - TC0	PB B
0xFFFF01000	TC1	Timer/Counter - TC1	PB B
0xFFFF01400	PWM	Pulse Width Modulation Controller - PWM	PB B
0xFFFF02000	ABDAC	Audio Bitstream DAC - ABDAC	PB B
0xFFFF02400	MCI	MultiMedia Card Interface - MCI	PB B
0xFFFF02800	AC97C	AC97 Controller - AC97C	PB B
0xFFFF02C00	ISI	Image Sensor Interface - ISI	PB B
0xFFFF03000	USBA	USB Configuration Interface - USBA	PB B
0xFFFF03400	SMC	Static Memory Controller - SMC	PB B
0xFFFF03800	SDRAMC	SDRAM Controller - SDRAMC	PB B
0xFFFF03C00	ECC	Error Correcting Code Controller - ECC	PB B

8.2 Interrupt Request Signal Map

The various modules may output interrupt request signals. These signals are routed to the Interrupt Controller (INTC). The Interrupt Controller supports up to 64 groups of interrupt requests. Each group can have up to 32 interrupt request signals. All interrupt signals in the same group share the same autovector address and priority level. Refer to the documentation for the individual submodules for a description of the semantic of the different interrupt requests.

The interrupt request signals in AT32AP7001 are connected to the INTC as follows:

Table 8-2. Interrupt Request Signal Map

Group	Line	Signal
0	0	COUNT-COMPARE match
	1	Performance Counter Overflow
2	0	DMACA BLOCK
	1	DMACA DSTT
	2	DMACA ERR
	3	DMACA SRCT
	4	DMACA TFR
3	0	SPI 0
4	0	SPI 1
5	0	TWI
6	0	USART0
7	0	USART1
8	0	USART2
9	0	USART3
10	0	SSC0
11	0	SSC1
12	0	SSC2
13	0	PIOA
14	0	PIOB
15	0	PIOC
16	0	PIOD
17	0	PIOE
18	0	PSIF
19	0	EIC0
	1	EIC1
	2	EIC2
	3	EIC3
20	0	PM
21	0	RTC

Table 8-2. Interrupt Request Signal Map

Group	Line	Signal
22	0	TC00
	1	TC01
	2	TC02
23	0	TC10
	1	TC11
	2	TC12
24	0	PWM
27	0	ABDAC
28	0	MCI
29	0	AC97C
30	0	ISI
31	0	USBA
32	0	EBI

8.3 DMACA Handshake Interface Map

The following table details the hardware handshake map between the DMACA and the peripherals attached to it :

Table 8-3. Hardware Handshaking Connection

Request	Hardware Handshaking Interface
MCI RX	0
MCI TX	1
ABDAC TX	2
AC97C CHANNEL A RX	3
AC97C CHANNEL A TX	4
AC97C CHANNEL B RX	5
AC97C CHANNEL B TX	6
EXTERNAL DMA REQUEST 0	7
EXTERNAL DMA REQUEST 1	8
EXTERNAL DMA REQUEST 2	9
EXTERNAL DMA REQUEST 3	10

8.4 Clock Connections

8.4.1 Timer/Counters

Each Timer/Counter channel can independently select an internal or external clock source for its counter:

Table 8-4. Timer/Counter clock connections

Timer/Counter	Source	Name	Connection
0	Internal	TIMER_CLOCK1	clk_osc32
		TIMER_CLOCK2	clk_pbb / 4
		TIMER_CLOCK3	clk_pbb / 8
		TIMER_CLOCK4	clk_pbb / 16
		TIMER_CLOCK5	clk_pbb / 32
	External	XC0	See Section 8.7
		XC1	
		XC2	
1	Internal	TIMER_CLOCK1	clk_osc32
		TIMER_CLOCK2	clk_pbb / 4
		TIMER_CLOCK3	clk_pbb / 8
		TIMER_CLOCK4	clk_pbb / 16
		TIMER_CLOCK5	clk_pbb / 32
	External	XC0	See Section 8.7
		XC1	
		XC2	

8.4.2 USARTs

Each USART can be connected to an internally divided clock:

Table 8-5. USART clock connections

USART	Source	Name	Connection
0	Internal	CLK_DIV	clk_pba / 8
1			
2			
3			

8.4.3 SPIs

Each SPI can be connected to an internally divided clock:

Table 8-6. SPI clock connections

SPI	Source	Name	Connection
0	Internal	CLK_DIV	clk_pba / 32
1			

8.4.4 USBA

OSC1 is connected to the USB HS Phy and must be 12 MHz when using the USBA.

8.5 External Interrupt Pin Mapping

External interrupt requests are connected to the following pins::

Table 8-7. External Interrupt Pin Mapping

Source	Connection
NMI_N	PB24
EXTINT0	PB25
EXTINT1	PB26
EXTINT2	PB27
EXTINT3	PB28

8.6 Nexus OCD AUX port connections

If the OCD trace system is enabled, the trace system will take control over a number of pins, irrespectively of the PIO configuration. Two different OCD trace pin mappings are possible, depending on the configuration of the OCD AXS register. For details, see the *AVR32 AP Technical Reference Manual*.

Table 8-8. Nexus OCD AUX port connections

Pin	AXS=0	AXS=1
EVTI_N	EVTI_N	EVTI_N
MDO[5]	PB09	PC18
MDO[4]	PB08	PC14
MDO[3]	PB07	PC12
MDO[2]	PB06	PC11
MDO[1]	PB05	PC06
MDO[0]	PB04	PC05
EVTO_N	PB03	PB28
MCKO	PB02	PC02
MSEO[1]	PB01	PC01
MSEO[0]	PB00	PC00

8.7 Peripheral Multiplexing on IO lines

The AT32AP7001 features five PIO controllers, PIOA to PIOE, that multiplex the I/O lines of the peripheral set. Each PIO Controller controls up to thirty-two lines.

Each line can be assigned to one of two peripheral functions, A or B. The tables in the following pages define how the I/O lines of the peripherals A and B are multiplexed on the PIO Controllers.

Note that some output only peripheral functions might be duplicated within the tables.

8.7.1 PIO Controller A Multiplexing

Table 8-9. PIO Controller A Multiplexing

QFP208	I/O Line	Peripheral A	Peripheral B
27	PA00	SPI0 - MISO	SSC1 - RX_FRAME_SYNC
28	PA01	SPI0 - MOSI	SSC1 - TX_FRAME_SYNC
29	PA02	SPI0 - SCK	SSC1 - TX_CLOCK
30	PA03	SPI0 - NPCS[0]	SSC1 - RX_CLOCK
31	PA04	SPI0 - NPCS[1]	SSC1 - TX_DATA
32	PA05	SPI0 - NPCS[2]	SSC1 - RX_DATA
175	PA06	TWI - SDA	USART0 - RTS
176	PA07	TWI - SCL	USART0 - CTS
35	PA08	PSIF - CLOCK	USART0 - RXD
38	PA09	PSIF - DATA	USART0 - TXD
39	PA10	MCI - CLK	USART0 - CLK
40	PA11	MCI - CMD	TC0 - CLK0
41	PA12	MCI - DATA[0]	TC0 - A0
42	PA13	MCI - DATA[1]	TC0 - A1
43	PA14	MCI - DATA[2]	TC0 - A2
44	PA15	MCI - DATA[3]	TC0 - B0
45	PA16	USART1 - CLK	TC0 - B1
46	PA17	USART1 - RXD	TC0 - B2
47	PA18	USART1 - TXD	TC0 - CLK2
48	PA19	USART1 - RTS	TC0 - CLK1
49	PA20	USART1 - CTS	SPI0 - NPCS[3]
50	PA21	SSC0 - RX_FRAME_SYNC	PWM - PWM[2]
51	PA22	SSC0 - RX_CLOCK	PWM - PWM[3]
54	PA23	SSC0 - TX_CLOCK	TC1 - A0
55	PA24	SSC0 - TX_FRAME_SYNC	TC1 - A1
72	PA25	SSC0 - TX_DATA	TC1 - B0
73	PA26	SSC0 - RX_DATA	TC1 - B1
74	PA27	SPI1 - NPCS[3]	TC1 - CLK0
75	PA28	PWM - PWM[0]	TC1 - A2

Table 8-9. PIO Controller A Multiplexing

76	PA29	PWM - PWM[1]	TC1 - B2
77	PA30	PM - GCLK[0]	TC1 - CLK1
78	PA31	PM - GCLK[1]	TC1 - CLK2

8.7.2 PIO Controller B Multiplexing

Table 8-10. PIO Controller B Multiplexing

QFP208	I/O Line	Peripheral A	Peripheral B
144	PB00	ISI - DATA[0]	SPI1 - MISO
145	PB01	ISI - DATA[1]	SPI1 - MOSI
146	PB02	ISI - DATA[2]	SPI1 - NPCS[0]
147	PB03	ISI - DATA[3]	SPI1 - NPCS[1]
148	PB04	ISI - DATA[4]	SPI1 - NPCS[2]
149	PB05	ISI - DATA[5]	SPI1 - SCK
150	PB06	ISI - DATA[6]	MCI - CMD[1]
151	PB07	ISI - DATA[7]	MCI - DATA[4]
152	PB08	ISI - HSYNC	MCI - DATA[5]
153	PB09	ISI - VSYNC	MCI - DATA[6]
158	PB10	ISI - PCLK	MCI - DATA[7]
159	PB11	PSIF - CLOCK[1]	ISI - DATA[8]
160	PB12	PSIF - DATA[1]	ISI - DATA[9]
161	PB13	SSC2 - TX_DATA	ISI - DATA[10]
162	PB14	SSC2 - RX_DATA	ISI - DATA[11]
163	PB15	SSC2 - TX_CLOCK	USART3 - CTS
164	PB16	SSC2 - TX_FRAME_SYNC	USART3 - RTS
165	PB17	SSC2 - RX_FRAME_SYNC	USART3 - TXD
166	PB18	SSC2 - RX_CLOCK	USART3 - RXD
167	PB19	PM - GCLK[2]	USART3 - CLK
168	PB20	ABDAC - DATA[1]	AC97C - SDO
169	PB21	ABDAC - DATA[0]	AC97C - SYNC
170	PB22	ABDAC - DATAN[1]	AC97C - SCLK
171	PB23	ABDAC - DATAN[0]	AC97C - SDI
33	PB24	NMI_N	DMACA - DMARQ[0]
34	PB25	EXTINT0	DMACA - DMARQ[1]
80	PB26	EXTINT1	USART2 - RXD
81	PB27	EXTINT2	USART2 - TXD
82	PB28	EXTINT3	USART2 - CLK
100	PB29	PM - GCLK[3]	USART2 - CTS
101	PB30	PM - GCLK[4]	USART2 - RTS