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Features

- **Ultra High Performance**
  - **System Speeds to 100 MHz**
  - **Array Multipliers > 50 MHz**
  - **10ns Flexible SRAM**
  - **Internal 3-State Capability in each Cell**
- **FreeRAM™**
  - **Flexible, Single/Dual Port, Sync/Async 10 ns SRAM**
  - **2,048 - 18,432 Bits of Distributed SRAM Independent of Logic Cells**
- **84 - 384 PCI Compliant I/Os**
  - **3V/5V Capability**
  - **Programmable Output Drive**
  - **Fast, Flexible Array Access Facilitates Pin-Locking**
  - **Pin Compatible with XC4000, XC5200 FPGAs**
- **8 Global Clocks**
  - **Fast, Low Skew Clock Distribution**
  - **Programmable Rising/Falling Edge Transitions**
  - **Distributed Clock Shut-Down Capability for Low Power Management**
  - **Global Reset/Asynchronous Reset Options**
  - **4 Additional Dedicated PCI Clocks**
- **Cache Logic® Dynamic Full/Partial Reconfigurability In-System**
  - **Unlimited Reprogrammability via Serial or Parallel Modes**
  - **Enables Adaptive Designs**
  - **Enables Fast Vector Multiplier Updates**
  - **QuickChange™ Tools for Fast, Easy Design Changes**
- **Pin-Compatible Package Options**
  - **Plastic Leaded Chip Carriers (PLCC)**
  - **Thin, Plastic Quad Flat Packs (VQFP, TQFP, PQFP)**
  - **Ball Grid Arrays (BGA)**
  - **Pin Grid Arrays (PGAs)**
- **Industry-Standard Design Tools**
  - **Seamless Integration (Libraries, Interface, Full Back-Annotation) with Concept, Everest, Exemplar, Mentor, OrCAD, Synario, Synopsys, Verilog, Veribest, Viewlogic, Synplicity**
  - **Timing Driven Placement & Routing**
  - **Automatic/Interactive Multi-Chip Partitioning**
  - **Fast, Efficient Synthesis**
  - **Over 50 Automatic Component Generators Create 1000's of Reusable, Fully Deterministic Logic and RAM Functions**
- **Intellectual Property Cores**
  - **Fir Filters, UARTs, PCI, FFT and other System Level Functions**
- **Easy Migration to Atmel Gate Arrays for High Volume Production**

Device	AT40K05	AT40K10	AT40K20	AT40K40
Usable Gates	5K - 10K	10K - 20K	20K - 30K	40K - 50K
RowsXColumns	16 x 16	24 x 24	32 x 32	48 x 48
Cells	256	576	1,024	2,304
Registers	256	576	1,024	2,304
RAM Bits	2,048	4,608	8,192	18,432
I/O (max)	128	192	256	384

AT40K FPGAs with FreeRAM™

AT40K05
AT40K10
AT40K20
AT40K40

Rev. 0896B–01/99

Description

The AT40K is a family of fully PCI-compliant, SRAM-based FPGAs with distributed 10ns programmable synchronous/asynchronous, dual port/single port SRAM, 8 global clocks, Cache Logic ability (partially or fully reconfigurable without loss of data), automatic component generators, and range in size from 5,000 to 50,000 usable gates. I/O counts range from 128 to 384 in industry standard packages ranging from 84-pin PLCC to 475-pin BGA, and support 3.3V and 5V designs.

The AT40K is designed to quickly implement high performance, large gate count designs through the use of synthesis and schematic-based tools used on a PC, Sun and HP platform. Atmel's design tools provide seamless integration with industry standard tools from Cadence (Concept/Verilog), Everest, Exemplar, Mentor, OrCAD, Synario, Veribest, and Viewlogic.

The AT40K can be used as a Coprocessor for high speed (DSP/Processor-based) designs by implementing a variety of compute-intensive, arithmetic functions. These include adaptive finite impulse response (FIR) filters, fast Fourier transforms (FFT), convolvers, interpolators and discrete-cosine transforms (DCT) that are required for video compression and decompression, encryption, convolution and other multimedia applications.

Fast, Flexible and Efficient SRAM

The AT40K FPGA offers a patented distributed 10ns SRAM capability where the RAM can be used without losing logic resources. Multiple independent, synchronous or asynchronous, dual port or single port RAM functions (FIFO, scratch pad, etc.) can be created using Atmel's macro generator tool.

Fast, Efficient Array & Vector Multipliers

The AT40K's patented 8-sided core cell with direct horizontal, vertical and diagonal cell-to-cell connections implements ultra fast array multipliers without using any busing resources. The AT40K's Cache Logic capability enables a large number of design coefficients and variables to be implemented in a very small amount of silicon, enabling vast improvement in system speed at much lower cost than conventional FPGAs.

Cache Logic Design

The AT40K is the only FPGA family capable of implementing Cache Logic (Dynamic full/partial logic reconfiguration, without loss of data, on-the-fly) for building adaptive logic and systems. As new logic functions are required, they can be loaded into the logic cache without losing the data already there or disrupting the operation of the rest of the chip; replacing or complementing the active logic. The AT40K can act as a reconfigurable coprocessor.

Automatic Component Generators

The AT40K is the only FPGA family capable of implementing user-defined, automatically generated, macros in multiple designs; speed and functionality are unaffected by the macro orientation or density of the target device. This enables the fastest, most predictable and efficient FPGA design approach and minimizes design risk by reusing already proven functions. The Automatic Component Generators work seamlessly with industry standard schematic and synthesis tools to create the fastest, most efficient designs available.

The patent-pending AT40K Series architecture employs a symmetrical grid of small yet powerful cells connected to a flexible busing network. Independently controlled clocks and resets govern every column of cells. The array is surrounded by programmable I/O.

Devices range in size from 5,000 to 50,000 usable gates in the initial family, and 256 to 2,304 registers. Pin locations are consistent throughout the AT40K Series for easy design migration in the same package footprint. AT40K Series FPGAs utilize a reliable 0.6 micron single-poly, triple-metal CMOS process and are 100% factory-tested. Atmel's PC- and workstation-based Integrated Development System is used to create AT40K Series designs. Multiple design entry methods are supported.

The Atmel architecture was developed to provide the highest levels of performance, functional density and design flexibility in an FPGA. The cells in the Atmel array are small, efficient and can implement any pair of Boolean functions of (the same) three inputs or any single Boolean function of four inputs. The cell's small size leads to arrays with large numbers of cells, greatly multiplying the functionality in each cell. A simple, high-speed busing network provides fast, efficient communication over medium and long distances

The Symmetrical Array

At the heart of the Atmel architecture is a symmetrical array of identical cells (Figure 1). The array is continuous from one edge to the other, except for bus repeaters spaced every four cells (Figure 2). At the intersection of each repeater row and column is a 32 x 4 RAM block accessible by adjacent buses. The Ram can be configured as either a single-ported or dual-ported RAM, with either synchronous or asynchronous operation.

Figure 1. Symmetrical Array Surrounded by I/O (AT40K20)

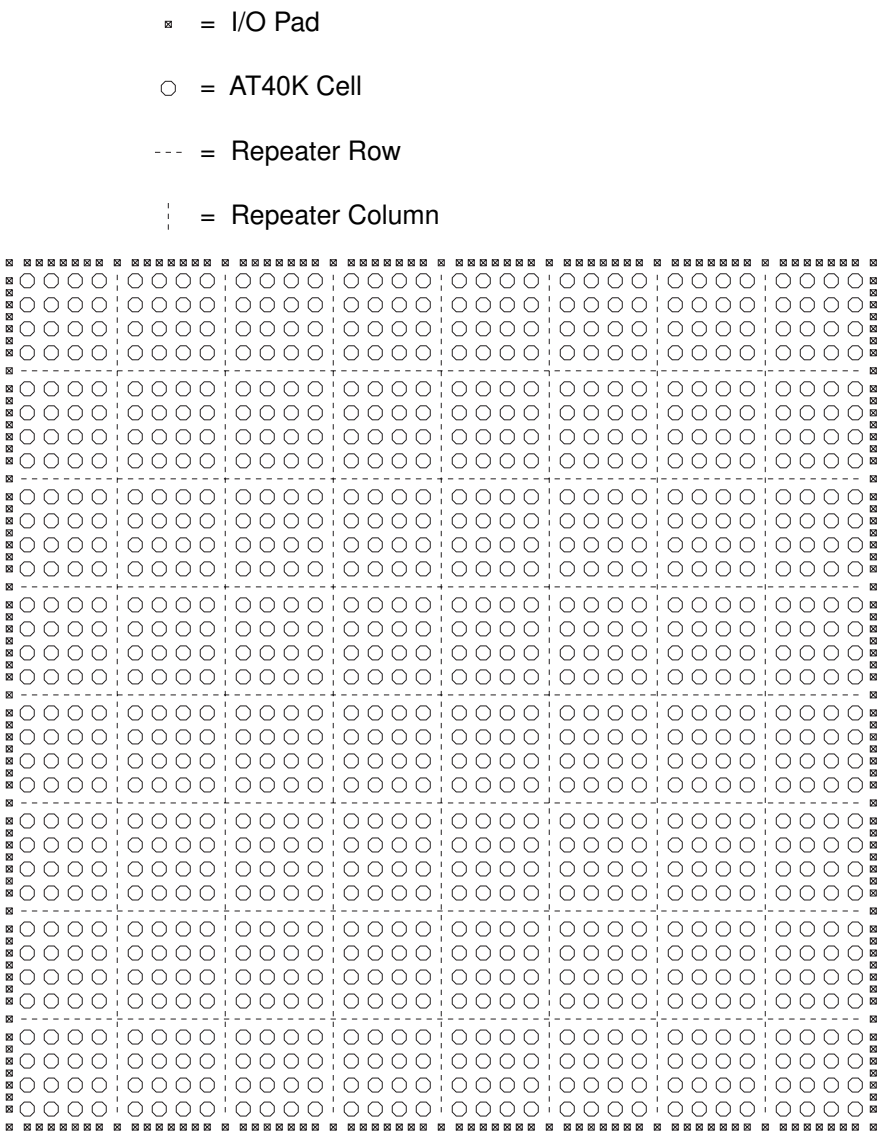
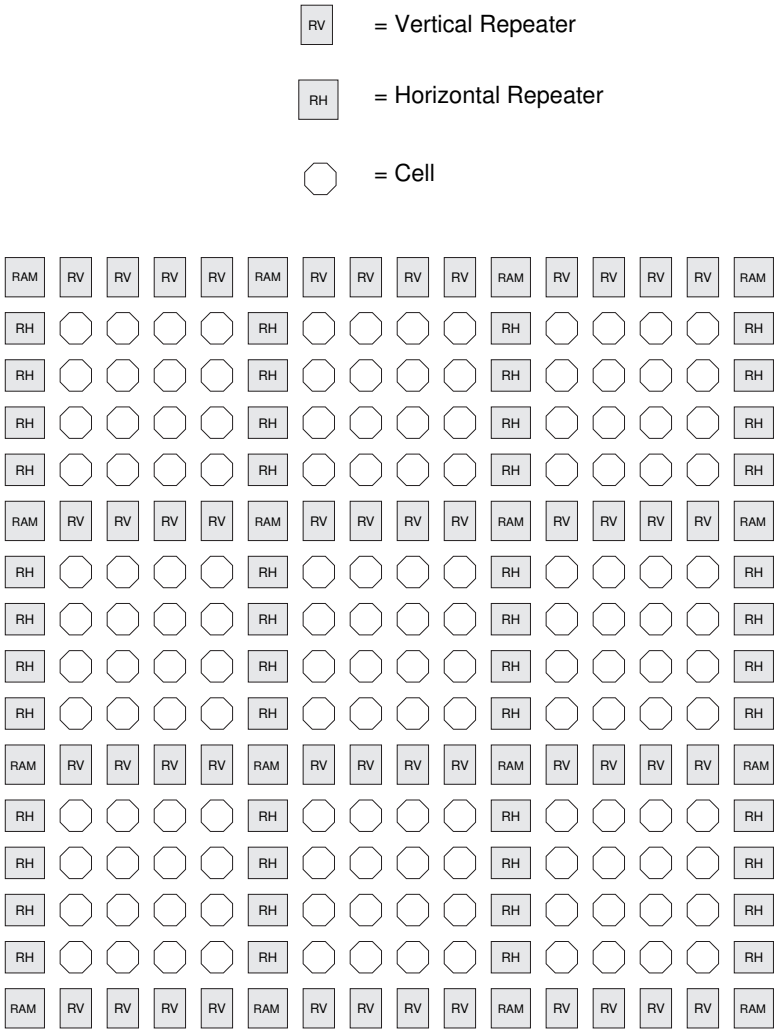


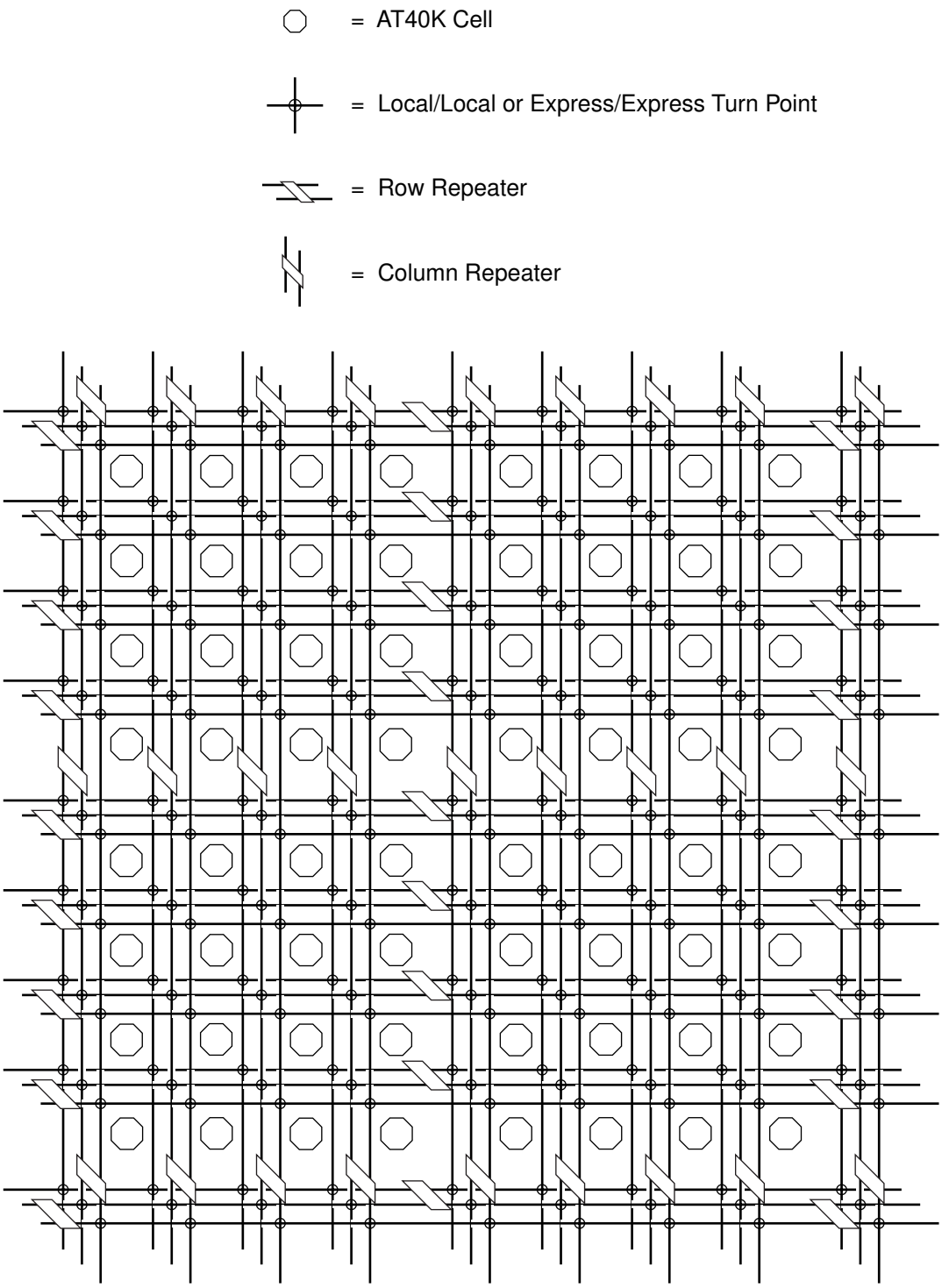
Figure 2. Floorplan (representative portion)



The Busing Network

Figure 3 depicts one of five identical busing planes. Each plane has 3 bus resources: a local-bus resource (the middle bus) and 2 express-bus resources. Bus resources are connected via repeaters. Each repeater has connections to two adjacent local-bus segments and two express-bus segments. Each local-bus segment spans four cells and connects to consecutive repeaters. Each express-bus segment spans eight cells and “leapfrogs” or bypasses a repeater. Repeaters regenerate signals and can connect any bus to any other bus (all pathways are legal) on the same plane. Although not shown, a local bus can bypass a repeater via a programmable pass gate allowing long on-chip three state buses to be created. Local/Local turns are implemented through pass gates in the cell-bus interface (see following page). Express/Express turns are implemented through separate pass gates distributed throughout the array.

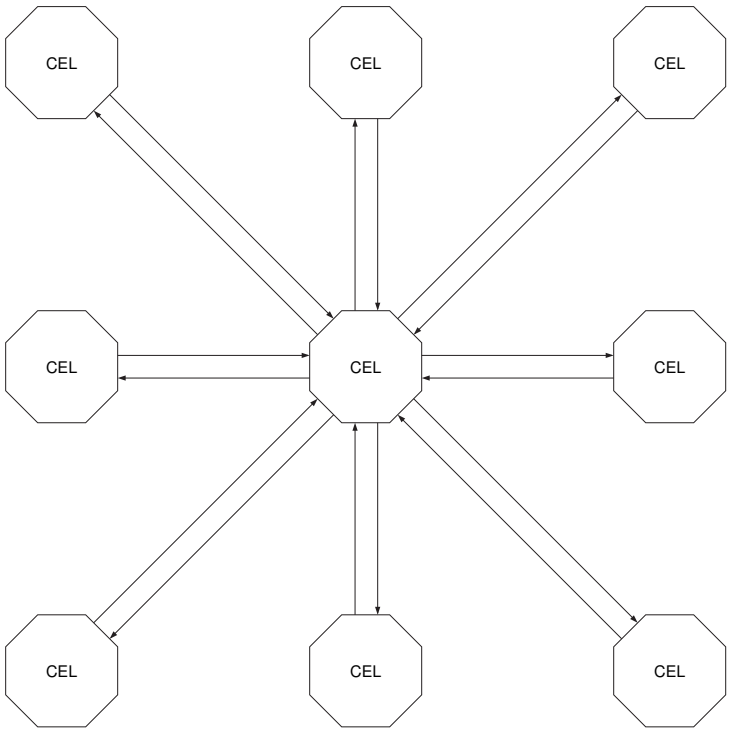
Figure 3. Busing Plane (one of five)



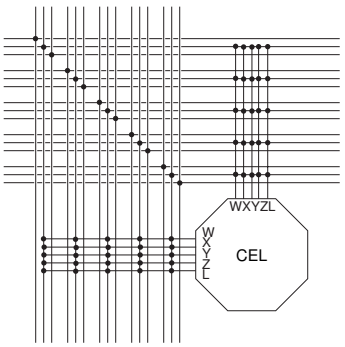
Cell Connections

Figure 4(a) depicts direct connections between a cell and its eight nearest neighbors. Figure 4(b) shows the connections between a cell five horizontal local buses (one per busing plane) and five vertical local buses (one per busing plane).

Figure 4. Cell Connections



(a) Cell to Cell Connections

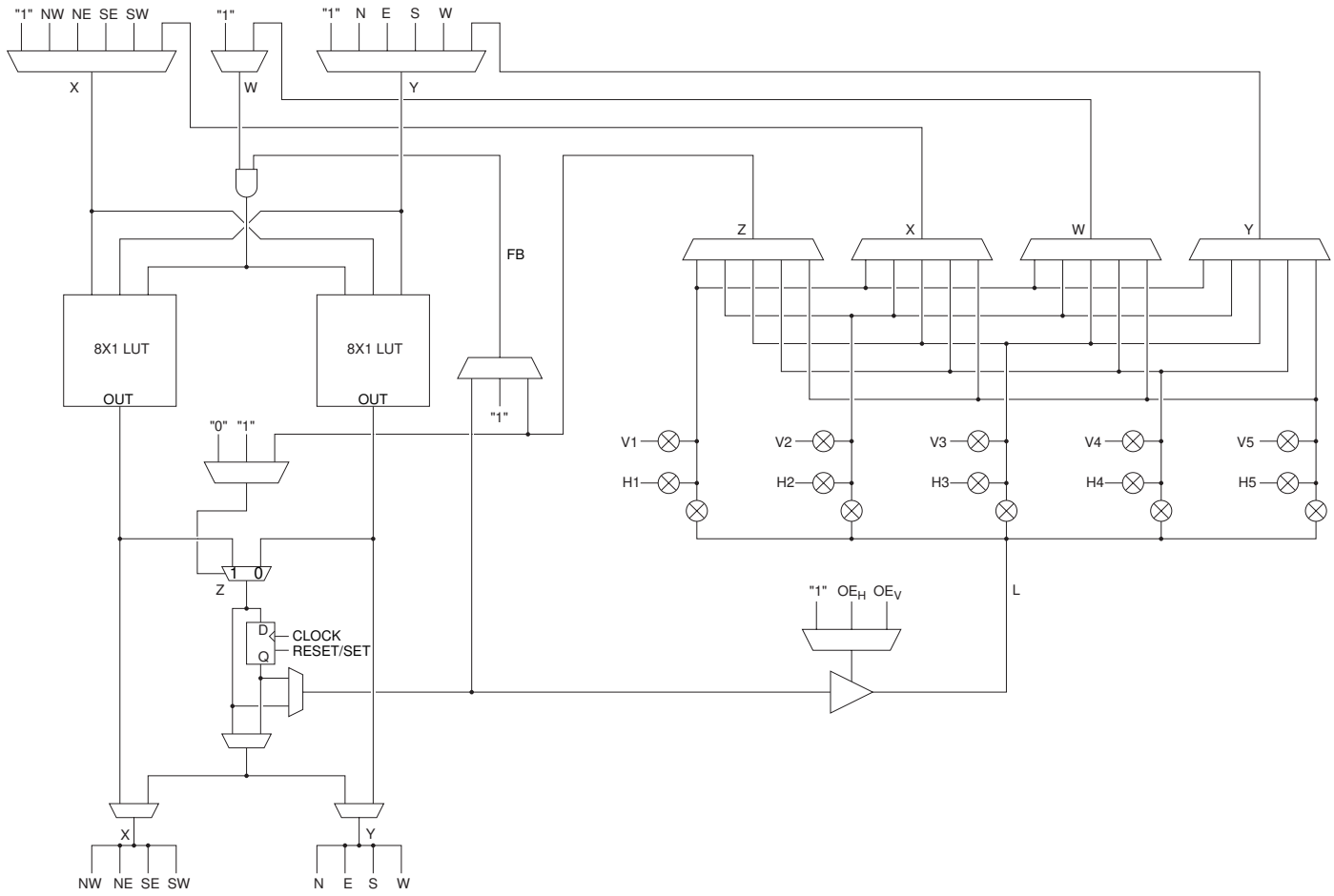


(b) Cell to Bus Connections

The Cell

Figure 5 depicts the AT40K cell. Configuration bits for separate muxes and pass gates are independent. All permutations of programmable muxes and pass gates are legal. Vn is connected to the vertical local bus in plane n. Hn is connected to the horizontal local bus in plane n. A local/local turn in plane n is achieved by turning on the two pass gates connected to Vn and Hn. Up to five simultaneous local/local turns are possible.

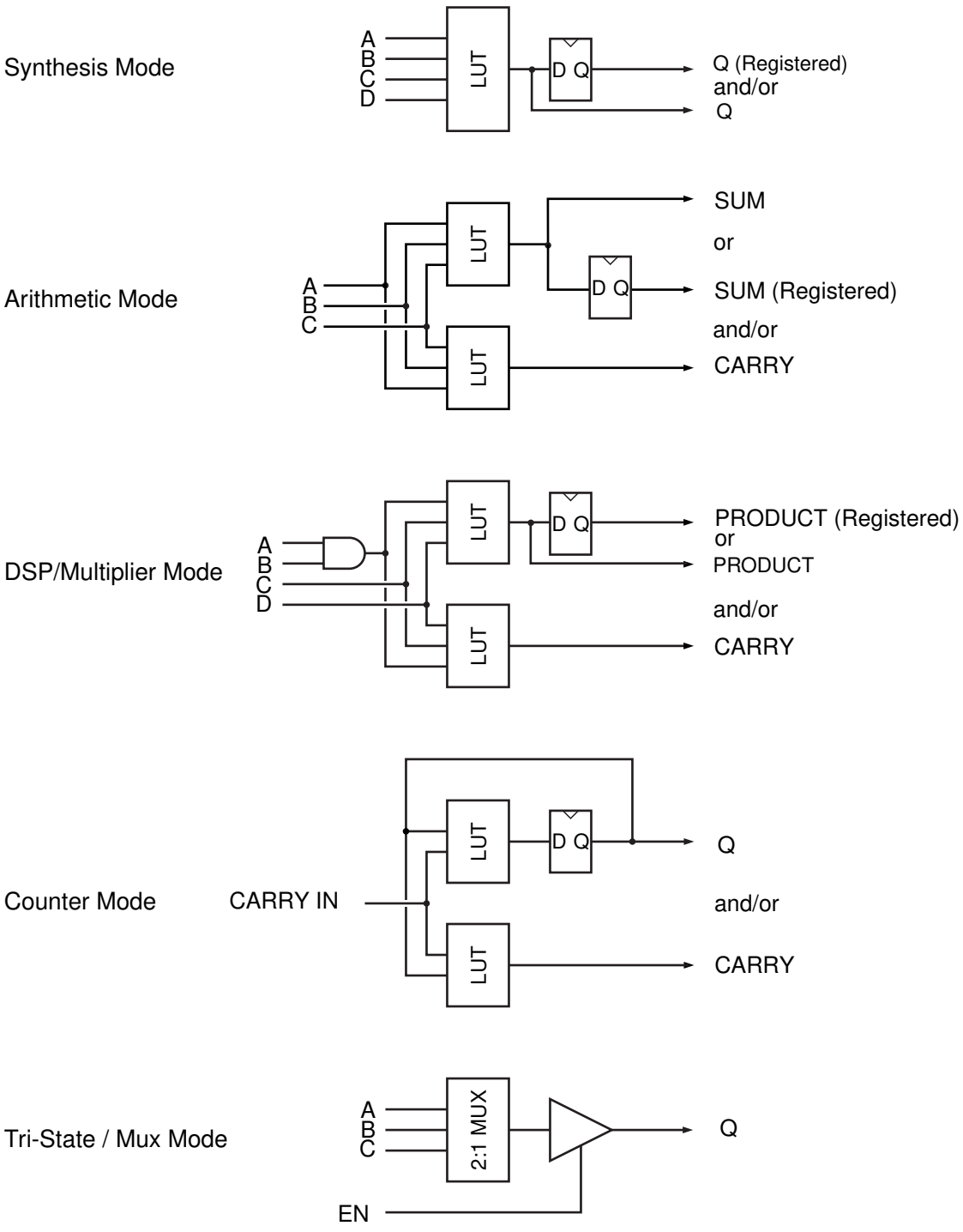
Figure 5. The Cell



X = Diagonal Direct Connect or Bus
Y = Orthogonal Direct Connect or Bus
W = Bus Connection
Z = Bus Connection
FB = Internal Feedback

The core cell can be configured in several “modes”. The core cell flexibility makes the AT40K architecture well suited to most digital design application areas (see Figure 6).

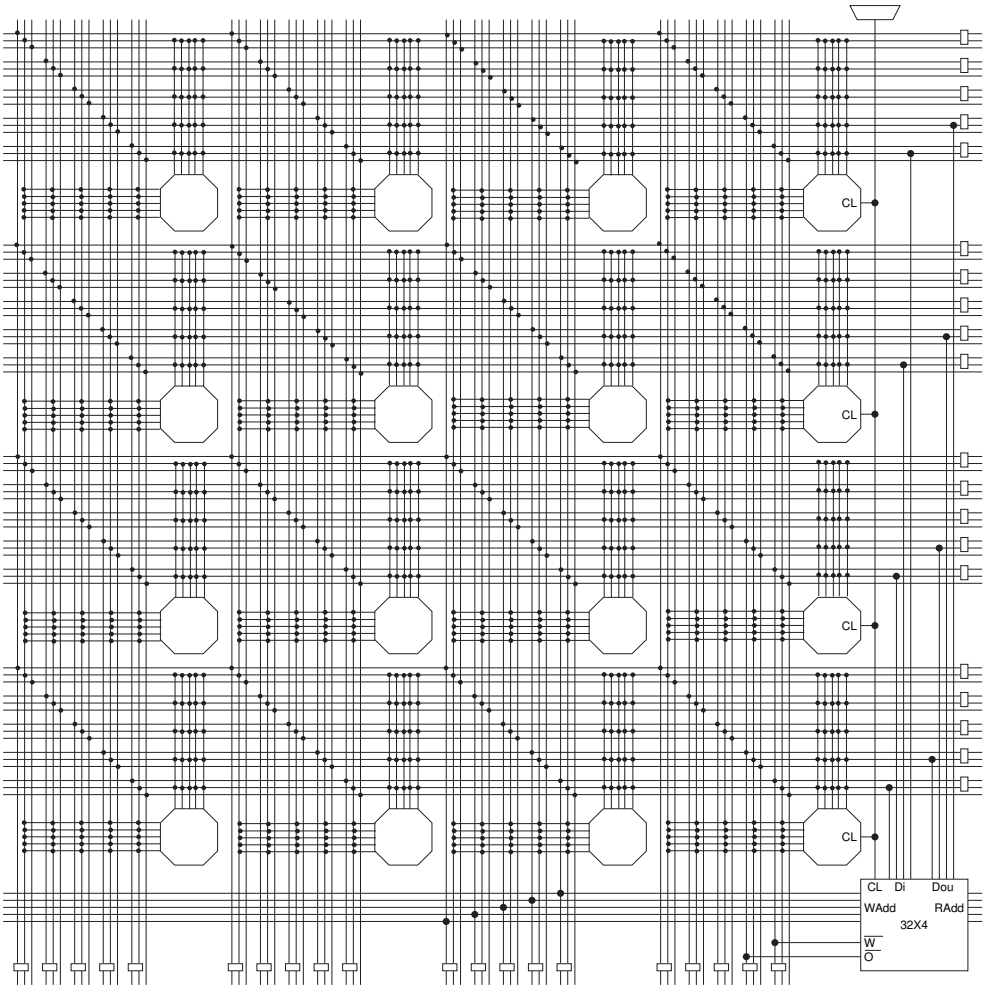
Figure 6. Some Single Cell Modes



RAM

32 x 4 Dual-Ported RAM blocks are dispersed throughout the array as shown in Figure 7. A four-bit Input Data Bus connects to four horizontal local buses distributed over four sector rows (plane 1). A four-bit Output Data Bus connects to four horizontal local buses distributed over four sector rows (plane 2). A five-bit Input-Address Bus connects to five vertical express buses in same column. A five-bit Output-Address Bus connects to five vertical express buses in same column. WAddr (Write Address) and RAddr (Read Address) alternate positions in horizontally aligned RAM blocks. For the left-most RAM blocks, RAddr is on the left and WAddr is on the right. For the right-most RAM blocks, WAddr is on the left and RAddr is tied off. For single-ported RAM, WAddr is the READ/WRITE address port and Din is the (bi-directional) data port. Right-most RAM blocks can be used only for single-ported memories. /WE & /OE connect to the vertical express buses in the same column. WAddr, RAddr, /WE and /OE connect to express buses that are full length at array edge.

Figure 7. RAM Connections (One Ram Block)



Reading and writing the 32 x 4 Dual-Port RAM are independent of each other. Reading the 32 x 4 Dual-Port RAM is completely asynchronous. Latches are transparent; when Load is logic 1, data flows through; when Load is logic 0, data is latched. Each bit in the 32 x 4 Dual-Port RAM is also a transparent latch. The front-end latch and the memory latch together form an edge-triggered flip flop. When a Bit = 7 Nibble is (Write) addressed and LOAD is Logic 1 and $\overline{WE}$ is logic 0, DATA flows through the bit. When a nibble is not (Write) addressed or LOAD is logic 0 or $\overline{WE}$ is logic 1, DATA is latched in the nibble. The two CLOCK muxes are controlled together; they both select CLOCK or they both select “1”. CLOCK is obtained from the clock for the sector-column immediately to the left and immediately above the RAM block. Writing any value to the RAM Clear Byte during configuration clears the RAM (see Bit Map Spec).

Figure 8. RAM Logic

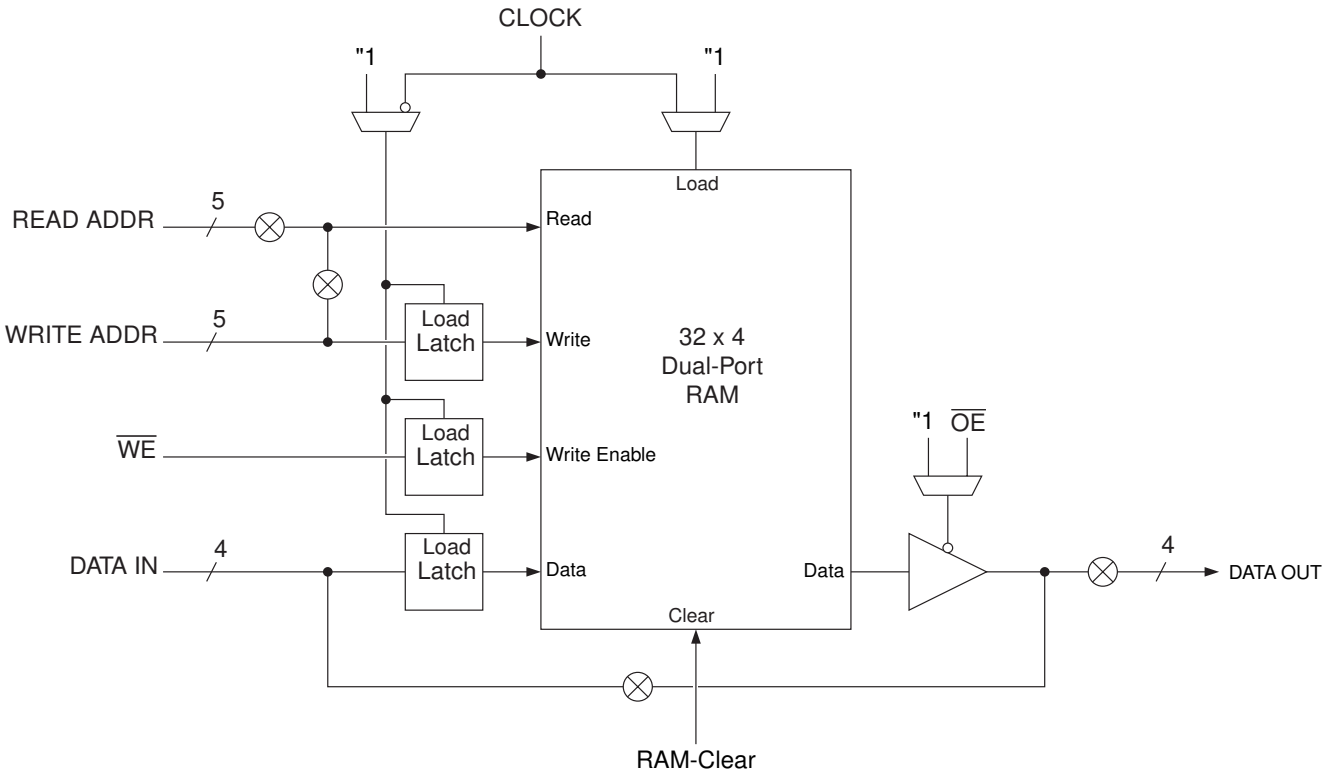
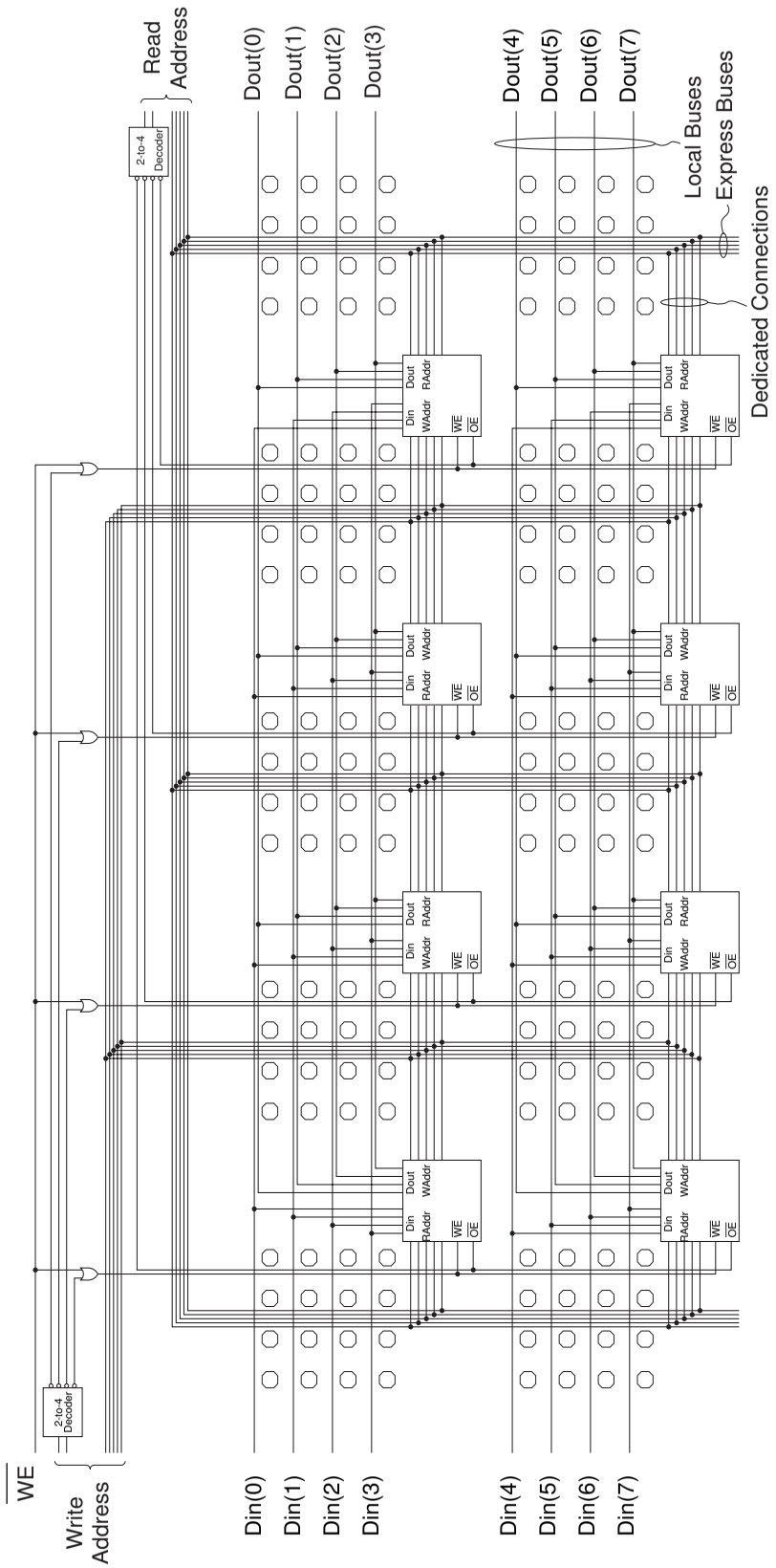


Figure 9. RAM Example: 128 x 8 Dual-Ported RAM (asynchronous)



Clocking and Set/Reset

Each of 8 dedicated Global Clock buses is connected to a dual-use Global Clock pad (GCK1 - GCK8). An internal signal can be placed on a Global Clock bus by routing that signal to a Global Clock pad. Each column of the array has a Column Clock selected from one of the 8 Global Clock buses. The extreme-left Column Clock mux has two additional inputs from dual-use pins FCK1 & FCK2 to provide fast clocking to left-side I/O. The extreme-right Column Clock mux has two additional inputs from dual-use pins FCK3 & FCK4 to provide fast clocking to right-side I/O. Each sector column of 4 cells can be clocked from a (Plane 4) express bus or from the Column Clock. Clocking to the 4 cells can be disabled. The Plane 4 express bus used for clocking is half length at the array edge. The clock provided to each sector column of 4 cells can be either inverted or not inverted. The register in each cell is triggered on a rising clock edge. On power up, constant “0” is provided to each registers clock pins.

A dedicated Global Set/Reset bus can be driven by any USER I/O pad, except those used for clocking, Global or Fast. An internal signal can be placed on the Global Set/Reset bus by routing that signal to the pad programmed as the Global Set/Reset input. Global Set/Reset is distributed to each column of the array. Each sector column of 4 cells can be Set/Reset by a (Plane 5) express bus or by the Global Set/Reset. The Plane 5 express bus used for Set/Reset is half length at array edge. The Set/Reset provided to each sector column of 4 cells can be either inverted or not inverted. The function of the Set/Reset input of a register (either Set or Reset) is determined by a configuration bit in each cell. The Set/Reset input of a register is Active Low (logic 0). Setting or resetting of a register is asynchronous. On power up, a logic 1 (a high) is provided by each register, i.e., all registers are set at power up.

Figure 10. Clocking (for one column of cells)

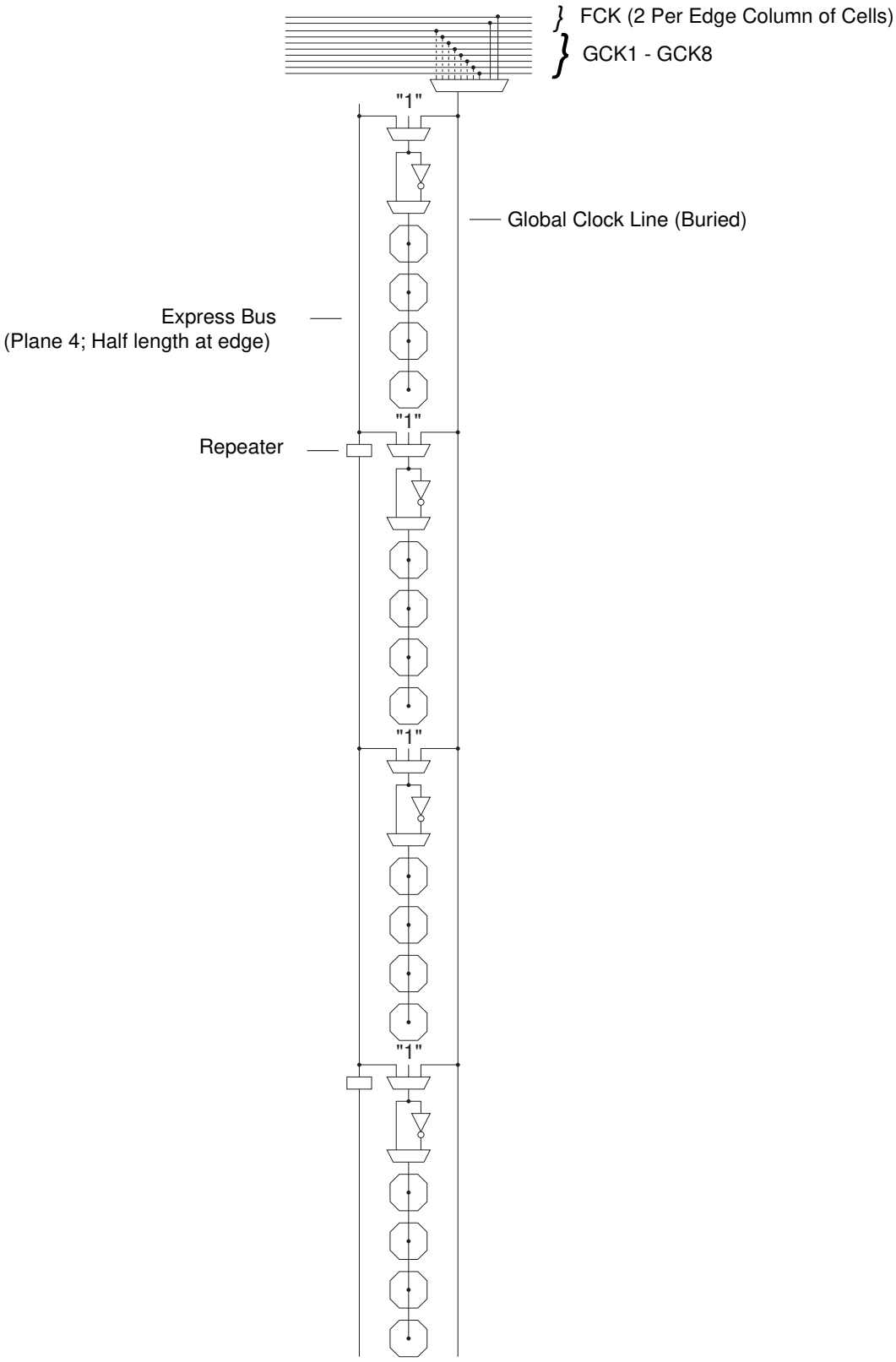
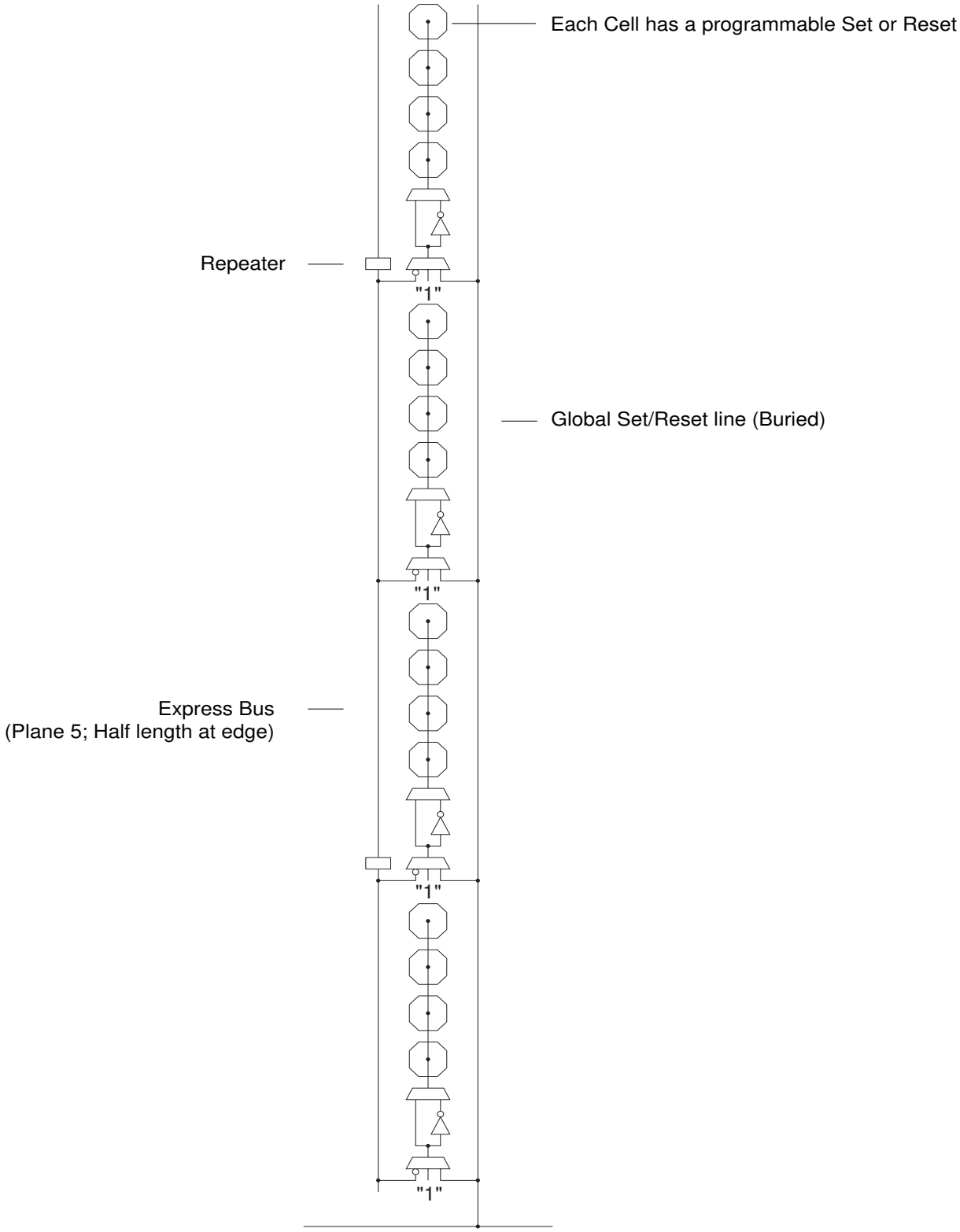
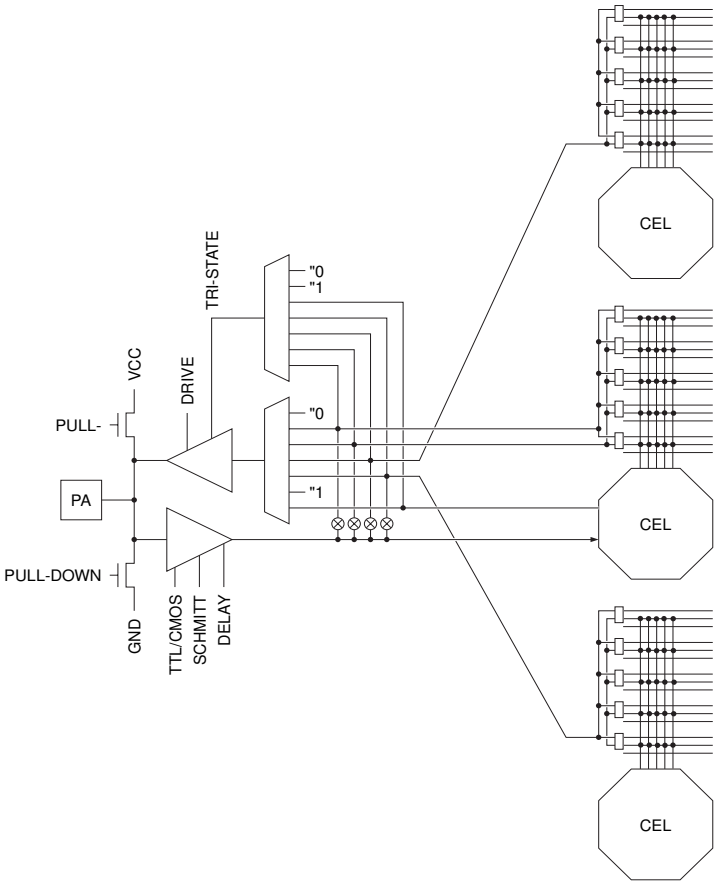


Figure 11. Set/Reset (for one column of cells)

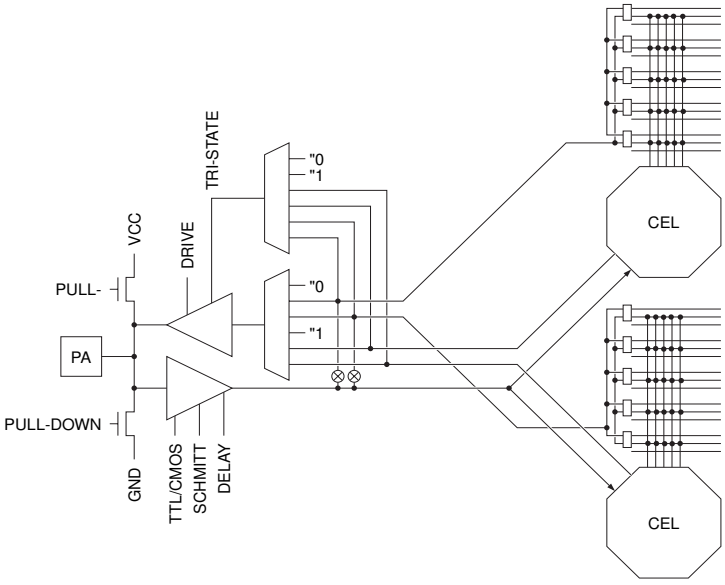


Any User I/O can drive Global Set/Reset line

Figure 12. West I/O (Mirrored for East I /O)

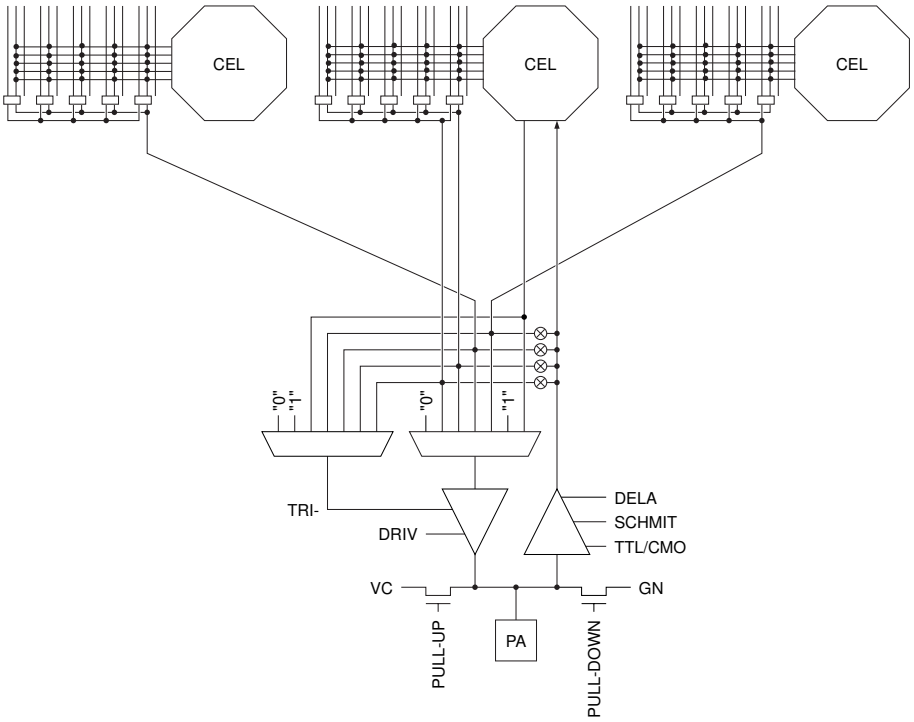


(a) Primary

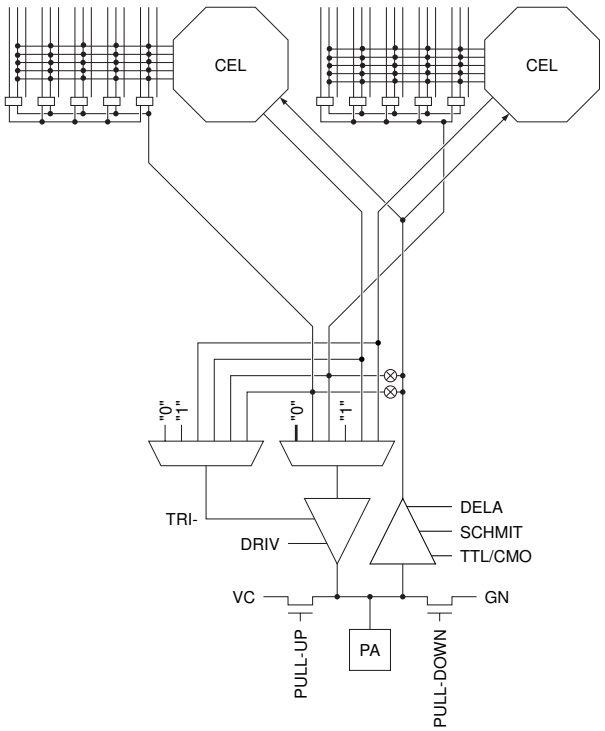


(a) Secondary

Figure 13. South I/O (Mirrored for North I/O)

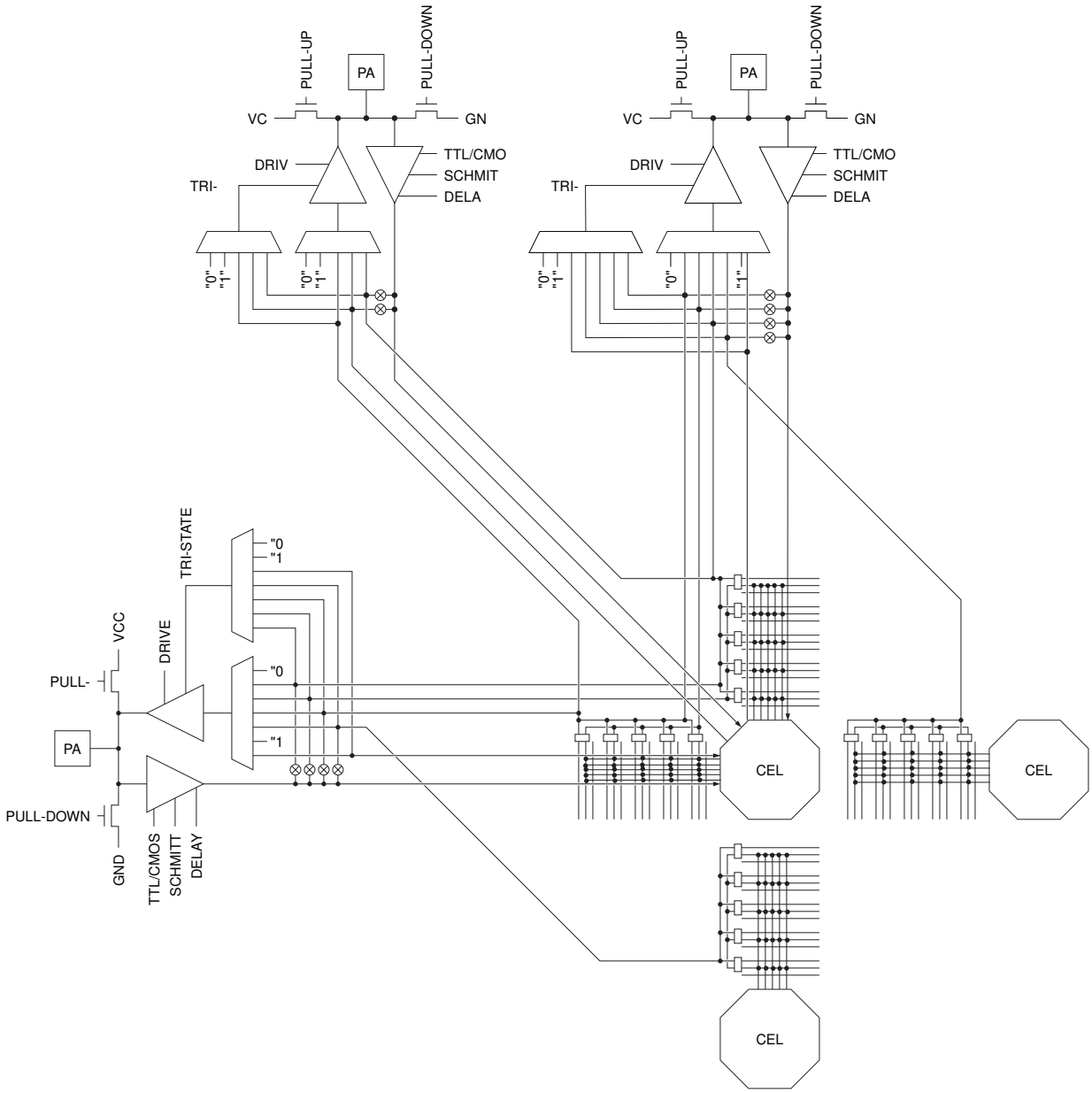


(a) Primary



(a) Secondary

Figure 14. North/West Corner, (similar for NE/SE/SW corners)



Some of the bus resource on ATK40K is used as a dual-function resource. Table 1 shows which buses are used in a dual-function mode and which bus plane is used. The ATK40K software tools are designed to accommodate dual-function buses in an efficient manner.

Table 1. Dual-Function Buses

Function	Type	Plane(s)	Direction	Comments
Cell Output Enable	Local	5	Horizontal and Vertical	
RAM Output Enable	Express	2	Vertical	Bus full length at array edge Bus in first column to left of RAM block
RAM Write Enable	Express	1	Vertical	Bus full length at array edge Bus in first column to left of RAM block
RAM Address	Express	1-5	Vertical	Buses full length at array edge Buses in second column to left of RAM block
RAM Data In	Local	1	Horizontal	
RAM Data Out	Local	2	Horizontal	
Clocking	Express	4	Vertical	Bus half length at array edge
Set/Reset	Express	5	Vertical	Bus half length at array edge

Absolute Maximum Ratings - 5V Commercial/Industrial*

Symbol	Parameter	Conditions	Min	Max	Units
V_{CC}	Supply Voltage	With respect to GND	-0.5	7.0	V
V_I	DC Input Voltage(1)	With respect ot GND	-0.5	7.0	V
V_O	DC Output Voltaage	With respect ot GND	-0.5	7.0	V
T_{STG}	Storage Temperature		-65°C	+150°C	
T_J	Junction Temperature			+150°C	
T_L	Lead Temperature (Soldering, 10 sec.)			+250°C	
ESD		R_{ZAP} = 1.5K, C_{ZAP} = 100 pF		2000	V

Note: 1. Minimum voltage of -0.5V DC which may undershoot to -2.0V for pulses of less than 20 ns.

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range - 5V Operation

		AT40K05-2 AT40K10-2 AT40K20-2 AT40K40-2 Commercial	AT40K05-2 AT40K10-2 AT40K20-2 AT40K40-2 Industrial	AT40K05-2 AT40K10-2 AT40K20-2 AT40K40-2 Military
Operating Temperature (Case)		0°C - 70°C	-40°C - 85°C	-55°C - 125°C
V_{CC} Power Supply		5V ± 5%	5V ± 10%	5V ± 10%
Input Voltage Level (TTL)	High (V_{IHT})	2.0V - V_{CC}	2.0V - V_{CC}	2.0V - V_{CC}
	Low (V_{ILT})	0V - 0.8V	0V - 0.8V	0V - 0.8V
Input Voltage Level (CMOS)	High (V_{IHC})	70% - 100% V_{CC}	70% - 100% V_{CC}	70% - 100% V_{CC}
	Low (V_{ILC})	0 - 30% V_{CC}	0 - 30% V_{CC}	0 - 30% V_{CC}

DC Characteristics - 5V Operation - Commercial/Industrial/Military

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High-Level Input Voltage	CMOS	70% V_{CC}			V
		TTL	2.0			V
V_{IL}	Low-Level Input Voltage	CMOS	-0.3		30% V_{CC}	V
		TTL	-0.3		0.8	V
V_{OH}	High-Level Output Voltage	I_{OH} = 6mA V_{CC} = V_{CC} min	4.0			V
		I_{OH} = 14mA V_{CC} = V_{CC} min	4.0			V
		I_{OH} = 20mA Comm. = 4.75V Ind./Military = 4.5V	4.0			V
V_{OL}	Low-Level Output Voltage	I_{OL} = -6mA Comm. = 4.75V Ind./Military = 4.5V			0.4	V
		I_{OL} = -14mA Comm. = 4.75V Ind./Military = 4.5V			0.4	V
		I_{OL} = -20mA Comm. = 4.75V Ind./Military = 4.5V			0.4	V
I_{IH}	High-Level Input Current	V_{IN} = V_{CC} max			10	µA
		With pulldown, V_{IN} = V_{CC}	125	250	500	µA
I_{IL}	Low-Level Input Current	V_{IN} = V_{SS}	-10			µA
		With pullup, V_{IN} = V_{SS}	-500	-250	-125	µA
I_{OZH}	High-Level Tristate Output leakage current	Without pulldown, V_{IN} = V_{CC}			10	µA
		With pulldown, V_{IN} = V_{CC}	125	250	500	µA
I_{OZL}	Low-Level Tristate Output leakage current	Without pullup, V_{IN} = V_{SS} max	-10			µA
		With pullup, V_{IN} = V_{SS} max	-500	-250	-125	µA
I_{CC}	Standby Current Consumption	Standby, unprogrammed		0.6	1	mA
C_{IN}	Input Capacitance	All pins			10	pF

AC Timing Characteristics - 5V Operation

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 4.75V, temperature = 70°C
Minimum times based on best case: V_{CC} = 5.25V, temperature = 0°C
Maximum delays are the average of t_{PDLH} and t_{PDHL}.

Cell Function	Parameter	Path	-2	Units	Notes
Core					
2 input gate	t_{PD}(max)	x/y -> x/y	1.8	ns	1 unit load
3 input gate	t_{PD}(max)	x/y/z -> x/y	2.1	ns	1 unit load
3 input gate	t_{PD}(max)	x/y/w -> x/y	2.2	ns	1 unit load
4 input gate	t_{PD}(max)	x/y/w/z -> x/y	2.2	ns	1 unit load
fast carry	t_{PD}(max)	y -> y	1.4	ns	1 unit load
fast carry	t_{PD}(max)	x -> y	1.7	ns	1 unit load
fast carry	t_{PD}(max)	y -> x	1.8	ns	1 unit load
fast carry	t_{PD}(max)	x -> x	1.5	ns	1 unit load
fast carry	t_{PD}(max)	w -> y	2.2	ns	1 unit load
fast carry	t_{PD}(max)	w -> x	2.3	ns	1 unit load
fast carry	t_{PD}(max)	z -> y	2.3	ns	1 unit load
fast carry	t_{PD}(max)	z -> x	1.7	ns	1 unit load
DFF	t_{PD}(max)	q -> x/y	1.8	ns	1 unit load
DFF	t_{setup}(min)	x/y -> clk		ns	
DFF	t_{hold}(min)	x/y -> clk		ns	
DFF	t_{PD}(max)	R -> x/y	2.2	ns	1 unit load
DFF	t_{PD}(max)	S -> x/y	2.2	ns	1 unit load
DFF	t_{PD}(max)	q -> w	1.8	ns	
incremental --> L	t_{PD}(max)	x/y -> L	1.5	ns	1 unit load
Local output enable	t_{PZX}(max)	oe -> L	1.4	ns	1 unit load
Local output enable	t_{PXZ}(max)	oe -> L	1.8	ns	

AC Timing Characteristics - 5V Operation

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 4.75V, temperature = 70°C
Minimum times based on best case: V_{CC} = 5.25V, temperature = 0°C
Max delays are the average of t_{PDLH} and t_{PDHL}.

All input IO characteristics measured from a V_{IH} of 50% of V_{DD} at the pad (CMOS threshold) to the internal V_{IH} of 50% of V_C.
All output IO characteristics are measured as the average of t_{PDLH} and t_{PDHL} to the pad V_{IH} of 50% of V_{CC}.

Cell Function	Parameter	Path	-2	Units	Notes
Repeaters					
Repeater	t_{PD}(max)	L->E	1.3	ns	1 unit load
Repeater	t_{PD}(max)	E->E	1.3	ns	1 unit load
Repeater	t_{PD}(max)	L->L	1.3	ns	1 unit load
Repeater	t_{PD}(max)	E->L	1.3	ns	1 unit load
Repeater	t_{PD}(max)	E->IO	0.8	ns	1 unit load
Repeater	t_{PD}(max)	L->IO	0.8	ns	1 unit load

All input IO characteristics measured from a V_{IH} of 50% at the pad (CMOS threshold) to the internal V_{IH} of 50% of V_{CC}.
All output IO characteristics are measured as the average of t_{PDLH} and t_{PDHL} to the pad V_{IH} of 50% of V_{CC}.

Cell Function	Parameter	Path	-2	Units	Notes
IO					
Input	t_{PD}(max)	pad -> x/y	1.2	ns	no extra delay
Input	t_{PD}(max)	pad -> x/y	3.6	ns	1 extra delay
Input	t_{PD}(max)	pad -> x/y	7.3	ns	2 extra delays
Input	t_{PD}(max)	pad -> x/y	10.8	ns	3 extra delays
Output, slow	t_{PD}(max)	x/y/E/L -> pad	5.9	ns	50pf load
Output, medium	t_{PD}(max)	x/y/E/L -> pad	4.8	ns	50pf load
Output, fast	t_{PD}(max)	x/y/E/L -> pad	3.9	ns	50pf load
Output, slow	t_{PZX}(max)	oe -> pad	6.2	ns	50pf load
Output, low	t_{PXZ}(max)	oe -> pad	1.3	ns	50pf load
Output, medium	t_{PZX}(max)	oe -> pad	4.8	ns	50pf load
Output, medium	t_{PXZ}(max)	oe -> pad	1.9	ns	50pf load
Output, fast	t_{PZX}(max)	oe -> pad	3.7	ns	50pf load
Output, fast	t_{PXZ}(max)	oe -> pad	1.6	ns	50pf load

AC Timing Characteristics - 5V Operation

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 4.75V, temperature = 70°C
Minimum times based on best case: V_{CC} = 5.25V, temperature = 0°C
Max delays are the average of t_{PDLH} and t_{PDHL}.

Clocks and Reset Input buffers are measured from a V_{IH} of 1.5V at the input pad to the internal V_{IH} of 50% of V_{CC}.
Maximum times for clock input buffers and internal drivers are measured for rising edge delays only.

Cell Function	Parameter	Path	Device	-2	Units	Notes
Global Clocks and Set/Reset						
GCLK Input buffer	t_{PD}(max)	pad -> clock	AT40K05	1.1	ns	rising edge clock
		pad -> clock	AT40K10	1.2	ns	
		pad -> clock	AT40K20	1.2	ns	
		pad -> clock	AT40K40	1.4	ns	
FCLK Input buffer	t_{PD}(max)	pad -> clock	AT40K05	0.7	ns	rising edge clock
		pad -> clock	AT40K10	0.8	ns	
		pad -> clock	AT40K20	0.8	ns	
		pad -> clock	AT40K40	0.8	ns	
Clock column driver	t_{PD}(max)	clock -> colclk	AT40K05	0.8	ns	rising edge clock
		clock -> colclk	AT40K10	0.9	ns	
		clock -> colclk	AT40K20	1.0	ns	
		clock -> colclk	AT40K40	1.1	ns	
Clock sector driver	t_{PD}(max)	colclk -> secclk	AT40K05	0.5	ns	rising edge clock
		colclk -> secclk	AT40K10	0.5	ns	
		colclk -> secclk	AT40K20	0.5	ns	
		colclk -> secclk	AT40K40	0.5	ns	
GSRN Input buffer	t_{PD}(max)	pad -> GSRN	AT40K05	3.0	ns	
		colclk -> secclk	AT40K10	3.7	ns	
		colclk -> secclk	AT40K20	4.3	ns	
		colclk -> secclk	AT40K40	5.6	ns	
Global clock to output	t_{PD}(max)	clock pad -> out	AT40K05	8.3	ns	rising edge clock
		clock pad -> out	AT40K10	8.4	ns	fully loaded clock tree
		clock pad -> out	AT40K20	8.6	ns	rising edge DFF
		clock pad -> out	AT40K40	8.8	ns	20mA output buffer
						50 pf pin load
Output, fast	t_{PD}(max)	clock pad -> out	AT40K05	7.9	ns	rising edge clock
		clock pad -> out	AT40K10	8.0	ns	fully loaded clock tree
		clock pad -> out	AT40K20	8.1	ns	rising edge DFF
		clock pad -> out	AT40K40	8.3	ns	20mA output buffer
						50 pf pin load

AC Timing Characteristics - 5V Operation

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 4.75V, temperature = 70°C
Minimum times based on best case: V_{CC} = 5.25V, temperature = 0°C
Max delays are the average of t_{PDLH} and t_{PDHL}.

Cell Function	Parameter	Path	-2	Units	Notes
Async RAM					
Write	t_{WECYC}(min)	cycle time	8.0	ns	
Write	t_{WEL}(min)	we	3.0	ns	pulse width low
Write	t_{WEH}(min)	we	3.0	ns	pulse width high
Write	t_{setup}(min)	wr addr setup-> we	2.0	ns	
Write	t_{hold}(min)	wr addr hold -> we	0.0	ns	
Write	t_{setup}(min)	din setup -> we	2.0	ns	
Write	t_{hold}(min)	din hold -> we	0.0	ns	
Write	t_{hold}(min)	oe hold -> we	0.0	ns	
Write/Read	t_{PD}(max)	din -> dout	4.6	ns	rd addr = wr addr
Read	t_{PD}(max)	rd addr -> dout	3.1	ns	
Read	t_{PZX}(max)	oe -> dout	1.6	ns	
Read	t_{PXZ}(max)	oe -> dout	2.0	ns	
Sync RAM					
Write	t_{CYC}(min)	cycle time	8.0	ns	
Write	t_{CLKL}(min)	clk	3.0	ns	pulse width low
Write	t_{CLKH}(min)	clk	3.0	ns	pulse width high
Write	t_{setup}(min)	we setup-> clk	2.0	ns	
Write	t_{hold}(min)	we hold -> clk	0.0	ns	
Write	t_{setup}(min)	wr addr setup-> clk	2.0	ns	
Write	t_{hold}(min)	wr addr hold -> clk	0.0	ns	
Write	t_{setup}(min)	wr data setup-> clk	2.0	ns	
Write	t_{hold}(min)	wr data hold -> clk	0.0	ns	
Write/Read	t_{PD}(max)	din -> dout	4.6	ns	rd addr = wr addr
Write/Read	t_{PD}(max)	clk -> dout	3.5	ns	rd addr = wr addr
Read	t_{PD}(max)	rd addr -> dout	3.1	ns	
Read	t_{PZX}(max)	oe -> dout	1.6	ns	
Read	t_{PXZ}(max)	oe -> dout	2.0	ns	

Absolute Maximum Ratings - 3.3V Commercial/Industrial*

Symbol	Parameter	Conditions	Min	Max	Units
V_{CC}	Supply Voltage	With respect to GND	-0.5	7.0	V
V_I	DC Input Voltage[1]	With respect ot GND	-0.5	7.0	V
V_O	DC Output Voltaage	With respect ot GND	-0.5	7.0	V
T_{STG}	Storage Temperature		-65°C	+150°C	
T_J	Junction Temperature			+150°C	
T_L	Lead Temperature (Soldering, 10 sec.)			+250°C	
ESD		R_{ZAP} = 1.5K, C_{ZAP} = 100 pF		2000	V

Note: 1. Minimum voltage of -0.5V DC which may undershoot to -2.0V for pulses of less than 20 ns.

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range - 3.3V Operation

		AT40K05LV-4/3/2 AT40K10LV-4/3/2 AT40K20LV-4/3/2 AT40K40LV-4/3/2 Commercial	**AT40K05LV-4/3/2 AT40K10LV-4/3/2 AT40K20LV-4/3/2 AT40K40LV-4/3/2 Industrial**
Operating Temperature (Case)		0°C - 70°C	-40°C - 85°C
V_{CC} Power Supply		3.3V ± 0.3V	3.3V ± 0.3V
Input Voltage Level (CMOS)	High (V_{IHC})	70% - 100% V_{CC}	70% - 100% V_{CC}
	Low (V_{ILC})	0 - 30% V_{CC}	0 - 30% V_{CC}