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Features

- Number of keys: up to 16 keys, and one slider (constructed from 2 to 8 keys)
- Number of I/O lines: 11 (3 dedicated - configurable for input or output, 8 shared - output only), PWM control for LED driving
- Technology: patented spread-spectrum charge-transfer (transverse mode)
- Key outline sizes: 6 mm x 6 mm or larger (panel thickness dependent); widely different sizes and shapes possible
- Key spacings: 8 mm or wider, center to center (panel thickness dependent)
- Slider design: 2 to 8 keys placed in sequence, same design as keys
- Electrode design: two-part electrode shapes (drive-receive); wide variety of possible layouts
- PCB layers required: one layer (with jumpers), two layers (no jumpers)
- Electrode materials: PCB, FPCB, silver or carbon on film, ITO on film
- Panel materials: plastic, glass, composites, painted surfaces (low particle density metallic paints possible)
- Adjacent metal: compatible with grounded metal immediately next to keys
- Panel thickness: up to 3 mm glass, 2.5 mm plastic (key size dependent)
- Key sensitivity: individually settable via simple commands over I^2C-compatible interface
- Interface: I^2C-compatible slave mode (100 kHz)
- Moisture tolerance: best in class
- Power: 1.8 V to 5.5 V
- Package: 28-pin 4 x 4 mm MLF RoHS compliant
- Signal processing: self-calibration, auto drift compensation, noise filtering, Adjacent Key Suppression® technology
- Applications: laptop, mobile, consumer appliances, PC peripheral etc.
- Patents: AKS® (patented Adjacent Key Suppression) technology
  QMatrix® (patented charge-transfer method)
  QSlide® (patented charge-transfer method) (patent-pending QSlide sensing configuration)
- This datasheet is applicable to revision 1.0 chips only

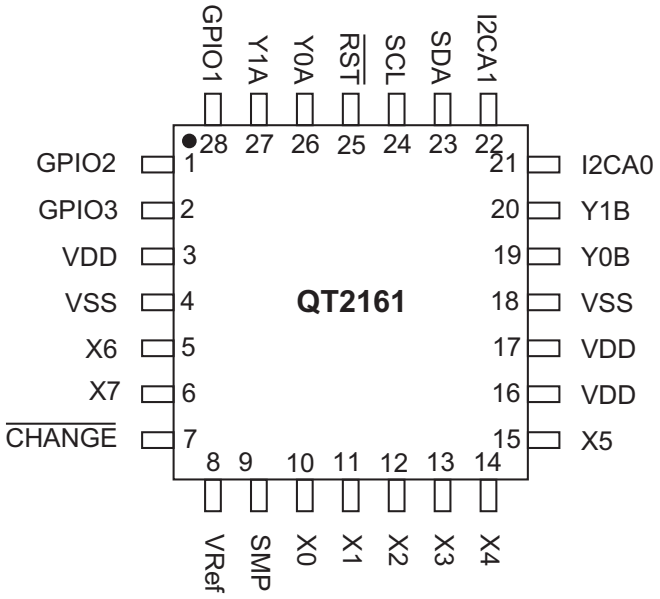
QSlide, 16-key QMatrix Sensor IC

AT42QT2161

9614A–AT42–08/10

1. Pinout and Schematic

1.1 Pinout Configuration



1.2 Pin Description

Table 1-1. Pin Listing

Pin	Function	I/O	Comments	If Unused, Connect To...
1	GPIO2	I/O	General purpose input/output 2	–
2	GPIO3	I/O	General purpose input/output 3	–
3	Vdd	P	Power	–
4	Vss	P	Ground	–
5	X6	O	X matrix drive line / shared GPO X6	Leave open
6	X7	O	X matrix drive line / shared GPO X7	Leave open
7	$\overline{\text{CHANGE}}$	OD	State change notification	Leave open
8	Vref	P	Ground	–
9	SMP	O	Sample output.	–
10	X0	O	X matrix drive line / shared GPO X0	Leave open
11	X1	O	X matrix drive line / shared GPO X1	Leave open
12	X2	O	X matrix drive line / shared GPO X2	Leave open
13	X3	O	X matrix drive line / shared GPO X3	Leave open

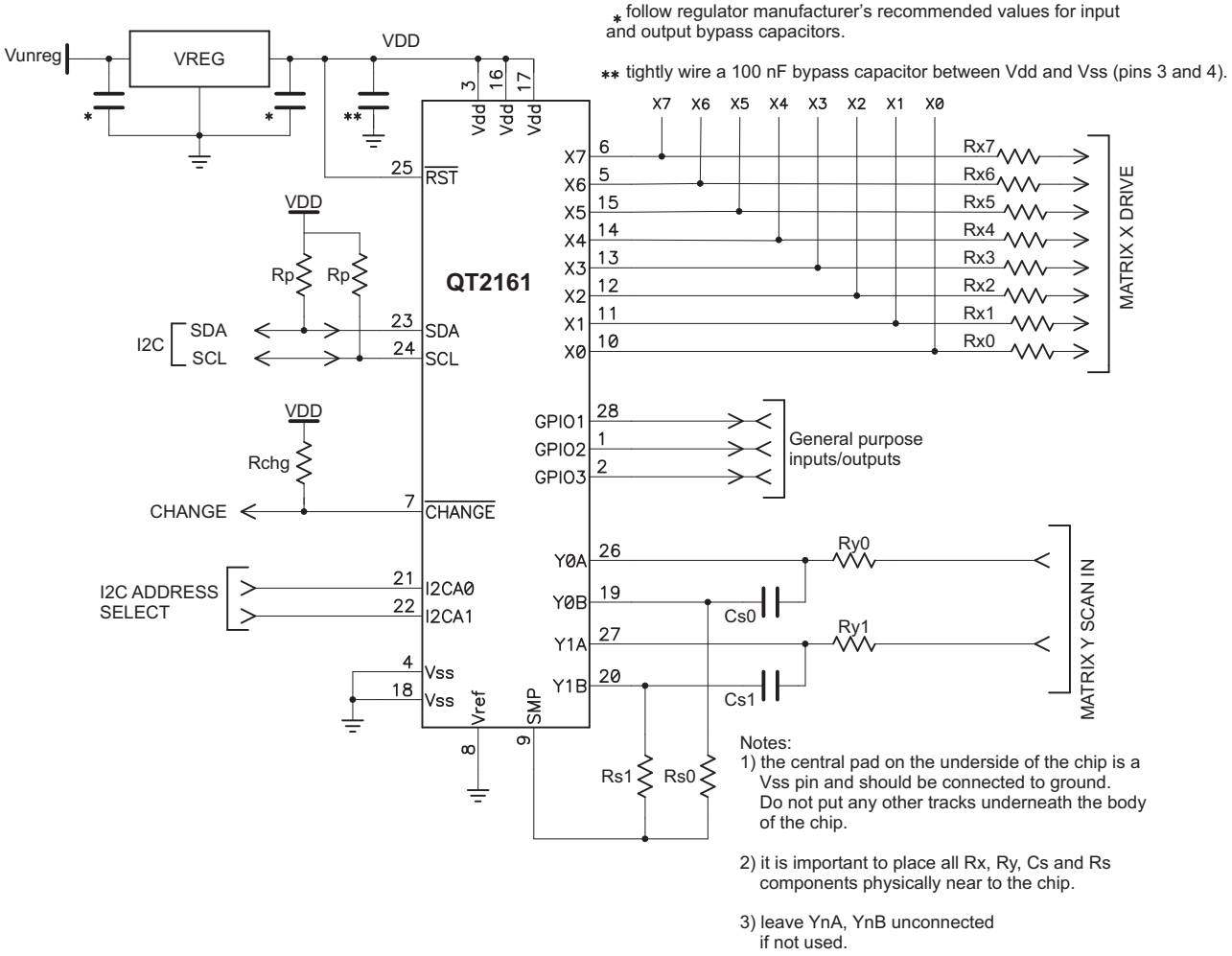
Table 1-1. Pin Listing (continued)

Pin	Function	I/O	Comments	If Unused, Connect To...
14	X4	O	X matrix drive line / shared GPO X4	Leave open
15	X5	O	X matrix drive line / shared GPO X5	Leave open
16	Vdd	P	Power	–
17	Vdd	P	Power	–
18	Vss	P	Ground	–
19	Y0B	I/O	Y line connection	Leave open
20	Y1B	I/O	Y line connection	Leave open
21	I2CA0	I	I^2C-compatible address select	–
22	I2CA1	I	I^2C-compatible address select	–
23	SDA	OD	Serial Interface Data	–
24	SCL	OD	Serial Interface Clock	–
25	$\overline{RST}$	I	Reset low; has internal 30 kΩ - 60 kΩ pull-up resistor	Leave open or Vdd
26	Y0A	I/O	Y line connection	Leave open
27	Y1A	I/O	Y line connection	Leave open
28	GPIO1	I/O	General purpose input/output 1	–

I	Input only	I/O	Input and output
O	Output only, push-pull	P	Ground or power
OD	Open drain output		

1.3 Schematics

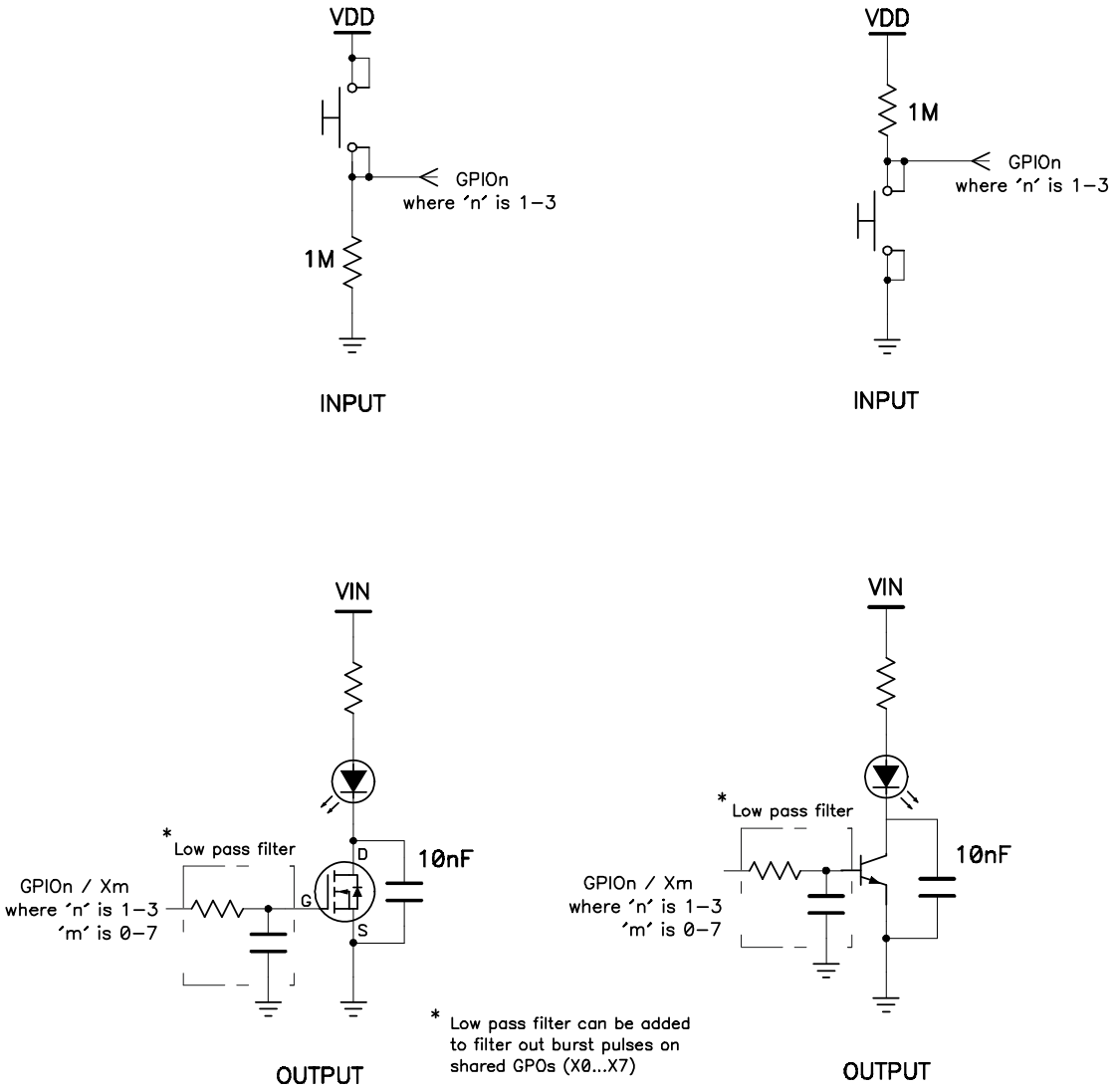
Figure 1-1. Typical Circuit



Re Figure 1-1 check the following sections for component values:

- Section 3.3 on page 8: Cs capacitors (Cs0 – Cs1)
- Section Note: on page 10: Sample resistors (Rs0 – Rs1)
- Section 3.7 on page 10: Matrix resistors (Rx0 – Rx7, Ry0 – Ry1)
- Section 3.11 on page 14: Voltage levels
- Section 5.4 on page 23: SDA, SCL pull-up resistors (Rp)
- Section 3.2 on page 8: $\overline{\text{CHANGE}}$ resistor (Rchg)
- Section 3.2 on page 8: I²C-compatible addresses

Figure 1-2. Inputs/Outputs



2. Overview

2.1 Introduction

The AT42QT2161-MMU (QT2161) is a digital burst mode charge-transfer (QT™) sensor designed specifically for matrix layout touch controls. It can use up to 16 keys and a slider (constructed from 2 – 8 keys). There are three dedicated General Purpose Input/Outputs (GPIOs) which can be used as inputs for mechanical switches etc. or as driven outputs. There are eight shared General Purpose Outputs (GPOs) (X0 – X7) which are driven outputs only. There is PWM control for all GPIO/GPOs.

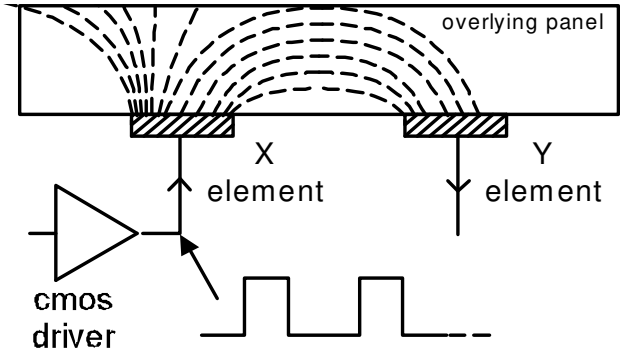
QMatrix® employs transverse QT sensing, a technology that senses changes in electrical charge forced across two electrode elements by a pulse edge (see Figure 2-1). The QT2161 allows a wide range of key sizes and shapes to be mixed.

The QT2161 includes all signal processing functions necessary to provide stable sensing under a wide variety of changing conditions. Only a few external parts are required for operation. The entire circuit can be built within a few square centimeters of single-sided PCB area. CEM-1 and FR1 punched, single-sided materials can be used for the lowest possible cost. The PCB's rear can be mounted flush on the back of a glass or plastic panel using a conventional adhesive, such as 3M VHB two-sided adhesive acrylic film.

The device uses an I^2C-compatible interface to allow key data to be extracted and to permit individual key parameter setup. The command structure is designed to minimize the amount of data traffic while maximizing the amount of information conveyed.

In addition to normal operating and setup functions the device can also report back actual signal strengths.

Figure 2-1. Field Flow Between X and Y Elements



2.2 Keys and Slider

The QT2161 is capable of a maximum of 16 keys. These can be located anywhere within an electrical grid of 8X and 2Y scan lines.

A lesser number of enabled keys will cause any unused acquisition burst timeslots to be pared from the sampling sequence, to optimize acquire speed and lessen power consumption. Thus, if only 8 keys are actually enabled, only 8 timeslots are used for scanning.

Additional processing can be done on the keys to form a slider. The slider will have to start at X0 and use only Y0. The slider can consist of a minimum of 2 keys and a maximum of 8 keys.

2.3 Enabling/Disabling Keys

Keys can be enabled by setting a nonzero burst length. A zero burst length disables the key.

3. Hardware and Functional

3.1 Matrix Scan Sequence

The circuit operates by scanning each key sequentially, key by key. Key scanning begins with location X = 0, Y = 0 (key 0). X axis keys are known as *rows* while Y axis keys are referred to as *columns* although this has no reflection on actual wiring. Keys are scanned sequentially by row, for example the sequence X0Y0 X1Y0 – X7Y0, X0Y1, X1Y1... etc. Keys are also numbered from 0 – 15. Key 0 is located at X0Y0. Table 3-1 shows the key numbering.

Table 3-1. Key Numbers

	X7	X6	X5	X4	X3	X2	X1	X0	
Y0	7	6	5	4	3	2	1	0	Key numbers
Y1	15	14	13	12	11	10	9	8	

Each key is sampled in a burst of acquisition pulses whose length is determined by the Setups parameter BL (Section 3.2 on page 8); this can be set on a per-key basis. A burst is completed entirely before the next key is sampled; at the end of each burst the resulting signal is converted to digital form and processed. The burst length directly impacts key gain; each key can have a unique burst length in order to allow tailoring of key sensitivity on a key-by-key basis.

3.2 Burst Paring

Keys that are disabled by setting their burst length to zero have their bursts removed from the scan sequence to save scan time and thus power. The QT2161 operates on a fixed 16 ms cycle and will go to sleep after all acquisitions and processing is done till the next 16 ms cycle starts. As a consequence, the fewer keys, the less power is consumed.

3.3 Cs Sample Capacitor Operation

Cs capacitors (Cs0 – Cs1) absorb charge from the key electrodes on the rising edge of each X pulse. On each falling edge of X, the Y matrix line is clamped to ground to allow the electrode and wiring charges to neutralize in preparation for the next pulse. With each X pulse charge accumulates on Cs causing a staircase increase in its differential voltage.

After the burst completes, the device clamps the Y line to ground causing the opposite terminal to go negative. The charge on Cs is then measured using an external resistor to ramp the negative terminal upwards until a zero crossing is achieved. The time required to zero cross becomes the measurement result.

The Cs capacitors should be connected as shown in Figure 1-1 on page 4. The value of these capacitors is not critical but 4.7 nF is recommended for most cases. They should be 10 percent X7R ceramic. If the transverse capacitive coupling from X to Y is large enough the voltage on a Cs capacitor can saturate, destroying gain. In such cases the burst length should be reduced and/or the Cs value increased. See Section 3.4.

If a Y line is not used its corresponding Cs capacitor may be omitted and the pins left floating.

3.4 Sample Capacitor Saturation

Cs voltage saturation at a pin YnB is shown in Figure 3-1. Saturation begins to occur when the voltage at a YnB pin becomes more negative than -0.25V at the end of the burst. This nonlinearity is caused by excessive voltage accumulation on Cs inducing conduction in the pin protection diodes. This badly saturated signal destroys key gain and introduces a strong thermal coefficient which can cause phantom detection. The cause of this is either from the burst length being too long, the Cs value being too small, or the X – Y transfer coupling being too large. Solutions include loosening up the key structure interleaving, more separation of the X and Y lines on the PCB, increasing Cs, and decreasing the burst length.

Increasing Cs will make the part slower; decreasing burst length will make it less sensitive. A better PCB layout and a looser key structure (up to a point) have no negative effects.

Cs voltages should be observed on an oscilloscope with the matrix layer bonded to the panel material; if the Rs side of any Cs ramps more negative than -0.25 volts during any burst (not counting overshoot spikes which are probe artifacts), there is a potential saturation problem.

Figure 3-2 shows a defective waveform similar to that of Figure 3-1, but in this case the distortion is caused by excessive stray capacitance coupling from the Y line to AC ground; for example, from running too near and too far alongside a ground trace, ground plane, or other traces. The excess coupling causes the charge-transfer effect to dissipate a significant portion of the received charge from a key into the stray capacitance. This phenomenon is more subtle; it can be best detected by increasing BL to a high count and watching what the waveform does as it descends towards and below -0.25V. The waveform will appear deceptively straight, but it will slowly start to flatten even before the -0.25V level is reached.

A correct waveform is shown in Figure 3-3. Note that the bottom edge of the bottom trace is substantially straight (ignoring the downward spikes).

Unlike other QT circuits, the Cs capacitor values on QT2161 devices have no effect on conversion gain. However, they do affect conversion time.

Unused Y lines should be left open.

Figure 3-1. VCs – Nonlinear During Burst
(Burst too long, or Cs too small, or X-Y transcapacitance too large)

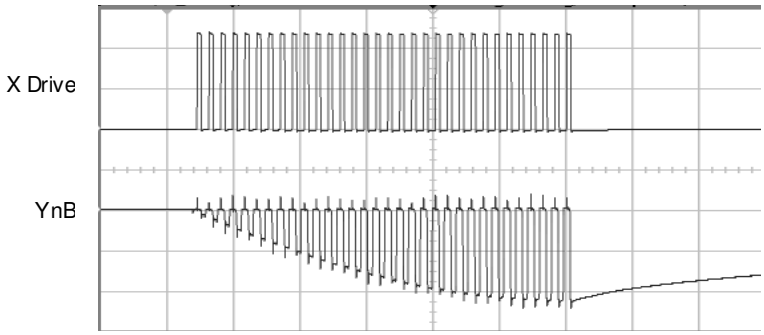


Figure 3-2. VCs – Poor Gain, Nonlinear During Burst
(Excess capacitance from Y line to Gnd)

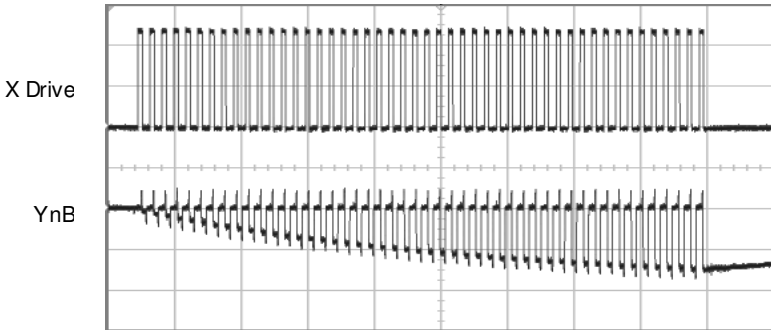


Figure 3-3. VCs – Correct

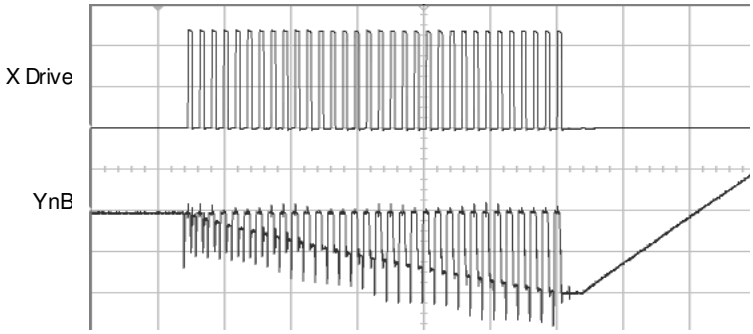
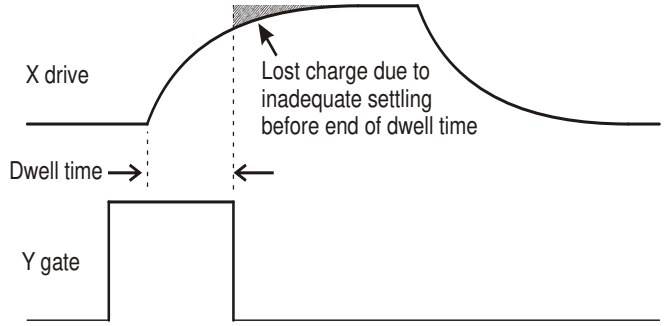


Figure 3-4. Drive Pulse Roll-off and Dwell Time



Note: The Dwell time is a minimum of ~250 ns - see Section 3.7

3.5 Sample Resistors

The sample resistors (Rs0 – Rs1) are used to perform single-slope ADC conversion of the acquired charge on each Cs capacitor. These resistors directly control acquisition gain; larger values of Rs will proportionately increase signal gain. For most applications Rs should be 1 MΩ. Unused Y lines do not require an Rs resistor.

3.6 Signal Levels

The signal values should normally be in the range of 200 to 750 counts with properly designed key shapes and values of Rs. However, long adjacent runs of X and Y lines can also artificially boost the signal values, and induce signal saturation; this is to be avoided. The X-to-Y coupling should come mostly from intra-key electrode coupling, not from stray X-to-Y trace coupling.

The signal swing from the smallest finger touch should preferably exceed 8 counts, with 12 being a reasonable target. The signal threshold setting (NTHR) should be set to a value guaranteed to be less than the signal swing caused by the smallest touch.

Increasing the burst length (BL) parameter will increase the signal strengths, as will increasing the sampling resistor (Rs) values.

3.7 Matrix Series Resistors

The X and Y matrix scan lines can use series resistors (Rx0 – Rx7 and Ry0 – Ry1 respectively) for improved EMC performance (Figure 1-1 on page 4).

X drive lines require Rx in most cases to reduce edge rates and thus reduce RF emissions. Values range from 1 kΩ to 20 kΩ, typically 1 kΩ.

Y lines need Ry to reduce EMC susceptibility problems and in some extreme cases, ESD. Typical Y values are about 1 kΩ. Y resistors act to reduce noise susceptibility problems by forming a natural low-pass filter with the Cs capacitors.

It is essential that the Rx and Ry resistors and Cs capacitors be placed very close to the chip. Placing these parts more than a few millimeters away opens the circuit up to high frequency interference problems (above 20 MHz) as the trace lengths between the components and the chip start to act as RF antennae.

The upper limits of Rx and Ry are reached when the signal level and hence key sensitivity are clearly reduced. The limits of Rx and Ry will depend on key geometry and stray capacitance, and thus an oscilloscope is required to determine optimum values of both.

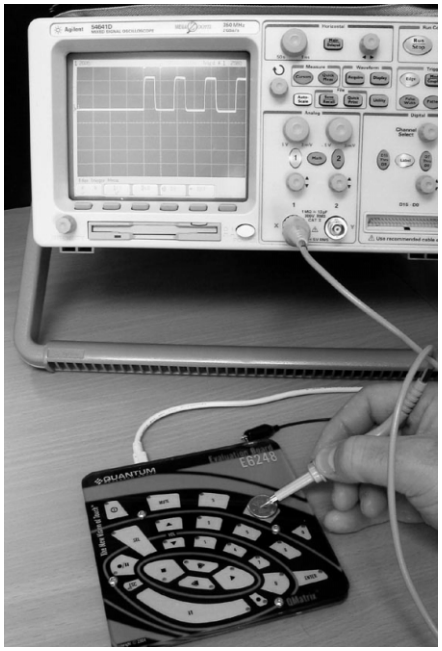
Dwell time is the duration in which charge coupled from X to Y is captured (Figure 3-4 on page 10). Increasing Rx values will cause the leading edge of the X pulses to increasingly roll off, causing the loss of captured charge (and hence loss of signal strength) from the keys.

The dwell time is a minimum of 250 ns. If the X pulses have not settled within 250 ns, key gain will be reduced; if this happens, either the stray capacitance on the X line(s) should be reduced (by a layout change, for example by reducing X line exposure to nearby ground planes or traces), or, the Rx resistor needs to be reduced in value (or a combination of both approaches).

One way to determine X line settling time is to monitor the fields using a patch of metal foil or a small coin over the key (Figure 3-5). Only one key along a particular X line needs to be observed, 250 ns dwell time should exceed the observed 95 percent settling of the X-pulse by 25 percent or more.

In almost all cases, Ry should be set equal to Rx, which will ensure that the charge on the Y line is fully captured into the Cs capacitor.

Figure 3-5. Probing X-Drive Waveforms With a Coin



3.8 Key Design

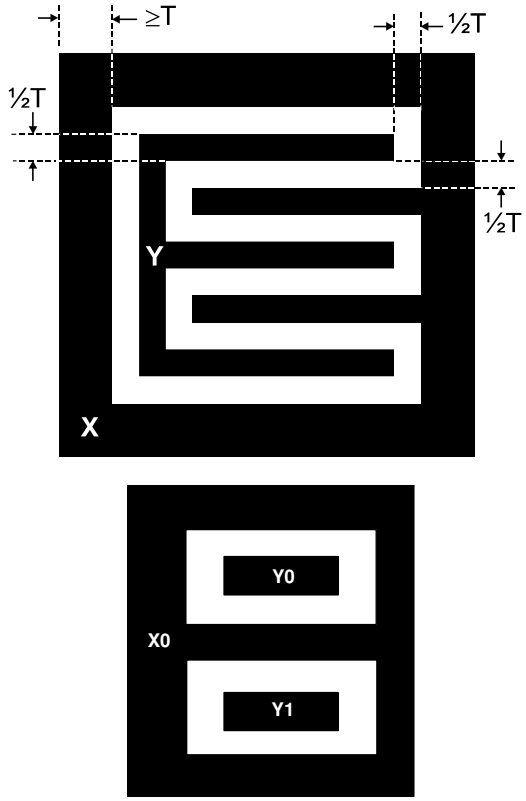
Circuits can be constructed out of a variety of materials including conventional FR-4, Flexible Printed Circuit Boards (FPCB), silver silk-screened on PET plastic film, and even inexpensive punched single-sided CEM-1 and FR-2.

The actual internal pattern style is not as important as the need to achieve regular X and Y widths and spacings of sufficient size to cover the desired graphical key area or a little bit more; ~3 mm oversize is acceptable in most cases, since the key's electric fields drop off near the edges anyway. The overall key size can range from 6 mm x 6 mm up to 100 mm x 100 mm but these are not hard limits. The keys can be any shape including round, rectangular, square, etc. The internal pattern can be interdigitated as shown in Figure 3-6.

For small, dense keypads, electrodes such as shown in the lower half of Figure 3-6 can be used. Where the panels are thin (under 2 mm thick) the electrode density can be quite high.

For better surface moisture suppression, the outer perimeter of X should be as wide as possible, and there should be no ground planes near the keys. The variable “T” in this drawing represents the total thickness of all materials that the keys must penetrate.

Figure 3-6. Recommended Key Structure



Note: “T” should ideally be similar to the complete thickness the fields need to penetrate to the touch surface. Smaller dimensions will also work but will give less signal strength. If in doubt, make the pattern coarser. The lower figure shows a simpler structure used for compact key layouts, for example for mobile phones. A layout with a common X drive and two receive electrodes is depicted

3.9 Setting the Slider

3.9.1 Introduction

Groups of keys can be configured as a slider, in addition to their use as keys. The slider uses the Y0 line of the matrix and must start at X0, with the keys placed in consecutive numerical order. The slider can take up a programmable number of keys on the Y0 line. The remaining keys on that Y line behave as normal.

Positional data is calculated in a customizable range of 2 bits (0 – 3) to 8 bits (0 – 255). Geometric constraints may mean that the data will not reach the full range. Thinner dielectric or the use of more keys in a slider will increase the data range towards the ends.

Stability of the reported position will be dependent on the amount of signal on the slider keys. Running at higher resolutions, with a thick panel might produce a fluctuating reported position.

Key sizes should be in the 5 – 7 mm range when used in the slider to get the best linearity. The slider should be made up of however many of these elements are required to fit their dimensions.

The slider will be treated as an object in the Adjacent Key Suppression (AKS) groupings. The keys in the slider would normally be set to the same burst length and threshold, although adjustments can be made in these at the expense of linearity.

3.9.2 AKS Technology and the Slider

There can be up to three AKS groups, implemented so that only one key in each group may be reported as being touched at any one time. The AKS technique will lock onto the dominant key, and until this key is released, other keys in the group will not be reported as in detection. This allows a user to slide a finger across multiple keys with only the dominant key reporting touch. Each key may be in one of the groups 1 – 3, or in group 0 meaning that it is not AKS enabled.

Keys in the slider are not able to use AKS technique against each other. This is necessary to enable smooth scrolling. Multiple keys within the slider can be in detect at the same time, regardless of the AKS settings. The AKS technique will, however, work against keys outside the object or within another object. For example, if a slider is in the same AKS group as keys, then touching anywhere on the slider will cause the AKS technique to suppress the keys. Similarly touching the keys first will suppress the slider.

Note: For normal operation all keys in the slider should be placed in the same AKS group.

3.10 PCB Layout, Construction

3.10.1 Overview

It is best to place the chip near the touch keys on the same PCB so as to reduce X and Y trace lengths, thereby reducing the chances for EMC problems. Long connection traces act as RF antennae. The Y (receive) lines are much more susceptible to noise pickup than the X (drive) lines.

Even more importantly, all signal related discrete parts (resistors and capacitors) should be very close to the body of the chip. Wiring between the chip and the various resistors and capacitors should be as short and direct as possible to suppress noise pickup.

Ground planes, if used, should be placed under or around the QT chip itself and the associated resistors and capacitors in the circuit, under or around the power supply, and back to a connector. Ground planes can be used to shield against radiated noise, but at the expense of a reduction in sensitivity as described previously.

Note: When using ground planes/floods, parasitic capacitance on Y lines can lead to reduced charge-transfer efficiency. For noise suppression, ground planes/floods can be beneficial around and between keys on the touch side of the PCB. However, it is advisable to route Y lines on the PCB layer furthest away from the plane/flood, to reduce parasitic capacitance. Cross-hatched ground patterns can act as effective shields, while helping to reduce parasitic capacitance. Ground planes/floods around the chip are generally acceptable, taking into account the same considerations as for the Y line parasitics.

3.10.2 LED Traces and Other Switching Signals

Digital switching signals near the Y lines will induce transients into the acquired signals, deteriorating the SNR performance of the device. Such signals should be routed away from the Y lines, or the design should be such that these lines are not switched during the course of signal acquisition (bursts).

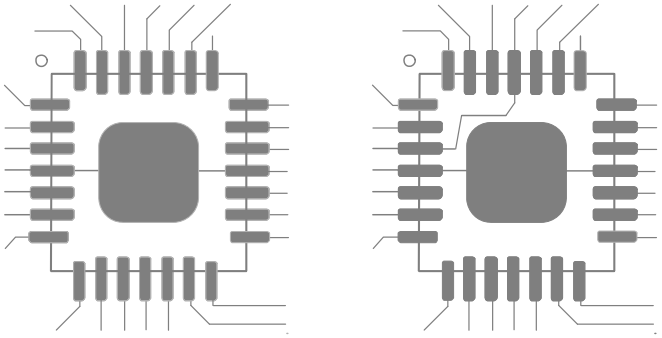
LED terminals which are multiplexed or switched into a floating state and which are within or physically very near a key structure (even if on another nearby PCB) should be bypassed to either Vss or Vdd with at least a 10nF capacitor to suppress capacitive coupling effects which can induce false signal shifts. The bypass capacitor does not need to be next to the LED, in fact it can be quite distant. The bypass capacitor is noncritical and can be of any type.

LED terminals which are constantly connected to Vss or Vdd do not need further bypassing.

3.10.3 Tracks

The central pad on the underside of the chip should be connected to ground. Do not run any tracks underneath the body of the chip, only ground.

Figure 3-7. Position of Tracks



Example of good tracking Example of bad tracking

3.10.4 PCB Cleanliness

Modern no-clean flux is generally compatible with capacitive sensing circuits.

CAUTION: If a PCB is reworked in any way, it is almost guaranteed that the behavior of the no-clean flux will change. This can mean that the flux changes from an inert material to one that can absorb moisture and dramatically affect capacitive measurements due to additional leakage currents. If so, the circuit can become erratic and exhibit poor environmental stability.

If a PCB is reworked in any way, clean it thoroughly to remove all traces of the flux residue around the capacitive sensor components. Dry it thoroughly before any further testing is conducted.

3.11 Power Supply Considerations

See Section 9.2 on page 44 for the Vdd range and short-term power supply fluctuations. If the power supply fluctuates slowly with temperature, the device will track and compensate for these changes automatically with only minor changes in sensitivity. If the supply voltage drifts or shifts quickly, the drift compensation mechanism will not be able to keep up, causing sensitivity anomalies or false detections.

As the device uses the power supply itself as an analog reference, the power should be very clean and come from a separate regulator. A standard inexpensive Low Dropout (LDO) type regulator should be used that is not also used to power other loads such as LEDs, relays, or other high current devices. Load shifts on the output of the LDO can cause Vdd to fluctuate enough to cause false detection or sensitivity shifts.

Caution: A regulator IC shared with other logic devices can result in erratic operation and is **not** advised.

A regulator can be shared among two or more QT devices on one board.

A single ceramic 0.1uF bypass capacitor, with short traces, should be placed very close to supply pins 3 and 4 of the IC. Failure to do so can result in device oscillation, high current consumption, erratic operation etc. Pins 16 and 17 do not require bypassing if the traces between these pins and power traces are short.

3.12 Startup/Calibration Times

The device requires initialization times of approximately 70 ms. The $\overline{\text{CHANGE}}$ line will go low and calibration will start (takes 15 matrix scans), after this start up period is over.

3.13 Calibration

Calibration does not occur periodically. Keys are only calibrated on power-up and when:

- Enabled

  AND

  – held in detect for too long. The negative recalibration delay (NRD) period is specified by the user

  OR

  – the signal delta value is greater than the positive threshold value, defined as reference value plus three-quarters of the negative threshold

  OR

  – the user issues a recalibrate command

An interrupt on the $\overline{\text{CHANGE}}$ pin occurs when there is a change in the key status bytes. An interrupt will occur on calibration only if at least one of the keys or objects was in detect as recalibration will then cause a status change.

3.14 Reset Input

The $\overline{\text{RST}}$ pin can be used to reset the device to simulate a power-down cycle, in order to bring the device up into a known state should communications with the device be lost. The pin is active low, and a low pulse lasting at least 10µs must be applied to this pin to cause a reset.

If an external hardware reset is not used, the reset pin may be connected to Vdd.

3.15 Spread Spectrum Acquisitions

QT2161 uses spread-spectrum burst modulation. This has the effect of drastically reducing the possibility of EMI effects on the sensor keys, while simultaneously spreading RF emissions. This feature is hard-wired into the device and cannot be disabled or modified.

Spread spectrum is configured as a frequency chirp over a wide range of frequencies for robust operation.

3.16 Detection Integrator

See also Section 3.2 on page 8.

The device features a detection integration mechanism, which acts to confirm a detection in a robust fashion. A per-key counter is incremented each time the key has exceeded its threshold and stayed there for a number of acquisitions. When this counter reaches a preset limit the key is finally declared to be touched.

For example, if the limit value is 10, then the device has to exceed its threshold and stay there for 10 acquisitions in succession without going below the threshold level, before the key is declared to be touched. If on any acquisition the signal is not seen to exceed the threshold level, the counter is cleared and the process has to start from the beginning.

3.17 Sleep

The device operates on a fixed 16 ms cycle time basis. The device will perform a set of measurements and then sleep for the rest of the cycle to conserve power.

There are two user-configurable sleep modes; Low Power (LP) mode and SLEEP mode.

The **LP** setting (see Section 3.2 on page 8) is used for conserving power when there are no touches and is set to be a long time period. This will determine how often the device wakes up to do drift compensation. It also determines the maximum response time to the first touch after inactivity.

When a valid touch is registered, the device enters minimum cycle time (16 ms) for a faster response to key touch and object operation. The device will stay in this mode if it continues to see keys being touched and released. There is a user-selectable inactivity timeout i.e. the awake timeout.

The measurement period needs to be shorter than the 16 ms fixed cycle time for optimum operation. If the measurement time exceeds the 16 ms fixed cycle time, a CYCLE OVERRUN bit is set in the general status register. The QT2161 will still operate if the 16 ms fixed cycle time is exceeded, but the timing for the timed parameters, e.g. drift compensation negative recalibration time out etc. will slightly change.

A low power setting of zero causes the device to enter an ultra-low power mode (**SLEEP**), where no measurements are carried out. SLEEP mode also stops the internal watchdog timer, so that the part is totally dormant, and current drain is <2µA. The PWM function will not be carried out during SLEEP, therefore it is recommended driving the GPIOs/GPOs to known states before entering SLEEP mode.

The QT2161 wakes from SLEEP mode if there is an address match on the I^2C-compatible bus, a hardware reset on the $\overline{RST}$ pin or an LP mode is set. If the Wake option is set for the dedicated GPIO inputs, then the QT2161 will trigger the $\overline{CHANGE}$ line if a change in status (either positive or negative going edge) of the respective GPIO is detected, in SLEEP mode.

3.18 General Purpose Inputs/Outputs

There are three dedicated GPIOs (GPIO1 – 3) and eight GPOs shared with X lines (X0 – 7). Shared GPOs are always outputs, whereas dedicated GPIOs can be set to be outputs or inputs.

GPIOs set to input can be used for reading dome switches or logic signals. Outputs can be used to drive LEDs, or other devices. It is recommended driving external devices through the use of bipolar transistors or MOSFETs, so as not to affect capacitive sensing if a load fluctuates the power rail by drawing/sinking too much current.

All GPOs and GPIOs set to output can be PWM driven, if the corresponding PWM bit is set. Note that the PWM duty cycle will be an approximation, as GPIOs will not be switched during acquisition bursts.

The dedicated GPIOs have a Wake option, that if enabled will enable dedicated GPIOs set as inputs, to be read in SLEEP mode.

Note that shared GPOs (X0 – X7) are driven by the burst pulses during acquisition bursts, if the corresponding X line is used in the keys/slider. A low pass filter can be inserted to eliminate these burst pulses, as shown in Figure 1-2 on page 5.

4. I²C-compatible Bus Operation

4.1 Interface Bus

More detailed information about the I²C-compatible bus protocol is available from www.i2C-bus.org. Devices are connected onto the I²C-compatible bus as shown in Figure 4-1. Both bus lines are connected to Vdd via pull-up resistors. The bus drivers of all I²C-compatible devices must be open-drain type. This implements a wired-AND function which allows any and all devices to drive the bus, one at a time. A low level on the bus is generated when a device outputs a zero.

Figure 4-1. I²C-compatible Interface Bus

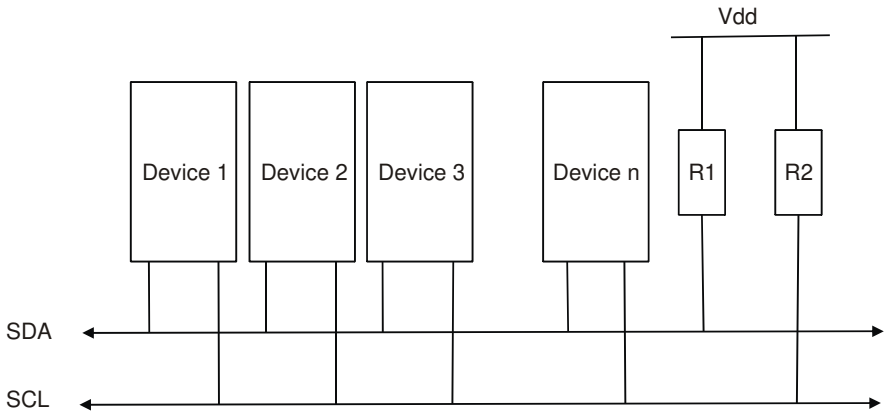


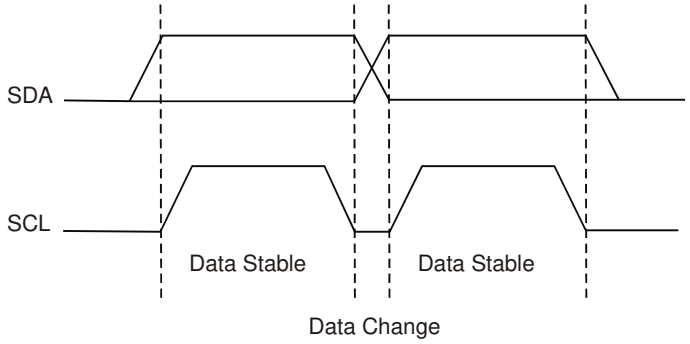
Table 4-1. I²C-compatible Bus Specifications

Parameter	Unit
Address space	7-bit
Maximum bus speed (SCL)	100 kHz
Hold time START condition	4 µs minimum
Setup time for STOP condition	4 µs minimum
Bus free time between a STOP and START condition	4.7 µs minimum
Rise times on SDA and SCL	1 µs maximum

4.2 Transferring Data Bits

Each data bit transferred on the bus is accompanied by a pulse on the clock line. The level of the data line must be stable when the clock line is high; The only exception to this rule is for generating START and STOP conditions.

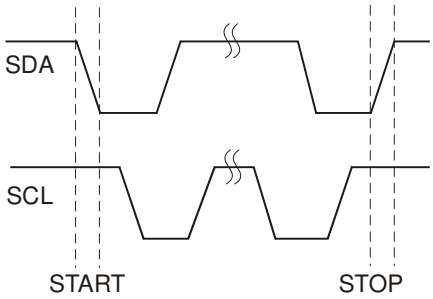
Figure 4-2. Data Transfer



4.3 START and STOP Conditions

The host initiates and terminates a data transmission. The transmission is initiated when the host issues a START condition on the bus, and is terminated when the host issues a STOP condition. Between START and STOP conditions, the bus is considered busy. As shown in Figure 4-3, START and STOP conditions are signaled by changing the level of the SDA line when the SCL line is high.

Figure 4-3. START and STOP Conditions

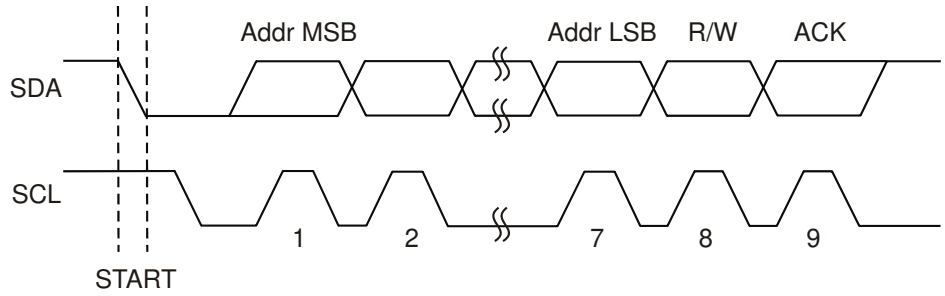


4.4 Address Packet Format

All address packets are 9 bits long, consisting of 7 address bits, one READ/WRITE control bit and an acknowledge bit. If the READ/WRITE bit is set, a read operation is performed, otherwise a write operation is performed. When the device recognizes that it is being addressed, it will acknowledge by pulling SDA low in the ninth SCL (ACK) cycle. An address packet consisting of a slave address and a READ or a WRITE bit is called SLA+R or SLA+W, respectively.

The most significant bit of the address byte is transmitted first. The address sent by the host must be consistent with that selected with the option jumpers.

Figure 4-4. Address Packet Format



4.5 Data Packet Format

All data packets are 9 bits long, consisting of one data byte and an acknowledge bit. During a data transfer, the host generates the clock and the START and STOP conditions, while the Receiver is responsible for acknowledging the reception. An acknowledge (ACK) is signaled by the Receiver pulling the SDA line low during the ninth SCL cycle. If the Receiver leaves the SDA line high, a NACK is signaled.

4.6 Combining Address and Data Packets Into a Transmission

A transmission consists of a START condition, an SLA+R/W, one or more data packets and a STOP condition. The wired-ANDing of the SCL line is used to implement handshaking between the host and the device. The device extends the SCL low period by pulling the SCL line low whenever it needs extra time for processing between the data transmissions.

Holding down either SCL or SDA for clock stretching or any other purpose will slow down the operation of the QT2161. This stretching is used while QT2161 processes data just received, or prepares data to send. QT2161 needs to clock stretch (see Section 9.4 on page 45 for timing) to complete certain actions before ACK of transfer. If SCL or SDA is continuously held low for more than ~12 ms, this will be deemed as a error condition and the I^2C-compatible unit reset.

Note: Each write or read cycle must end with a STOP condition. The QT2161 may not respond correctly if a cycle is terminated by a new START condition.

Figure 4-6 shows a typical data transmission. Note that several data bytes can be transmitted between the SLA+R/W and the STOP.

Figure 4-5. Data Packet Format

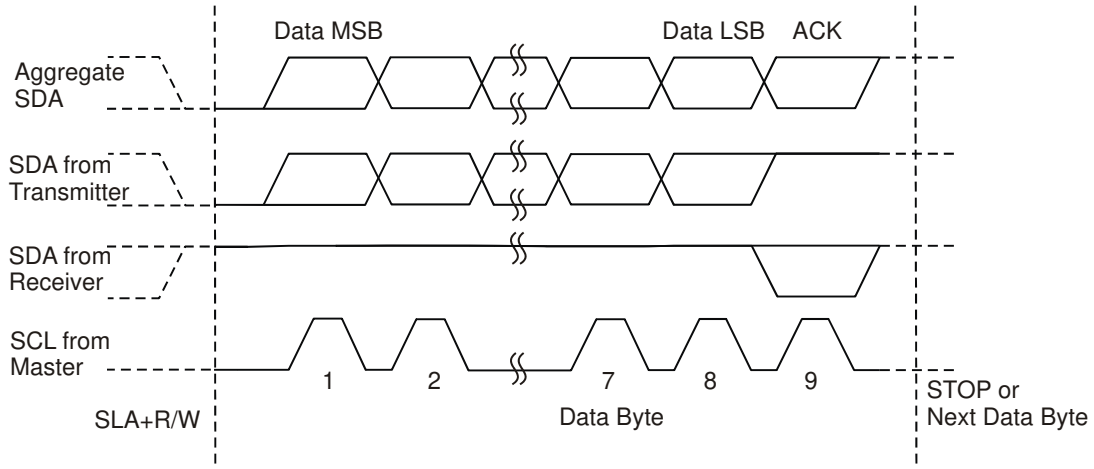
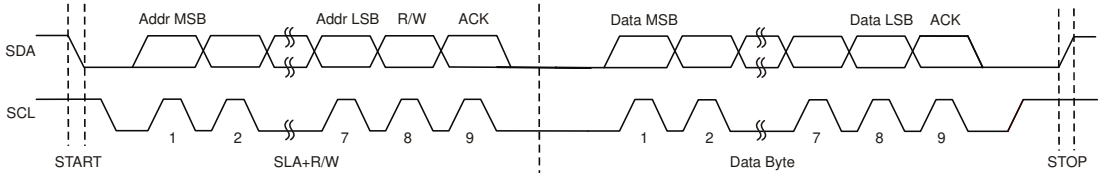


Figure 4-6. Packet Transmission



5. Interfaces

5.1 I²C-compatible Protocol

The I²C-compatible protocol is based around access to an address table and supports multibyte reads and writes.

Note: Each write or read cycle must end with a stop condition. The QT2161 may not respond correctly if a cycle is terminated by a new start condition.

5.2 I²C-compatible Addresses

Four preset I²C-compatible addresses are selectable through pin I2CA0 and I2CA1 (Table 5-1).

Table 5-1. I²C-compatible Addresses

I2CA1	I2CA0	Address
0	0	0x0D
0	1	0x17
1	0	0x44
1	1	0x6B

5.3 Data Read/Write

5.3.1 Writing Data to the Device

The sequence of events required to write data to the device is shown next.

Key	
S	Start condition
SLA+W	Slave address plus write bit
A	Acknowledge bit
MemAddress	Target memory address within device
Data	Data to be written
P	Stop condition

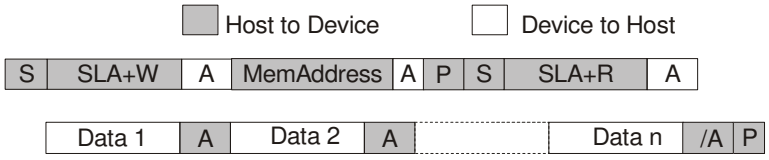
The host initiates the transfer by sending the START condition, and follows this by sending the slave address of the device together with the Write-bit. The device sends an ACK. The host then sends the memory address within the device it wishes to write to. The device sends an ACK. The host transmits one or more data bytes; each will be acknowledged by the device.

If the host sends more than one data byte, they will be written to consecutive memory addresses. The device automatically increments the target memory address after writing each data byte. After writing the last data byte, the host should send the STOP condition.

The host should not try to write beyond address 255 because the device will not increment the internal memory address beyond this.

5.3.2 Reading Data From the Device

The sequence of events required to read data from the device is shown next.



The host initiates the transfer by sending the START condition, and follows this by sending the slave address of the device together with the Write-bit. The device sends an ACK. The host then sends the memory address within the device it wishes to read from. The device sends an ACK.

The host must then send a STOP and a START condition followed by the slave address again but this time accompanied by the Read-bit. The device will return an ACK, followed by a data byte. The host must return either an ACK or NACK. If the host returns an ACK, the device will subsequently transmit the data byte from the next address. Each time a data byte is transmitted, the device automatically increments the internal address. The device will continue to return data bytes until the host responds with a NACK. The host should terminate the transfer by issuing the STOP condition.

5.4 SDA, SCL

The I²C-compatible bus transmits data and clock with SDA and SCL. They are open-drain; that is I²C-compatible master and slave devices can only drive these lines low or leave them open. The termination resistors (Rp) pull the line up to Vdd if no I²C-compatible device is pulling it down.

The termination resistors commonly range from 1 kΩ to 10 kΩ and should be chosen so that the rise times on SDA and SCL meet the I²C-compatible specifications (1µs maximum).

5.5 CHANGE Pin

The $\overline{\text{CHANGE}}$ pin is an active low open drain output that can be used to alert the host of any changes to any of the 5 status bytes (address 2 to 6), thus reducing the need for wasteful I²C-compatible communications. After setting up the QT2161, the host can simply not communicate with the device, except when the $\overline{\text{CHANGE}}$ pin goes active.

$\overline{\text{CHANGE}}$ goes inactive again only when the host performs a read from all status bytes which have changed.

Poll rate: The host can make use of the $\overline{\text{CHANGE}}$ pin output to initiate a communication; this will guarantee the optimal polling rate.

If the host cannot make use of the $\overline{\text{CHANGE}}$ pin, the poll rate should be no faster than once per matrix scan (see Section 9.4 on page 45). Anything faster will not provide new information and will slow down the chip operation.

The $\overline{\text{CHANGE}}$ pin requires a pull-up resistor, with a typical value of ~100 kΩ.

6. Communications Protocol

6.1 Introduction

The device is address mapped. All communications consist of writes to, and reads from, locations in an 8-bit address map. Table 6-1 shows the address map of QT2161.

Table 6-1. Memory Map

Address	Use	Access
0	Chip ID	Read
1	Major/minor code version	Read
2	General Status	Read
3	Key Status 1	Read
4	Key Status 2	Read
5	Slider Touch Position	Read
6	GPIO Read	Read
7	Sub-revision	–
8 – 9	Reserved – 0x00	–
10	Calibrate	Read/Write
11	Reset	Read/Write
12	LP Mode	Read/Write
13	Burst Repetition	Read/Write
14	Reserved – 0x00	Read/Write
15	Neg Drift Compensation	Read/Write
16	Pos Drift Compensation	Read/Write
17	Normal DI Limit	Read/Write
18	Neg Recal Delay	Read/Write
19	Drift Hold Time/AWAKE	Read/Write
20	Slider Control	Read/Write
21	Slider Options	Read/Write
22 – 37	Key 0 – 15 Key Control	Read/Write
38 – 53	Key 0 – 15 Neg Threshold	Read/Write
54 – 69	Key 0 – 15 Burst Length	Read/Write
70	GPIO/GPO Drive 1	Read/Write

Table 6-1. Memory Map (continued)

Address	Use	Access
71	GPIO/GPO Drive 2	Read/Write
72	Reserved – 0x00	Read/Write
73	GPIO Direction 2	Read/Write
74	GPIO/GPO PWM 1	Read/Write
75	GPIO/GPO PWM 2	Read/Write
76	PWM Level	Read/Write
77	GPIO Wake	Read/Write
78	Common change Keys 1	Read/Write
79	Common change Keys 2	Read/Write
80 – 99	Reserved – 0x00	–
100 – 131	Key 0 – 15 Signals	Read
132 – 163	Key 0 – 15 References	Read

Note: Reserved areas can be read or written to, to simplify communications. If written to, only write 0x00.

6.2 Address 0: Chip ID

Table 6-2. Chip ID

Address	b7	b6	b5	b4	b3	b2	b1	b0
0	Chip ID							

There is an 8-bit chip ID, which is set at 0x3D.

6.3 Address 1: Code Version

Table 6-3. Code Version

Address	b7	b6	b5	b4	b3	b2	b1	b0
1	Major Version				Minor Version			

There is an 8-bit major and minor version of firmware code revision. The top nibble of the firmware version register contains the major version (e.g. **1**.0) and the bottom nibble contains the minor version (e.g. 1.**0**).