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Atmel AT42QT2640

64-key 8-slider/wheel QMatrix FMEA IEC/EN/UL60730 Touch Sensor IC

PRELIMINARY DATASHEET

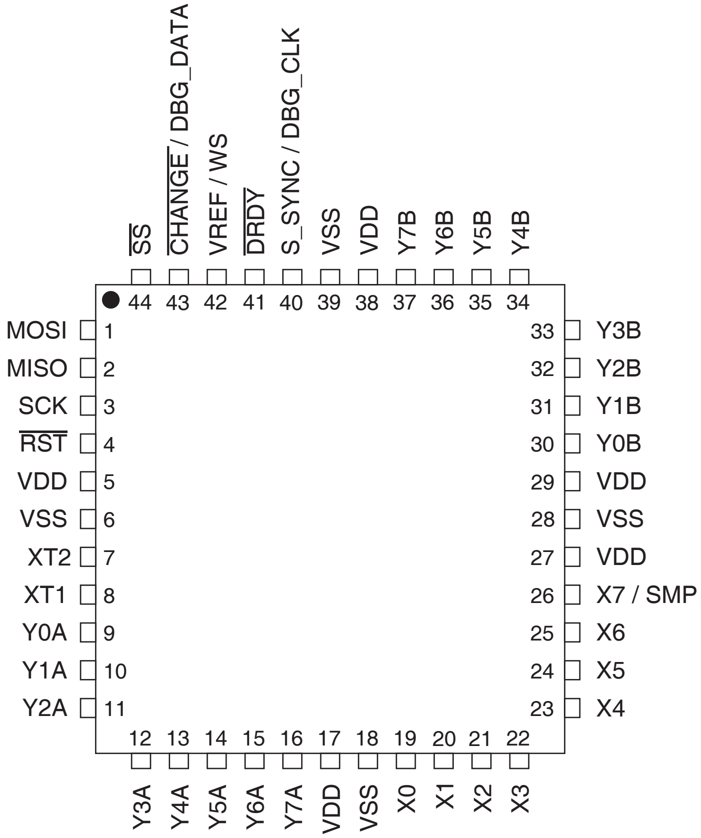
Features

- Number of channels:
  - Up to 64 keys
  - Up to eight sliders/wheels, each with 8-bit resolution
- Technology:
  - Patented charge-transfer (transverse mode), with frequency hopping
- Key outline sizes:
  - 5 mm × 5 mm or larger (panel thickness dependent); widely different sizes and shapes possible
- Key spacings:
  - 6 mm or wider, center to center (panel thickness dependent)
- Electrode design:
  - Two-part electrode shapes (drive-receive); wide variety of possible layouts
- Layers required:
  - One layer (with jumpers), two layers (no jumpers)
- Electrode materials:
  - PCB, FPCB, silver or carbon on film, ITO on film
- Panel materials:
  - Plastic, glass, composites, painted surfaces (low particle density metallic paints possible)
- Adjacent Metal:
  - Compatible with grounded metal immediately next to keys
- Panel thickness:
  - Up to 50 mm glass, 20 mm plastic (key size dependent)
- Key sensitivity:
  - Individually settable over serial interface
- Interfaces:
  - SPI slave (4 MHz max. clock)
  - CHANGE status indication pin
  - Debug output
- Signal processing:
  - Self-calibration, auto drift compensation, noise filtering, Adjacent Key Suppression® (AKS®)
- FMEA compliant design features

- IEC/EN/UL60730 compliant design features
  - UL approval
  - VDE compliance
  - For use in both class B and class C safety-critical products
- Detects and Reports Key Failure
- Power:
  - 4.75 V to 5.25 V
- Package:
  - 44-pin 10 × 10 mm TQFP RoHS compliant

1. Pinout and Schematic

1.1 Pinout Configuration



1.2 Pin Descriptions

Table 1-1. Pin Listing

Pin	Name	Type	Comments	If Unused, connect To...
1	MOSI	I	SPI data input	–
2	MISO	O	SPI data output	–
3	SCK	I	SPI clock input	–
4	$\overline{\text{RST}}$	I	Reset low; has internal 30 kΩ – 60 kΩ pull-up resistor. This pin should be controlled by the host.	Vdd
5	VDD	P	Power	–
6	VSS	P	Ground	–
7	XT2	O	Ceramic resonator or crystal,16 MHz	–
8	XT1	I		–
9	Y0A	I/O	Y line connection	Leave open
10	Y1A	I/O	Y line connection	Leave open
11	Y2A	I/O	Y line connection	Leave open
12	Y3A	I/O	Y line connection	Leave open
13	Y4A	I/O	Y line connection	Leave open
14	Y5A	I/O	Y line connection	Leave open
15	Y6A	I/O	Y line connection	Leave open
16	Y7A	I/O	Y line connection	Leave open
17	VDD	P	Power	–
18	VSS	P	Ground	–
19	X0	O	X matrix drive line	Leave open
20	X1	O	X matrix drive line	Leave open
21	X2	O	X matrix drive line	Leave open
22	X3	O	X matrix drive line	Leave open
23	X4	O	X matrix drive line	Leave open
24	X5	O	X matrix drive line	Leave open
25	X6	O	X matrix drive line	Leave open
26	X7 / SMP	O	X matrix drive line / Sample output	Leave open / –
27	VDD	P	Power	–
28	VSS	P	Ground	–
29	VDD	P	Power	–

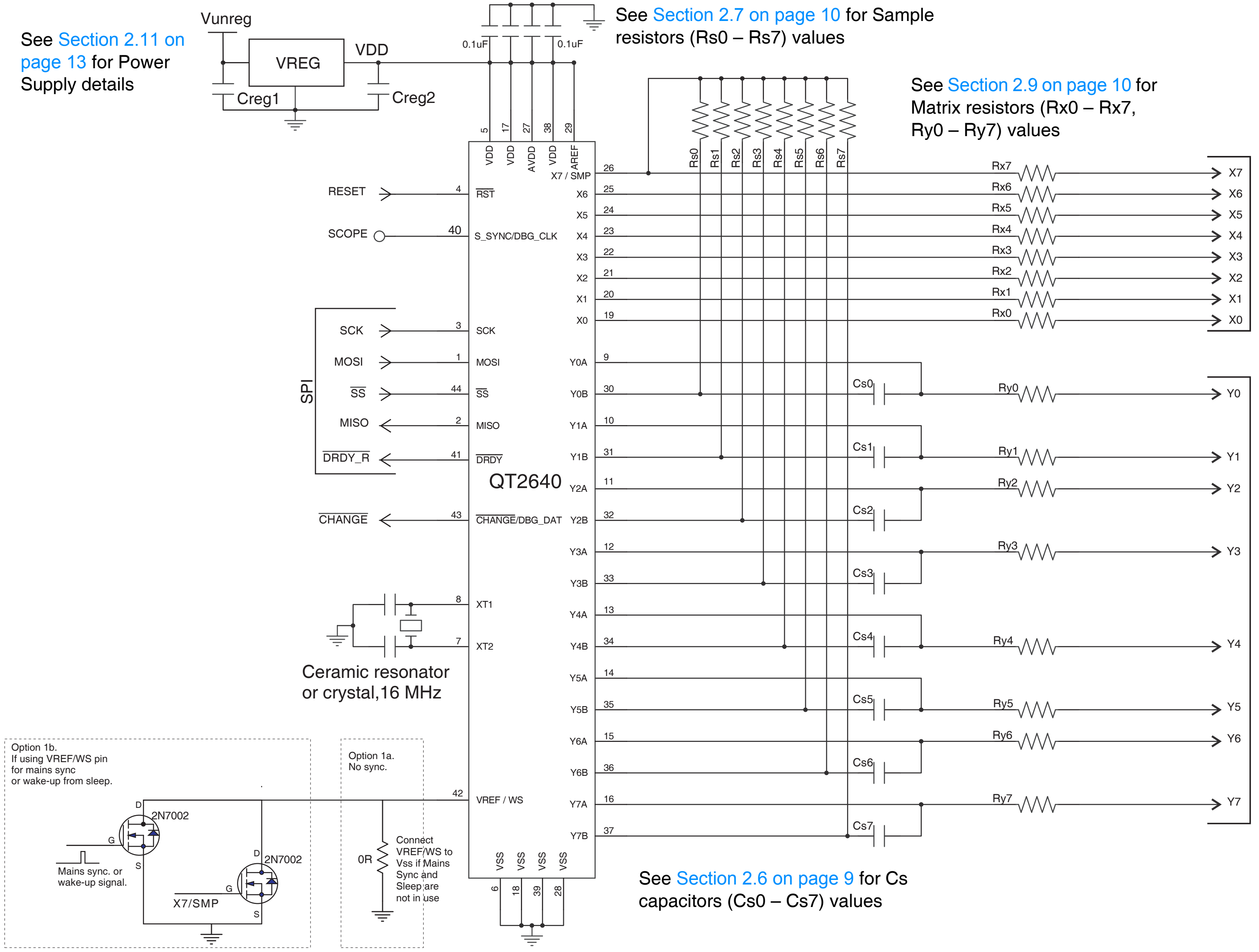
Table 1-1. Pin Listing (Continued)

Pin	Name	Type	Comments	If Unused, connect To…
30	Y0B	I/O	Y line connection	Leave open
31	Y1B	I/O	Y line connection	Leave open
32	Y2B	I/O	Y line connection	Leave open
33	Y3B	I/O	Y line connection	Leave open
34	Y4B	I/O	Y line connection	Leave open
35	Y5B	I/O	Y line connection	Leave open
36	Y6B	I/O	Y line connection	Leave open
37	Y7B	I/O	Y line connection	Leave open
38	VDD	P	Power	–
39	VSS	P	Ground	–
4O	S_SYNC / DBG_CLK	O	Scope Synchronization output or Debug Clock	Leave open
41	$\overline{\text{DRDY}}$	OD	This pin MUST be used. 1 = comms ready; need a 100 µs grace period before checking. Open-drain with internal 20 kΩ – 50 kΩ pull-up resistor	–
42	VREF/ WS	I	Connect to Vss unless using sleep or mains sync / Wake-up from sleep input and/or sync input	– VSS
43	$\overline{\text{CHANGE}}$ / DBG_DATA	OD / O	Key touch change, active low. Has internal 20 kΩ – 50 kΩ pull-up resistor. / Debug Data	Leave open
44	$\overline{\text{SS}}$	I	SPI slave select; has internal 20 kΩ – 50 kΩ pull-up resistor	–

I	Input only	O	Output only, push-pullI/O	Input/output
OD	Open drain output	P	Ground or power	

1.3 Schematic

Figure 1-1. Typical Circuit


See Section 2.11 on page 13 for Power Supply details

See Section 2.7 on page 10 for Sample resistors (Rs0 – Rs7) values

See Section 2.9 on page 10 for Matrix resistors (Rx0 – Rx7, Ry0 – Ry7) values

See Section 2.6 on page 9 for Cs capacitors (Cs0 – Cs7) values

Ceramic resonator or crystal,16 MHz

Option 1b.
If using VREF/WS pin
for mains sync
or wake-up from sleep.

Option 1a.
No sync.

Connect VREF/WS to Vss if Mains Sync and Sleep are not in use

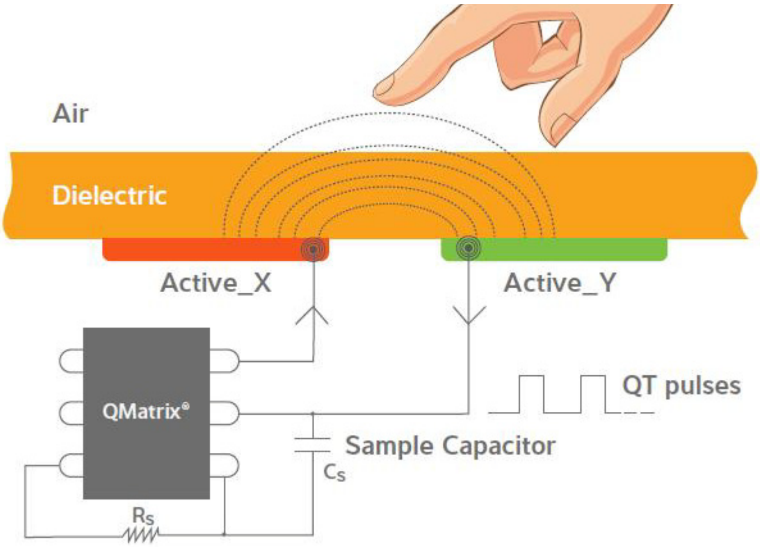
2. Hardware and Functional

2.1 Introduction

The AT42QT2640 (QT2640) is a digital burst-mode sensor, designed specifically for QMatrix layout touch controls; it includes all signal processing functions necessary to provide stable sensing under a wide variety of changing conditions. Only a few external parts are required for operation. The entire circuit can be built within a few square centimeters of single-sided PCB area. CEM-1 and FR1 punched, single-sided materials can be used for the lowest possible cost. The PCB rear can be mounted flush on the back of a glass or plastic panel using a conventional adhesive, such as 3M VHB two-sided adhesive acrylic film.

The QT2640 employs QMatrix transverse charge-transfer (QT™) sensing – a technology that senses changes in electrical charge forced across two electrode elements by a pulse edge (see Figure 2-1).

Figure 2-1. Field Flow Between X and Y Elements



The QT2640 allows a wide range of key sizes and shapes to be mixed together in a single touch panel, and is designed for use with up to 64 keys, and up to eight sliders and wheels, or a mixture of keys, sliders and wheels.

The QT2640 uses a memory mapped SPI interface to allow key data to be extracted and to permit individual key parameter setup. The structure is designed to minimize the amount of data traffic while maximizing the amount of information conveyed.

In addition to normal operating and setup functions the QT2640 can also report back actual signal strengths and error codes.

QmBtn™ software for the PC can be used to program the operation of the IC as well as read back key status and signal levels in real time.

A Debug output interface is also supported, which can be used to monitor many operating variables during product development.

The QT2640 incorporates many tests and checks to enable a product to achieve FMEA and IEC/EN/UL60730 compliance. The results of some tests need to be checked by the host. To achieve a compliant design, the host must read back the test results and confirm their validity.

The QT2640 is able to scan the touch matrix twice as fast as previous generation devices; it can take twice the number of samples in a given time frame. This means the QT2640 is much better equipped to continue normal operation in the face of heavy noise.

See Appendix C. on page 69 for information on conducted noise immunity.

2.2 Key Numbers

The keys are numbered from 0 – 63. Table 2-1 shows the key numbering.

Table 2-1. Key Numbers

	X7	X6	X5	X4	X3	X2	X1	X0	
Y0	7	6	5	4	3	2	1	0	Key numbers
Y1	15	14	13	12	11	10	9	8	
Y2	23	22	21	20	19	18	17	16	
Y3	31	30	29	28	27	26	25	24	
Y4	39	38	37	36	35	34	33	32	
Y5	47	46	45	44	43	42	41	40	
Y6	55	54	53	52	51	50	49	48	
Y7	63	62	61	60	59	58	57	56	

2.3 Matrix Scan Sequence

Key scanning begins with location X = 0, Y = 0 (key 0). All keys on X0 are scanned first, then X1 and finishing with all keys on X7 (for example, the sequence X0Y0, X0Y1 – X0Y7, X1Y0 – X1Y7 … X7Y1 – X7Y6, X7Y7). Table 2-1 shows the key numbering.

All keys on the same X line are excited together in a burst of acquisition pulses whose length is determined by the setups parameter BL (see Section 5.5 on page 41); this can be set to a different value for each key. A burst is completed entirely before the next X line is excited. At the end of each burst the resulting signals, one for each Y line, are converted to digital form and processed. The burst length directly impacts key gain. Each key can have a different burst length in order to allow tailoring of key sensitivity. Although all keys on an entire X line are excited simultaneously, the charge is selectively captured at each Y line according to the burst length selected.

2.4 Enabling/Disabling Keys – Burst Removal

Unused keys are always removed from the computation sequence in order to optimize speed. If all keys are disabled on any given X, the entire X line is also removed from the burst sequence. If only two X lines have enabled keys, only two timeslots are used for scanning.

The NDIL parameter is used to enable and disable keys in the matrix. Setting NDIL = 0 for a key disables it (Section 5.3 on page 39). Keys that are disabled are eliminated from the scan sequence to save scan time and thus power. If all keys on an X line are disabled, the burst for the entire X line is removed from the scan sequence, further saving time and power. This has the consequence of affecting the scan rate of the entire matrix as well as the time required for initial matrix calibration. It does not affect the time required to calibrate an individual key once the matrix is initially calibrated after power-up or reset.

It is very important that only those keys that physically exist are enabled. All non-existent keys must be disabled (NDIL = 0) otherwise other keys in the matrix can incorrectly report their signal as zero.

2.5 Oscillator

The oscillator can use either a quartz crystal or a ceramic resonator. In all cases, XT1 and XT2 must both be loaded with low-value capacitors to ground. These capacitors should be in the range 12 pF to 22 pF. Follow the manufacturer's recommendations for the appropriate value within this range. Resonators and crystals requiring loading capacitors outside this range are unsuitable for operation with the QT2640.

A resistor of value 1MΩ is connected internally between XT1 and XT2.

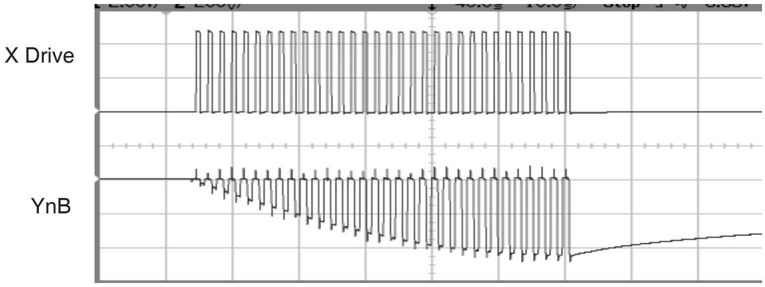
The frequency of oscillation should be 16 MHz ±2%.

2.6 Sample Capacitor; Saturation Effects

The charge sampler capacitors on the Y pins (Cs0 – Cs7) should be NPO (preferred), X7R ceramics or PPS film; NPO offers the best stability. The value of these capacitors is not critical but 4.7 nF is recommended for most cases.

Cs voltage saturation is shown in Figure 2-2. This nonlinearity is caused by excessive voltage accumulation on Cs inducing conduction in the pin protection diodes. This badly saturated signal destroys key gain and introduces a strong thermal coefficient which can cause phantom detection.

Figure 2-2. VCs – Nonlinear During Burst
(Burst too long, or Cs too small, or X-Y transcapacitance too large)



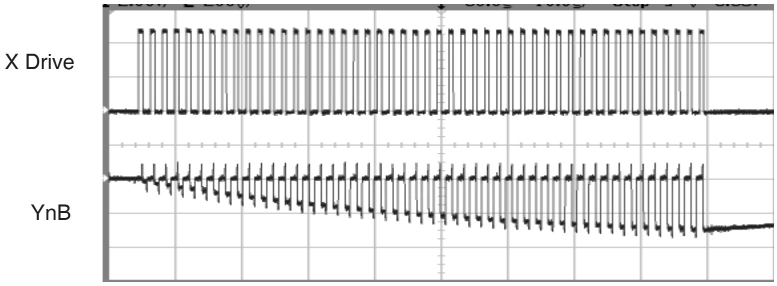
The cause of this is either from the burst length being too long, the Cs value being too small, or the X-Y transfer coupling being too large. Solutions include loosening up the interdigitation of key structures, greater separation of the X and Y lines on the PCB, increasing Cs, and decreasing the burst length.

Increasing Cs makes the part slower; decreasing burst length makes it less sensitive. A better PCB layout and a looser key structure (up to a point) have no negative effects.

Cs voltages should be observed on an oscilloscope with the matrix layer bonded to the panel material; if the Rs side of any Cs ramp is more negative than –0.25 V during any burst (not counting overshoot spikes which are probe artifacts), there is a potential saturation problem.

Figure 2-3 shows a defective waveform similar to that of Figure 2-2, but in this case the distortion is caused by excessive stray capacitance coupling from the Y line to AC ground; for example, from running too near and too far alongside a ground trace, ground plane, or other traces. The excess coupling causes the charge-transfer effect to dissipate a significant portion of the received charge from a key into the stray capacitance.

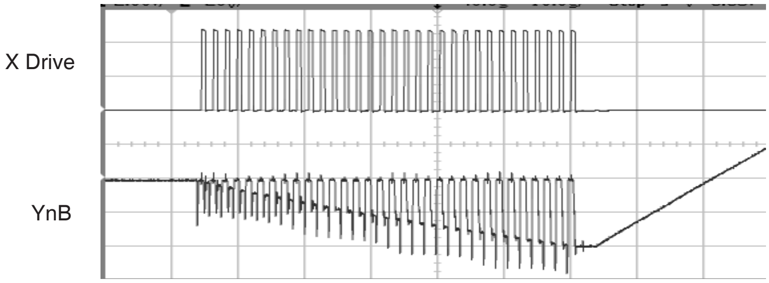
Figure 2-3. VCs – Poor Gain, Nonlinear During Burst
(Excess capacitance from Y line to Gnd)



This phenomenon is more subtle; it can be best detected by increasing BL to a high count and watching what the waveform does as it descends towards and below –0.25 V. The waveform appears deceptively straight, but it slowly starts to flatten even before the –0.25 V level is reached.

A correct waveform is shown in Figure 2-4. Note that the bottom edge of the bottom trace is substantially straight (ignoring the downward spikes).

Figure 2-4. VCs – Correct



Unlike other QT circuits, the Cs capacitor values on QT2640 have no effect on conversion gain. However, they do affect conversion time.

Unused Y lines should be left open.

2.7 Sample Resistors

The sample resistors (Rs0 – Rs7) are used to perform single-slope analog-to-digital (ADC) conversion of the acquired charge on each Cs capacitor. These resistors directly control acquisition gain; larger values of Rs proportionately increase signal gain. Values of Rs can range from 220 kΩ to 4.7 MΩ. A value of 470 kΩ is typical for most purposes.

Unused Y lines do not require an Rs resistor.

2.8 Signal Levels

Using Atmel's QmBtn software it is easy to observe the absolute level of signal received by the sensor on each key. The signal values should normally be in the range of 250 to 750 counts with properly designed key shapes (see the *Touch Sensors Design Guide*, available on Atmel's website www.atmel.com). However, long adjacent runs of X and Y lines can also artificially boost the signal values, and induce signal saturation: this is to be avoided. The X-to-Y coupling should come mostly from intra-key electrode coupling, not from stray X-to-Y trace coupling.

QmBtn software is available free of charge on the Atmel website.

The signal swing from the smallest finger touch should preferably exceed 10 counts, with 15 being a reasonable target. The signal threshold setting (NTHR) should be set to a value guaranteed to be less than the signal swing caused by the smallest touch.

Increasing the burst length (BL) parameter increases the signal strengths as will increasing the sampling resistor (Rs) values.

2.9 Matrix Series Resistors

The X and Y matrix scan lines should use series resistors (Rx0 – Rx7 and Ry0 – Ry7 respectively) for improved EMC performance (Figure 1-1 on page 6).

X drive lines require Rx in most cases to reduce edge rates and thus reduce RF emissions. Values range from 1 kΩ to 100 kΩ, typically 1 kΩ.

Y lines need Ry to reduce EMC susceptibility problems and in some extreme cases, ESD. Values range from 1 kΩ to 100 kΩ, typically 1 kΩ. Y resistors act to reduce noise susceptibility problems by forming a natural low-pass filter with the Cs capacitors.

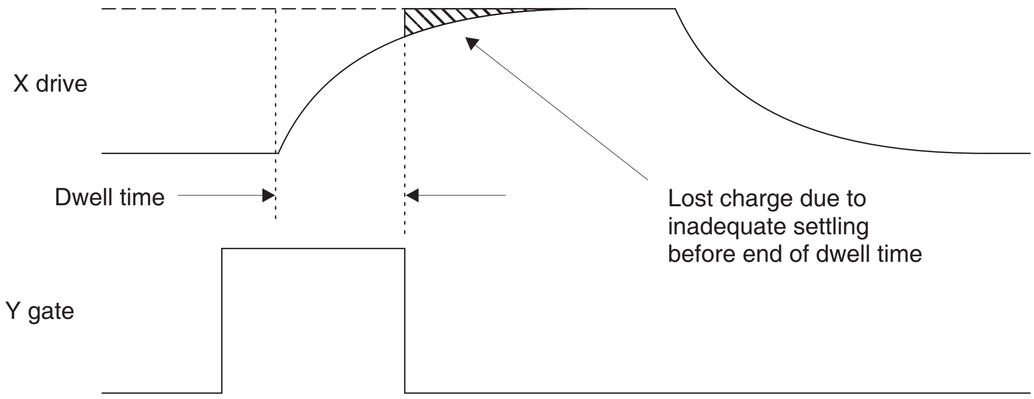
It is essential that the Rx and Ry resistors and Cs capacitors be placed very close to the chip. Placing these parts more than a few millimeters away opens the circuit up to high frequency interference problems (above 20 MHz) as the trace lengths between the components and the chip start to act as RF antennas.

The upper limits of Rx and Ry are reached when the signal level and hence key sensitivity are clearly reduced. The limits of Rx and Ry depend on key geometry and stray capacitance, and thus an oscilloscope is required to determine optimum values of both.

Dwell time is the duration in which charge coupled from X to Y is captured (Figure 2-5 on page 11). Increasing the dwell time increases the signal levels lost to higher values of Rx and Ry, as shown in Figure 2-5. Too short a dwell time causes charge to be 'lost', if there is too much rising edge roll-off. Lengthening the dwell time causes this lost charge to be recaptured, thereby restoring key sensitivity. In the QT2640 dwell time is adjustable (see Section 5.8 on page 46).

Dwell time problems can also be solved by either reducing the stray capacitance on the X line(s) (by a layout change – for example, by reducing X line exposure to nearby ground planes or traces) or the Rx resistor needs to be reduced in value (or a combination of both approaches).

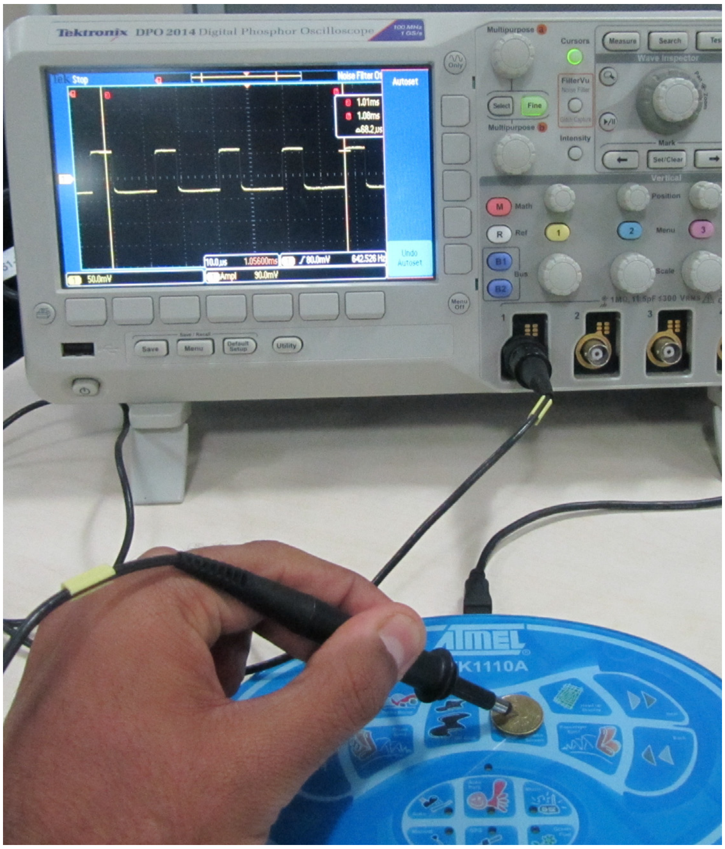
Figure 2-5. Drive Pulse Roll-off and Dwell Time


X drive
Dwell time
Lost charge due to inadequate settling before end of dwell time
Y gate

Note: The Dwell time is a minimum of ~125 ns – see Section 5.8 on page 46

One way to determine X line settling time is to monitor the fields using a patch of metal foil or a small coin over the key (see Figure 2-6). Only one key along a particular X line needs to be observed, as each of the keys along a particular X line are identical. The dwell time should exceed the observed 95% settling of the X-pulse by 25% or more.

Figure 2-6. Probing X-Drive Waveforms With a Coin



2.10 PCB Layout, Construction

2.10.1 Overview

It is best to place the chip near the touch keys on the same PCB so as to reduce X and Y trace lengths, thereby reducing the chances for EMC problems. Long connection traces act as RF antennas. The Y (receive) lines are much more susceptible to noise pickup than the X (drive) lines.

Even more importantly, all signal related discrete parts (resistors and capacitors) should be very close to the body of the chip. Wiring between the chip and the various resistors and capacitors should be as short and direct as possible to suppress noise pickup.

Ground planes and traces should NOT be used around the keys and the Y lines from the keys. Ground areas, traces, and other adjacent signal conductors that act as AC ground (such as Vdd) absorb the received key signals and reduce signal-to-noise ratio (SNR) and thus are counterproductive. Ground planes around keys also make water film effects worse.

Ground planes, if used, should be placed under or around the QT2640 chip itself and the associated resistors and capacitors in the circuit, under or around the power supply, and back to a connector, but nowhere else.

2.10.2 LED Traces and Other Switching Signals

Digital switching signals near the Y lines induce transients into the acquired signals, deteriorating the SNR performance of the QT2640. Such signals should be routed away from the Y lines, or the design should be such that these lines are not switched during the course of signal acquisition (bursts).

LED terminals which are multiplexed or switched into a floating state and which are within or physically very near a key structure (even if on another nearby PCB) should be bypassed to either Vss or Vdd with at least a 10 nF capacitor of any type, to suppress capacitive coupling effects which can induce false signal shifts. LED terminals which are constantly connected to Vss or Vdd do not need further bypassing.

2.10.3 PCB Cleanliness

Modern no-clean flux is generally compatible with capacitive sensing circuits.

CAUTION: If a PCB is reworked in any way, it is highly likely that the behavior of no-clean flux will change. This can mean that the flux changes from an inert material to one that can absorb moisture and dramatically affect capacitive measurements due to additional leakage currents. If so, the circuit can become erratic and exhibit poor environmental stability.

If a PCB is reworked in any way, clean it thoroughly to remove all traces of the flux residue around the capacitive sensor components. Dry it thoroughly before any further testing is conducted.

2.11 Power Supply Considerations

For Vdd information see Section 6.1 and Section 6.2 on page 59.

As the QT2640 uses the power supply as an analog reference, the power should be very clean and come from a separate regulator. A standard inexpensive Low Dropout (LDO) type regulator should be used; it should not also be used to power other loads such as relays or other high current devices. Load shifts on the output of the LDO can cause Vdd to fluctuate enough to cause false detection or sensitivity shifts.

Ceramic 0.1 µF bypass capacitors should be placed very close and routed with short traces to all power pins of the IC. There should be at least four such capacitors around the part.

2.12 Startup/Calibration Times

The QT2640 employs a rigorous initialization and self-check sequence for IEC/EN/UL60730 compliance. If the self-tests are passed, the last step in this sequence enables the serial communication interface. The communication interface is not enabled if a safety critical fault is detected during the startup sequence. The QT2640 requires initialization times as follows:

1. Normal reset to ability to communicate: 110 ms.
2. From very first power-up to ability to communicate:
   4.7 s (one time event to initialize all of EEPROM, or to recover EEPROM copy from Flash in the event of EEPROM corruption).
3. From power-up to ability to communicate:
   190 ms in the event the setups have been changed and the part needs to back up the EEPROM to Flash.

The QT2640 determines a reference level for each key by calibrating all the keys immediately after initialization. Each key is calibrated independently and in parallel with all other enabled keys. Calibration takes between 11 and 62 keyscan cycles; each cycle being made up of one sample from each enabled key. The QT2640 ends calibration for a key if its reference has converged with the signal DC level. The calibration time is shortest when the keys signals are stable, typically increasing with increasing noise levels to the maximum of 62 keyscan cycles.

An error is reported for each key where calibration continues for the maximum number of keyscan cycles and the key's reference does not appear to have converged with the signals DC level. Noise levels can vary from key to key such that some keys may take longer to calibrate than others. However, the QT2640 can report during this interval that the key(s) affected are still in calibration via the QT2640 status bits. Table 2-2 shows keyscan cycle times and calibration times per key versus dwell time and burst length for all 64 keys enabled. The values given assume the factory default settings except where noted.

Table 2-2. Keyscan Cycle and Calibration Times

Setups	Keyscan Cycle Time	Calibration Time (min)	Calibration Time (max)

BL = 0 (16 pulses)
DWELL = 0 (125 ns)
Rs = 470 kW
Signal level = 200 counts
	7 ms	77 ms (11 × 7)	434 ms (62 × 7)

2.13 Reset Input

Should communications with the QT2640 be lost, the $\overline{\text{RST}}$ pin can be used to reset the QT2640 to simulate a power-down cycle, in order to then bring the QT2640 up into a known state. The pin is active low, and a low pulse lasting at least 10 µs must be applied to this pin to cause a reset.

To provide for proper operation during power transitions the QT2640 has an internal brownout detector set to 4 V.

The reset pin has an internal 30 kΩ – 60 kΩ resistor. A 2.2 µF capacitor plus a diode to Vdd can be connected to this pin as a traditional reset circuit, but this is not necessary.

Where the QT2640 has detected a failure of one of the internal IEC/EN/UL60730 checks and has subsequently locked up in an infinite loop, only a power cycle or an external hardware reset can restore normal operation. It is strongly recommended that the host has control over the $\overline{\text{RST}}$ pin.

If an external hardware reset is not used, this pin may be connected to Vdd or left floating.

2.14 Detection Integrators

See also Section 5.3 on page 39.

The device features a detection integration mechanism, which acts to confirm a detection in a robust fashion. A per-key counter is incremented each time the key has exceeded its threshold and is decremented each time the key does not exceed its threshold. When this counter reaches a preset limit the key is finally declared to be touched.

For example, if the limit value is 10, then the device has to exceed its threshold and stay there for a minimum of 10 acquisitions before the key is declared to be touched.

The QT2640 uses a two-tier confirmation mechanism having two such counters for each key. These can be thought of as inner loop and outer loop confirmation counters. The inner counter is referred to as the fast DI; this acts to confirm a detection via rapid successive acquisition bursts, at the expense of delaying the sampling of the next key. Each key has its own fast DI counter and limit value; these limits can be changed via the setups block on a per-key basis.

The outer counter is referred to as the normal DI; this DI counter increments whenever the fast DI counter has reached its limit value. The normal DI counter also has a limit value which can be set on a per-key basis. If a normal DI counter reaches its terminal count, the corresponding key is declared to be touched and becomes active. Note that the normal DI can only be incremented once per complete keyscan cycle; that is, more slowly, whereas the fast DI is incremented “on the spot” without interruption.

The net effect of this mechanism is a multiplication of the inner and outer counters and hence a highly noise-resistant sensing method. If the inner limit is set to 5, and the outer to 3, the net effect is a minimum of 5 × 3 = 15 threshold crossings to declare a key as active.

2.15 Sleep

The QT2640 can be configured for automatic sleep using the Sleep Drift Compensation (SDC) setup together with the Request Sleep command, and woken with a rising signal edge applied to the VREF/WS pin.

If the sleep feature is enabled using SDC (see Section 5.7.3 on page 45), and the Request Sleep command has been issued (Section 4.13 on page 35), the QT2640 sleeps whenever possible to conserve power. Periodically, it should be woken by the host using the VREF/WS pin. Upon being woken, the matrix is scanned and the QT2640 returns to sleep unless there is activity which demands further attention. The QT2640 returns to sleep automatically after a period of inactivity, the duration of which is defined by the AWAKE feature (see Section 5.12 on page 48).

At least one full matrix scan is always performed after waking up and before returning to sleep. At the end of each matrix scan, the part returns to sleep unless recent activity, such as a touch event, demands further attention. If there has been recent activity, the part performs another complete matrix scan before attempting to sleep once again. This process is repeated indefinitely until the activity stops and the part returns to sleep, or the Request Sleep command is revoked; The Request Sleep command is revoked upon receipt of the first byte of an SPI communications sequence.

Key touch activity forces the matrix scanning into free run whereby each matrix scan is not interleaved with sleep. The QT2640 will not sleep if any of the following conditions are present:

- SDC = 0
- The Request Sleep command has not been issued, or has been revoked
- The timer configured with AWAKE is running
- $\overline{\text{DRDY}}$ asserted (low level)
- $\overline{\text{SS}}$ low (assume host trying to send a command)
- A command is being processed or response data is being returned or pending return to the host
- Any key calibrating
- Any key in detect
- Any key touch delta exceeds the threshold (positive or negative)

Sleep should be used with caution if the QT2640 is being used in an FMEA or IEC/EN/UL60730 compliant design because all operations are stopped within the QT2640 while the part is asleep and the host might have difficulty distinguishing between the IEC/EN/UL60730 counters appearing to run slow because the part is intermittently sleeping, and faulty operation. However, in the knowledge it has configured the QT2640 for sleep, the host can take this into account. For example, the host could wake the QT2640 at suitable intervals, check for correct operation and then return the QT2640 to sleep.

2.16 FMEA Tests

Failure Modes and Effects Analysis (FMEA) is a tool used to determine critical failure problems in control systems. FMEA analysis is being applied increasingly to a wide variety of applications including domestic appliances. To survive FMEA testing the control board must survive any single problem in a way that the overall product can either continue to operate in a safe way, or shut down.

The most common FMEA requirements regard opens and shorts analysis of adjacent pins on components and connectors. However, other criteria must usually be taken into account, for example complete QT2640 failure.

The QT2640 incorporates a number of special self-test features which allow products to pass such FMEA tests easily, and enable key failure to be detected. These tests are performed in an extra burst slot after the last enabled key.

The sequence of tests are performed repeatedly during normal running once all initialization is complete. During initialization, all FMEA error flags are cleared. Any FMEA errors are reported as the tests are performed for the first time.

The FMEA testing is done on all enabled keys in the matrix, and results are reported via the serial interface. Disabled keys are not tested.

Assuming the part does not sleep, the interval from the start of one set of FMEA tests to the start of the next set, never exceeds 2 s.

Also, since the QT2640 only communicates in slave mode, the host can determine immediately if the QT2640 has suffered a catastrophic failure.

The FMEA tests performed are:

- X drive line shorts to Vdd and Vss
- X drive line shorts to other pins
- X drive signal deviation
- Y line shorts to Vdd and Vss
- Y line shorts to other pins
- X to Y line shorts
- Cs capacitor checks including shorts and opens
- Vref test
- Key gain (see Section 5.10.1 on page 47)

Other tests incorporated into the QT2640 include:

- A test for signal levels against a preset minimum value (Lower Signal Limit (LSL) setup, see Section 5.9 on page 46). If any signal level falls below this level, an error flag is generated.
- 16-bit CRC communications checks on all data returns.

2.17 IEC/EN/UL60730 Compliance

The QT2640 also incorporates special test features which, together with the FMEA tests, allow products to achieve IEC/EN/UL60730 compliance with ease. IEC/EN/UL60730 compliance demands dynamic verification of all safety related components and sub-components within a product. The QT2640 is able to verify some sub-components internally, but others require verification by a separate, independent processing unit with another timing source.

To this end the QT2640 exposes a number of internal operating parameters through its serial communications interface and requires the cooperation of a host to check and verify these parameters regularly. It is also necessary for the host to verify the communications by checking and validating the CRC, which the QT2640 appends to data returns. If a CRC check should fail, the host should not rely on the data but retry the transmission.

Occasional CRC failures might be anticipated as a result of noise spikes. Repeated CRC failures might indicate a safety-critical failure. Where the QT2640 is able to verify sub-components internally, but any such verification fails, the QT2640 disables serial communication and locks up in an infinite loop. The host can detect this condition if repeated CRC failures are observed.

During normal operation the host must perform regular reads of the IEC/EN/UL60730 counters (see Section 4.3 on page 31) to verify correct operation of the QT2640. The host must also perform regular reads of the QT2640 status (see Section 4.4 on page 32) and verify there are no errors reported. The FMEA error flag, LSL error flag and Host CRC error flag must all be considered as part of an IEC/EN/UL60730 compliant design.

The host can try to recover from any safety critical failure by resetting the QT2640 using its $\overline{\text{RST}}$ pin. The host should allow a grace period in consideration of the start-up and initialisation time the QT2640 requires after reset to ability to communicate (see Section 2.12 on page 13).

The sub-components that the QT2640 is able to verify internally are tested repeatedly during the normal running of the device, and the various tests run in parallel. As each test ends the result is recorded and the test is restarted. The real time that elapses from the start of each test to the start of the next iteration of the same test is called the failure detect time, or hazard time, the maximum time for which an error could be undetected.

Each test is broken down into a number of smaller parts, each of which is processed in turn during each matrix scan. Each test is therefore completed either after a number of matrix scans, as shown in Table 2-3.

Table 2-3. Test run times (measured in matrix scans)

Test	Required Matrix Scans to complete test
FMEA	8
Other	18
Variable Memory	2304
Firmware CRC	1984
Setups CRC	60

Table 2-4 shows matrix scan times for setups that yield the shortest matrix scan time and a much longer scan time resulting from the use of long dwell and low frequency settings.

Table 2-4. Matrix Scan Times

Setups Conditions	Matrix Scan Time (ms)

BL = 0 (16 pulses),
DWELL = 0 (0.13 µs),
FREQ0 = 1,
All keys enabled,
FHM = 0,
MSYNC = 0 (Off),
SDC = 0 (sleep disabled),
DEBUG = 0 (Off).
	8.5

BL = 3 (64 pulses),
DWELL = 13 (5.1 µs),
FREQ0 = 25,
All keys enabled,
FHM = 0,
MSYNC = 0 (Off),
SDC = 0 (sleep disabled),
DEBUG = 0 (Off).
	17

Longer matrix scan times are possible than those shown in Table 2-4 by using even longer dwell times and higher values for FREQ0 (lower burst frequencies), but these are considered extreme settings.

Table 2-5 shows the failure detect times for the internal tests assuming a matrix scan time of 9 ms, which is valid for typical setups.

Table 2-5. Failure Detect Time

Test	Failure Detect Time (ms)
FMEA	72
Other	162
Variable Memory	20,736
Firmware CRC	17,856
Setups CRC	540
Note: Conditions: Matrix scan time = 9ms. QT2640 does not sleep for duration of tests.	

Longer failure detect times are possible than those shown in Table 2-5 where the matrix scan time is longer. The failure detect times are proportional to the matrix scan time. The failure detect time for other setups can therefore be determined by observing the matrix scan time using an oscilloscope and scaling the times given in Table 2-5 accordingly. Alternatively, the failure detect times can be calculated by taking the numbers from Table 2-3 and multiplying them by the matrix scan time.

Unnecessarily long settings of dwell and low burst frequencies should be avoided because these will also result in undesirably long failure detect times.

2.17.1 UL approval / VDE compliance

The QT2640 has been given a compliance test report by VDE and is approved by UL as a component suitable for use in both class B and class C safety critical products. By using this device and following the safety critical information throughout this datasheet, manufacturers can easily add a touch sense interface to their product, and be confident it can also readily pass UL or VDE testing.

2.18 VREF/WS pin

The VREF/WS pin is shared for multiple purposes: **VREF** definition, a **W**ake-up signal, and a **Sync** signal. Its fundamental purpose is to provide the reference voltage at the internal VREF node for the analogue-to-digital conversion of each sample. Secondary uses are as an input for a noise synchronisation signal, and as an input for wake-up from sleep mode.

During the conversion of each sample to digital form, the VREF/WS pin is coupled to the internal VREF node, and must be maintained at a stable voltage near Vss. If the sync and sleep features are not in use, VREF/WS can be connected directly to Vss.

The sync and wake signals are able to share a single pin together with VREF through the use of time division multiplexing because the sync and wake signals are not needed while the device is performing a matrix scan.

When MSYNC is enabled, a sync pulse triggers one full matrix scan, with a delay necessary between the end of each matrix scan and the sync pulse to trigger the next one. During the matrix scan, the VREF/WS pin is used to define VREF. Once the matrix scan is complete, the pin is available for use as the noise sync input.

If the sleep feature is used (see SDC), the wake-up signal must occur when the device is sleeping and not while it is performing a matrix scan.

A simple external circuit is required when either MSYNC or sleep are enabled. This circuit, consisting of two transistors connected in open-drain mode, with their drains both connected to VREF/WS operates together with a dynamic internal pull-up at the VREF/WS pin. See the schematic of Figure 1-1 on page 6 for an example circuit arrangement. One transistor couples the sync signal or the wake-up signal to VREF/WS, and the other is used to define VREF during each analogue-to-digital conversion, with the open-drain arrangement allowing the VREF definition to temporarily override the sync or wake-up signal. Most transistors are suitable for this purpose, including low-cost MOSFETs such as 2N7002 and BSS138.

If either MSYNC is enabled or if sleep is used, an internal pull-up, with value between 20 kΩ and 50 kΩ, is applied to the VREF/WS pin whenever the QT2640 is waiting for a sync signal or is in sleep mode. At all other times the VREF/WS pin is internally maintained near Vss, although this is not sufficient alone to guarantee the stable VREF definition needed during each conversion.

Wake-up from sleep and the sync feature are both triggered by a rising edge at the VREF/WS pin.

2.19 X7/SMP pin

The SMP function shares a pin with the X7 matrix drive line. Pin X7/SMP drives both functions but at different times, so there is no conflict between them. It generates the burst for X7 and, quite independently, it generates the SMP digital conversion signal for all samples on all X lines, despite the fact it shares a pin with X7.

This pin must be connected to both the X7 matrix line and the digital sample ramp resistors Rs0 – Rs7 (See Figure 1-1 on page 6). It can never be left unconnected. Even if X7 is not used, the X7/SMP pin must still be connected to the Rs resistors.

2.20 Frequency Hopping

The QT2640 supports frequency hopping to avoid a clash between the sampling frequency and noise at specific frequencies elsewhere in products or product-operating environments. It tries to hop away from the noise.

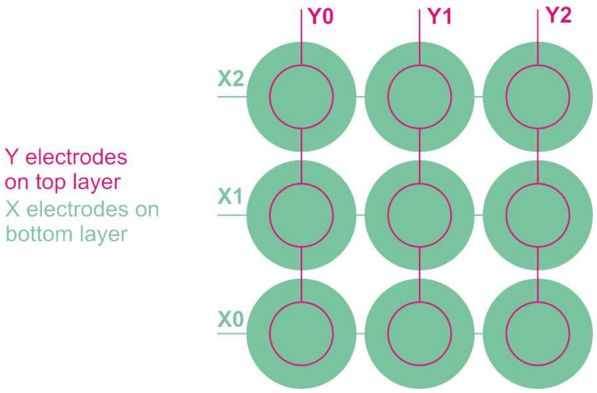
During the acquisition bursts, a sequence of pulses are emitted with a particular spacing, which equates to a particular sampling frequency. If the latter should coincide with significant noise generated elsewhere, touch sensing may be seriously impaired or false detections may occur.

To help combat such noise, the burst frequency can either be preset to one specific frequency (hopping disabled) away from the noisy frequency, or frequency hopping can be enabled and set to switch dynamically between three specific configured frequencies or even set to sweep a configured range of frequencies.

2.21 Key Design

Figure 2-7 shows part of a keypad laid out with a regular matrix of 3 x 3 keys using electrode patterns based on a flooded-X design.

Figure 2-7. Key Example Electrode Patterns



Flooded-X designs are one of the easiest to implement, produce excellent results with many overlay panels and can be considered first for all new QT2640 designs where a 2-layer PCB is intended for the touch interface.

For more information about the electrode design for sliders and wheels refer to the design guide listed in Appendix C. on page 69.

2.22 Sliders/Wheels

The QT2640 supports up to eight sliders and wheels in any combination, each constructed from a group of between two and eight consecutively numbered keys on the same Y line. A slider is an array of keys laid out to form a one dimensional track along the length of which a single touch position is reported with 8-bit resolution. A wheel, whilst also reporting a single touch with 8-bit resolution, is laid out as equal pieces of a pie to form a circle or wheel, typically with an insensitive void at the hub.

Keys that are used to form a slider/wheel cannot also be used as individual keys. The standard key processing must be disabled, by setting SLD, when the key is used in the construction of a slider or wheel.

At a minimum, setups SLD, SSN and SLEN must be configured to indicate which keys are used in sliders/wheels, where each slider/wheel starts in the logical key matrix, and how many keys have been used to construct each. In addition, SW is used to declare the type as either slider or wheel, position hysteresis can be programmed using SPH, a filter can be enabled with SF, and SRS can be used to adapt the reported position to fit the 8-bit full scale deflection.

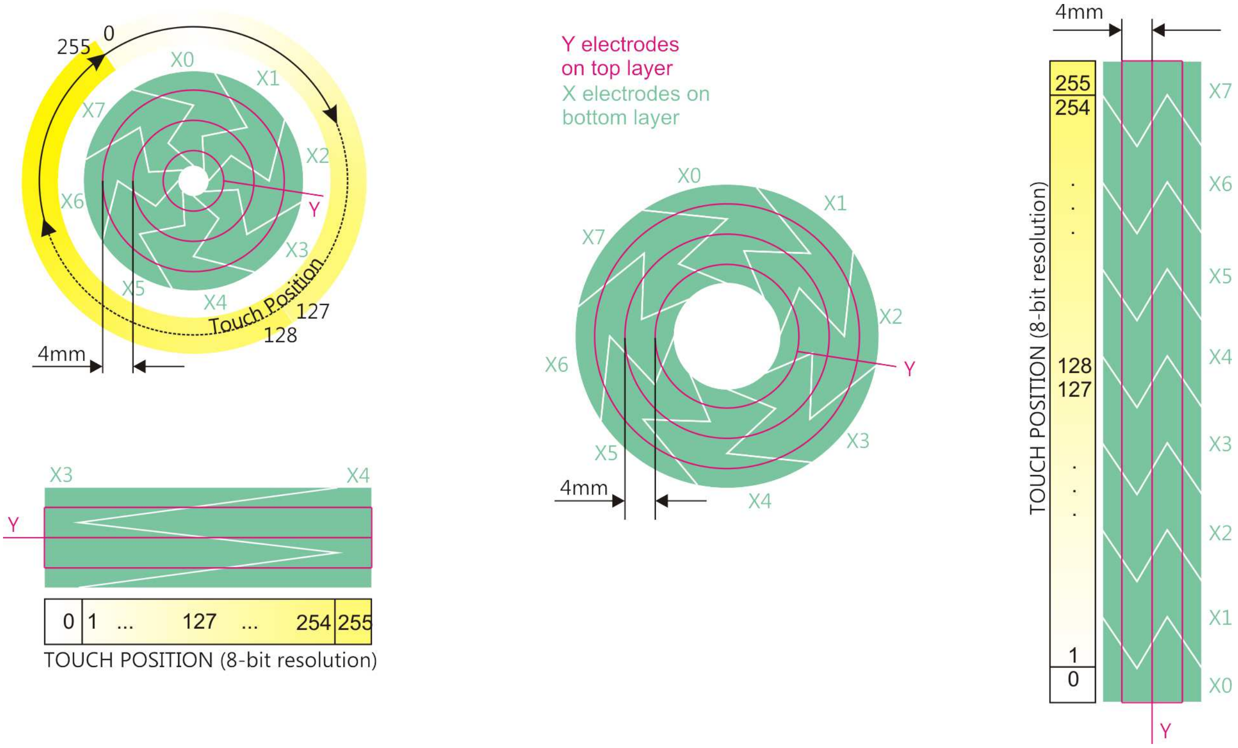
The group of keys used to form a slider/wheel may start almost anywhere within the logical matrix of keys provided the entire group is located on the same Y line. A group is not allowed to span across Y lines. For example, a slider formed from two keys can start at any X line from X0 to X6, but cannot start at X7, the last key on the Y line, whereas one formed from eight keys can only start at X0. All other keys on the same Y line as a slider/wheel but not used in the slider/wheel behave as normal. A single Y line can be used for more than one slider/wheel; Up to four sliders/wheels can be constructed on the same Y line.

The slider is physically constructed using a group of keys placed adjacent to each other. A minimum group size of two keys and a maximum group size of eight keys may be used, but the group must be laid out sequentially in numerical key order.

A slider can be constructed very simply by placing standard key patterns adjacent to each other, but other designs, for example ones based on flooded-X, can deliver better results. Short sliders can be constructed from just two keys, while better resolution will be achieved in longer sliders using a greater number of keys.

Figure 2-8 on page 21 shows some example slider and wheel electrode patterns based on flooded-X design. Two sliders are shown, a horizontal one based on just two keys, and a vertical one based on eight keys. The 2-key based horizontal slider uses keys from X3 and X4 arbitrarily as an example only.

Figure 2-8. Slider & Wheel Example Electrode Patterns



Flooded-X designs are one of the easiest to implement, for sliders and wheels as well as keys, produce excellent results with many overlay panels and can be considered first for all new QT2640 designs where a 2-layer PCB is intended for the touch interface.

For more information about the electrode design for sliders and wheels refer to the design guide listed in Appendix C. on page 69.

Setups NDIL, NTHR and NRD for a slider/wheel are all taken from the lowest numbered key in the slider group, but ignored at all other keys within the group. AKS is non-functional for sliders and must be disabled for all slider members. The fast detect integrator cannot be used within a slider and so FDIL must be set to 1 for all slider members.

3. Serial Communications

3.1 Introduction

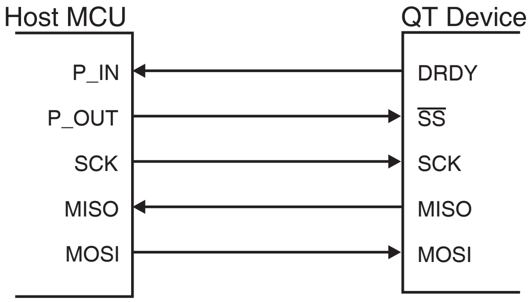
The QT2640 uses an SPI interface for communications with a host. The QT2640 always operates as a slave and must be driven from the host acting as SPI master.

The device also includes a Debug output interface, which can be used to monitor many operating variables during product development.

3.2 SPI Interface

The SPI host device always initiates communications sequences. This is intentional for FMEA and IEC/EN/UL60730 purposes so that the host always has total control over the communications with the QT2640. Even return data is controlled by the host. The QT2640 employs a CRC on return data to provide for robust communications.

Figure 3-1. Communications Signals – SPI



There is an essential $\overline{\text{DRDY}}$ line that handshakes transmissions. This is needed by the host from the QT2640 to ensure that transmissions are not sent when the QT2640 is busy or has not yet processed a prior transfer. If the host does not observe the correct $\overline{\text{DRDY}}$ timing, random communication errors may result.

Initiating or Resetting Communications: After a reset, or should communications be lost due to noise or out-of-sequence reception, the host should repeatedly wait for a period not less than the QT2640 communications time-out (20 ms ±5 ms). The host should then read location 0, followed by the CRC bytes, until the correct response is received back from location 0 and validated by the CRC. Location 0 should read as `1A` hex (26 decimal). The host can then resume normal run mode communications from a clean start.

Poll Rate: The typical poll rate in normal run operation should be no faster than once per 10 ms; 25 ms is more than fast enough to extract status data.

SPI communications operate only in slave mode, and obey $\overline{\text{DRDY}}$ control signaling. The clocking is as follows:

Clock idle:	High
Clock shift out edge:	Falling
Clock data in edge:	Rising
Max clock rate:	4 MHz

SPI requires five signals to operate:

MOSI: Master-out / Slave-in data pin, used as an input for data from the host (master). This pin should be connected to the MOSI (DO) pin of the host device.

MISO: Master-in / Slave-out data pin, used as an output for data to the host. This pin should be connected to the MISO (DI) pin of the host. MISO floats in three-state mode between bytes when $\overline{\text{SS}}$ is high, to facilitate multiple devices on one SPI bus.

SCK: SPI clock, input only clock from host. The host must shift out data on the falling SCK edge and the QT2640 clocks data in on the rising edge. The QT2640 likewise shifts data out on the falling edge of SCK back to the host so that the host can shift the data in on the rising edge.

Note: SCK must idle high; it should never float.

$\overline{\text{SS}}$: Slave select, input only. Acts as a framing signal to the sensor from the host. $\overline{\text{SS}}$ must be low before and during each byte transfer with the host. It must not go high again until the SCK line has returned high; $\overline{\text{SS}}$ must idle high. This pin includes an internal pull-up resistor of 20 kΩ – 50 kΩ. When $\overline{\text{SS}}$ is high, MISO floats.

$\overline{\text{DRDY}}$: Data Ready, active-high, indicates to the host that the QT2640 is ready to send or receive data. This pin idles high and is an open-drain output with an internal 20 kΩ – 50 kΩ pull-up resistor. Most communications failures are the result of failure to properly observe the $\overline{\text{DRDY}}$ timing.

Serial communications pacing is controlled by $\overline{\text{DRDY}}$. Use of $\overline{\text{DRDY}}$ is critical to successful communications with the QT2640. The host is permitted to perform an SPI transfer only when $\overline{\text{DRDY}}$ has returned high. After each SPI byte transfer $\overline{\text{DRDY}}$ goes low after a short delay and remains low until the QT2640 is ready for another transfer. A short delay occurs before $\overline{\text{DRDY}}$ is driven low because the QT2640 may be otherwise busy and requires a finite time to respond. $\overline{\text{DRDY}}$ may go low only for a few microseconds. During the period from the end of one transfer until $\overline{\text{DRDY}}$ goes low and back high again, the host should not perform another transfer. Therefore, before each byte transmission, including the first byte of each sequence, the host should first check that $\overline{\text{DRDY}}$ is high again.

If the host wants to perform a byte transfer with the QT2640 it should behave as follows:

1. Wait at least 100 µs after the previous SPI transfer (time S5 in Figure 3-2 on page 24: $\overline{\text{DRDY}}$ is guaranteed to go low before this 100 µs expires).
2. Wait until $\overline{\text{DRDY}}$ is high (it may already be high again).
3. Perform the next SPI transfer with the QT2640.

The time it takes for $\overline{\text{DRDY}}$ to go high again after each transfer depends if the host is performing

A setups write, or is performing a read, as follows:

Setups write: ≤ 20 ms

Read: ≤ 1 ms

The $\overline{\text{DRDY}}$ times above are valid when the maximum operating frequency (FREQ0 = 1) is used. These times increase as the operating frequency is reduced. With very low operating frequency add 5 ms to the above times. With the Debug interface enabled, add 11ms to the above times.

Other $\overline{\text{DRDY}}$ specifications:

Min time $\overline{\text{DRDY}}$ is low: 1 µs

Min time $\overline{\text{DRDY}}$ is low after reset: 80 ms

Null Bytes: When the QT2640 responds with data requested in a read operation, the host should issue null bytes (0x00) in order to recover the response bytes back. The host should not start a new communications sequence until all the response and CRC bytes are accepted back from the QT2640.

Timeout: A successful communications sequence consists of a number of byte transfers. The QT2640 expects each byte transfer within a sequence to occur within 20 ms (± 5 ms) of the previous transfer. If more than 20 ms elapses between any two bytes, the QT2640 abandons the current sequence and starts a new sequence at the next byte transfer.

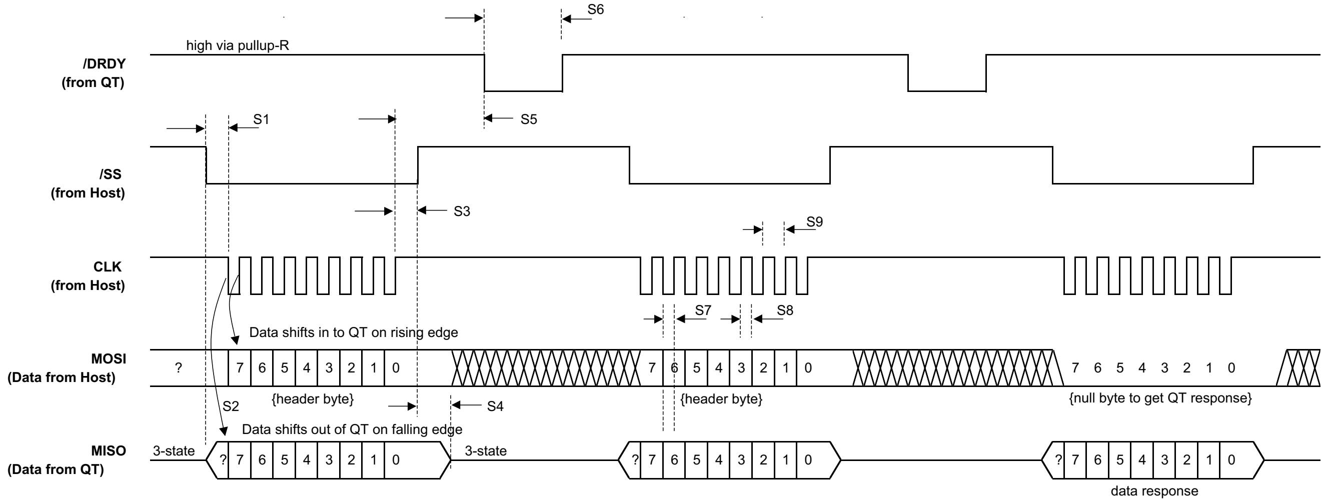
Wake-up: The QT2640 can be configured to automatically sleep, but the host must awaken the QT2640, when required, with a rising signal edge at the VREF/WS pin, which should be accomplished through a simple transistor as described in Section 2.18 on page 18.

With the $\overline{\text{SS}}$ line used to drive this transistor, the host can simply pulse $\overline{\text{SS}}$ to wake the QT2640. The host should not send an actual SPI byte to prevent the QT2640 from seeing a byte it cannot properly interpret due to timing errors during wake-up. There is an interval of approximately 1.5 ms from the pulse on VREF/WS before the QT2640 is able to resume processing. Transmissions to the QT2640 within this interval are discarded.

SPI Line Noise: In some designs it is necessary to run SPI lines over ribbon cable across a lengthy distance on a PCB. This can introduce ringing, ground bounce, and other noise problems which can introduce false SPI clocking or false data. Simple RC networks and slower data rates are helpful to resolve these issues.

A CRC check appends all data responses in order to detect transmission errors to a high level of certainty.

Figure 3-2. SPI Slave Mode Timing



S1 > 125 ns	S2 < 20 ns	S3 > 25 ns	S4 < 20 ns	
S5 < 100 µs	S6 > 1 µs	S7 >125 ns	S8 > 125 ns	S9 > 250 ns
Note: See “Timing Specifications” on page 60 for more detailed definitions.				

3.3 Writing Data to the Device

The sequence of events required to write data to the device is shown below:

Byte	1		2		3		4	
MOSI	Mem.Addr.bits 7..0	D	bit 7: 0 = write bit 6: n, bit 8 bits 5..3: undefined bits 2..0: Mem.Addr.bits 10..8	D	n. bits 7..0	D	Data	D
MISO	U		U		U		U	

Table 3-1. Key to Write Sequence

Byte #	Symbol	Description
1, 2	Mem.Addr.	Target memory address within QT2640. This is an 11-bit address formed with bits from both Byte 1 and Byte 2. The 3 most significant bits are from Byte 2, bits 10..8, and the 8 least significant bits are from Byte 1.
	U	Undefined data byte, should be ignored.
	D	Delay 100 µs then wait until $\overline{\text{DRDY}}$ high.
2	write	Set bit 7 to zero, indicating write operation to the QT2640.
2, 3	n	# bytes to write, a 9-bit value with the most significant bit located in Byte 2, bit 6.
4+	Data	Data byte(s) to write to QT2640.

The host initiates a write sequence by sending a sequence of three header bytes followed by n data bytes. The three header bytes define the internal memory address to be written to, the flag to indicate a write operation (0), and n, the number of QT2640 addresses to be written. See Table 3-1. After n data bytes have been written, the QT2640 automatically terminates the write operation and will start a new SPI sequence with the next byte transfer.

Between each byte transfer, the host must follow the $\overline{\text{DRDY}}$ handshake procedure (wait 100 µs and then wait until $\overline{\text{DRDY}}$ is high). If the host sends more than one data byte, they are written to consecutive memory addresses, the device automatically increments the target memory address after writing each data byte.

The host should not try to write beyond the last setups address.

The raw SPI protocol defines simultaneous bidirectional byte transfers. For each byte sent from the host, another byte is received back from the slave. During a write sequence, the bytes returned by the QT2640 are undefined and should be ignored.

3.4 Reading Data From the Device

The sequence of events required to read data from the device is shown below:

Byte	1		2		
MOSI	Mem.Addr.bits 7..0	D	bit 7: 1 = read bit 6: n, bit 8 bits 5..3: undefined bits 2..0: Mem.Addr.bits 10..8	D	…
MISO	U		U		

	3		4										
…	n. bits 7..0	D	NULL	D	NULL	D	…	NULL	D	NULL	D	NULL	D
	U		Data 1		Data 2		…	Data n		CRC LSB		CRC MSB	