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Features

- **USB 2.0 Full Speed Host/Function Processor**
 - Real-time Host/Function Switching Capability
 - Internal USB and System Interface Controllers
 - 32-bit Generic System Processor Interface with DMA
 - Separate TX and RX Buffers for Host and Function Operations
 - In-System Firmware Upgrade
- **Autonomous USB Host Operation without System Processor Intervention**
 - Device Enumeration
 - USB Protocol Management
 - Bus Bandwidth Reclamation
 - Status Handling
 - Control, Bulk, Interrupt and Isochronous Transfers
 - Supports Up to 7 USB Devices Concurrently
- **Full-speed Function Controller**
 - 1 Bi-directional Control Endpoint
 - 6 Programmable (Maximum Packet Size and Endpoint Type) Endpoints
 - Control, Interrupt, Bulk and Isochronous Transfer Support
 - Automatic Retry for Non-Isochronous Endpoints
- **Integrated USB Firmware**
 - Easy-to-use, ANSI C Compliant API USB Device Driver Development
 - Embedded, OS Agnostic USB Host Stack
 - Embedded System Interface Controller Driver
 - Embedded USB Hub Driver
- 6 MHz Operation
- 1.8 V and 3.3 V Operation
- 100-pin LQFP Package

Description

Atmel's AT43USB370 is a USB 2.0 compliant, dual-role, full-speed Host/Function processor designed specifically to enable point-to-point USB connectivity for embedded devices. It features an integrated USB host stack, a system interface driver, on-chip USB signaling hardware, 32-bit generic system processor interface with DMA support, and on-the-fly host/function switching capability.

The on-chip USB hardware features a USB transceiver, a serial interface engine (SIE), a SIE controller, and an SOF generation block. It supports the physical and data link layer of the USB protocol whereas the USB transaction layer is implemented in firmware.

In host mode, the integrated USB firmware consists of the Host USB Controller Driver (HUSBCD) running on the USB Controller (USBC) and the Host System Interface Controller Driver (HSICD) resident on the System Interface Controller (SIC). The HUSBCD provides complete USB protocol management including device enumeration, transaction management, scheduling and frame management, and bus reclamation. The HSICD serves as an interface between the HUSBCD and applications resident on the external system processor. It handles all of the high-level data flow management during a USB transaction. Together, the HUSBCD and the HSICD deliver complete USB host operations autonomously, without the intervention of the system processor.



USB 2.0 Full-Speed Host/Function Processor

AT43USB370

Rev. 3340B-USB-12/03



The AT43USB370 communicates with the external system processor through its generic 32-bit host processor interface. This system interface contains 2 Kbytes of FIFO and a DMA engine designed to ensure maximum bus utilization. The automatic USB retry mechanism minimizes data traffic across the system interface.

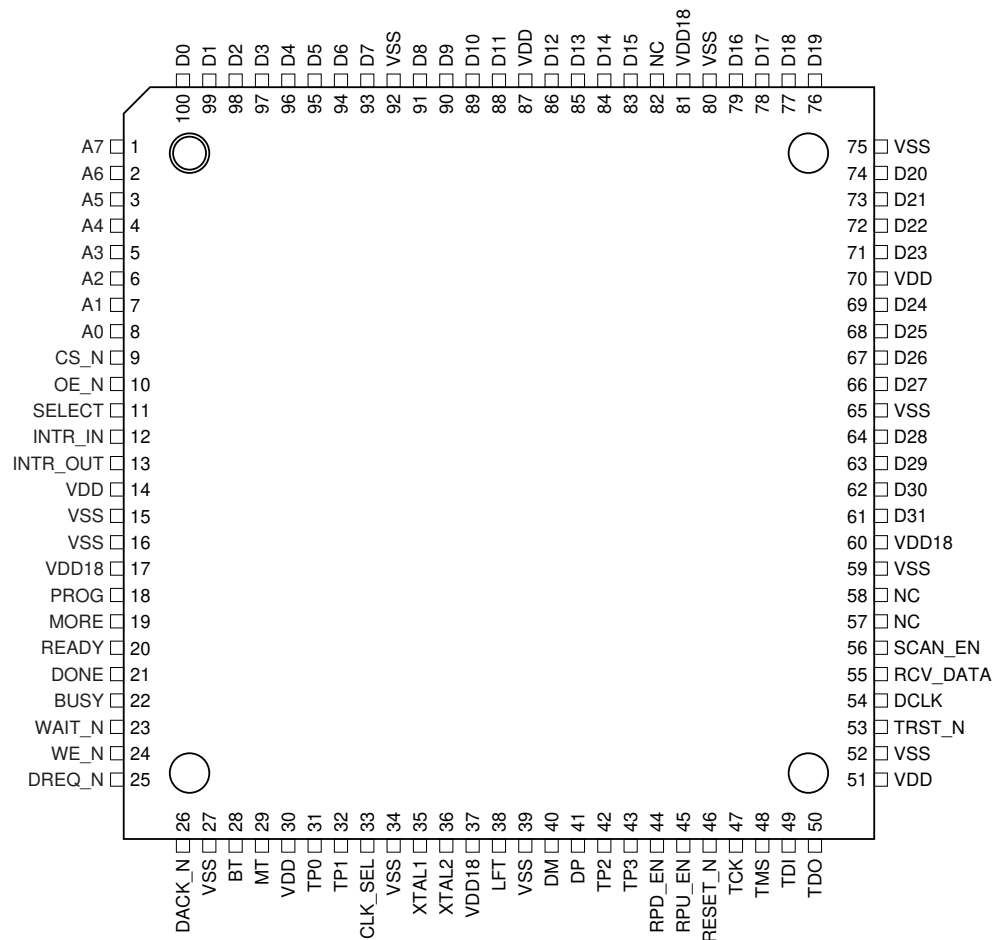
As a function, the AT43USB370 operates in full-speed mode. It supports one control endpoint and a maximum of six programmable (maximum packet size and endpoint type) endpoints. The internal USB controller runs the function firmware that manages USB enumeration and data flow control without system processor intervention.

Communication between the AT43USB370 firmware and applications resident in the system processor is realized through a small set of ANSI C compliant, system interface Application Protocol Interfaces (APIs). This API set encapsulates the complete USB functionality. It is used as the basic building blocks for constructing application specific USB device drivers of any type.

The AT43USB370, with its highly integrated USB hardware/firmware architecture, not only hides the complexity of the traditional USB design, but also frees system resources from being burdened by timing critical USB activities. It is an ideal solution for point-to-point USB connectivity in the resource constrained embedded environment.

Pin Configuration

Figure 1. AT43USB370 100-lead LQFP



Pin Assignment

Pin #	Signal	Type	Pin #	Signal	Type	Pin #	Signal	Type
1	A7	Input	35	XTAL1	Input	69	D24	Bi-directional
2	A6	Input	36	XTAL2	Output	70	VDD	Power Supply/Gnd
3	A5	Input	37	VDD18	Power Supply/Gnd	71	D23	Bi-directional
4	A4	Input	38	LFT	Input	72	D22	Bi-directional
5	A3	Input	39	VSS	Power Supply/Gnd	73	D21	Bi-directional
6	A2	Input	40	DM	Bi-directional	74	D20	Bi-directional
7	A1	Input	41	DP	Bi-directional	75	VSS	Power Supply/Gnd
8	A0	Input	42	TP2	Input	76	D19	Bi-directional
9	CS_N	Input	43	TP3	Input	77	D18	Bi-directional
10	OE_N	Input	44	RPD_EN	Output	78	D17	Bi-directional
11	SELECT	Input	45	RPU_EN	Output	79	D16	Bi-directional
12	INTR_IN	Input	46	RESET_N	Input	80	VSS	Power Supply/Gnd
13	INTR_OUT	Output	47	TCK	Input	81	VDD18	Power Supply/Gnd
14	VDD	Power Supply/Gnd	48	TMS	Input	82	NC	Not Connected
15	VSS	Power Supply/Gnd	49	TDI	Input	83	D15	Bi-directional
16	VSS	Power Supply/Gnd	50	TDO	Output	84	D14	Bi-directional
17	VDD18	Power Supply/Gnd	51	VDD	Power Supply/Gnd	85	D13	Bi-directional
18	PROG	Input	52	VSS	Power Supply/Gnd	86	D12	Bi-directional
19	MORE	Input	53	TRST_N	Input	87	VDD	Power Supply/Gnd
20	READY	Output	54	DCLK	Output	88	D11	Bi-directional
21	DONE	Input	55	RCV_DATA	Output	89	D10	Bi-directional
22	BUSY	Output	56	SCAN_EN	Input	90	D9	Bi-directional
23	WAIT_N	Output	57	NC	Not Connected	91	D8	Bi-directional
24	WE_N	Input	58	NC	Not Connected	92	VSS	Power Supply/Gnd
25	DREQ_N	Output	59	VSS	Power Supply/Gnd	93	D7	Bi-directional
26	DACK_N	Input	60	VDD18	Power Supply/Gnd	94	D6	Bi-directional
27	VSS	Power Supply/Gnd	61	D31	Bi-directional	95	D5	Bi-directional
28	BT	Input	62	D30	Bi-directional	96	D4	Bi-directional
29	MT	Input	63	D29	Bi-directional	97	D3	Bi-directional
30	VDD	Power Supply/Gnd	64	D28	Bi-directional	98	D2	Bi-directional
31	TP0	Input	65	VSS	Power Supply/Gnd	99	D1	Bi-directional
32	TP1	Output	66	D27	Bi-directional	100	D0	Bi-directional
33	CLK_SEL	Input	67	D26	Bi-directional			
34	VSS	Power Supply/Gnd	68	D25	Bi-directional			



Pin Description

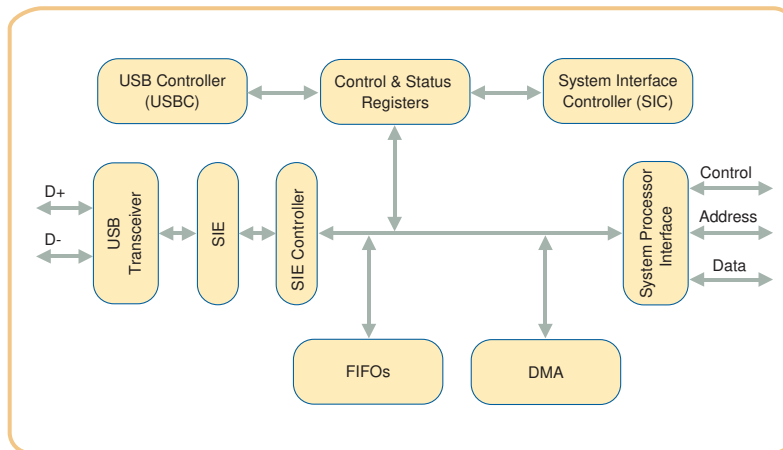
Pin Name	Type	Description
A[7:0]	Input	ADDRESS BUS – System Address Bus
CS_N	Input	CHIP_SELECT – from System Processor. Active Low
OE_N	Input	OUTPUT_ENABLE – from System Processor. Active Low
SELECT	Input	PROCESSOR_SELECT – from System Processor – used to select between the USB Controller (USBC) and System Interface Controller (SIC) when firmware is downloaded to these controllers through the System Processor. Logic “1” selects SIC and Logic “0” selects USBC.
INTR_IN	Input	Interrupt to AT43USB370 – from System Processor. Active High
INTR_OUT	Output	Interrupt from AT43USB370 – to System Processor. Active High
VDD	Power Supply/Gnd	3.3V Power Supply
VSS	Power Supply/Gnd	Ground
VDD18	Power Supply/Gnd	1.8V Power Supply
PROG	Input	PROGRAM_LOAD_ENABLE – from System Processor – used when the program is downloaded in the USB Controller and System Interface Controller through the System Processor. Active High
MORE	Input	PIO Mode Handshake Signal – from System Processor. Active High
READY	Output	READY – to System Processor – used when the program is downloaded in the USB Controller and System Interface Controller through the System Processor. Active High
DONE	Input	DONE – from System Processor – used when the program is downloaded in the USB Controller and System Interface Controller through the System Processor. Active High
BUSY	Output	BUSY – to System Processor – used when the System Interface Controller is busy in an interrupt service routine and does not want the System Processor to issue an interrupt. Active High
WAIT_N	Output	WAIT – to System Processor. Active Low
WE_N	Input	WRITE_ENABLE – from System Processor. Active Low
DREQ_N	Output	DMA Request – to System Processor – used to signal to the System Processor that the AT43USB370 wants to start a DMA transfer. Active Low
DACK_N	Input	DMA Acknowledge – from System Processor. Active Low
BT	Input	BIST – Test Signal
MT	Input	Memory – Test Signal
TP0	Input	Test Pin 0
TP1	Output	Test Pin 1
TP2	Input	Test Pin 2
TP3	Input	Test Pin 3
CLK_SEL	Input	External/PLL Clock Selection – Low selects crystal-PLL clock source while a High uses XTAL1, bypassing the PLL.
XTAL1	Input	Oscillator Input – Input to the inverting oscillator amplifier.
XTAL2	Output	Oscillator Output – Output of the inverting oscillator amplifier.
LFT	Input	PLL Loop Filter – For proper operation of the PLL, this pin should be connected through a 2.2 nF capacitor in parallel with a 470 Ω resistor in series with a 22 nF capacitor to ground (VSS). Both capacitors must be high quality ceramic.

Pin Description (Continued)

Pin Name	Type	Description
DP	Bi-directional	D+ (USB Line)
DM	Bi-directional	D- (USB Line)
RPD_EN	Output	Pull Down Enable
RPU_EN	Output	Pull Up Enable
RESET_N	Input	RESET – Active Low
TCK	Input	JTAG Clock
TMS	Input	JTAG Mode Select
TDI	Input	JTAG Serial Data IN
TDO	Output	JTAG Serial Data OUT
TRST_N	Input	JTAG Reset – Active Low
DCLK	Output	Recovered SIE DPLL Clock
RCV_DATA	Output	Recovered Serial Data
SCAN_EN	Input	Scan Test Enable
NC	–	Not Connected
D[31:0]	Bi-directional	System Data Bus

Block Diagram

Figure 2. AT43USB370 Hardware





Architectural Overview

The AT43USB370 host/function processor is available in the SRAM version. It utilizes two on-chip microcontrollers, the USB controller (USBC) and the System Interface Controller (SIC) to off-load USB related processing from the system processor. On power-up or reset, the system processor downloads the appropriate firmware into the USBC and SIC via the system bus interface.

Functionally, the USBC manages the low-level USB protocol such as enumeration, frame management and transaction scheduling, in addition to handling USB hub driver. The SIC provides data flow management to and from the system processor. It is responsible for constructing USB packets of appropriate sizes, handling retries, channeling data to and from FIFOs, and providing API support to the external system processor.

The USBC and the SIC share the same set of on-chip Control and Status Registers with the System Processor Interface. The system interface logic makes use of this register set to facilitate data exchange between the AT43USB370 and the system processor. In a typical design scenario, the AT43USB370 appears as a memory mapped peripheral to the system processor. Externally accessible registers are shown in Table 1 on page 11. The read and write accesses to the system interface registers by the system processor are made through external memory operations on the system bus.

The system processor connects to the AT43USB370 through the generic 32-bit system processor interface. The system interface signals consist of an address bus, a data bus, a chip select, a read enable and write enable. The on-chip DMA engine provides maximum data throughput between the system processor and the on-chip USB FIFO blocks. The system processor communicates with the DMA engine through standard DMA signaling.

The embedded USB hardware consists of a USB Transceiver, a Serial Interface Engine (SIE), a SIE Controller, an SOF (Start of Frame) Generation and a FIFO block. The FIFO block is divided into a 128-bytes control endpoint and 2 Kbytes of memory block dynamically configurable to support different data endpoint requirements.

The AT43USB370 can be configured to operate either in host mode or function mode. The mode of operation is determined by writing corresponding values to the specified registers and downloading the corresponding USBC and SIC firmware to the AT43USB370. The AT43USB370 commences its operation once it is configured.

The AT43USB370 requires an external 6-MHz crystal to provide a reference clock frequency for the on-chip PLL. The PLL provides all of internal clock sources required for the AT43USB370.

Please note that the AT43USB370 signals use level detection, not edge detection.

Functional Description

USB Transceiver

A Universal Serial Bus Revision 2.0 compliant transceiver is embedded in the AT43USB370. The transceiver provides the physical layer signaling and is capable of transmitting and receiving serial data at 12 Mbps and 1.5 Mbps. The driver portion of the transceiver is differential while the receiver section is comprised of a differential and two single-ended receivers. Internally, the transceiver interfaces to the Serial Interface Engine. Externally, the transceiver interfaces directly with the USB connectors and cables through external termination resistors.

Serial Interface Engine (SIE)

The SIE is implemented entirely in hardware. It performs the following functions:

- Clock and Data Recovery from incoming USB data stream
- Serial/parallel conversion
- NRZI encoding/decoding
- CRC calculation (generation and checking)
- Generating full-speed and low-speed USB physical layer signaling
- Device connection/disconnection detection
- Token generation (IN, OUT, SOF, SETUP etc.)
- Keep Alive signal for low-speed devices
- Bit stuffing and unstuffing

SIE Controller

This block serves as the interfaces between the SIE and the USBC. It decodes the commands received from the USBC and updates the status after the end of a USB transaction. This block also controls the FIFOs for data and control packets and provides the USB Controller access to these FIFOs for internal data management such as automatic retries for failed transactions.

USB Controller

This internal microcontroller is dedicated to managing the USB Protocol in both the host mode and the function mode. The Control and Status registers of the AT43USB370 are mapped into its data memory for fast and easy access. The firmware running on this controller determines its operating mode, either host or function.

System Interface Controller

This internal microcontroller serves as an interface between the USB Controller and the external system processor. Firmware running on this controller manages the data flow to and from the system processor. It also provides a generic USB device driver interface to system applications.

FIFO

The FIFO block contains one data FIFO block and one control FIFO block. The control FIFO has a 128 bytes of memory which is divided into one TX and one RX control FIFO. AT43USB370 uses this FIFO for the bi-directional control endpoint.

The data FIFO has 2 Kbytes of memory. The FIFO control logic allows for dynamic configuration of the data FIFO. In host mode, the FIFO memory is divided into 1 Kbytes of TX transfer and 1 Kbytes of RX transfer. The HUSB CD uses this memory for storing data packets. In the event of an error during a USB transaction, the SIE controller is informed of the error and the transaction is retried.

In function mode, the FIFO is divided into two 1 Kbytes blocks, one for the IN endpoints and one for the OUT endpoints. Each of the 1 Kbytes endpoint block can then be dynamically configured during runtime to support up to 3 endpoint in the same direction, but of varying maximum packet sizes.

Control and Status Registers

This block is used to configure the AT43USB370 at the start of operation. The USBC and the SIC share this register set with the system processor interface logic.

By default this block is pre-configured for Host operation with the DMA enabled for the 32-bit data bus. In function mode, this block is used to define the number and nature of the endpoints for the function. A maximum of 3 IN and 3 OUT endpoints can be specified aside from the bi-directional control endpoint. Endpoint type and, maximum packet size and other parameters are also defined using this block.

A subset of the Control and Status register set, the System Processor Interface registers, is accessible by the system processor as external memory locations. It is used to facilitate data exchange between the system processor and the AT43USB370.

System Processor Interface

The system processor interface provides 32-bit bi-directional data paths to the external processor for read and write operations to the AT43USB370's System Interface registers and FIFO. The AT43USB370 appears as a memory mapped peripheral to the external system processor. The interface logic requires a number of control lines and an 8-bit address bus.

DMA

The DMA engine provides DMA support for the system processor to transfer data between the processor's memory and the AT43USB370's internal FIFO. The system processor's DMA controller controls the DMA operation through standard DMA Request and Acknowledgement signals. The AT43USB370 can only operate as a DMA slave.

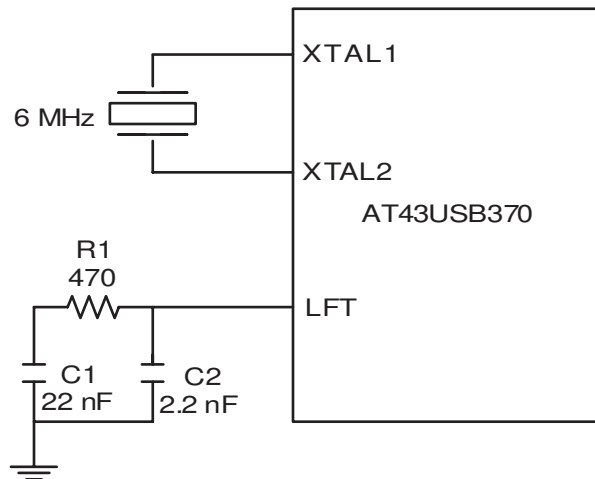
Oscillator and PLL

XTAL1 and XTAL2 are the clock pins to the AT43USB370. An external oscillator or a crystal can be connected to these pins. All clock signals required to operate the AT43USB370 are derived from the on-chip PLL. The on-chip PLL is of a special, low-drive type, designed to operate with most of the 6-MHz crystals without any external components. The crystal must be of the parallel resonance type requiring a load capacitance of about 10 pF. If the crystal requires a higher value capacitance, external capacitors can be added to the two terminals of the crystal and ground to meet the required value. To assure a quick start-up, a crystal with a high Q, or low ESR, should be used.

The 48-MHz clock can also be externally sourced. In this case, the clock source is connected to XTAL1 pin with XTAL2 pin left open and the CLK_SEL pin tied to logic "1".

For proper operation of the PLL, an external RC filter consisting of a series RC network of 470 Ω and 22 nF in parallel with a 2.2 nF capacitor must be connected from the LFT pin to V_{SS} . Only high-quality ceramic capacitors are recommended. Figure 3 shows the required crystal and external circuitry.

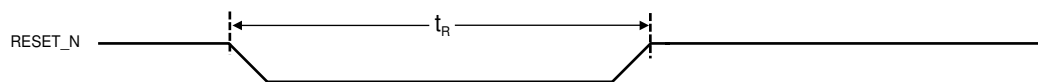
Figure 3. Oscillator and PLL



Reset

The reset signal to the AT43USB370 is active low. On reset, both the USBC and SIC are initialized and the System Processor Interface Registers are restored to their default values. Figure 4 shows the Reset timing diagram. For Reset timing, see Table 5 on page 47.

Figure 4. Reset Timing



Power Supply

The AT43USB370 requires an external supply of 3.3 V and 1.8 V.

Firmware Download Mechanism

The AT43USB370 provides an in-system programming of the USBC and the SIC through the external system processor. Programming requires SELECT, PROG, READY and DONE control signals. These control I/Os are dedicated to in-system firmware download and are not used during normal operation.

The firmware is downloaded in the program memories (SRAM) of the internal controllers after power-up or reset. The SELECT signal is used to select the USBC or the SIC for programming. The PROG signal is used to mark the start and end of firmware download. The READY and DONE signals are used for handshaking during successive programming write cycles.

The programming sequence of an internal controller is described as follows:

1. One of the controllers is selected using the SELECT pin of the AT43USB370. Logic low selects the USBC and logic high selects the SIC. The order of programming of the controllers is immaterial. Any of the controllers can be programmed first.
2. The PROG pin is asserted high by the system processor to indicate the start of programming.
3. The system processor writes to a dummy address (anywhere in the AT43USB370 addressable space of the memory mapping) to assert CS_N and WE_N to AT43USB370.
4. The system processor writes the 32-bit program word on the data bus.
5. The system processor waits for READY to be asserted high by the AT43USB370.
6. AT43USB370 asserts READY logic high to signal to the system processor that the 32-bit data word has been written to the program memory of the selected controller.
7. The system processor asserts the DONE signal high after detecting logic high on READY
8. AT43USB370 asserts READY logic low.
9. The system processor asserts logic low on DONE.
10. This completes one 32-bit write cycle of the controller's programming. Steps 2 to 8 repeated until the entire firmware is downloaded in the program memory of the selected controller.
11. Step 1 is then repeated to select the remaining controller. Step 2 to 9 are repeated to program the remaining controller.
12. The PROG is de-asserted by the system processor once the firmware download is complete. This signals an end of in-system programming of the AT43USB370.

The 32-bit word written by the system processor to its system bus must conform to the following format:

- Bits15:0: Address of the instruction

- Bits 31:16: The actual instruction itself

Both controllers reset internally and start executing the firmware when PROG is de-asserted. The AT43USB370 starts its operation as a USB host or USB function depending upon the firmware downloaded by the system processor.

Figure 5 and Figure 6 illustrate the programming waveform for the USBC and the SIC respectively.

Figure 5. Typical USB Controller's Programming Waveform

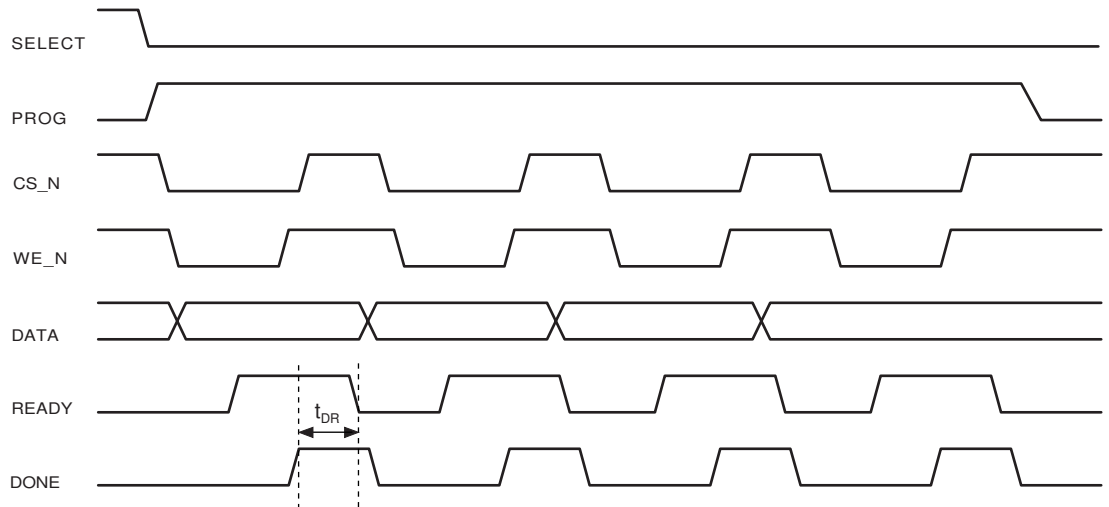
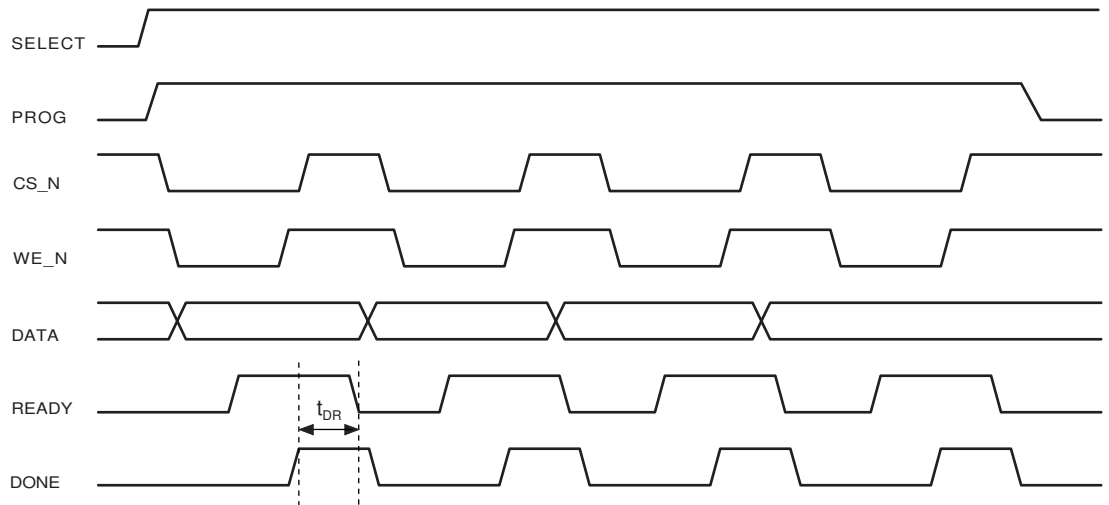


Figure 5 shows the programming waveform for the SIC.

Figure 6. Typical System Interface Controller Programming Waveform



System Processor Interface Register Set

The System Processor Interface register set is used by the AT43USB370 to interact with the system processor. The same register set is used in both the host and the function modes except where explicitly stated. All registers are 32-bit wide and require access on 4-bytes boundaries.

Reading a register for which the external system processor does not have read access will yield a zero value result. Writing to a register for which the external system processor does not have write access has no effect. For detailed usage of the registers, please refer to the *AT43USB370 Software Development Guide*.

Naming Convention

The following naming convention applies to the System Processor Interface Register Set.

- Three different fields in the register name are separated by underscores '_'
- The first field in the register name is a prefix indicating the Write access identification literal:
 - USBP indicates the register is always written by the AT43USB370 USB Processor
 - SYSP indicates the register is always written by the system processor
- The second field in the register name indicates the functionality of the register
- The third field in the register name is a suffix 'REG' common to all the registers

Table 1. System Processor Interface Register Set

S.N.	Address	Host/Device	Name	Function
1	0x00	H/D	SYSP_CMD_REG	Command Register
2	0x04	H/D	USBP_REQ_REG	Request Register
3	0x08	H	SYSP_CMDID_REG	Command ID Register (System Processor)
4	0x0C	H/D	USBP_CMDID_REG	Command ID Register (USB Processor)
5	0x10	H/D	USBP_EXECMDID_REG	Executed Command ID Register
6	0x14	H/D	USBP_CMDRESP_REG	Command Response Register
7	0x18	H	SYSP_DEVADDR_REG	Device Address Register (System Processor)
8	0x1C	H	USBP_DEVADDR_REG	Device Address Register (USB Processor)
9	0x20	H/D	SYSP_EPADDR_REG	Endpoint Address Register (System Processor)
10	0x24	H	USBP_EPADDR_REG	Endpoint Address Register (USB Processor)
11	0x28	H	SYSP_PKTTYPE_REG	Packet Type Register
12	0x2C	H	USBP_CLASSCD_REG	Class Code Register
13	0x30	H	USBP_SCLASSCD_REG	Subclass Code Register
14	0x34	H	USBP_PRTLCD_REG	Protocol Code Register
15	0x38	H	USBP_VENDID_REG	Vendor ID Register
16	0x3C	H	USBP_PRODID_REG	Product ID Register
17	0x40	H	USBP_HUBADDR_REG	Hub's Device Address Register
18	0x44	H	USBP_PORTNUM_REG	Hub's Port Number Register
19	0x48	H	SYSP_PKTSIZE_REG	Packet Size Register
20	0x4C	H	SYSP_RTYCNT_REG	Retry Count Register
21	0x50	H/D	SYSP_XFRMODE_REG	Data Transfer Mode Register

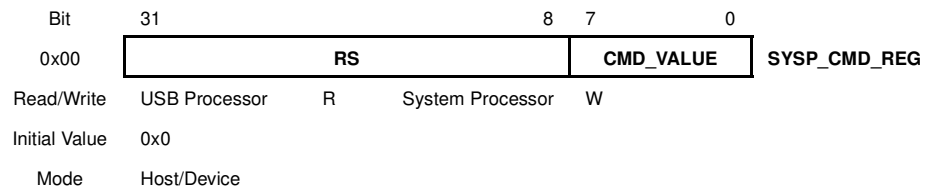
Table 1. System Processor Interface Register Set (Continued)

S.N.	Address	Host/Device	Name	Function
22	0x54	H/D	SYSP_SNDADDR_REG	Send Data Address Register
23	0x58	H/D	SYSP_SNDCNT_REG	Send Data Count Register
24	0x5C	H/D	SYSP_GETADDR_REG	Get Data Address Register
25	0x60	H/D	SYSP_GETCNT_REG	Get Data Count Register
26	0x64	H/D	USBP_XFRADDR_REG	Transfer Address Register
27	0x68	H/D	USBP_XFRCNT_REG	Transfer Count Register
28	0x6C	H	USBP_CNTXFRD_REG	Count Transferred Register
29	0x70	D	SYSP_CMDPARAM_REG	Command Parameter Register
30	0x74	D	USBP_CONGNUM_REG	Device Configuration Number Register
31	0x78	D	USBP_INTRNUM_REG	Device Interface Number Register
32	0x7C	D	USBP_ALSTNUM_REG	Device Alternate Setting Number Register
33	0x80	D	USBP_REQPARAM0_REG	Request Parameter 0 Register
34	0x84	D	USBP_REQPARAM1_REG	Request Parameter 1 Register
35	0x88	H/D	PRMS_HANDSHAKE_REG	Parameters Handshake Register
36	0x8C - 0xFE		Reserved	Unused
37	0xFF	H/D	SYSP_FIFODATA_REG	FIFO Data Access Register

Register Set Description

SYSP_CMD_REG – Command Register

The system processor software writes in this register.



- **Bit 7:0 - CMD_VALUE**

Unique value of the command issued by the system processor software. The following values are valid.

- **Bit 31:8 - RS**

Reserved. Must be reset to zero by the system processor software.

This register is used by the system processor software to write the command code while issuing a command to the USB processor. After power-up or reset, this register will contain the value of 0x00.

USBP_REQ_REG – Request Register

The USB processor writes in this register.

Bit	31	8	7	0		
0x04	RS			REQ_VALUE		USBP_REQ_REG
Read/Write	USB Processor	W	System Processor	R		
Initial Value	0x0					
Mode	Host/Device					

• **Bit 7:0 - REQ_VALUE**

Unique value of the request issued by the USB processor. The following definitions are valid.

• **Bit 31:8 - RS**

Reserved. Reset to zero by the USB processor.

This register is used by the USB processor to write the request code while issuing a request to the system processor software. After power-up or reset, this register will contain the value of 0x00.

SYSP_CMDID_REG – Command ID Register (System Processor)

The system processor software writes in this register.

Bit	31	8	7	0		
0x08	RS			SCMD_ID		SYSP_CMDID_REG
Read/Write	USB Processor	R	System Processor	W		
Initial Value	0x0					
Mode	Host					

• **Bit 7:0 - SCMD_ID**

Command ID of the command referenced by the system processor software.

• **Bit 31:8 - RS**

Reserved. Must be reset to zero by the system processor software.

This register is used by the system processor software to write the Command ID of a particular command issued earlier. This may be required where a reference to some previous command is required while issuing the command. After power-up or reset, this register will contain the value of 0x00.

USBP_CMDID_REG – Command ID Register (USB Processor)

The USB processor writes in this register.

Bit	31		8	7	0		
0x0C	RS				UCMD_ID		USBP_CMDID_REG
Read/Write	USB Processor	W	System Processor	R			
Initial Value	0x0						
Mode	Host/Device						

- **Bit 7:0 - UCMD_ID**

Command ID of the command issued by the USB processor.

- **Bit 31:8 - RS**

Reserved. Reset to zero by the USB processor.

This register is used by the USB processor to write the Command ID in response to a command issued by the system processor software. After power-up or reset, this register will contain the value of 0x00.

USBP_EXECMDID_REG – Executed Command ID Register

The USB processor writes in this register

Bit	31		8	7	0		
0x10	RS				EXE_CMD_ID		USBP_EXECMDID_REG
Read/Write	USB Processor	W	System Processor	R			
Initial Value	0x0						
Mode	Host/Device						

- **Bit 7:0 - EXE_CMD_ID**

Command ID of the command executed.

- **Bit 31:8 - RS**

Reserved. Reset to zero by the USB processor.

This register is used by the USB processor to write the Command ID of a particular command executed by the USB processor. After power-up or reset, this register will contain the value of 0x00.

USBP_CMDRESP_REG – Command Response Register

The USB processor writes in this register.

Bit	31	8	7	0		
0x14	RS			CMD_RESP		USBP_CMDRESP_REG
Read/Write	USB Processor	W	System Processor	R		
Initial Value	0x0					
Mode	Host/Device					

- **Bit 7:0 - CMD_RESP**

Response of the command executed.

- **Bit 31:8 - RS**

Reserved. Reset to zero by the USB processor.

SYSP_DEVADDR_REG – Device Address Register (System Processor)

The system processor software writes in this register.

Bit	31	8	7	0		
0x18	RS			SDEV_ADDR		SYSP_DEVADDR_REG
Read/Write	USB Processor	R	System Processor	W		
Initial Value	0x0					
Mode	Host					

- **Bit 7:0 - SDEV_ADDR**

Device address of the target device.

- **Bit 31:8 - RS**

Reserved. Must be reset to zero by the system processor software.

This register is used by the system processor software to write the address of the device for which a command is being issued to the USB processor. After power-up or reset, this register will contain the value of 0x00.

USBP_DEVADDR_REG – Device Address Register (USB Processor)

The USB processor writes in this register.

Bit	31			8	7	0	
0x1C	RS				UDEV_ADDR		USBP_DEVADDR_REG
Read/Write	USB Processor	W		System Processor	R		
Initial Value	0x0						
Mode	Host						

- **Bit 7:0 - UDEV_ADDR**

Device address of the target device.

- **Bit 31:8 - RS**

Reserved. Reset to zero by the USB processor.

This register is used by the USB processor to write the address of the device for which a request is being issued to the system processor software. After power-up or reset, this register will contain the value of 0x00.

SYSP_EPADDR_REG – Endpoint Address Register (System Processor)

The system processor software writes in this register.

Bit	31			4	3	0	
0x20	RS				SEP_ADDR		SYSP_EPADDR_REG
Read/Write	USB Processor	R		System Processor	W		
Initial Value	0x0						
Mode	Host/Device						

- **Bit 3:0 - SEP_ADDR**

Endpoint address of the target endpoint.

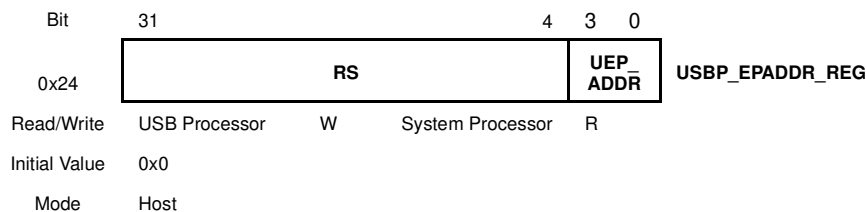
- **Bit 31:4 - RS**

Reserved. Must be reset to zero by the system processor software.

This register is used by the system processor software to specify the endpoint address. After power-up or reset, this register will contain the value of 0x00

USBP_EPADDR_REG – Endpoint Address Register (USB Processor)

The USB processor writes in this register.



- **Bit 3:0 - UEP_ADDR**

Endpoint address of the target endpoint.

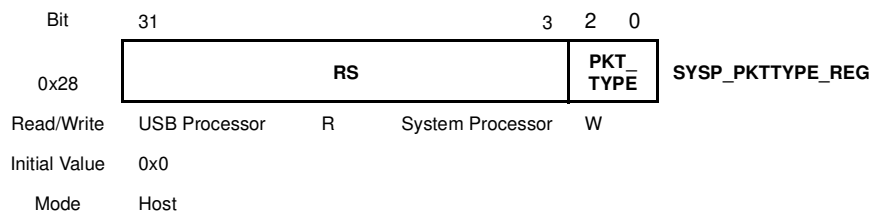
- **Bit 31:4 - RS**

Reserved. Must be reset to zero by the USB processor.

This register is used by the USB processor to specify the endpoint address. After power-up or reset, this register will contain the value of 0x00.

SYSP_PKTTYPE_REG – Packet Type Register

The system processor software writes in this register.



- **Bit 2:0 - PKT_TYPE**

Packet type (IN/OUT/SETUP) with data toggle (0/1) value of the packet. The following definitions are valid.

PKT_TYPE	Value (Hex)	Description
PKT_NO_DT	00	Packet Type - Data Toggle Value Not Specified. Data Toggle will be managed internally by the USB processor
PKT_DATA_0	01	Packet Type - Data Toggle 0
PKT_DATA_1	02	Packet Type - Data Toggle 1
PKT_SETUP	03	Packet Type - Setup

- **Bit 31:3 - RS**

Reserved. Must be reset to zero by the system processor software.

This register is used by the system processor software to write the packet type and data toggle value while issuing a request to the system processor software. After power-up or reset, this register will contain the value of 0x00.

USBP_CLASSCD_REG – Class Code Register

The USB processor writes in this register.

Bit	31			8	7			0	
0x2C	RS				CLASS_CD				USBP_CLASSCD_REG
Read/Write	USB Processor	W		System Processor		R			
Initial Value	0x0								
Mode	Host								

- **Bit 7:0 - CLASS_CD**

Class code value of the device.

- **Bit 31:8 - RS**

Reserved. Reset to zero by the USB processor.

This register is used by the USB processor to write the class code value while issuing a request to the system processor software. After power-up or reset, this register will contain the value of 0x00.

USBP_SCLASSCD_REG – Subclass Code Register

The USB processor writes in this register.

Bit	31			8	7			0	
0x30	RS				SCLASS_CD				USBP_SCLASSCD_REG
Read/Write	USB Processor	W		System Processor		R			
Initial Value	0x0								
Mode	Host								

- **Bit 7:0 - SCLASS_CD**

Subclass code value of the device.

- **Bit 31:8 - RS**

Reserved. Reset to zero by the USB processor.

This register is used by the USB processor to write the sub-class code value while issuing a request to the system processor software. After power-up or reset, this register will contain the value of 0x00.

USBP_PRTLCD_REG – Protocol Code Register

The USB processor writes in this register.

Bit	31	8	7	0		
0x34	RS			PRTL_CD		USBP_PRTLCD_REG
Read/Write	USB Processor	W	System Processor	R		
Initial Value	0x0					
Mode	Host					

- **Bit 7:0 - PRTL_CD**

Protocol code value of the device.

- **Bit 31:8 - RS**

Reserved. Reset to zero by the USB processor.

This register is used by the USB processor to write the protocol code value while issuing a request to the system processor software. After power-up or reset, this register will contain the value of 0x00.

USBP_VENDID_REG – Vendor ID Register

The USB processor writes in this register.

Bit	31	16	15	0		
0x38	RS			VEND_ID		USBP_VENDID_REG
Read/Write	USB Processor	W	System Processor	R		
Initial Value	0x0					
Mode	Host					

- **Bit 15:0 - VEND_ID**

Vendor ID of the USB device.

- **Bit 31:16 - RS**

Reserved. Reset to zero by the HSCID.

This register is used by the USB processor to specify the Vendor ID while issuing a request to the system processor software. After power-up or reset, this register will contain the value of 0x00.

USBP_PRODID_REG – Product ID Register

The USB processor writes in this register.

Bit	31	16	15	0	
0x3C	RS		PROD_ID		USBP_PRODID_REG
Read/Write	USB Processor	W	System Processor	R	
Initial Value	0x0				
Mode	Host				

- **Bit 15:0 - PROD_ID**

Product ID of the USB device.

- **Bit 31:16 - RS**

Reserved. Reset to zero by the USB processor.

This register is used by the USB processor to specify the Product ID while issuing a request to the system processor software. After power-up or reset, this register will contain the value of 0x00.

USBP_HUBADDR_REG – Hub's Device Address Register

The USB processor writes in this register.

Bit	31	8	7	0	
0x40	RS		HUB_ADDR		USBP_HUBADDR_REG
Read/Write	USB Processor	W	System Processor	R	
Initial Value	0x0				
Mode	Host				

- **Bit 7:0 - HUB_ADDR**

Device address of the hub to which the USB device is connected.

- **Bit 31:8 - RS**

Reserved. Reset to zero by the USB processor.

This register is used by the USB processor to write the device address of the hub to which a USB device is connected while issuing a request to the system processor software. After power-up or reset, this register will contain the value of 0x00.

USBP_PORTNUM_REG – Hub's Port Number Register

The USB processor writes in this register.

Bit	31			8	7			0	
0x44	RS				PORT_NUM				USBP_PORTNUM_REG
Read/Write	USB Processor		W	System Processor		R			
Initial Value	0x0								
Mode	Host								

- **Bit 7:0 - PORT_NUM**

Port number of the hub to which the USB device is connected.

- **Bit 31:8 - RS**

Reserved. Reset to zero by the USB processor.

This register is used by the USB processor to write the port number of the hub to which a USB device is connected while issuing a request to the system processor software. After power-up or reset, this register will contain the value of 0x00.

SYSP_PKT_SIZE – Packet Size Register

The system processor software writes in this register.

Bit	31			16	15			0	
0x48	RS				PKT_SIZE				USBP_PKT_SIZE_REG
Read/Write	USB Processor		R	System Processor		W			
Initial Value	0x0								
Mode	Host								

- **Bit 15:0 - PKT_SIZE**

Packet size in bytes.

- **Bit 31:16 - RS**

Reserved. Must be reset to zero by the system processor software.

This register is used by the system processor software to specify the Packet Size while issuing a command to the USB processor. This packet size is used by the USB processor for every transaction associated with this command. After power-up or reset, this register will contain the value of 0x00

SYSP_RTycNT_REG – Retry Count Register

The system processor software writes in this register.

Bit	31			8	7	0	
0x4C	RS				RTY_CNT		SYSP_RTycNT_REG
Read/Write	USB Processor	R		System Processor	W		
Initial Value	0x0						
Mode	Host						

- **Bit 7:0 - CMD_VALUE**

Retry Count for every transaction associated with this command.

- **Bit 31:8 - RS**

Reserved. Must be reset to zero by the system processor software.

This register is used by the system processor software to specify the retry count for every transaction associated with this command while issuing a command to the USB processor. After power-up or reset, this register will contain the value of 0x00.

SYSP_XFRMODE_REG – Data Transfer Mode Register

The system processor software writes in this register.

Bit	31			1	0		
0x50	RS				TMODE		SYSP_XFRMODE_REG
Read/Write	HSICD	R		System Processor	W		
Initial Value	0x0						
Mode	Host/Device						

- **Bit 1:0 - TMODE**

Data Transfer Mode.

TMODE	Value (Hex)	Description
XFRMODE_DMA	01	(Data) Transfer Mode - DMA
XFRMODE_DMA	02	(Data) Transfer Mode - Direct FIFO

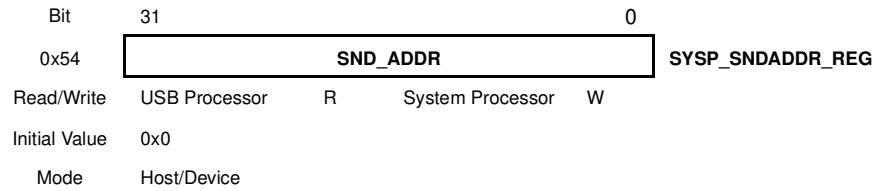
- **Bit 31:2 - RS**

Reserved. Must be reset to zero by the system processor software.

This register is used by the system processor to specify the mode with which it wants to transfer data while issuing a command to the HSICD. After power-up or reset, this register will contain the value of 0x00.

SYSP_SNDADDR_REG – Send Data Address Register

The system processor software writes in this register.



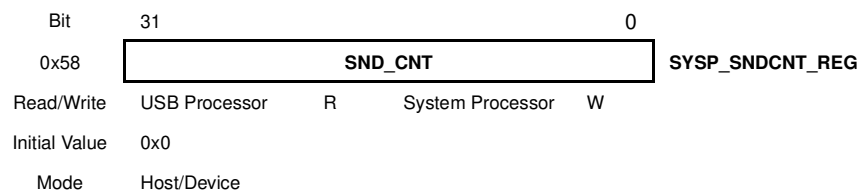
• **Bit 31:0 - SND_ADDR**

Start Address of the buffer for sending data.

This register is used by the system processor software to specify the start address of the data buffer while issuing a command to the USB processor to transfer data from the system processor software's memory to a USB device. After power-up or reset, this register will contain the value of 0x00.

SYSP_SNDCNT_REG – Send Data Count Register

The system processor software writes in this register.



• **Bit 31:0 - SND_CNT**

Count of the buffer for sending data.

This register is used by the system processor software to specify the size of the data buffer while issuing a command to the USB processor to transfer data from the system processor software's memory to the USB device. This is the size of the buffer whose address is specified in Send Data Address Register. After power-up or reset, this register will contain the value of 0x00.

SYSP_GETADDR_REG – Get Data Address Register

The system processor software writes in this register.

Bit	31			0
0x5C	GET_ADDR			SYSP_GETADDR_REG
Read/Write	USB Processor	R	System Processor	W
Initial Value	0x0			
Mode	Host/Device			

- **Bit 31:0 - GET_ADDR**

Start Address of the buffer for storing data.

This register is used by the system processor software to specify the start address of the data buffer while issuing a command to the USB processor to transfer data from the USB device to the system processor software's memory. After power-up or reset, this register will contain the value of 0x00.

SYSP_GETCNT_REG – Get Data Count Register

The system processor software writes in this register.

Bit	31			0
0x60	GET_CNT			SYSP_GETCNT_REG
Read/Write	USB Processor	R	System Processor	W
Initial Value	0x0			
Mode	Host/Device			

- **Bit 31:0 - GET_CNT**

Count of the data buffer for receiving data.

This register is used by the system processor software to specify the size of the data buffer while issuing a command to the USB processor to transfer data from the USB device to the system processor software's memory. This is the size of the buffer specified in Get Data Address Register. After power-up or reset, this register will contain the value of 0x00.

USBP_XFRADDR_REG – Transfer Address Register

The USB processor writes in this register.

Bit	31				0	
0x64	XFR_ADDR					USBP_XFRADDR_REG
Read/Write	USB Processor	W	System Processor	R		
Initial Value	0x0					
Mode	Host/Device					

- **Bit 31:0 - XFR_ADDR**

Address for the data transfer.

This register is used by the USB processor to specify the start address of the memory while issuing a request to system processor software to transfer data. After power-up or reset, this register will contain the value of 0x00.

USBP_XFRCNT_REG – Transfer Count Register

The USB processor writes in this register.

Bit	31				0	
0x68	XFR_CNT					USBP_XFRCNT_REG
Read/Write	USB Processor	W	System Processor	R		
Initial Value	0x0					
Mode	Host/Device					

- **Bit 31:0 - XFR_CNT**

Transfer count in bytes.

This register is used by the USB processor to specify the number of bytes while issuing a request to the system processor software to transfer data. This register specifies the count to be transferred from the location specified in the Transfer Address Register. After power-up or reset, this register will contain the value of 0x00.