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Features

- 5 Smart Card Interfaces
  - Compliance with ISO 7816, EMV2000, GIE-CB and GSM Standards
  - Direct Connection to the Smart Cards
    - Logic Level Shifters
    - Short Circuit Current Limitation
    - 4kV+ ESD Protection (MIL/STD 883 Class 3)
  - 1 or 2 Master Smart Card interfaces
    - Synchronous Card support (with C4 and C8 Contacts)
    - Card Detection and Automatic de-activation sequence on card extraction
  - 1 to 4 SAM/SIM cards (15 to 30mA each)
  - Programmable Voltage for each smart card
    - Class A: 5V ±0.4V at 60 mA (±0.25V at 65 mA with VCC= 5V±10%)
    - Class B: 3V ±0.2V at 60 mA
    - Class C: 1.8V ±0.14V at 40mA
  - Low Ripple Noise: < 200 mV
  - Programmable Activation Sequence
  - Automatic de-activation on card power-fail or over-current and system power-fail
  - Card Clock Stop High or Low for Card Power-down Modes
- Versatile Host Interface
  - Two Wire Interface (TWI) Link at 400kbit/s
    - Programmable Address allow up to 4 AT83C26 on the bus
  - Programmable Interrupt Output
- Reset Output Includes
  - Power-On Reset (POR)
  - Power-Fail Detector (PFD)
- Extended Voltage Operation: 3 to 5.5V
- Low Power Consumption
  - 5 mA Maximum Operating Current (without Smart Card)
  - 150 mA Maximum In-rush Current (each DC/DC)
  - 30 µA Typical Power-down Current (without Smart Card)
- 4 to 48 MHz Clock Input
- System clock derived from the external clock input
- Industrial Temperature Range: -40 to +85°C
- Packages: QFN48, VQFP48

Description

The AT83C26 is a smart card reader interface IC for smart card reader/writer applications such as EFT/POS terminals and set top boxes. It enables the management of any type of smart card from any kind of host. Up to 4 AT83C26 can be connected in parallel thanks to the programmable TWI address.

Its high efficiency DC/DC converters and low quiescent current in stand-by mode make it particularly suited to low power and portable applications. The reduced bill of material allows to lower significantly the system size and cost. A sophisticated protection system guarantees timely and controlled shutdown upon error conditions.

Multiple Smart Card Reader Interface With Power Management

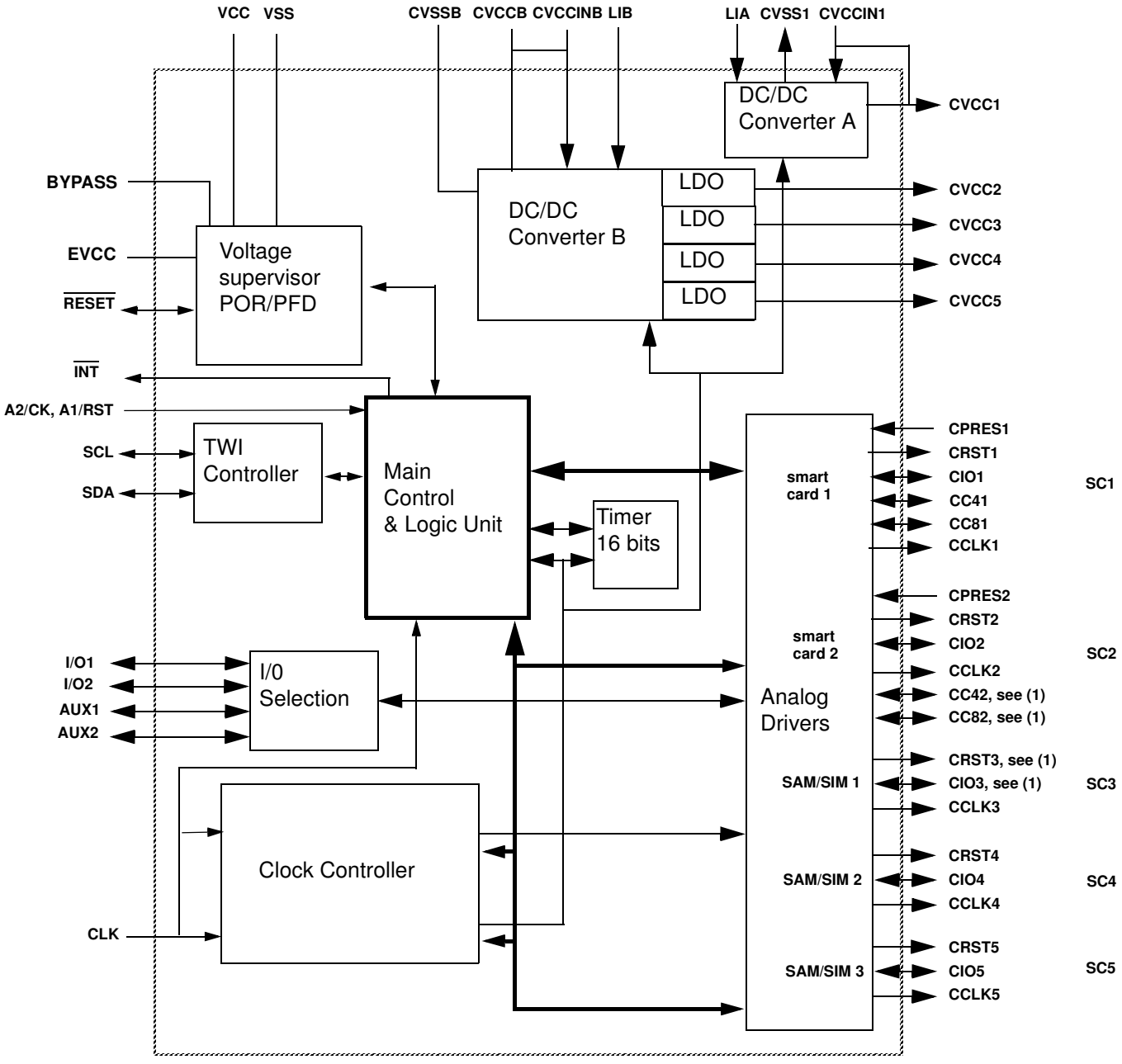
AT83C26

7511D–SCR–02/07

Acronyms

TWI: Two Wire Interface
POR: Power On Reset
PFD: Power Fail Detect
ART: Automatic Reset Transition
ATR: Answer To Reset

Block Diagram

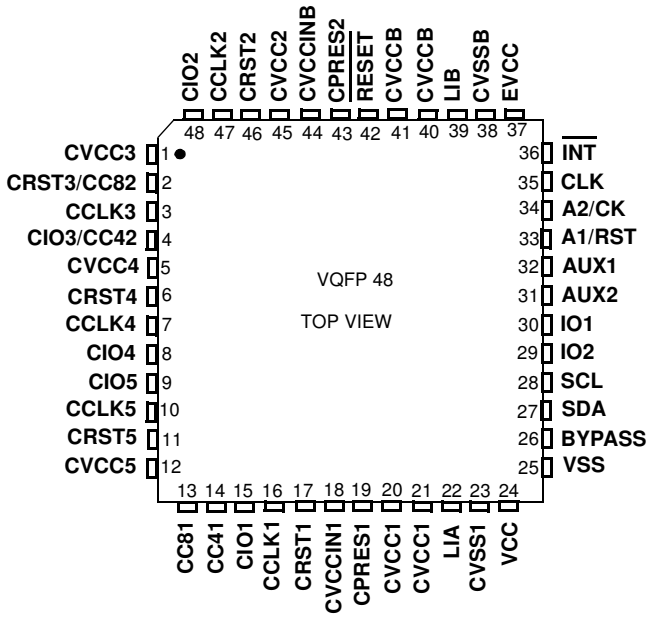


Note: 1. CRST3/CC82 are on the same pin. CIO3/CC42 are on the same pin. If complete Smart card 2 interface is used, SAM/SIM3 isn't available. Respectively, if SAM/SIM3 is used, complete Smart card 2 isn't available.

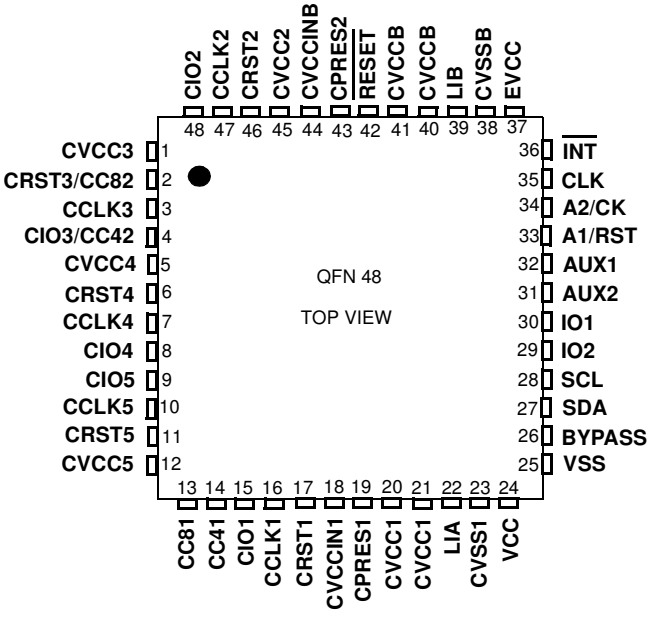
Pin Description

Pinout (Top View)

VQFP48 Pinout



QFN48 Pinout



Signals

Table 1. Ports Description

VQFP48 or QFN48 Pin number	Pad Name	Pad Internal Power Supply	Pad Type	Description
1	CVCC3		PWR	VCC pin for SC3 interface.
2	CRST3/CC82	CVCC3	I/O pull up	See SC2_CFG1 register: If SC2_FULL bit = 0, CRST pin for SC3 interface. If SC2_FULL bit = 1, CC8 pin for SC2 interface.
3	CCLK3	CVCC3	O	CCLK pin for SC3 interface.
4	CIO3/CC42	CVCC3	I/O pull up	See SC2_CFG1 register: If SC2_FULL bit = 0, CIO pin for SC3 interface. If SC2_FULL bit = 1, CC4 pin for SC2 interface.
5	CVCC4		PWR	VCC pin for SC4 interface.
6	CRST4	CVCC4	O	RST pin for SC4 interface.
7	CCLK4	CVCC4	O	CCLK pin for SC4 interface.
8	CIO4	CVCC4	I/O pull up	CIO pin for SC4 interface.
9	CIO5	CVCC5	I/O pull up	CIO pin for SC5 interface.
10	CCLK5	CVCC5	O	CCLK pin for SC5 interface.
11	CRST5	CVCC5	O	RST pin for SC5 interface.
12	CVCC5		PWR	VCC pin for SC5 interface.
13	CC81	CVCC1	I/O pull up	CC8 pin for SC1 interface.
14	CC41	CVCC1	I/O pull up	CC4 pin for SC1 interface.
15	CIO1	CVCC1	I/O pull up	CIO pin for SC1 interface.
16	CCLK1	CVCC1	O	CCLK pin for SC1 interface.
17	CRST1	CVCC1	O	RST pin for SC1 interface.
18	CVCCIN1		PWR	This pin must be connected to CVCC1 pins next to the package.
19	CPRES1	VCC	I pull up	Card presence for SC1 interface. An internal pull up to VCC can be activated in the pad if necessary using PULLUP1 bit in SC1_CFG1 register (activated by default).
20	CVCC1		PWR	VCC pin for SC1 interface. The two CVCC1 pins are connected together near the package. Only one wire goes to the smart card connector. The reason of two CVCC1 pins is to reduce noise.
21	CVCC1		PWR	VCC pin for SC1 interface.

Table 1. Ports Description (Continued)

VQFP48 or QFN48 Pin number	Pad Name	Pad Internal Power Supply	Pad Type	Description
22	LIA		PWR	DC/DCA input. LIA must be tied to VCC pin through an external coil (typically 10µH) and provides the current for the charge pump of the DC/DCA converter. It may be directly connected to VCC if the step-up converter is not used (see STEPREGA bit in SC1_CFG4 register and see minimum VCC values in Table 50.for class A and Table 51. for class B)
23	CVSS1		GND	DC/DCA input. This pin must be directly connected to the VSS of power supply.
24	VCC		PWR	VCC is used to power the internal voltage regulators and I/O buffers.
25	VSS		GND	Ground.
26	BYPASS	VCC	I	A high level on this pin activates a low power consumption mode with internal regulator bypassed.
27	SDA	VCC	I/O open drain	Micro controller interface function: TWI serial data. An external pull up must be connected on SDA pin (4.7kOhms).
28	SCL	VCC	I/O open drain	Micro controller interface function: TWI clock. An external pull up must be connected on SCL pin (4.7kOhms).
29	IO2	EVCC	I/O pull up	The behavior of this pin depends on IOSEL[3/0] bits values (see IO_SELECT register).
30	IO1	EVCC	I/O pull up	The behavior of this pin depends on IOSEL[3/0] bits values (see IO_SELECT register).
31	AUX2	EVCC	I/O pull up	The behavior of this pin depends on IOSEL[3/0] bits values (see IO_SELECT register).
32	AUX1	EVCC	I/O pull up	The behavior of this pin depends on IOSEL[3/0] bits values (see IO_SELECT register).
33	A1/RST	EVCC	I	The TWI address depends on the value present on this pin at reset. If CRST transparent mode is selected, the A1/RST signal is connected to CRST1 or CRST2 pins (see CRST_SEL1 and CRST_SEL2 bits respectively in SC1_CFG4 and SC2_CFG2 registers).
34	A2/CK	EVCC	I	The TWI address depends on the value present on this pin at reset. If CCLKn transparent mode is selected, the A2/CK signal is connected to CCLKn pins (with n=1 to 5). See CKSn[2:0] bits respectively in SC1_CFG1, SC2_CFG2, SC3_CFG2, SC4_CFG2, SC5_CFG2 registers.
35	CLK	EVCC	I	Master clock.
36	$\overline{INT}$	VCC	O open drain	Interruption status. An internal pull up to VCC can be activated in the pin if necessary using INT_PULLUP bit in SC1_CFG4 (deactivated by default).
37	EVCC		PWR	Extra supply voltage (Micro controller power supply). EVCC is used to supply the internal level shifters of host interface pins. EVCC is connected to the host power supply. EVCC voltage can be directly connected to VCC if the host power supply and the AT83C26 power supply is the same.

Table 1. Ports Description (Continued)

VQFP48 or QFN48 Pin number	Pad Name	Pad Internal Power Supply	Pad Type	Description
38	CVSSB		GND	DC/DCB input. This pin must be directly connected to the VSS of power supply.
39	LIB		PWR	DC/DCB input. LIB must be tied to VCC pin through an external coil (typically 10µH) and provides the current for the charge pump of the DC/DCB converter. It may be directly connected to VCC if the step-up converter is not used (see STEPREGB bit in DCDCB register and see minimum VCC values in Table 53.for class A and Table 54. for class B)
40	CVCCB		PWR	DC/DCB output. The two CVCCB pins are connected together near the package. CVCCB pin is only used for DC/DCB voltage measurements.The reason of two CVCCB pins is to reduce noise.
41	CVCCB		PWR	DC/DCB output.
42	$\overline{\text{RESET}}$	VCC	I/O open drain	Micro controller interface function: reset signal. • power on reset • A low level on this pin keeps the AT83C26 under reset even if applied on power-on. It also resets the AT83C26 if applied when the AT83C26 is running. • Asserting $\overline{\text{RESET}}$
43	CPRES2	VCC	I pull up	Card presence for SC2 interface. An internal pull to VCC can be activated in the pad if necessary using PULLUP2 bit in SC2_CFG1 register (activated by default).
44	CVCCINB		PWR	This pin must be connected to CVCCB pins next to the package.
45	CVCC2		PWR	VCC pin for SC2 interface.
46	CRST2	CVCC2	O	CRST pin for SC2 interface.
47	CCLK2	CVCC2	O	CCLK pin for SC2 interface.
48	CIO2	CVCC2	I/O pull up	CIO pin for SC2 interface.

Note: The ESD limit is 4kV for smart card pins and 2kV for others.

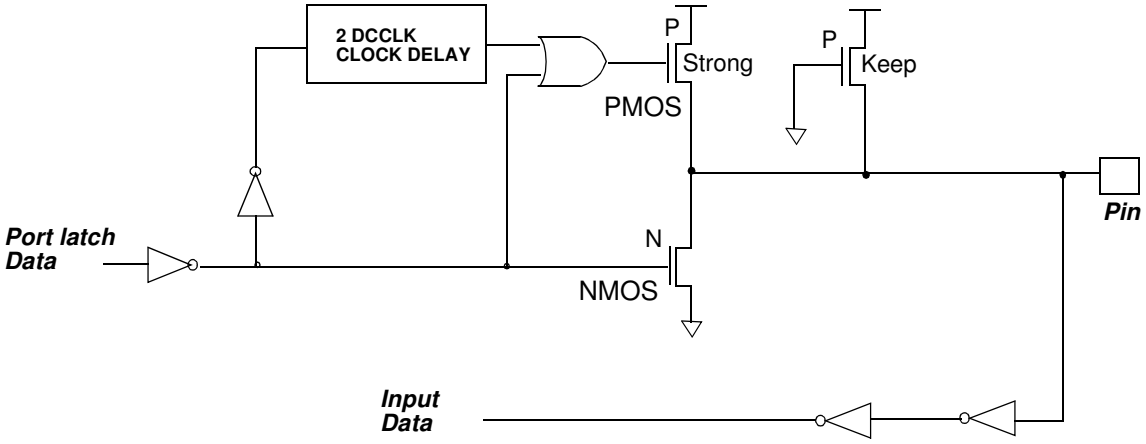
Pad Type Description

To simplify the understanding of Figure 1. to Figure 8., a shortcut is possible by replacing the weak transistor by a 100k Ohms pull-up resistor, the medium transistor by a 10k Ohms pull-up resistor and the strong transistor by a 1k Ohms pull-up resistor.

Input/Output with Pull-up Configuration (IO1, IO2, AUX1, AUX2)

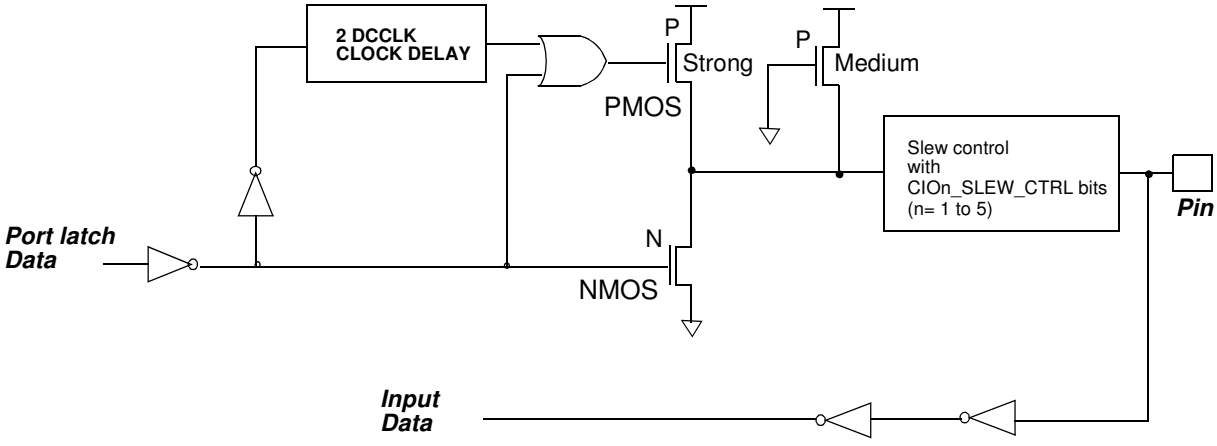
This output type can be used as both an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic high, it is weakly driven, allowing an external device to pull the pin low. When the port outputs a logic low state, it is driven strongly and able to sink a fairly large current.

Figure 1. Input/Output with Pull-up Configuration



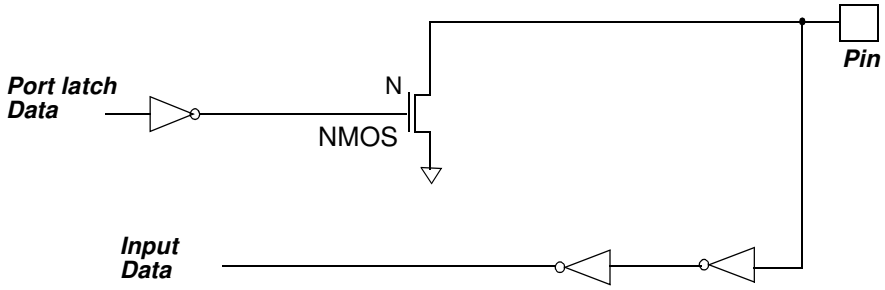
Input/Output with Pull-up Configuration (ClOn with n = 1, 2, 3, 4, 5) and (CC4n, CC8n with n = 1, 2)

Figure 2. Input/Output with Pull-up Configuration



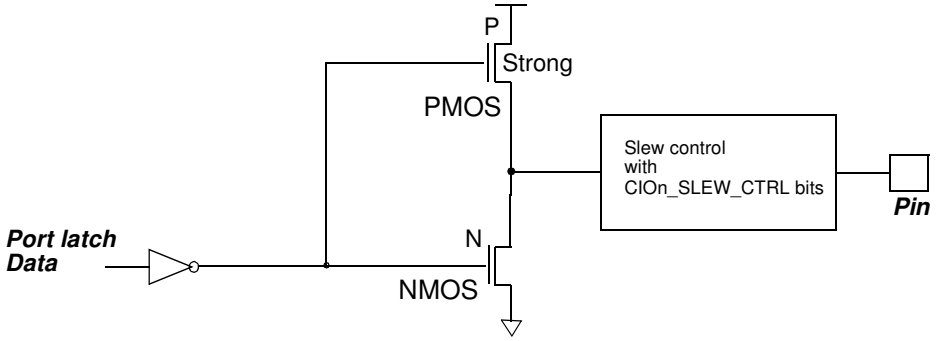
Input/Output with Open Drain Configuration (SDA, SCL, $\overline{\text{RESET}}$)

Figure 3. Input/Output with Open Drain Configuration



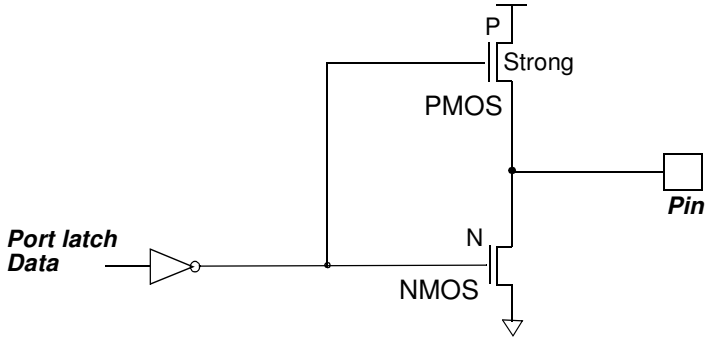
Output Configuration (CCLKn with n = 1, 2, 3, 4, 5)

Figure 4. Output Configuration



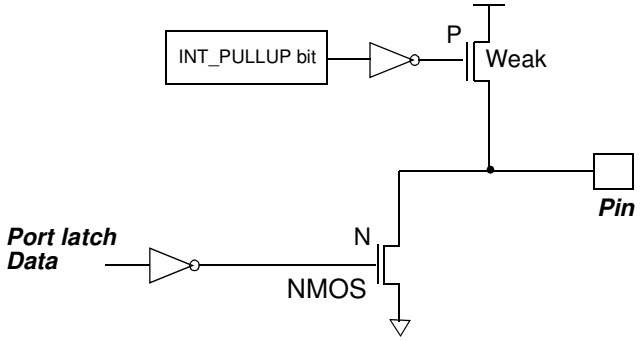
Output Configuration (CRSTn with n = 1, 2, 3, 4, 5)

Figure 5. Output Configuration



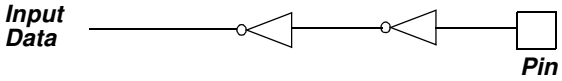
Open drain Output with programmable pull-up Configuration ($\overline{INT}$)

Figure 6. Open Drain Output with programmable pull-up



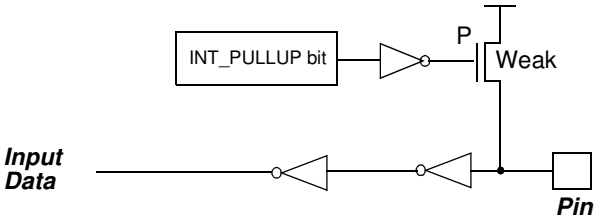
Input Configuration (A1, A2, CLK, BYPASS)

Figure 7. Input



Input with programmable pull-up Configuration (CPRES1, CPRES2)

Figure 8. Input with programmable pull-up



Operational Modes

TWI Bus Control

The Atmel Two-Wire Interface (TWI) interconnects components on a unique two-wire bus, made up of one clock line and one data line with speeds of up to 400 Kbits per second, based on a byte-oriented transfer format.

The TWI-bus interface can be used:

- To configure the AT83C26
- To select interface
- To select the operating mode of the card: 1.8V, 3V or 5V
- To configure the automatic activation sequence
- To start or stop sessions (activation and de-activation sequences)
- To initiate a warm reset
- To control the clock to the card in active mode
- To control the clock to the card in stand-by mode (stop LOW, stop HIGH or running)
- To enter or leave the card stand-by or power-down modes
- To select the interface (connection to the host I/O/C4/C8)
- To request the status (card present or not, over-current and out of range supply voltage occurrence)
- To drive and monitor the card contacts by software
- To accurately measure the ATR delay when automatic activation is used
- Re-use the AT83C24 command set for the first DC/DC and smart card interface with the following changes:
  - CKS extended to CONFIG2[0:3], CKS=8 selects CLK/3 and CKS>8 is reserved
  - The slave address byte for TWI write commands is 0100 $A_2A_1$10 and 0100 $A_2A_1$11 for TWI read commands

TWI Commands

Frame Structure

The structure of the TWI bus data frames is made of one or a series of write and read commands completed by STOP.

Write commands to the AT83C26 have the structure:

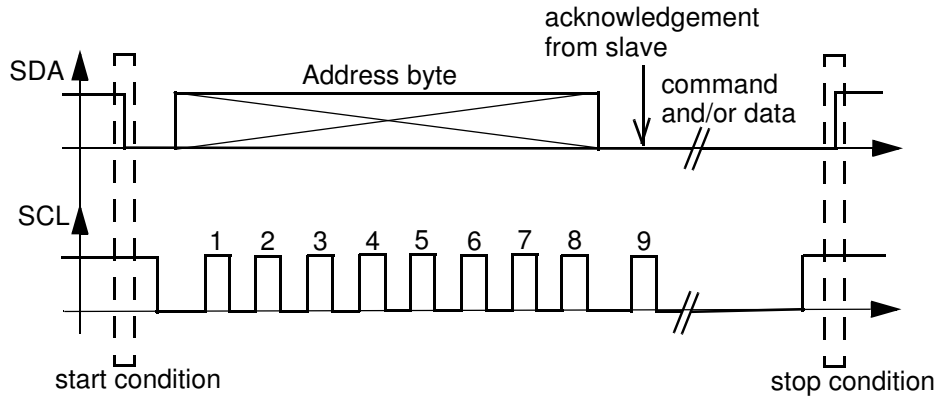
ADDRESS BYTE + COMMAND BYTE + DATA BYTE(S)

Read commands to the AT83C26 have the structure:

ADDRESS BYTE + DATA BYTE(S)

The ADDRESS BYTE is sampled on A2/CK and A1/RST **after each reset** (hard/soft/general call) but A2/CK, A1/RST can be used for transparent mode after the reset.

Figure 1. Data transfer on TWI bus

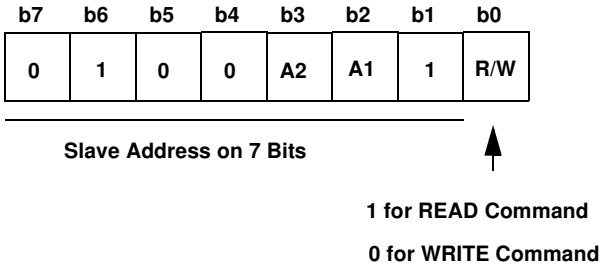


Address Byte

The first byte to send to the device is the address byte. The device controls if the hardware address (A2/CK, A1/RST pins on reset) corresponds to the address given in the address byte (A2, A1 bits).

If the level is not stable on A2/CK pin at reset, the user has to manage the possible address taken by the device.

Figure 2. Address Byte



Up to 4 devices can be connected on the same TWI bus. Each device is configured with a different combination on A2/CK, A1/RST pins. The address byte of each device for read/write operations are listed below.

Table 2. Address Byte Values

A2 (A2/CK pin)	A1 (A1/RST pin)	Address Byte for Read Command	Address Byte for Write Command
0	0	0x43	0x42
0	1	0x47	0x46
1	0	0x4B	0x4A
1	1	0x4F	0x4E

$\overline{\text{RESET}}$ pin

The TWI ADDRESS BYTE is sampled on A2/CK and A1/RST after a rising edge on $\overline{\text{RESET}}$ pin. The delay between the rising edge and the sampling of A2/CK and A1/RST is t1.

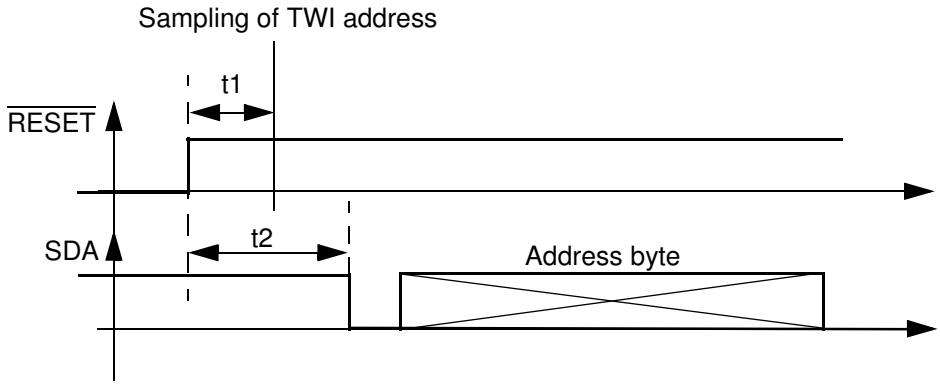
The value for t1 is 22 CLK period.

The minimum value for t2 is 40 CLK period. During the t2 time, the TWI bus is not ready to receive a command.

The CLK period depends on the frequency of the signal on CLK pin.

The $\overline{\text{RESET}}$ pin is an I/O with Open Drain. The host IO pin connected to $\overline{\text{RESET}}$ must be an I/O open drain (with external pull-up) or an I/O open drain with internal pull up.

Figure 3. Timings after reset



BYPASS pin

A high level on this pin activates a low power consumption mode.

At reset, the level on this pin must be fixed (VSS or VCC).

Before to set BYPASS pin, SHUTDOWNA and SHUTDOWNB bits must be set.

If SHUTDOWNA bit is set, DCDCA is switched off.

If SHUTDOWNB bit is set, DCDCB is switched off.

If SHUTDOWNA and SHUTDOWNB bits are set, the regulator is switched off.

If BYPASS pin is at a high level, the bandgaps are switched off.

Smart Card Interfaces

The AT83C26 enables the management of up to 5 smart card interfaces. Due to shared IOs between SC2 and SC3, the user should choose between a full SC2 interface (with CC4 and CC8) or SC3 interface.

The SC2_FULL bit in SC2_CFG1 register is used to select the SC2/SC3 interfaces configuration.

Table 3. SC2 and SC3 shared IOs

Pin name	SC2_FULL = 1 SC3 interface not available	SC2_FULL = 0 SC2 without CC4and CC8 + SC3 interface
CPRES2	CPRES2	CPRES2
CRST2	CRST2	CRST2
CIO2	CIO2	CIO2
CCLK2	CCLK2	CCLK2
CRST3/CC82	CC82	CRST3
CIO3/CC42	CC42	CIO3
CCLK3	unused	CCLK3

DCDC Converters

The DC/DC A converter is used to provide smart card voltage for the SC1 interface (CVCC1).

The DC/DC B converter is used to provide smart card voltage for the SCn interfaces (n=2, 3, 4, 5).

DC/DC converters need a clock of 4MHz (see Section “Clock Controller”). Two internal oscillators (one for each converter) provide the DC/DC clocks.

The DC/DCB output is connected on 4 LDO regulators (Low Drop Output) to generate CVCCn voltage (n=2, 3, 4, 5).

Clock Controller

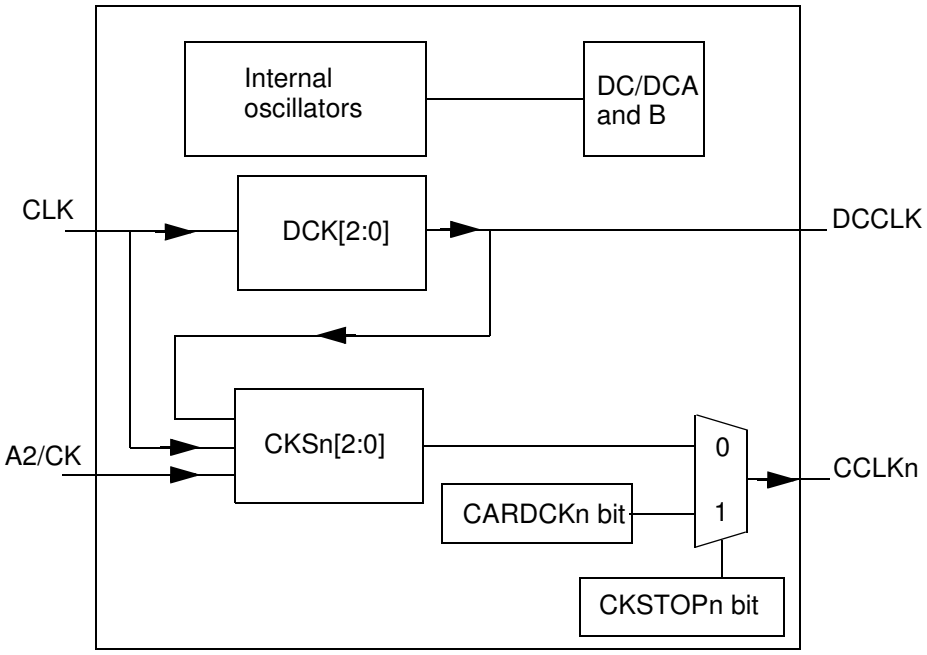
The clock controller outputs six clocks:

1. Five clocks for CCLK1, CCLK2, CCLK3, CCLK4 and CCLK5. Four different sources can be used: CLK pin, DCCLK signal, CARDCKn bit (n=1, 2, 3, 4, 5) or A2/CK.
2. A DCCLK clock used for pads and deactivation sequence.

Clock controller for SCn (n=1, 2, 3, 4, 5)

The transparent mode with A2/CK pin is available on SCn interface. The CKSn[2:0] register is used to select this transparent mode between A2/CK and CCLKn. The bit CKSTOPn must be cleared to have CCLKn running according to CKSn[2:0].

Figure 4. Clock Block Diagram with Software Activation



CRST controller

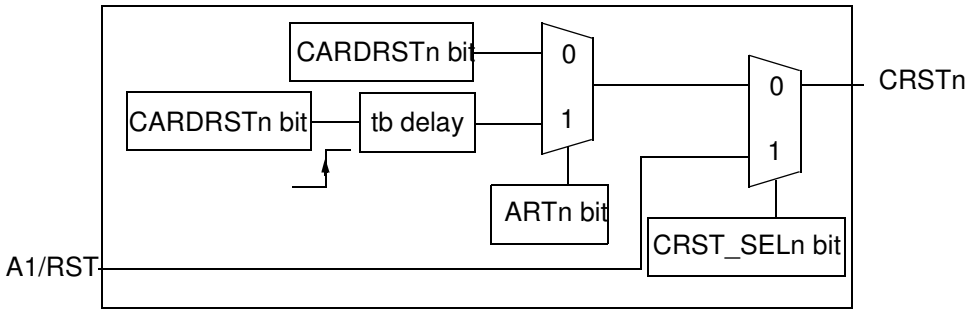
CRSTn for SCn interface (n=1, 2)

The CRSTn output pin is driven by the CARDRSTn bit value or by A1/RST pin.

Three modes are available:

- If the ARTn bit is reset, CRSTn pin is driven by CARDRSTn bit.
- If the ARTn bit is set, CRSTn pin is controlled and follows the “Automatic Reset Transition” (see Activation sequence page 25).
- A transparent mode with A1/RST pin.

Figure 5. CRSTn Block Diagram



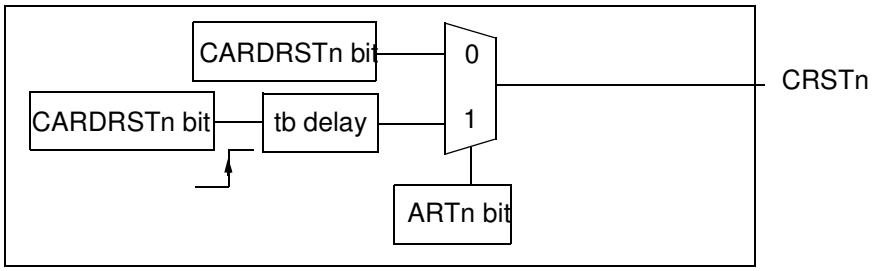
CRSTn for SCn interface (n= 3, 4, 5)

The CRSTn output pin is driven by the CARDRSTn bit value (see SCn_CFG2 register).

Two modes are available:

- If the ARTn bit is reset, CRSTn pin is driven by CARDRSTn bit.
- If the ARTn bit is set, CRSTn pin is controlled and follows the “Automatic Reset Transition” (see Activation sequence page 25).

Figure 6. CRSTn Block Diagram



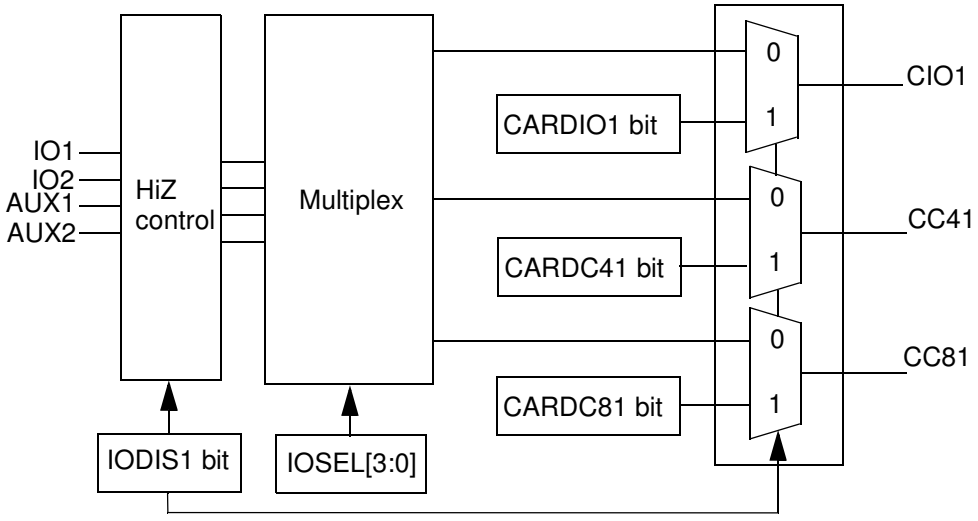
If SC2_FULL=1, the SC3 interface is not available.

CIO, CC4, CC8 controller

CIO1, CC41, CC81 controller for SC1 interface

The CIO1, CC41, CC81 output pins are driven respectively by CARDIO1, CARDC41, CARDC81 bits values or by I/O1, I/O2, AUX1or AUX2 signals. This selection depends of the IODIS1 bit value (SC1_INTERFACE register) and of IOSEL[3:0] bits value (IO_SELECT register).

Figure 7. CIO1, CC41, CC81 Block Diagram

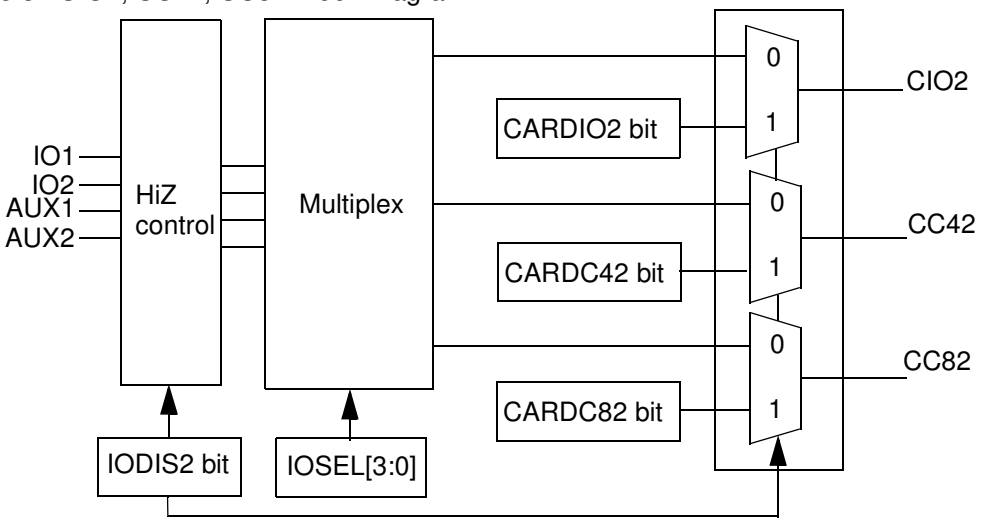


If IODIS1 is set, the CARDIO1 bit value is output on CIO1.The input selected by IOSEL for CIO1 is in High impedance state. CC41 and CC81 have the same behavior.

If IODIS1 is reset, data are bidirectional between the I/O1, I/O2, AUX1, AUX2 pins (see IO_SELECT register) and CIO1, CC41, CC81 pins.

CIO2, CC42, CC82 controller for SC2 interface

Figure 8. CIO2, CC42, CC82 Block Diagram

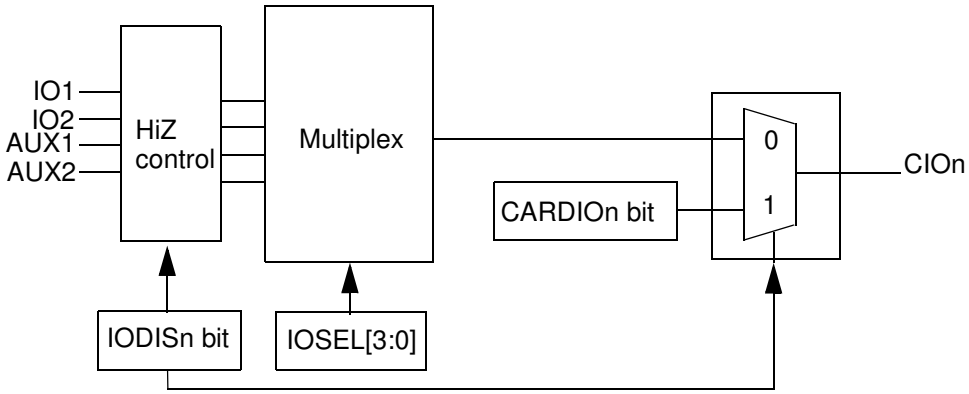


The SC2_FULL bit must be set to use CC42 and CC82.

CIOn controller for SCn interface (n=3, 4, 5)

The CIOn output pin is driven by CARDIOn bit values or by I/O1, I/O2, AUX1 or AUX2 signals. This selection depends of the IODISn bit value. If IODISn is reset, data are bidirectional between the I/O1, I/O2, AUX1, AUX2 pins (see IO_SELECT register) and CIOn pins.

Figure 9. CIOn Block Diagram



CIOn (n=1 to 5), CC41, CC81, CC42, CC82 transparent mode description

Two modes are available on CIOn, CC4n, CC8n signals:

- Bit control (a bit controls the output pin)
- Transparent mode (IO signal and CIO are linked after level shifter)

According to IO_SELECT register value and IODISn bits values, one of 4 input pins (IO1, IO2, AUX1 or AUX2) is linked to the selected output.

The idle state is the high level. Each signal is bidirectional.

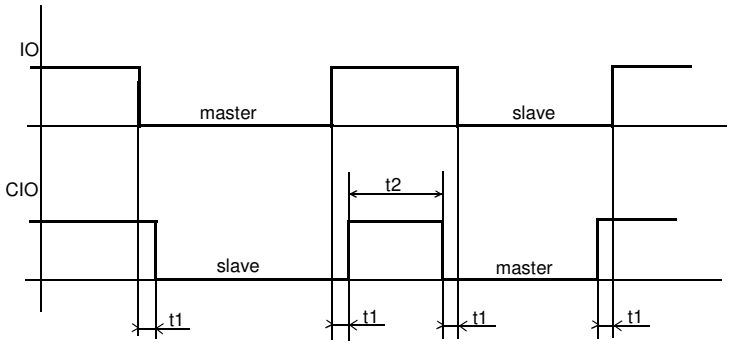
Transparent mode arbitration system

The first between IO and CIO to force a low level becomes the master.

The slave signal is grounded after t1 delay:

t1 max = 2* (CLK period).

Figure 10. Bidirectional mode



The minimum delay for a pulse at 0 or 1 to be detected is between 0.5 and 1.5 CLK period (depending on arrival time).

If IO and CIO are both grounded, CIO becomes the master.

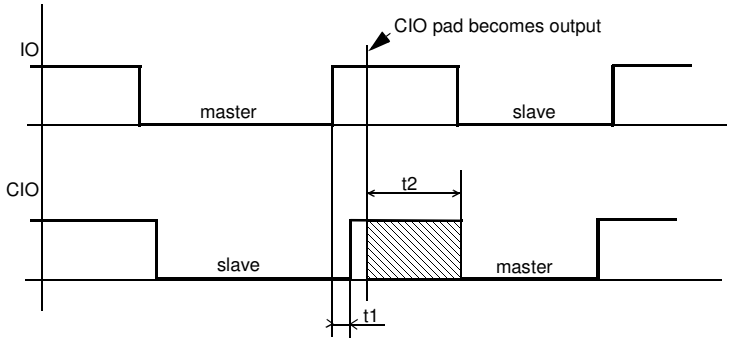
The minimum delay to switch of master without electrical conflict is equal to:

t2 min = 4 * (CLK period) + 2 * (DCCLK period) * (CLK period).

If a master switch appears before this minimum delay, the electrical conflict delay is:

t2 = 2 * (DCCLK period) * (CLK period)

Figure 11. Electrical conflict



CCLKn and CIOn (n=1 to 5) slew rate control

Three registers SLEW_CTRL_1, SLEW_CTRL_2 and SLEW_CTRL_3 control the slew rate of the CIOn and CCLKn signals. Each signal has 2 control bits.

An automatic mode is proposed. The VCARDn[1:0] value is used to automatically adjust the slew rate.

For specific cases, like long wires between AT83C26 and smart card connector for example, the user can forced the slew rate.

The rising edge and the falling edge are modified with the slew rate control for CCLKn.

Only the rising edge is modified on CIOn with the slew rate control.

See Table 63. to Table 68. in Electrical Characteristics.

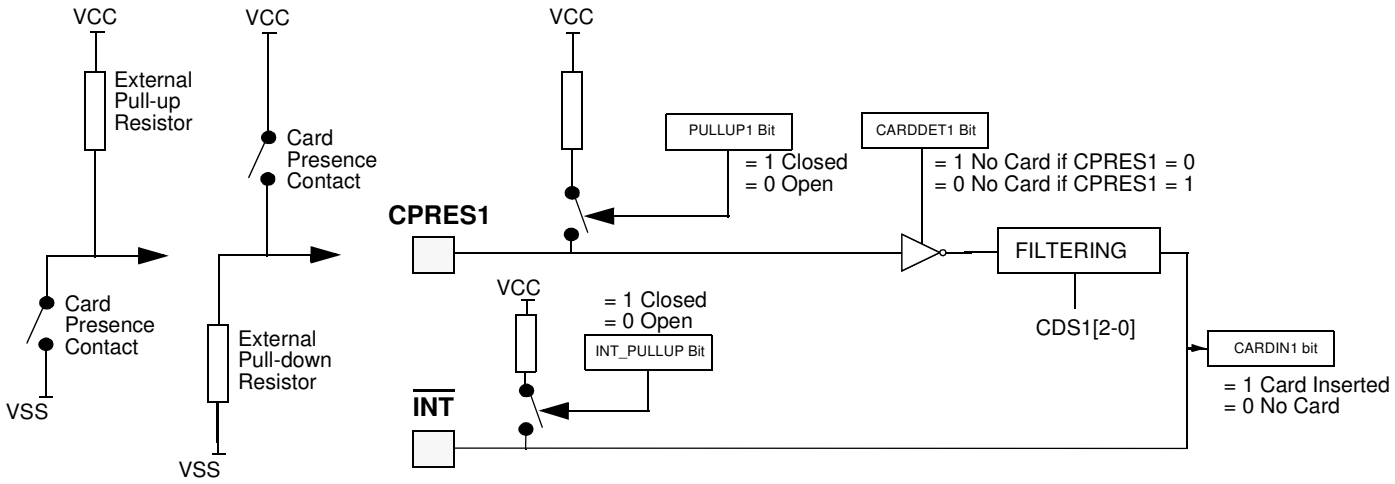
Card Presence Detection

Card presence detection for SC1 interface

The card presence signal is connected on the CPRES1 pin. The polarity of card presence contact is selected with the CARDDET1 bit (see SC1_CFG1 register). A programmable filtering is controlled with the CDS1[2-0] bits.

The internal pull-up on the CPRES1 pin can be disconnected in order to reduce the consumption. An external pull-up must be connected to Vcc. The PULLUP1 bit (see SC1_CFG1 register) controls this feature.

Figure 12. SC1 presence Input

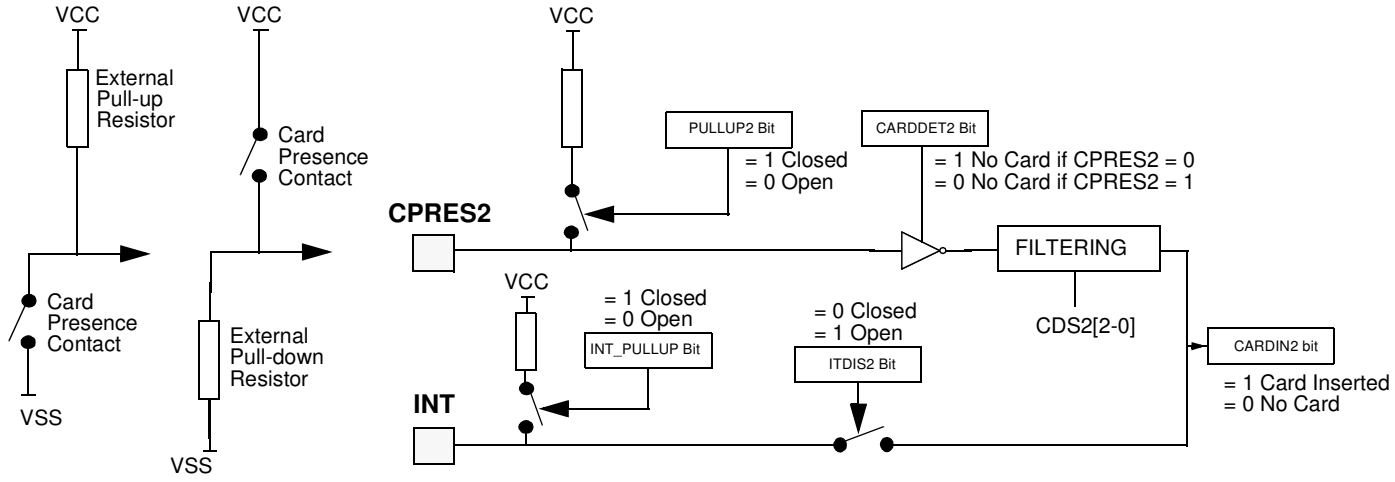


If the card presence contact is connected to Vcc, the internal pull-up must be disconnected and an external pull-down must be connected to the CPRES1 pin.

An interrupt can be generated if a card is inserted or extracted (see Section “Interrupts”, page 30).

Card Presence Detection for SC2 interface

Figure 13. SC2 presence Input



DC/DC converters

DC/DC A converter

The DC/DC A converter is controlled by VCARD1[1:0], SHUTDOWNA, ICCADJA, STEPREGA, VCARD_OK1 and DEMBOOSTA[1:0] bits.

The DC/DC A converter cannot be switched on while the CPRES1 pin remains inactive. If CPRES1 pin becomes inactive while the DC/DC A converter is operating an automatic shut down sequence of the DC/DC A converter is initiated by the electronics.

A write operation in VCARD1[1:0] (0x01, 0x02, 0x03) starts the DC/DC. When the output voltage remains within the voltage range specified by VCARD1[1:0], the VCARD_OK1 bit is set.

After a deactivation sequence (card extraction, DC/DC output voltage out of range, SHUTDOWNA bit =1...) the DC/DC A converter is automatically stopped.

It is mandatory to switch off the DC/DC A converter before entering in Power-down mode.

The DC/DC A Converter can work in two different modes which are selected by STEPREGA bit:

- Pump Mode (STEPREGA = 0): an external inductance of 10 µH must be connected between pins LIA and VCC. VCC can be higher or lower than CVCC1.
- Regulator mode (STEPREGA = 1): no external inductance is required but VCC must be always higher than CVCC+0.3V.

The current drawn from power supply by the DC/DC A converter is controlled during the startup phase in order to avoid high transient current mainly in Pump Mode which could cause the power supply voltage to drop dramatically. This control is done by means of bits DEMBOOSTA[1:0], which increases progressively the startup current level.

The DC/DCA sensitivity to any overflow current can be modified (20%) by using the ICCADJA bit (SC1_CFG3 register).

Initialization Procedure for DC/DC A converter

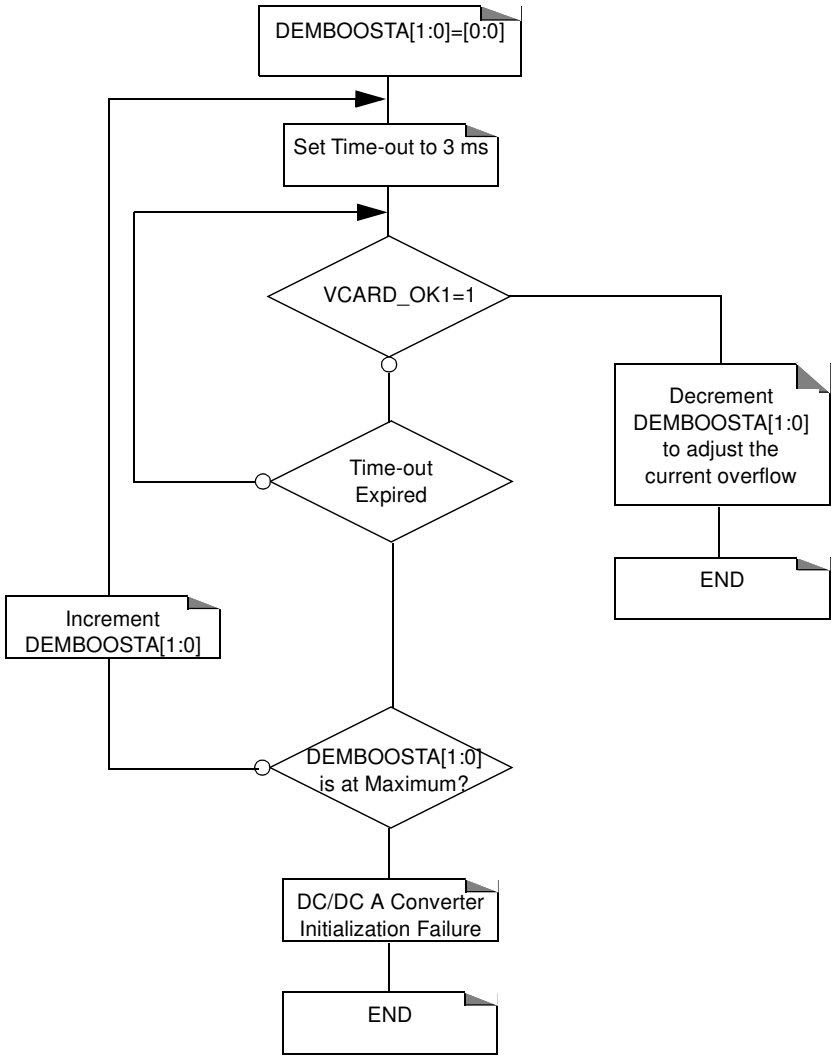
The initialization procedure is described in flow chart:

- Select the CVCC1 level by means of bits VCARD1[1:0] in SC1_CFG0 register,
- Set bits DEMBOOSTA[1:0] in SC1_CFG4 register following the current level control wanted.
- Monitor VCARD_OK1 bit in SC1_STATUS register in order to know when the DC/DC A Converter is ready (CVCC1 voltage has reached the expected level)

While VCC1 remains higher than 3.6V and startup current lower than 30 mA (depending on the load type), the DC/DC A converter should be ready without having to increment DEMBOOSTA[1:0] bits beyond [0:0] level. If at least one of the two conditions are not met (VCC < 3.6V or startup current > 30 mA), it will be necessary to increment the DEMBOOSTA[1:0] bits until the DC/DC converter is ready.

Increment of DEMBOOSTA[1:0] bits increases at the same time the current overflow level in the same proportion as the startup current. So once the DC/DC converter is ready it advised to decrement the DEMBOOSTA[1:0] bits to restore the overflow current to its normal or desired value.

Figure 9. DC/DC A Converter Initialization Procedure



DC/DC B converter

The DC/DC B converter is controlled by DCDCB register.

The DC/DC B converter can be switched on even if CPRES2 pin remains inactive.

A write operation in VDCB[1:0] (0x01, 0x02, 0x03) starts the DC/DC. When the output voltage remains within the voltage range specified by VDCB_OK[1:0], the VDCB_OK bit is set.

The DC/DC B Converter can work in two different modes which are selected by STEPREGB:

- Pump Mode (STEPREGB = 0): an external inductance of 10 µH must be connected between pins LIB and VCC. VCC can be higher or lower than selected voltage.
- Regulator mode (STEPREGB = 1): no external inductance is required but VCC must be always higher than selected voltage+0.3V.

The current drawn from power supply by the DC/DC B converter is controlled during the startup phase in order to avoid high transient current mainly in Pump Mode which could cause the power supply voltage to drop dramatically. This control is done by means of bits DEMBOOSTB[1:0], which increases progressively the startup current level.

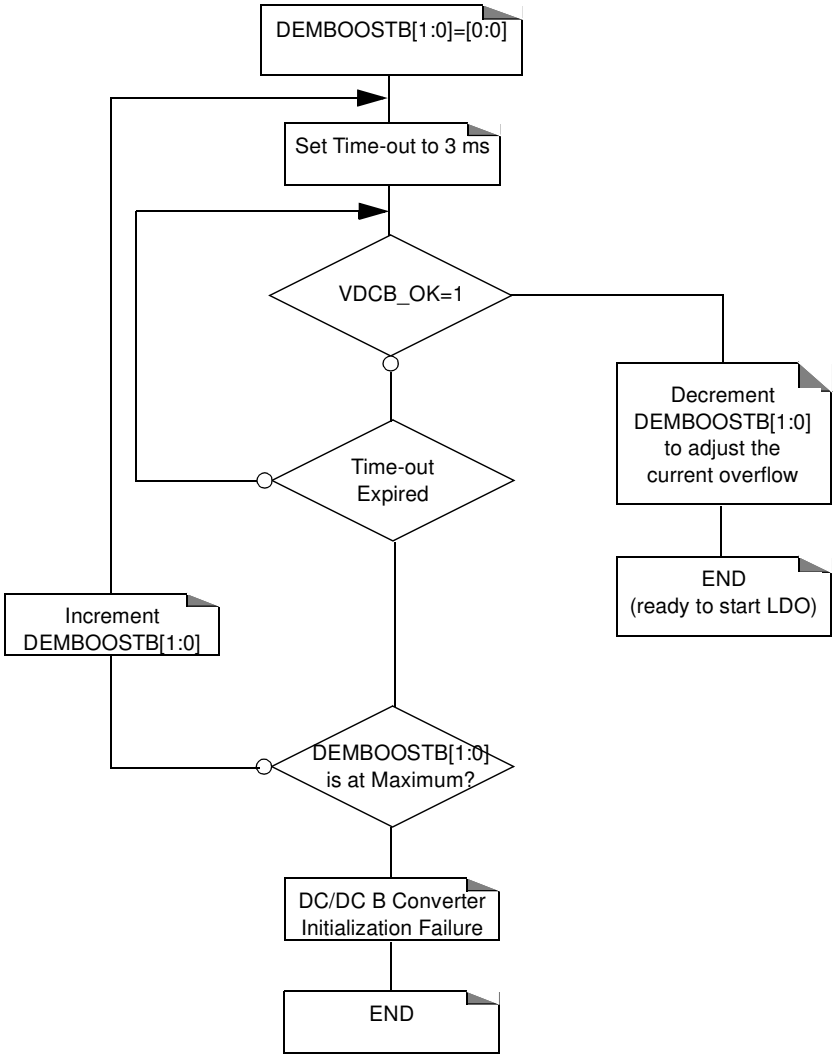
The DC/DCB sensitivity to any overflow current can be modified (20%) by using the ICCADJB bit (DC/DCB register).

Initialization Procedure for DC/DC B converter

The initialization procedure is described in flow chart:

- Select the DC/DC B level by means of bits VDCB[1:0] in DCDCB register,
- Set bits DEMBOOSTB[1:0] in INTERFACEB register following the current level control wanted.
- Monitor VDCB_OK bit in DCDCB register in order to know when the DC/DC B Converter is ready

Figure 10. DC/DC B Converter Initialization Procedure



Increment of DEMBOOSTB[1:0] bits increases at the same time the current overflow level in the same proportion as the startup current. So once the DC/DC B converter is ready it advised to decrement the DEMBOOSTB[1:0] bits to restore the overflow current to its normal or desired value.

LDO initialization Procedure

When the DC/DC B voltage rises the selected voltage (VDCB_OK=1), the card voltage selection on CVCC2, CVCC3, CVCC4 or CVCC5 starts the corresponding LDO.

The CVCC2 card voltage must be started in first (if needed). When the VCARD_OK2 is set, the CVCC3,CVCC4, CVCC5 card voltage are started one after each other (if needed) with the same procedure.

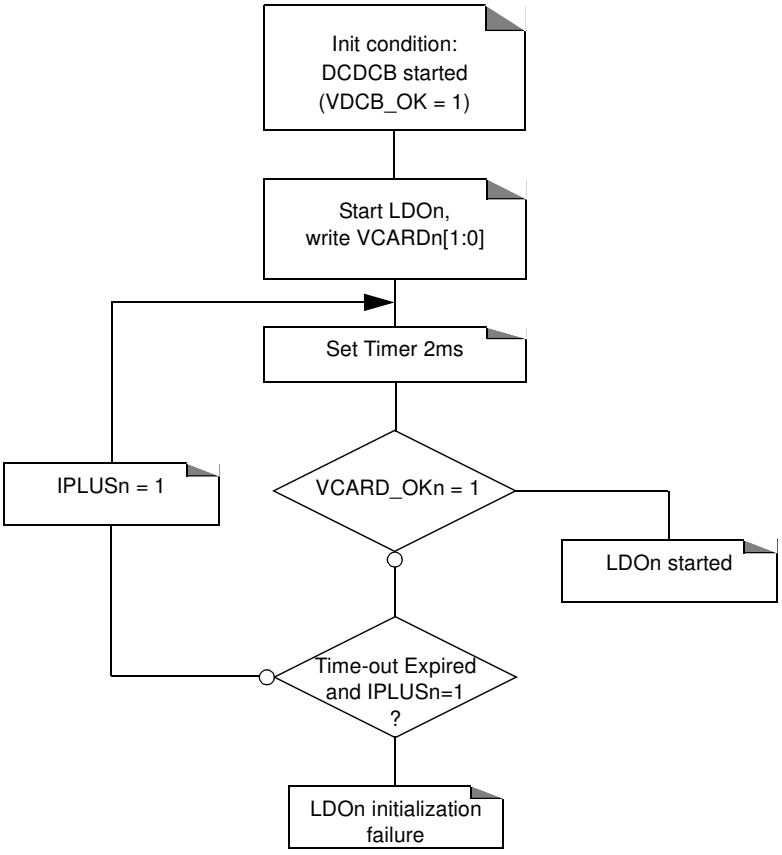
The LDO2, LDO3, LDO4 and LDO5 share the DC/DCB output current, for example 75mA max when CVCCB is pregrammed to 5V. (see Table 62.)

The SC2_FULL bit must be set to use SC2 full interface:

CIO3/CC42 is CC42 and CRST3/CC82 is CC82.

As the power supply of CIO3/CC42 and of CRST3/CC82 is CVCC3, when SC2_FULL=1, CVCC3 = CVCC2. The SC3 interface is disable and LDO3 receives LDO2 command (VCARD3[1:0] = VCARD2[1:0]).

Figure 11. LDOn Initialization Procedure (n = 2, 3, 4, 5)



The LDOn output voltage must be at 0V before to program 1.8V/3V/5V.

Activation Sequence Overview (n=1, 2, 3, 4, 5)

The activation sequence on SC1 is only available if a card is detected on CPRES1 (CARDIN1 bit = 1).

The activation sequence on SC2 is only available if a card is detected on CPRES2 (CARDIN2 bit = 1).

The activation sequence on SC3, SC4, SC5, is only available if DC/DC B is started (VDCB_OK = 1).

The SCn interface starts the activation sequence after a TWI write command in VCARDn[1:0] bits to program the CVCCn voltage.

The SC3, SC4, SC5 interfaces (SIM/SAM interfaces) don't have card presence detector.

After the DC/DC start, the user application will check the ATR to detect if a SIM/SAM is present in the connector.

The automatic reset transition mode (ART=1) controls the CRST pin and check if the first start bit of the ATR respects ISO7816 timings.

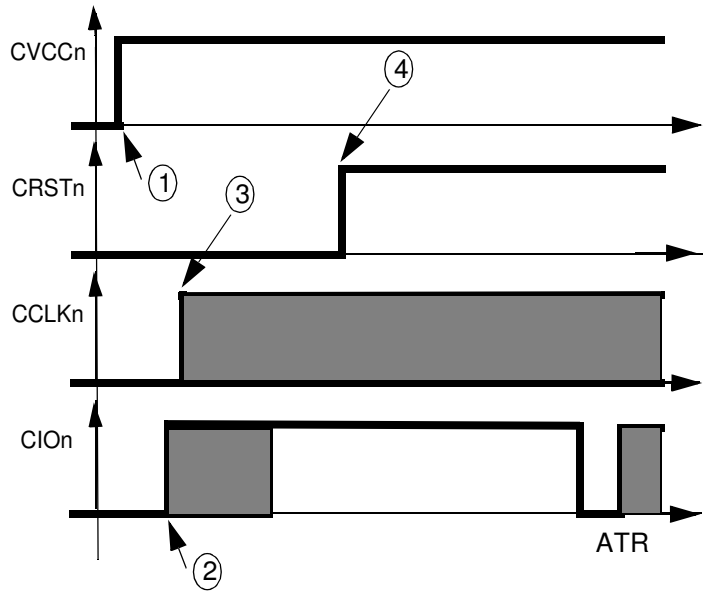
All status bits of an interface (see bits in registers with "This bit is cleared by hardware when this register is read") must be cleared before to start an activation sequence.

Software Activation for SCn interfaces (n=1, 2, 3, 4, 5) with ARTn bit = 0

The activation sequence is controlled by software using TWI commands, depending on the cards to support. For ISO 7816 cards, the following sequence can be applied:

1. Card Voltage is set by software to the required value (VCARDn[1:0] bits). The TWI writing command in VCARDn[1:0] starts the DC/DC (or LDO).
2. Wait of the end of the DC/DC (or LDO) init with a polling on VCARD_OKn bit or wait for $\overline{\text{INT}}$ to go Low. When VCARD_OKn bit is set (by hardware), CARDIOn bit should be set by software.
3. CKSTOPn, IODISn are programmed by software. CKSTOPn bit is reset to have the clock running. IODISn (see IO_SELECT for SC2, SC3, SC4, SC5) is reset to enable the transparent mode on CIOn,CC4n, CC8n.
4. CRSTn pin is controlled by software using CARDRSTn bit.

Figure 14. Software activation without automatic control (ARTn bit = 0)



Note:

– It is assumed that initially VCARDn[1:0], CARDCKn, CARDIOn and CARDRSTn bits are cleared, CKSTOPn and IODISn are set (those bits are further explained in the registers description)

– The user should check the AT83C26 status and possibly resume the activation sequence if one TWI transfer is not acknowledged during the activation sequence.

Software activation for SCn (n=1, 2, 3, 4, 5) interfaces and ARTn bit = 1

The following sequence can be applied:

1. Card Voltage is set by software to the required value (VCARDn1:0] bits in SCn_CFG0 register). This writing starts the DC/DC converter (or LDO).
2. Wait of the end of the DC/DC init (or LDO) with a polling on VCARD_OKn bit or wait for $\overline{\text{INT}}$ to go Low. When VCARD_OKn bit is set (by hardware), CARDIOn bit should be set by software.
3. CKSTOPn, IODISn are programmed by software. CKSTOPn bit is reset to have the clock running. IODISn is reset to enable the transparent mode on CIOn,CC4n, CC8n.
4. CARDRSTn bit is set by software.

Automatic Reset Transition description:

A 16-bit counter starts when CARDRSTn bit is set. It counts card clock cycles. The CRSTn signal is set when the counter reaches the TIMER_MSB and TIMER_LSB value which corresponds to the “tb” time (Figure 15).The counter is reseted when the CRSTn pin is released and it is stopped at the first start bit of the Answer To Request (ATR) on CIOn pin.

The CIOn pin is not checked during the first 200 clock cycles (ta, Figure 15). If the ATR arrives before the counter reaches TIMER_MSB and TIMER_LSB values, the activation sequence fails,