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Features

- **MPEG I/II-Layer 3 Hardwired Decoder**
  - **Stand-alone MP3 Decoder**
  - **48, 44.1, 32, 24, 22.05, 16 kHz Sampling Frequency**
  - **Separated Digital Volume Control on Left and Right Channels (Software Control using 31 Steps)**
  - **Bass, Medium, and Treble Control (31 Steps)**
  - **Bass Boost Sound Effect**
  - **Ancillary Data Extraction**
  - **CRC Error and MPEG Frame Synchronization Indicators**
- **20-bit Stereo Audio DAC**
  - **93 dB SNR Playback Stereo Channel**
  - **32 Ohm/ 20 mW Stereo Headset Drivers**
  - **Stereo Line Level Input, Differential Mono Auxiliary Input**
- **Programmable Audio Output for Interfacing with External Audio System**
  - **I^2S Format Compatible**
- **Mono Audio Power Amplifier**
  - **440mW on 8 Ohms Load**
- **USB Rev 1.1 Controller**
  - **Full Speed Data Transmission**
- **Built-in PLL**
  - **MP3 Audio Clocks**
  - **USB Clock**
- **MultiMediaCard® Interface, Secure Digital Card Interface**
- **Standard Full Duplex UART with Baud Rate Generator**
- **Power Management**
  - **Power-on Reset**
  - **Idle Mode, Power-down Mode**
- **Operating Conditions:**
  - **2.7 to 3V, ±10%, 25 mA Typical Operating at 25°C**
  - **37 mA Typical Operating at 25°C Playing Music on Earphone**
  - **Temperature Range: -40°C to +85°C**
  - **Power Amplifier Supply 3.2V to 5.5V**
- **Packages**
  - **CTBGA 100-pin**

Typical Applications

- MP3-Player
- PDA, Camera, Mobile Phone MP3
- Car Audio/Multimedia MP3
- Home Audio/Multimedia MP3
- Toys
- Industrial Background Music / Ads

Single-Chip MP3 Decoder with Full Audio Interface

AT83SND2CMP3A1
AT83SND2CMP3
AT83SND2CDVX

Rev. 7524D–MP3–07/07

Description

The AT83SND2CMP3 has been developped as a versatile remote controlled MP3 player for very fast MP3 feature implementation into most existing system. It perfectly fits features needed in mobile phones and toys, but can also be used in any portable equipment and in industrial applications.

Audio files and any other data can be stored in a Nand Flash memory or in a removable Flash card such as MultiMediaCard (MMC) or Secure Digital Card (SD). Music collections are very easy to build, as data can be stored using the standard FAT12/16 and FAT32 file system.

Thanks to the USB port, data can be transferred and maintained from and to any computer based on Windows®, Linux® and Mac OS®.

File system is controlled by the AT83SND2CMP3 so the host controller does not have to handle it.

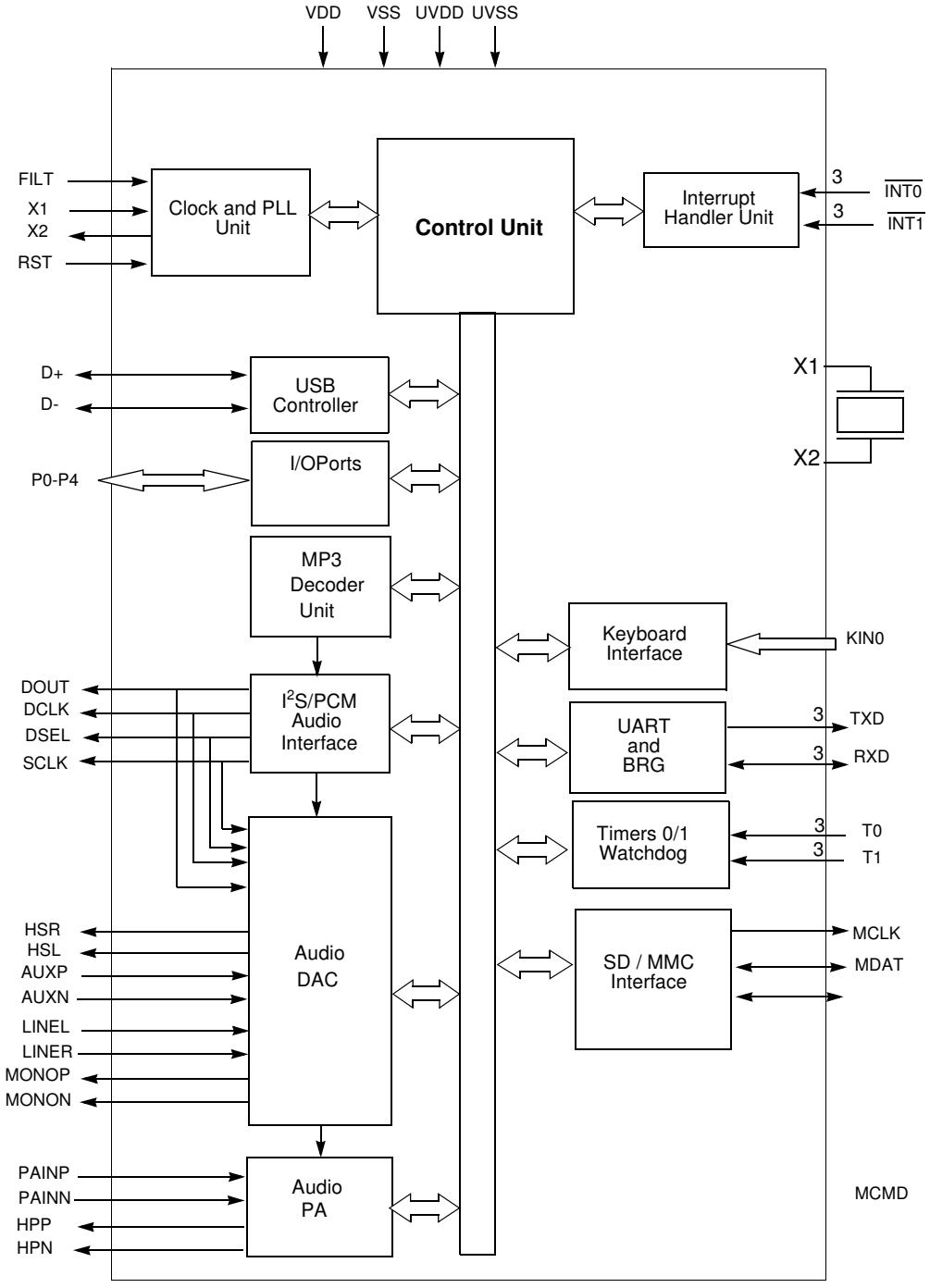
In addition to the USB device port, the MP3 audio system can be connected to any embedded host through a low cost serial link UART. Host controller can fully remote control the MP3 decoder behaviour using a command protocol over the serial link.

File system is controlled by the AT83SND2CMP3 so host controller does not have to handle it.

Files can also be uploaded or dowloaded from host environment to NAND Flash or Flash Card.

Block Diagram

Figure 1. Block Diagram

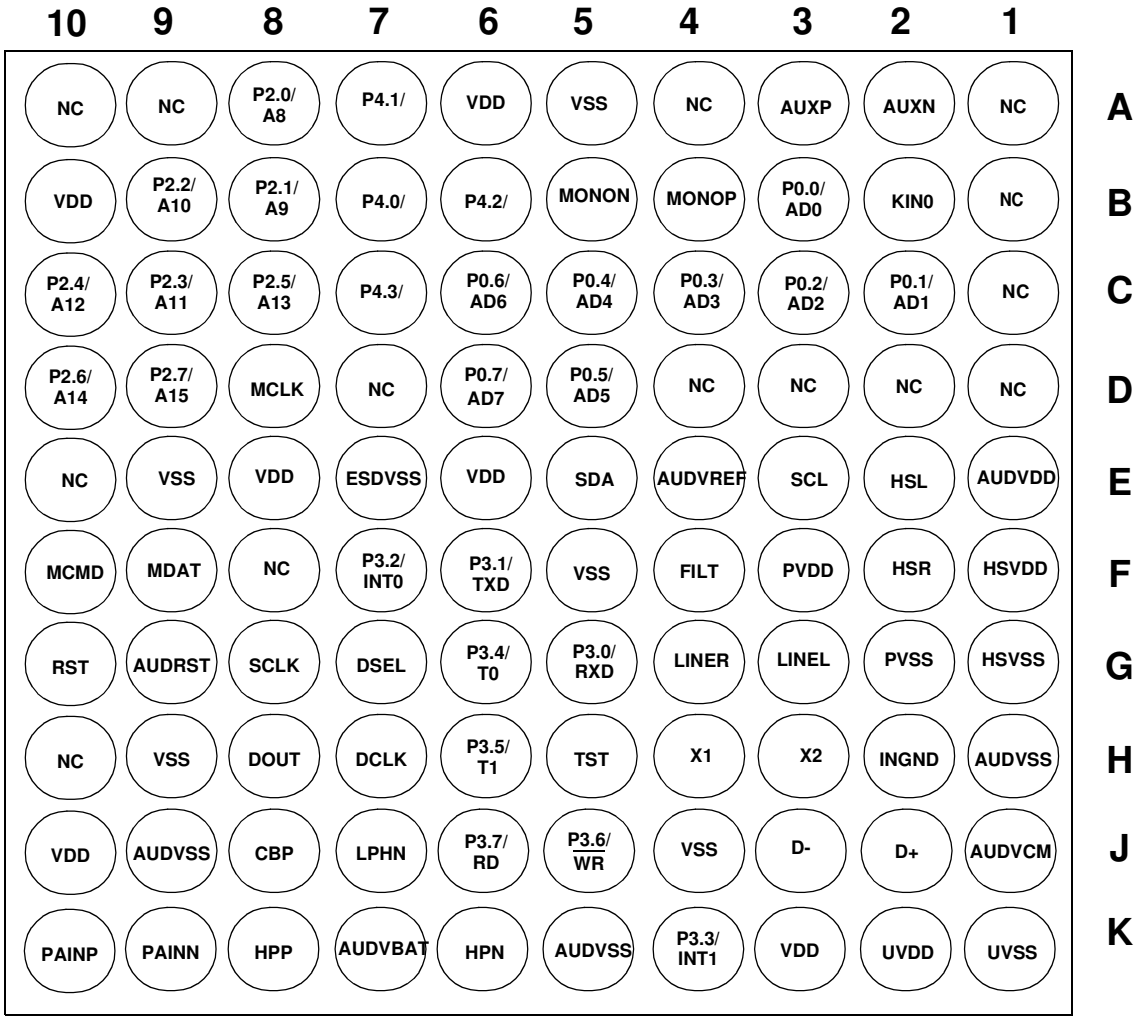


3 Alternate function of Port 3
4 Alternate function of Port 4

Pin Description

Pinouts

Figure 3. AT83SND2CMP3 100-pin BGA Package



1. NC = Do Not Connect

Signals

All the AT83SND2CMP3 signals are detailed by functionality in following tables.

Table 1. Ports Signal Description

Signal Name	Type	Description	Alternate Function
P0.7:0	I/O	**Port 0** P0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high impedance inputs. To avoid any parasitic current consumption, floating P0 inputs must be polarized to V_{DD} or V_{SS}.	AD7:0
P2.7:0	I/O	**Port 2** P2 is an 8-bit bidirectional I/O port with internal pull-ups.	A15:8
P3.7:0	I/O	**Port 3** P3 is an 8-bit bidirectional I/O port with internal pull-ups.	RXD TXD $\overline{INT0}$ $\overline{INT1}$ T0 T1 $\overline{WR}$ $\overline{RD}$
P4.3:0	I/O	**Port 4** P4 is an 8-bit bidirectional I/O port with internal pull-ups.	

Table 2. Clock Signal Description

Signal Name	Type	Description	Alternate Function
X1	I	**Input to the on-chip inverting oscillator amplifier** To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, its output is connected to this pin. X1 is the clock source for internal timing.	-
X2	O	**Output of the on-chip inverting oscillator amplifier** To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, leave X2 unconnected.	-
FILT	I	**PLL Low Pass Filter input** FILT receives the RC network of the PLL low pass filter.	-

Table 3. Timer 0 and Timer 1 Signal Description

Signal Name	Type	Description	Alternate Function
$\overline{INT0}$	I	**Timer 0 Gate Input** $\overline{INT0}$ serves as external run control for timer 0, when selected by GATE0 bit in TCON register. **External Interrupt 0** $\overline{INT0}$ input sets IE0 in the TCON register. If bit IT0 in this register is set, bit IE0 is set by a falling edge on INT0#. If bit IT0 is cleared, bit IE0 is set by a low level on INT0#.	P3.2

Signal Name	Type	Description	Alternate Function
$\overline{INT1}$	I	**Timer 1 Gate Input** $\overline{INT1}$ serves as external run control for timer 1, when selected by GATE1 bit in TCON register. **External Interrupt 1** $\overline{INT1}$ input sets IE1 in the TCON register. If bit IT1 in this register is set, bit IE1 is set by a falling edge on INT1#. If bit IT1 is cleared, bit IE1 is set by a low level on INT1#.	P3.3
T0	I	**Timer 0 External Clock Input** When timer 0 operates as a counter, a falling edge on the T0 pin increments the count.	P3.4
T1	I	**Timer 1 External Clock Input** When timer 1 operates as a counter, a falling edge on the T1 pin increments the count.	P3.5

Table 4. Audio Interface Signal Description

Signal Name	Type	Description	Alternate Function
DCLK	O	**DAC Data Bit Clock**	-
DOUT	O	**DAC Audio Data Output**	-
DSEL	O	**DAC Channel Select Signal** DSEL is the sample rate clock output.	-
SCLK	O	**DAC System Clock** SCLK is the oversampling clock synchronized to the digital audio data (DOUT) and the channel selection signal (DSEL).	-

Table 5. USB Controller Signal Description

Signal Name	Type	Description	Alternate Function
D+	I/O	**USB Positive Data Upstream Port** This pin requires an external 1.5 KΩ pull-up to V_{DD} for full speed operation.	-
D-	I/O	**USB Negative Data Upstream Port**	-

Table 6. MutiMediaCard Interface Signal Description

Signal Name	Type	Description	Alternate Function
MCLK	O	**MMC Clock output** Data or command clock transfer.	-
MCMD	I/O	**MMC Command line** Bidirectional command channel used for card initialization and data transfer commands. To avoid any parasitic current consumption, unused MCMD input must be polarized to V_{DD} or V_{SS}.	-
MDAT	I/O	**MMC Data line** Bidirectional data channel. To avoid any parasitic current consumption, unused MDAT input must be polarized to V_{DD} or V_{SS}.	-

Table 7. UART Signal Description

Signal Name	Type	Description	Alternate Function
RXD	I/O	**Receive Serial Data** RXD sends and receives data in serial I/O mode 0 and receives data in serial I/O modes 1, 2 and 3.	P3.0
TXD	O	**Transmit Serial Data** TXD outputs the shift clock in serial I/O mode 0 and transmits data in serial I/O modes 1, 2 and 3.	P3.1

Table 8. Keypad Interface Signal Description

Signal Name	Type	Description	Alternate Function
KIN0	I	**Keypad Input Line** Holding this pin high or low for 24 oscillator periods triggers a keypad interrupt.	-

Table 9. System Signal Description

Signal Name	Type	Description	Alternate Function
RST	I	**Reset Input** Holding this pin high for 64 oscillator periods while the oscillator is running resets the device. The Port pins are driven to their reset conditions when a voltage lower than V_{IL} is applied, whether or not the oscillator is running. This pin has an internal pull-down resistor which allows the device to be reset by connecting a capacitor between this pin and V_{DD}. Asserting RST when the chip is in Idle mode or Power-Down mode returns the chip to normal operation.	-
$\overline{TST}$	I	**Test Input** Test mode entry signal. This pin must be set to V_{DD}.	-

Table 10. Power Signal Description

Signal Name	Type	Description	Alternate Function
VDD	PWR	**Digital Supply Voltage** Connect these pins to +3V supply voltage.	-
VSS	GND	**Circuit Ground** Connect these pins to ground.	-
PVDD	PWR	**PLL Supply voltage** Connect this pin to +3V supply voltage.	-
PVSS	GND	**PLL Circuit Ground** Connect this pin to ground.	-
UVDD	PWR	**USB Supply Voltage** Connect this pin to +3V supply voltage.	-

Signal Name	Type	Description	Alternate Function
UVSS	GND	**USB Ground** Connect this pin to ground.	-

Table 11. Audio Power Signal Description

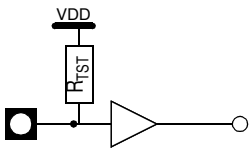
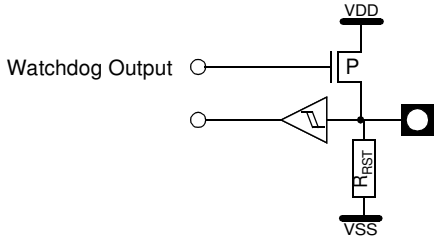
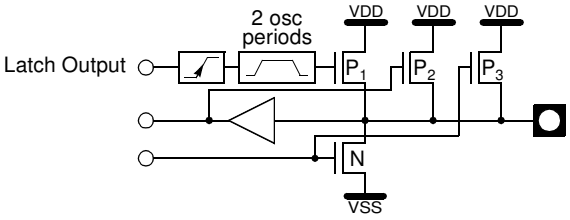
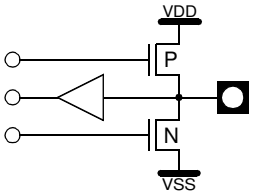
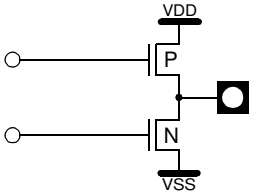
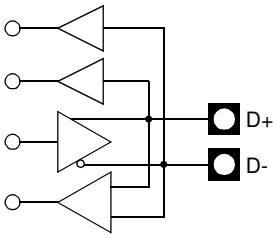
Signal Name	Type	Description	Alternate Function
AUDVDD	PWR	**Audio Digital Supply Voltage**	-
AUDVSS	GND	**Audio Circuit Ground** Connect these pins to ground.	-
ESDVSS	GND	**Audio Analog Circuit Ground for Electrostatic Discharge**. Connect this pin to ground.	-
AUDVREF	PWR	**Audio Voltage Reference pin for decoupling**.	-
HSVDD	PWR	**Headset Driver Power Supply**.	-
HSVSS	GND	**Headset Driver Ground.** Connect this pin to ground.	-
AUDVBAT	PWR	**Audio Amplifier Supply.**	-

Table 12. Stereo Audio Dac and Mono Power Amplifier Signal Description

Signal Name	Type	Description	Alternate Function
LPHN	O	**Low Power Audio Stage Output**	-
HPN	O	**Negative Speaker Output**	-
HPP	O	**Positivie Speaker Output**	-
CBP	O	**Audio Amplifier Common Mode Voltage Decoupling**	-
PAINN	I	**Audio Amplifier Negative Input**	-
PAINP	I	**Audio Amplifier Positive Input**	-
AUDRST	I	**Audio Reset (Active Low)**	-
MONON	O	**Audio Negative Monaural Driver Output**	-
MONOP	O	**Audio Positive Monaural Driver Output**	-
AUXP	I	**Audio Mono Auxiliary Positive Input**	-
AUXN	I	**Audio Mono Auxiliary Negative Input**	-
HSL	O	**Audio Left Channel Headset Driver Output**	-
HSR	O	**Audio Right Channel Headset Driver Output**	-
LINEL	I	**Audio Left Channel Line In**	-
LINER	I	**Audio Right Channel Line In**	-
INGND	I	**Audio Line Signal Ground Pin for decoupling**.	-
AUDVCM	I	**Audio Common Mode reference for decoupling**	-

Internal Pin Structure

Table 13. Detailed Internal Pin Structure

Circuit[1]	Type	Pins
	Input	$\overline{TST}$
	Input/Output	RST
	Input/Output	P3 P4
	Input/Output	P0 MCMD MDAT
	Output	ALE SCLK DCLK DOUT DSEL MCLK
	Input/Output	D+ D-

Notes: 1. For information on resistors value, input/output levels, and drive capability, refer to the DC Characteristics.
2. When the Two Wire controller is enabled, P_3 transistors are disabled allowing pseudo open-drain structure.

Clock Controller

The clock controller is based on an on-chip oscillator feeding an on-chip Phase Lock Loop (PLL). All internal clocks to the peripherals and CPU core are generated by this controller.

Oscillator

The X1 and X2 pins are the input and the output of a single-stage on-chip inverter (see Figure 4) that can be configured with off-chip components such as a Pierce oscillator (see Figure 5). Value of capacitors and crystal characteristics are detailed in the section “DC Characteristics”.

The oscillator outputs three different clocks: a clock for the PLL, a clock for the CPU core, and a clock for the peripherals as shown in Figure 4. These clocks are either enabled or disabled, depending on the power reduction mode as detailed in the section. The peripheral clock is used to generate the Timer 0, Timer 1, MMC, SPI, and Port sampling clocks.

Figure 4. Oscillator Block Diagram and Symbol

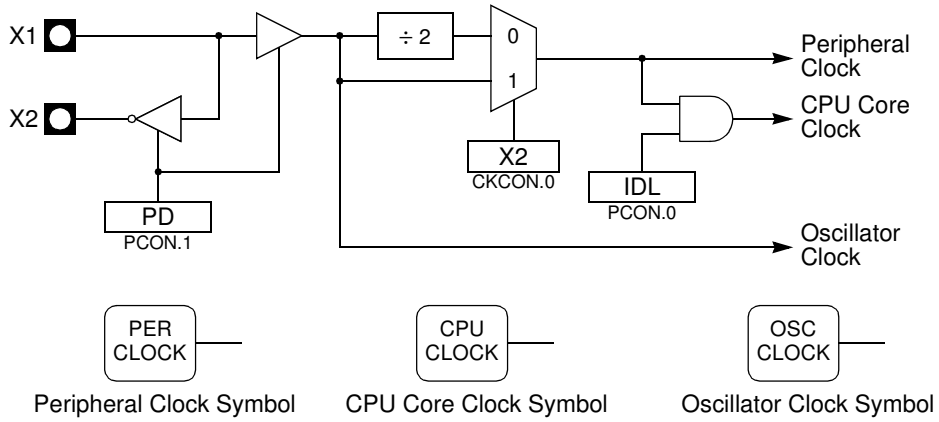
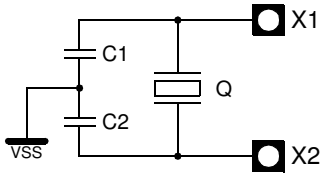


Figure 5. Crystal Connection



PLL

PLL Description

The PLL is used to generate internal high frequency clock (the PLL Clock) synchronized with an external low-frequency (the Oscillator Clock). The PLL clock provides the MP3 decoder, the audio interface, and the USB interface clocks. Figure 6 shows the internal structure of the PLL.

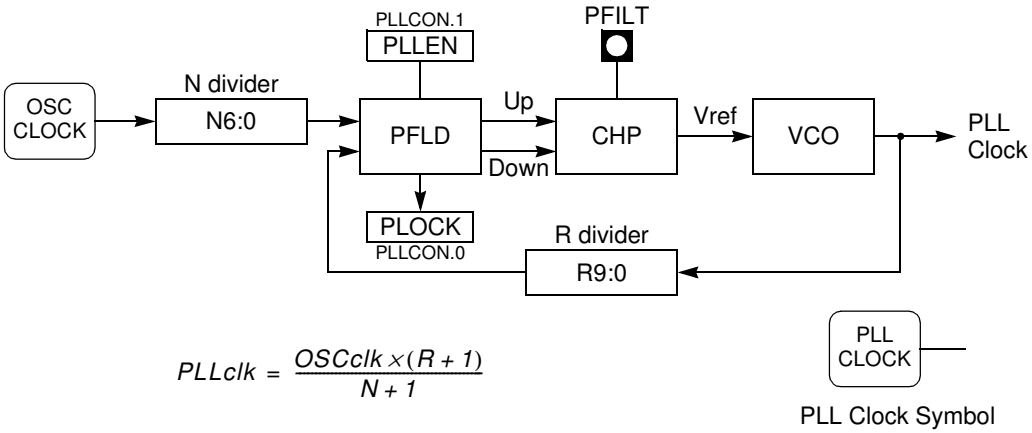
The PFLD block is the Phase Frequency Comparator and Lock Detector. This block makes the comparison between the reference clock coming from the N divider and the reverse clock coming from the R divider and generates some pulses on the Up or Down signal depending on the edge position of the reverse clock. The PLLEN bit in PLLCON register is used to enable the clock generation.

The CHP block is the Charge Pump that generates the voltage reference for the VCO by injecting or extracting charges from the external filter connected on PFILT pin (see

Figure 7). Value of the filter components are detailed in the Section “DC Characteristics”.

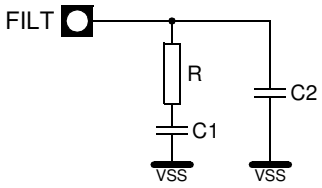
The VCO block is the Voltage Controlled Oscillator controlled by the voltage V_{ref} produced by the charge pump. It generates a square wave signal: the PLL clock.

Figure 6. PLL Block Diagram and Symbol



$$PLLclk = \frac{OSCclk \times (R + 1)}{N + 1}$$

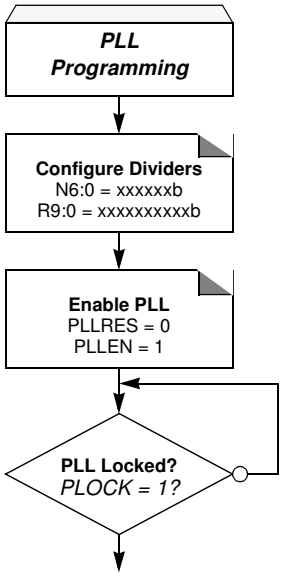
Figure 7. PLL Filter Connection



PLL Programming

The PLL is programmed using the flow shown in Figure 8. The PLL clock frequency will depend on MP3 decoder clock and audio interface clock frequencies.

Figure 8. PLL Programming Flow



MP3 Decoder

The product implements a MPEG I/II audio layer 3 decoder better known as MP3 decoder.

In MPEG I (ISO 11172-3) three layers of compression have been standardized supporting three sampling frequencies: 48, 44.1, and 32 kHz. Among these layers, layer 3 allows highest compression rate of about 12:1 while still maintaining CD audio quality. For example, 3 minutes of CD audio (16-bit PCM, 44.1 kHz) data, which needs about 32M bytes of storage, can be encoded into only 2.7M bytes of MPEG I audio layer 3 data.

In MPEG II (ISO 13818-3), three additional sampling frequencies: 24, 22.05, and 16 kHz are supported for low bit rates applications.

The AT83SND2CMP3 can decode in real-time the MPEG I audio layer 3 encoded data into a PCM audio data, and also supports MPEG II audio layer 3 additional frequencies.

Additional features are supported by the AT83SND2CMP3 MP3 decoder such as volume control, bass, medium, and treble controls, bass boost effect and ancillary data extraction.

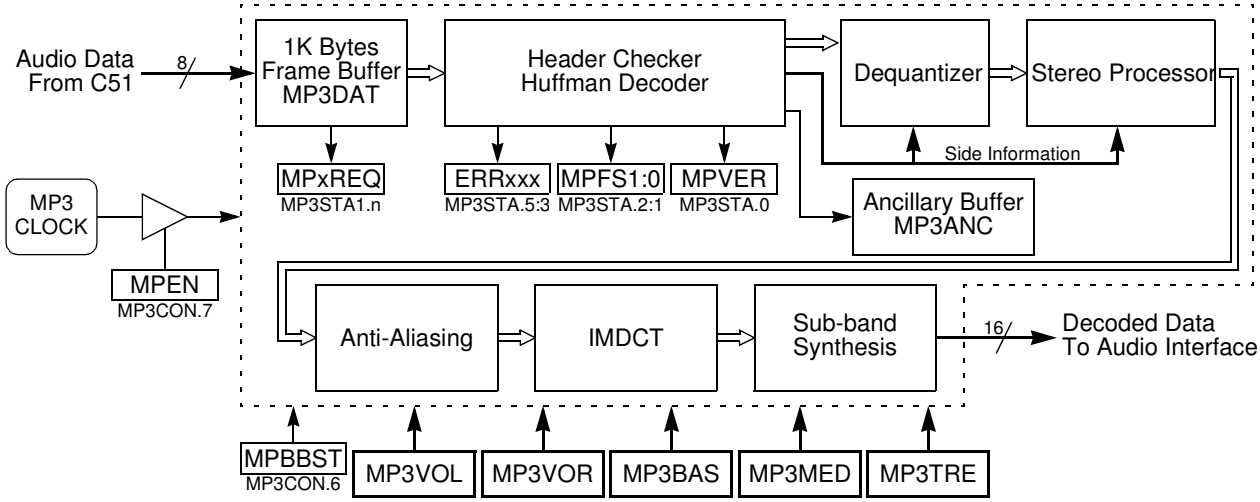
Decoder

Description

The core interfaces to the MP3 decoder through nine special function registers: MP3CON, the MP3 Control register; MP3STA, the MP3 Status register; MP3DAT, the MP3 Data register; MP3ANC, the Ancillary Data register; MP3VOL and MP3VOR, the MP3 Volume Left and Right Control registers; MP3BAS, MP3MED, and MP3TRE, the MP3 Bass, Medium, and Treble Control registers; and MPCLK, the MP3 Clock Divider register.

Figure 9 shows the MP3 decoder block diagram.

Figure 9. MP3 Decoder Block Diagram

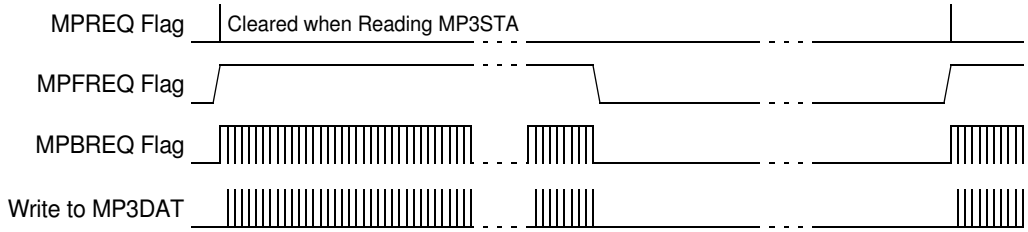


MP3 Data

The MP3 decoder does not start any frame decoding before having a complete frame in its input buffer[1]. In order to manage the load of MP3 data in the frame buffer, a hardware handshake consisting of data request and data acknowledgment is implemented. Each time the MP3 decoder needs MP3 data, it sets the MPREQ, MPFREQ and MPBREQ flags respectively in MP3STA and MP3STA1 registers. MPREQ flag can generate an interrupt if enabled as explained in Section “Interrupt”. The CPU must then load data in the buffer by writing it through MP3DAT register thus acknowledging the previous request. As shown in Figure 10, the MPFREQ flag remains set while data (i.e a frame) is requested by the decoder. It is cleared when no more data is requested and set again when new data are requested. MPBREQ flag toggles at every Byte writing.

Note: 1. The first request after enable, consists in 1024 Bytes of data to fill in the input buffer.

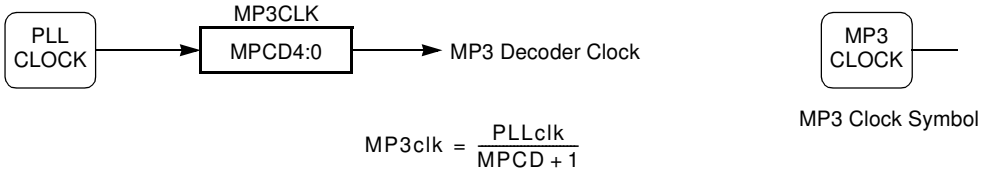
Figure 10. Data Timing Diagram



MP3 Clock

The MP3 decoder clock is generated by division of the PLL clock. The division factor is given by MPCD4:0 bits in MP3CLK register. Figure 11 shows the MP3 decoder clock generator and its calculation formula. The MP3 decoder clock frequency depends only on the incoming MP3 frames.

Figure 11. MP3 Clock Generator and Symbol



$$MP3clk = \frac{PLLclk}{MPCD + 1}$$

As soon as the frame header has been decoded and the MPEG version extracted, the minimum MP3 input frequency must be programmed according to Table 14.

Table 14. MP3 Clock Frequency

MPEG Version	Minimum MP3 Clock (MHz)
I	21
II	10.5

Audio Controls

Volume Control

The MP3 decoder implements volume control on both right and left channels. The MP3VOR and MP3VOL registers allow a 32-step volume control according to Table 15.

Table 15. Volume Control

VOL4:0 or VOR4:0	Volume Gain (dB)
00000	Mute
00001	-33
00010	-27
11110	-1.5
11111	0

Equalization Control

Sound can be adjusted using a 3-band equalizer: a bass band under 750 Hz, a medium band from 750 Hz to 3300 Hz and a treble band over 3300 Hz. The MP3BAS, MP3MED, and MP3TRE registers allow a 32-step gain control in each band according to Table 16.

Table 16. Bass, Medium, Treble Control

BAS4:0 or MED4:0 or TRE4:0	Gain (dB)
00000	- ∞
00001	-14
00010	-10
11110	+1
11111	+1.5

Frame Information

The MP3 frame header contains information on the audio data contained in the frame. These informations is made available in the MP3STA register for you information. MPVER and MPFS1:0 bits allow decoding of the sampling frequency according to Table 17. MPVER bit gives the MPEG version (2 or 1).

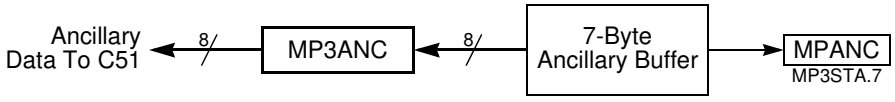
Table 17. MP3 Frame Frequency Sampling

MPVER	MPFS1	MPFS0	Fs (kHz)
0	0	0	22.05 (MPEG II)
0	0	1	24 (MPEG II)
0	1	0	16 (MPEG II)
0	1	1	Reserved
1	0	0	44.1 (MPEG I)
1	0	1	48 (MPEG I)
1	1	0	32 (MPEG I)
1	1	1	Reserved

Ancillary Data

MP3 frames also contain data bits called ancillary data. These data are made available in the MP3ANC register for each frame. As shown in Figure 12, the ancillary data are available by Bytes when MPANC flag in MP3STA register is set. MPANC flag is set when the ancillary buffer is not empty (at least one ancillary data is available) and is cleared only when there is no more ancillary data in the buffer. This flag can generate an interrupt as explained in Section “Interrupt”. When set, software must read all Bytes to empty the ancillary buffer.

Figure 12. Ancillary Data Block Diagram



Audio Output Interface

The product implements an audio output interface allowing the audio bitstream to be output in various formats. It is compatible with right and left justification PCM and I^2S formats and thanks to the on-chip PLL (see Section “Clock Controller”, page 10) allows connection of almost all of the commercial audio DAC families available on the market. The audio bitstream can be from 2 different types:

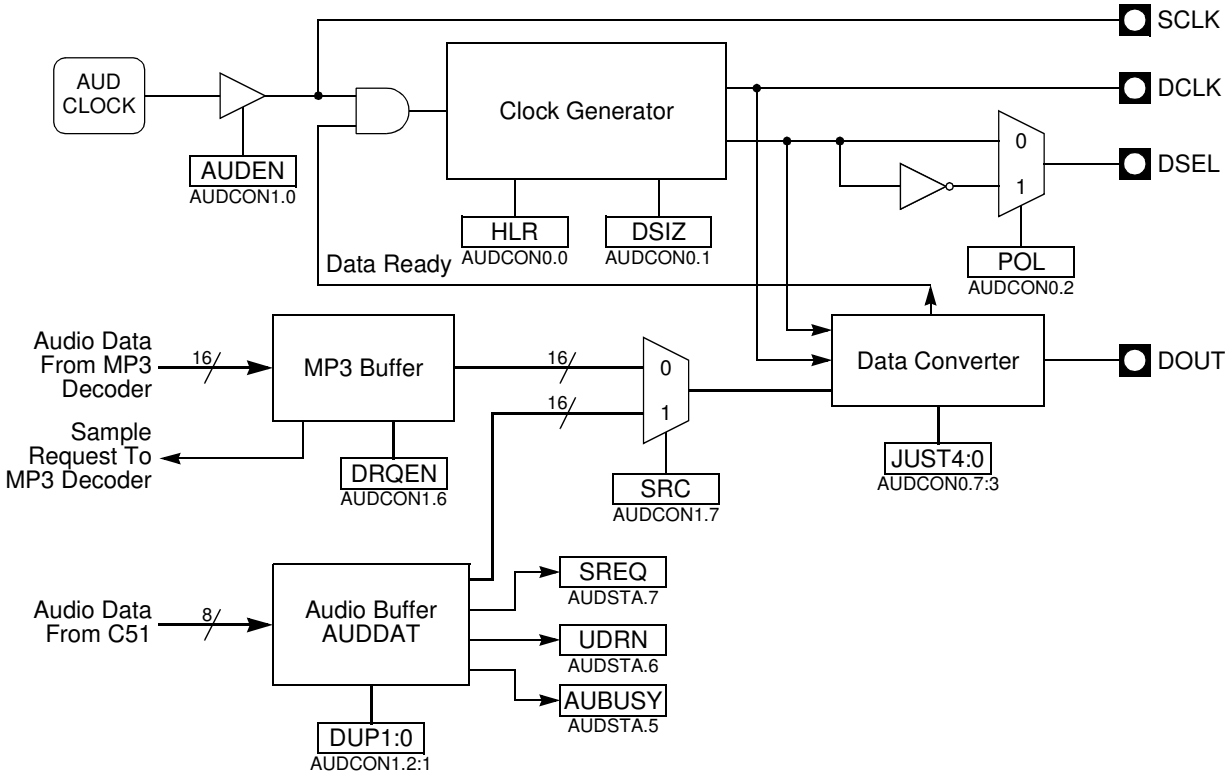
- The MP3 decoded bitstream coming from the MP3 decoder for playing songs.
- The audio bitstream coming from the MCU for outputting voice or sounds.

Description

The control unit core interfaces to the audio interface through five special function registers: AUDCON0 and AUDCON1, the Audio Control registers ; AUDSTA, the Audio Status register; AUDDAT, the Audio Data register; and AUDCLK, the Audio Clock Divider register.

Figure 13 shows the audio interface block diagram, blocks are detailed in the following sections.

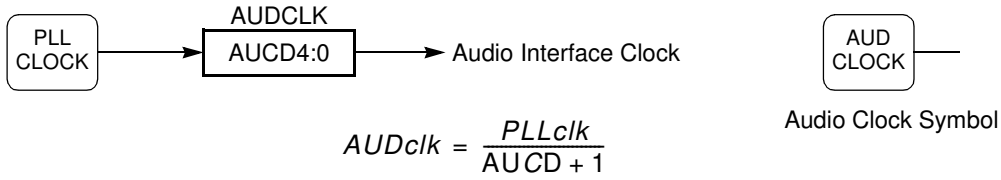
Figure 13. Audio Interface Block Diagram



Clock Generator

The audio interface clock is generated by division of the PLL clock. The division factor is given by AUCD4:0 bits in CLKAUD register. Figure 14 shows the audio interface clock generator and its calculation formula. The audio interface clock frequency depends on the incoming MP3 frames and the audio DAC used.

Figure 14. Audio Clock Generator and Symbol

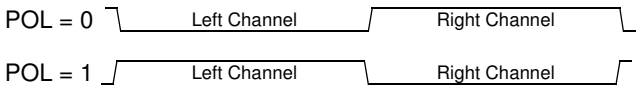


$$AUDclk = \frac{PLLclk}{AUCD + 1}$$

As soon as audio interface is enabled by setting AUDEN bit in AUDCON1 register, the master clock generated by the PLL is output on the SCLK pin which is the DAC system clock. This clock is output at 256 or 384 times the sampling frequency depending on the DAC capabilities. HLR bit in AUDCON0 register must be set according to this rate for properly generating the audio bit clock on the DCLK pin and the word selection clock on the DSEL pin. These clocks are not generated when no data is available at the data converter input.

For DAC compatibility, the bit clock frequency is programmable for outputting 16 bits or 32 bits per channel using the DSIZ bit in AUDCON0 register (see Section "Data Converter", page 17), and the word selection signal is programmable for outputting left channel on low or high level according to POL bit in AUDCON0 register as shown in Figure 15.

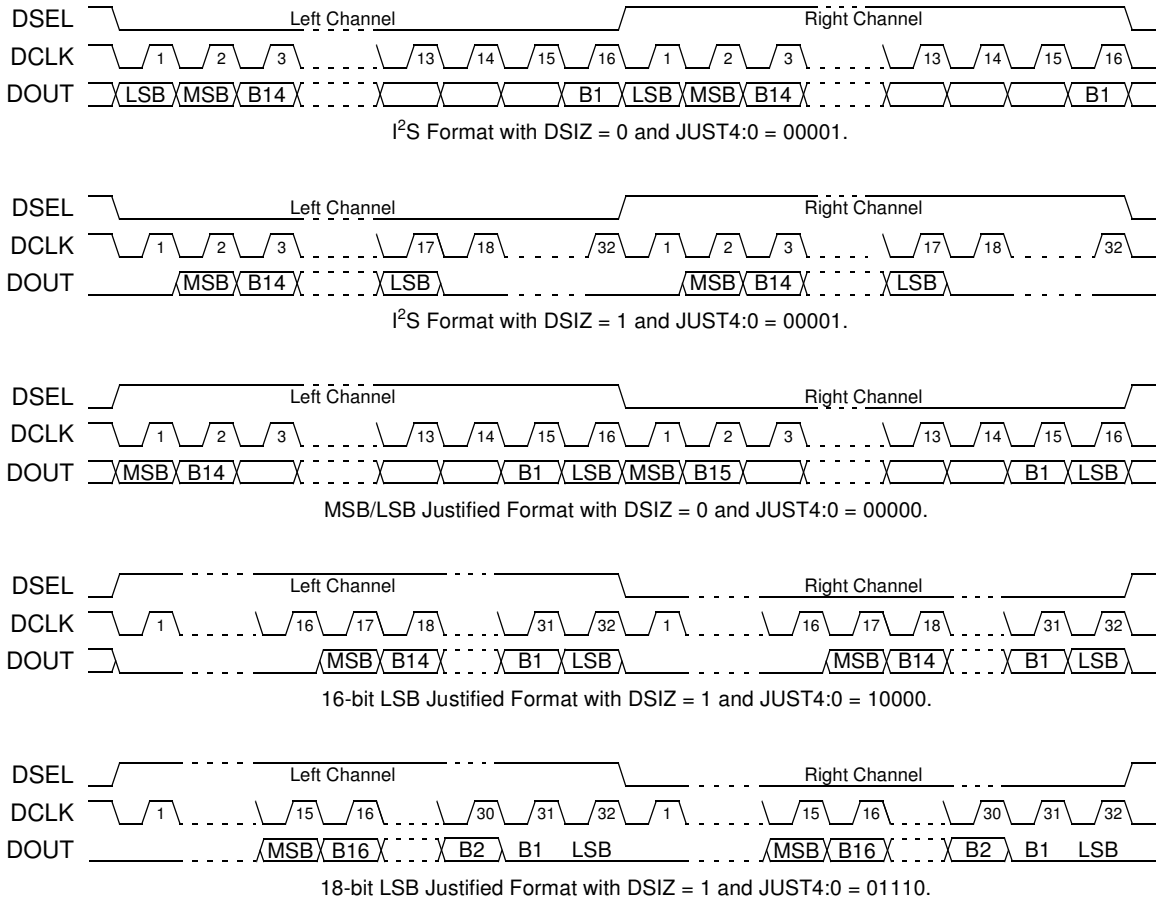
Figure 15. DSEL Output Polarity



Data Converter

The data converter block converts the audio stream input from the 16-bit parallel format to a serial format. For accepting all PCM formats and I^2S format, JUST4:0 bits in AUDCON0 register are used to shift the data output point. As shown in Figure 16, these bits allow MSB justification by setting JUST4:0 = 00000, LSB justification by setting JUST4:0 = 10000, I^2S Justification by setting JUST4:0 = 00001, and more than 16-bit LSB justification by filling the low significant bits with logic 0.

Figure 16. Audio Output Format



The data converter receives its audio stream from 2 sources selected by the SRC bit in AUDCON1 register. When cleared, the audio stream comes from the MP3 decoder (see Section “MP3 Decoder”, page 12) for song playing. When set, the audio stream is coming from the C51 core for voice or sound playing.

As soon as first audio data is input to the data converter, it enables the clock generator for generating the bit and word clocks.

Audio Buffer

In voice or sound playing mode, the audio stream comes from the C51 core through an audio buffer. The data is in 8-bit format and is sampled at 8 kHz. The audio buffer adapts the sample format and rate. The sample format is extended to 16 bits by filling the LSB to 00h. Rate is adapted to the DAC rate by duplicating the data using DUP1:0 bits in AUDCON1 register according to Table 18.

The audio buffer interfaces to the C51 core through three flags: the sample request flag (SREQ in AUDSTA register), the under-run flag (UNDR in AUDSTA register) and the busy flag (AUBUSY in AUDSTA register). SREQ and UNDR can generate an interrupt request as explained in Section "Interrupt Request", page 19. The buffer size is 8 Bytes large. SREQ is set when the samples number switches from 4 to 3 and reset when the samples number switches from 4 to 5; UNDR is set when the buffer becomes empty signaling that the audio interface ran out of samples; and AUBUSY is set when the buffer is full.

Table 18. Sample Duplication Factor

DUP1	DUP0	Factor
0	0	No sample duplication, DAC rate = 8 kHz (C51 rate).
0	1	One sample duplication, DAC rate = 16 kHz (2 x C51 rate).
1	0	2 samples duplication, DAC rate = 32 kHz (4 x C51 rate).
1	1	Three samples duplication, DAC rate = 48 kHz (6 x C51 rate).

MP3 Buffer

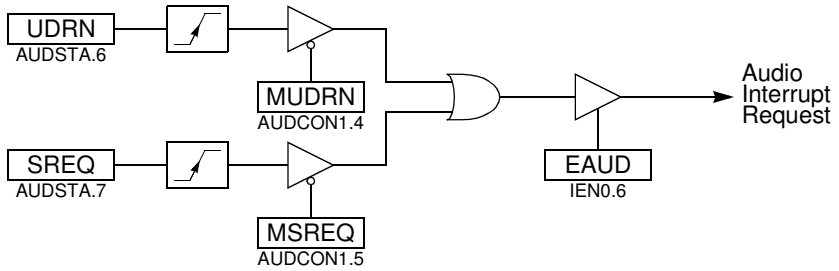
In song playing mode, the audio stream comes from the MP3 decoder through a buffer. The MP3 buffer is used to store the decoded MP3 data and interfaces to the decoder through a 16-bit data input and data request signal. This signal asks for data when the buffer has enough space to receive new data. Data request is conditioned by the DREQEN bit in AUDCON1 register. When set, the buffer requests data to the MP3 decoder. When cleared no more data is requested but data are output until the buffer is empty. This bit can be used to suspend the audio generation (pause mode).

Interrupt Request

The audio interrupt request can be generated by 2 sources when in C51 audio mode: a sample request when SREQ flag in AUDSTA register is set to logic 1, and an under-run condition when UDRN flag in AUDSTA register is set to logic 1. Both sources can be enabled separately by masking one of them using the MSREQ and MUDRN bits in AUDCON1 register. A global enable of the audio interface is provided by setting the EAUD bit in IEN0 register.

The interrupt is requested each time one of the 2 sources is set to one. The source flags are cleared by writing some data in the audio buffer through AUDDAT, but the global audio interrupt flag is cleared by hardware when the interrupt service routine is executed.

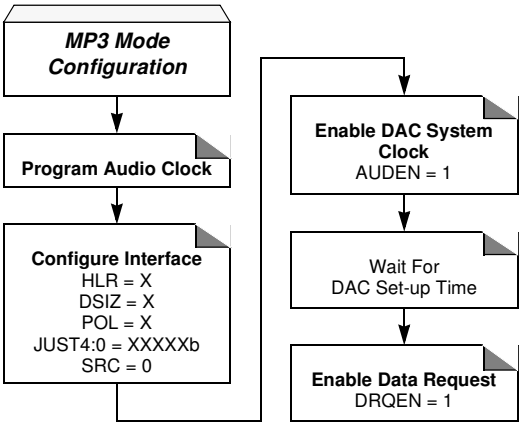
Figure 17. Audio Interface Interrupt System



MP3 Song Playing

In MP3 song playing mode, the operations to do are to configure the PLL and the audio interface according to the DAC selected. The audio clock is programmed to generate the 256·Fs or 384·Fs as explained in Section "Clock Generator", page 17. Figure 18 shows the configuration flow of the audio interface when in MP3 song mode.

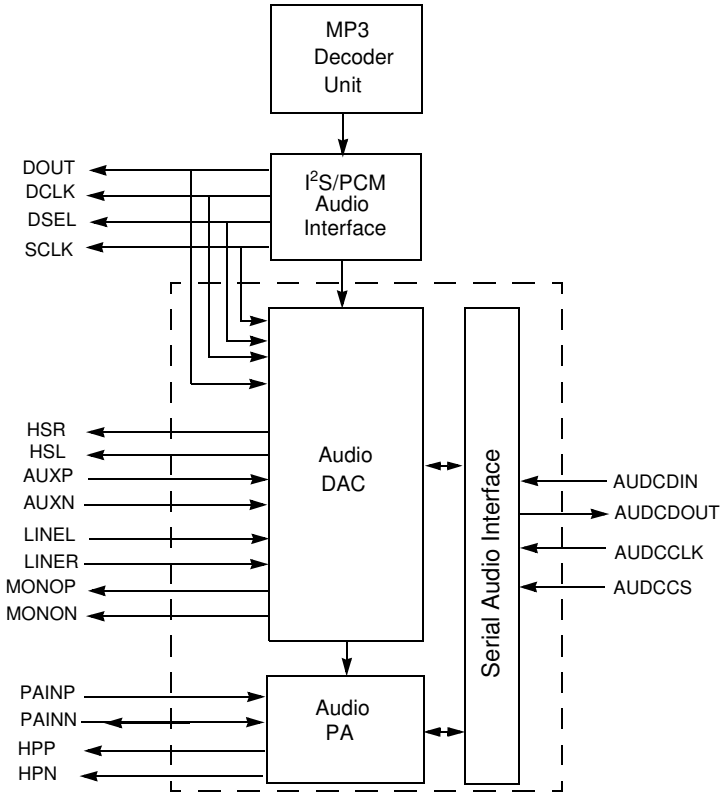
Figure 18. MP3 Mode Audio Configuration Flow



DAC and PA Interface

The AT83SND2CMP3 implements a stereo Audio Digital-to-Analog Converter and Audio Power Amplifier targeted for Li-Ion or Ni-Mh battery powered devices.

Figure 19. Audio Interface Block Diagram



DAC

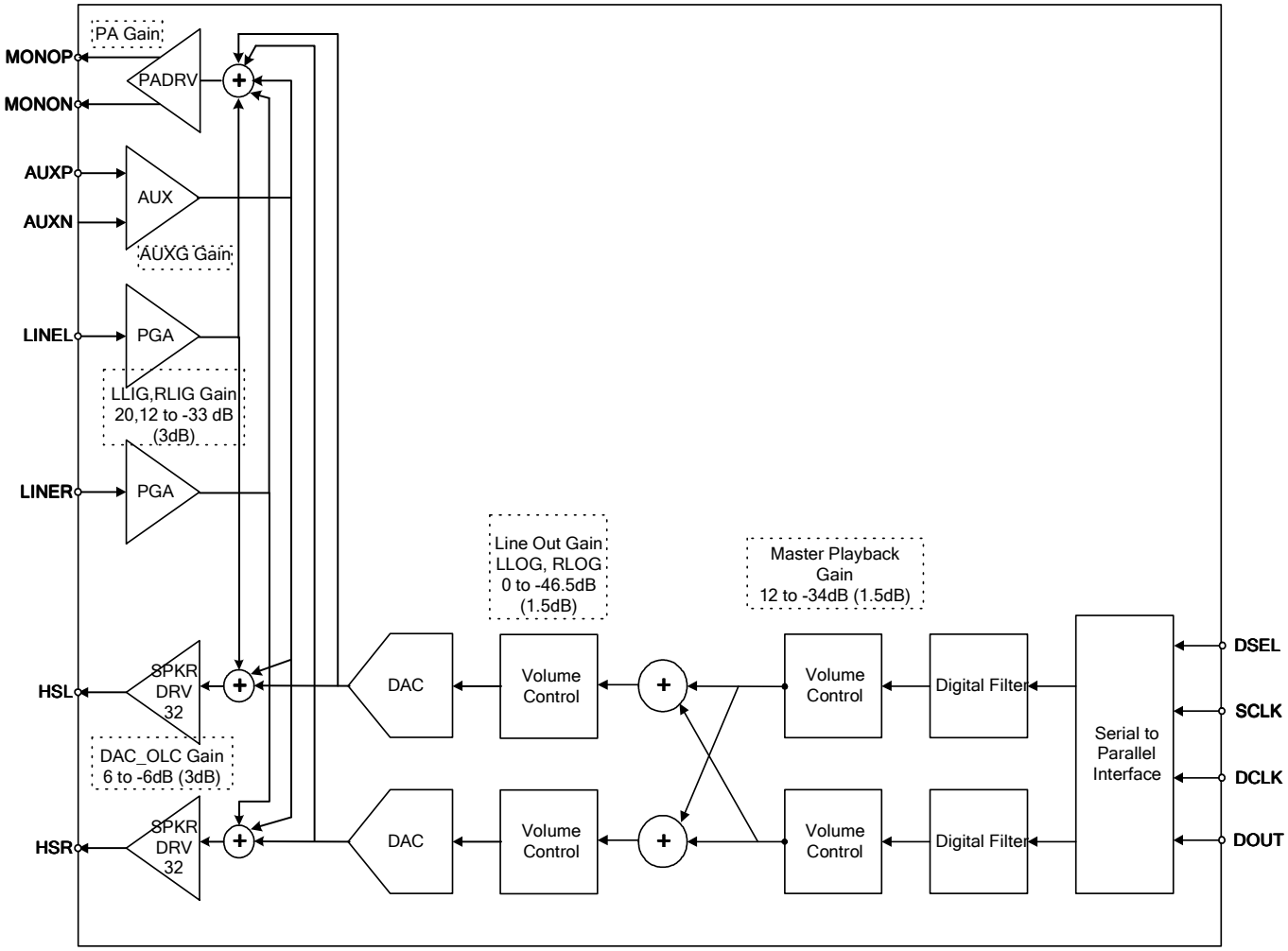
The Stereo DAC section is a complete high performance, stereo, audio digital-to-analog converter delivering 93 dB Dynamic Range. It comprises a multibit sigma-delta modulator with dither, continuous time analog filters and analog output drive circuitry. This architecture provides a high insensitivity to clock jitter. The digital interpolation filter increases the sample rate by a factor of 8 using 3 linear phase half-band filters cascaded, followed by a first order SINC interpolator with a factor of 8. This filter eliminates the images of baseband audio, remaining only the image at 64x the input sample rate, which is eliminated by the analog post filter. Optionally, a dither signal can be added that may reduce eventual noise tones at the output. However, the use of a multibit sigma-delta modulator already provides extremely low noise tones energy.

Master clock is 128 up to 512 times the input data rate allowing choice of input data rate up to 50 kHz, including standard audio rates of 48, 44.1, 32, 16 and 8 kHz. The DAC section is followed by a volume and mute control and can be simultaneously played back directly through a Stereo 32Ω Headset pair of drivers. The Stereo 32Ω Headset pair of drivers also includes a mixer of a LINEL and LINER pair of stereo inputs as well as a differential monaural auxiliary input (line level).

DAC Features

- **20 bit D/A Conversion**
- **72dB Dynamic Range, -75dB THD Stereo line-in or microphone interface with 20dB amplification**
- **93dB Dynamic Range, -80dB THD Stereo D/A conversion**
- **74dB Dynamic Range / -65dB THD for 20mW output power over 32 Ohm loads**
- **Stereo, Mono and Reverse Stereo Mixer**
- **Left/Right speaker short-circuit detection flag**
- **Differential mono auxiliary input amplifier and PA driver**
- **Audio sampling rates (Fs): 16, 22.05, 24, 32, 44.1 and 48 kHz.**

Figure 20. Stereo DAC functional diagram



Digital Signals Timing

Data Interface

To avoid noises at the output, the reset state is maintained until proper synchronism is achieved in the DAC serial interface:

- DSEL
- SCLK
- DCLK
- DOUT

The data interface allows three different data transfer modes:

Figure 21. 20 bit I2S justified mode

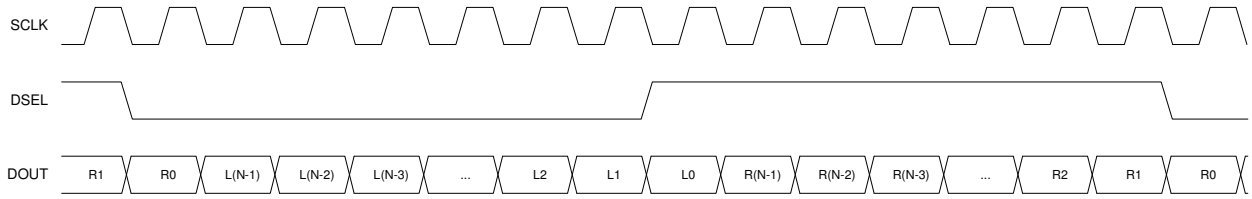


Figure 22. 20 bit MSB justified mode

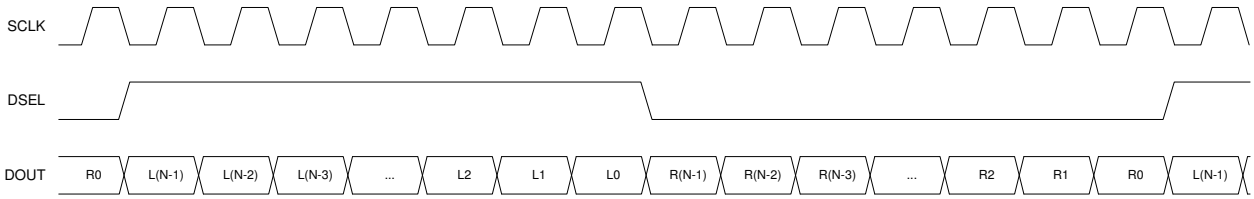
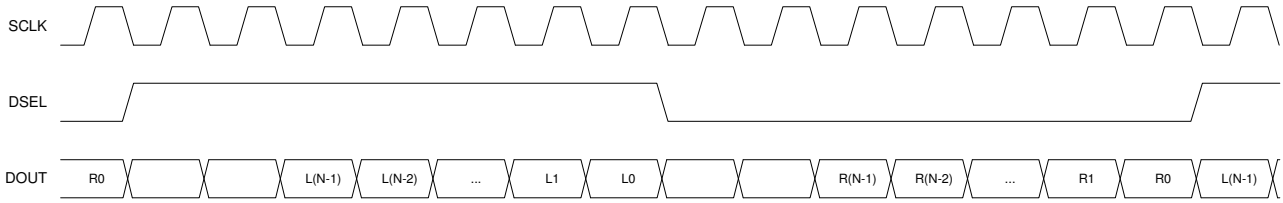


Figure 23. 20 bit LSB justified mode



The selection between modes is done using the DINTSEL 1:0 in DAC_MISC register (Table 40.) according with the following table:

DINTSEL 1:0	Format
00	I2S Justified
01	MSB Justified
1x	LSB Justified

The data interface always works in slave mode. This means that the DSEL and the DCLK signals are provided by microcontroller audio data interface.

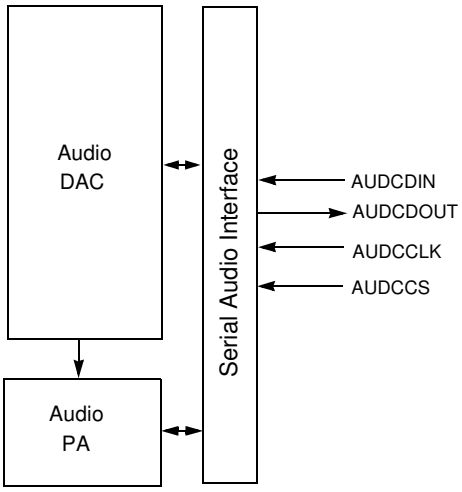
Serial Audio DAC Interface

The serial audio DAC interface is a Synchronous Peripheral Interface (SPI) in slave mode:

- AUDCDIN: is used to transfer data in series from the master to the slave DAC. It is driven by the master.
- AUDCDOUT: is used to transfer data in series from the slave DAC to the master. It is driven by the selected slave DAC.
- Serial Clock (AUDCCLK): it is used to synchronize the data transmission both in and out the devices through the AUDCDIN and AUDCDOUT lines.

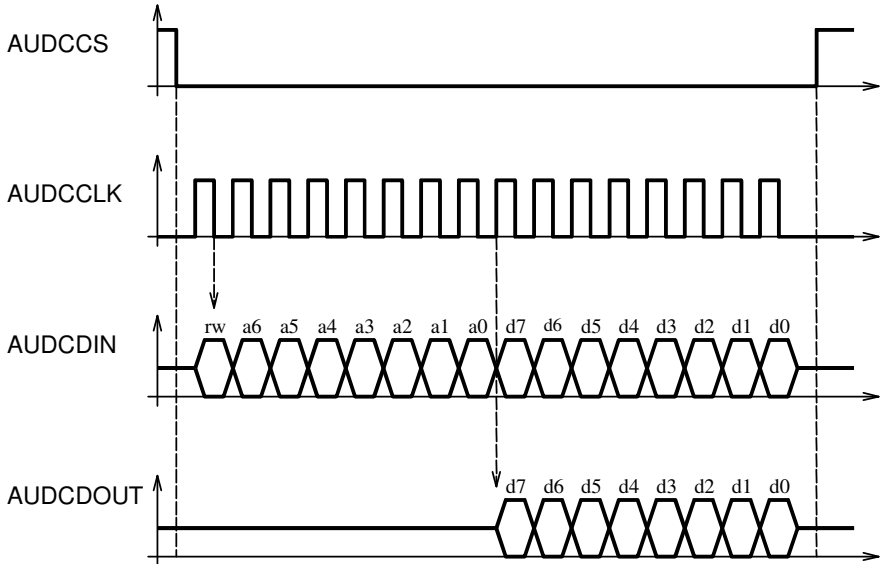
Note: Refer to Table 29. for DAC SPI Interface Description

Figure 24. Serial Audio Interface



Protocol is as following to access DAC registers:

Figure 25. Dac SPI Interface



DAC Interface SPI Protocol

On AUDCDIN, the first bit is a read/write bit. 0 indicates a write operation while 1 is for a read operation. The 7 following bits are used for the register address and the 8 last ones are the write data. For both address and data, the most significant bit is the first one.

In case of a read operation, AUDCDOUT provides the contents of the read register, MSB first.

The transfer is enabled by the AUDCCS signal active low. The interface is resetted at every rising edge of AUDCCS in order to come back to an idle state, even if the transfer does not succeed. The DAC Interface SPI is synchronized with the serial clock AUDC-

CLK. Falling edge latches AUDCDIN input and rising edge shifts AUDCDOUT output bits.

Note that the DLCK must run during any DAC SPI interface access (read or write).

Figure 26. DAC SPI Interface Timings

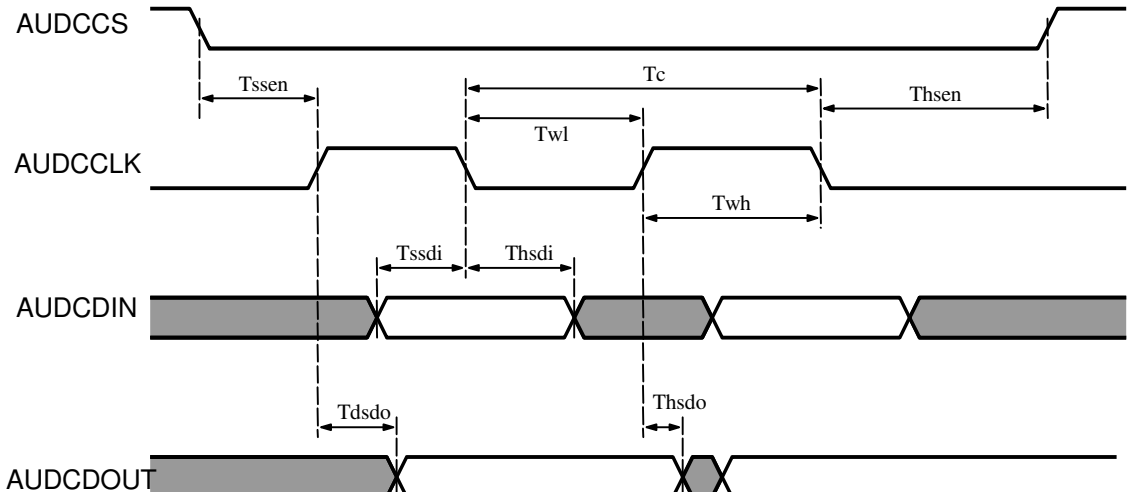


Table 19. Dac SPI Interface Timings

Timing parameter	Description	Min	Max
Tc	AUDCCLK min period	150 ns	-
Twl	AUDCCLK min pulse width low	50 ns	-
Twh	AUDCCLK min pulse width high	50 ns	-
Tssen	Setup time AUDCCS falling to AUDCCLK rising	50 ns	-
Thsen	Hold time AUDCCLK falling to AUDCCS rising	50 ns	-
Tssdi	Setup time AUDCDIN valid to AUDCCLK falling	20 ns	-
Thsdi	Hold time AUDCCLK falling to AUDCDIN not valid	20 ns	-
Tdsdo	Delay time AUDCCLK rising to AUDCDOUT valid	-	20 ns
Thsdo	Hold time AUDCCLK rising to AUDCDOUT not valid	0 ns	-