Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

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Features

- Audio Processor
  - Proprietary Digital Signal Processor
  - MP3 and WMA Decoders
  - WAV PCM and ADPCM Decoder/Coder with AGC
  - JPEG decoder
  - Video Animation (MTV up to 16fps)
- Audio Codec
  - 16-bit Stereo D/A Converters(3)
  - Headphone Amplifier with Analog Volume Control(3)
  - Microphone Pre-Amplifier with Bias Control
  - 16-bit Mono A/D Converter: Microphone or Line Inputs Recording
  - Stereo Lines Input for FM Playback or Mono Recording
  - 3-band EQ and Bass Boost and 3D Sound Effects
  - Graphical EQ
- Digital Audio DAC Interface
  - PCM / I^2S Format Compatible
- USB Rev 2.0 Controller
  - 7 Endpoints, Multiple Enumeration
  - High Speed Mode (480 Mbps)
  - Full Speed Mode (12 Mbps)
  - On The Go Full Speed Mode
- File Management
  - Fat 12, 16, 32 Management
  - Multiple Drive Management: Nand Flash, Card, U-Disk...
  - Multiple Folders and Sub-Folders (user defined)
  - Multiple File Read and Write
  - Playlist and Lyrics Support
- Data Flow Controller
  - 16-bit Multimedia Bus with 2 DMA Channels for high speed transfer with USB
- Nand Flash Controller
  - Multiple Nand as 1 Drive, Support All Page Size
  - Read up to 10MB/s, Write up to 8MB/s
  - Built-in ECC and Hardware Write Protection
- MultiMediaCard® Controller
  - MultiMediaCard 1-bit / 4-bits Modes (V4 compatible)
  - Secure Digital Card 1-bit / 4-bit Modes
- Man Machine Interface
  - Glueless Generic LCD Interface
  - Keyboard Interface
  - FM Tuner Input and Control including RDS
  - PSI I80 Slave Interface (EBI Compatible) up to 6Mbytes/s
  - SPI Master and Slave Modes
  - Full Duplex UART with Baud Rate Generator up to 6 Mbit/s (Rx, Tx, RTS, CTS)
- Control Processor
  - Enhanced 8-bit MCU C51 Core (F_{MAX} = 24 MHz)
  - 64K Bytes of Internal RAM for application code and data
  - Boot ROM Memory: Secured Nand Flash Boot Strap (standard), USB Boot Loader
  - Two 16-bit Timers/Counters: Hardware Watchdog Timer
  - In-System and In-Application Programming
- Power Management
  - 1.8V 40 mA Single AAA or AA Battery Powered(4)
  - Direct USB V_{BUS} Supply
  - 3V or 1.8V - 50 mA Regulator Output
  - Battery Voltage Monitoring
  - Power-on Reset, Idle, Power-Down, Power-Off Modes
  - Software Programmable MCU Clock
- Operating Conditions
  - Supply 1.8V to 5V for all Product range, plus 0.9V to 1.8V(4)

Single-Chip Digital Audio Decoder - Encoder with USB 2.0 Interface

AT85C51SND3B

Preliminary

7632D–MP3–01/07

  - **25 mA Typical Operating at 25°C (estimation to be confirmed)**
  - **Temperature Range: -40°C to +85°C**
- **Packages**
  - **LQFP100, BGA100, Dice**

Notes: 1. See Ordering Information
2. AT85C51SND3B1 & AT85C51SND3B2 only
3. AT85C51SND3B2 only

Description

Digital Music Players, Mobile Phones need ready to use low-cost solutions for very fast time to market. The AT85C51SND3B with associated firmware embeds in a single chip all features, hardware and software, for Digital Music Players, Mobile Phones and Industrial or Toys applications: MP3 decoder, WMA decoder, Display interface, serial interface, parallel interface, USB high speed and USB host.

Close to a plug and play solution for most applications, the AT85C51SND3B drastically reduces system development for the best time to market. The AT85C51SND3B handles full file system management with Nand Flash and Flash Cards, including full detection and operation of a thumb drive. The AT85C51SND3Bx is used either as a master controller, or as a slave controller interfacing easily with most of the base-band or host processors available on the market.

The AT85C51SND3B includes Power Management with: 5V USB V_{BUS} direct supply, 2.7V to 3.6V supply, 1.8V supply or alkaline battery supply (0.9V to 1.8V). External Nand Flash or Flash Card can be supplied by the AT85C51SND3B at 1.8V or 3V.

The AT85C51SND3B supports many applications including: mobile phones, music players, portable navigation, car audio, music in shopping centers, applications including MMC/SD Flash Cards in Industrial applications.

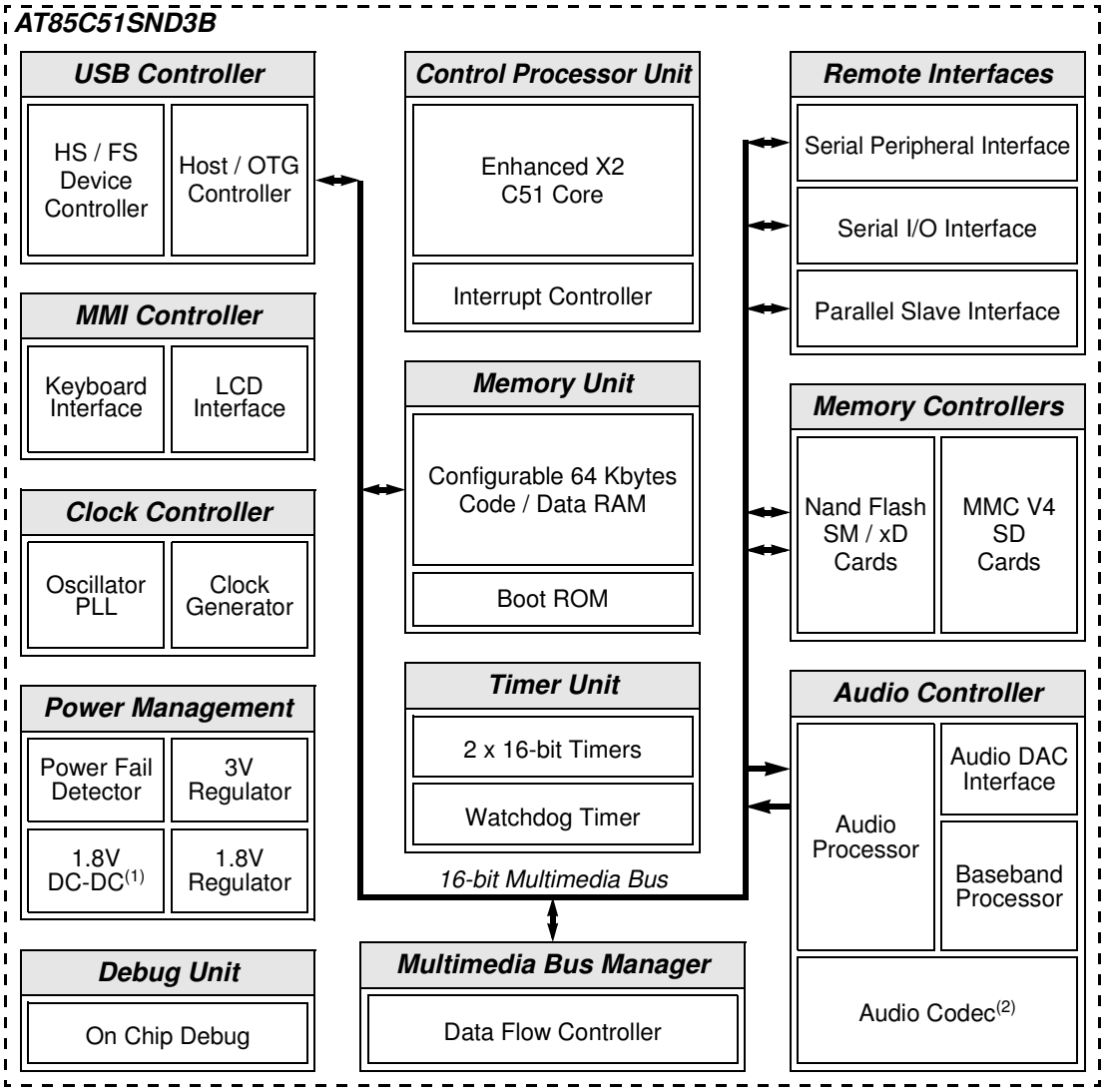
To facilitate custom applications with the AT85C51SND3B, a development kit AT85DVK-07 and a reference design AT85RFD-07 are available with hardware and firmware database.

Key Features

- Firmware to support
  - MP3
  - WMA
  - ADPCM/WAV voice or line recording
  - JPEG Decoder
- Audio Codec
  - Internal DAC
  - FM inputs
- Memory Support
  - Up to 4x Nand-Flash
  - SD/MMC cards
- USB
  - High Speed, Full Speed
  - OTG (reduced Host)

Block Diagram

Figure 1. AT85C51SND3B Block Diagram



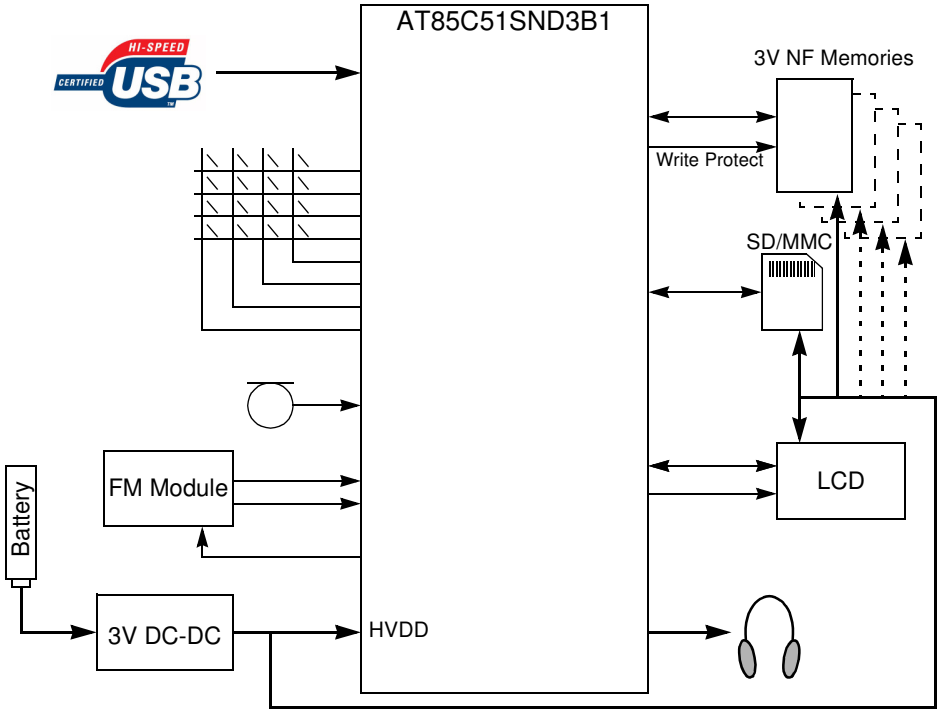
Notes: 1. AT85C51SND3B2 only
2. AT85C51SND3B1 & AT85C51SND3B2 only

Application Information

The AT85C51SND3B derivatives allow design of 2 typical applications which differentiate by the power supply voltage:

- The Very Low Voltage System
  The player operates at 1.8V and allows very low power consumption.
- The Low Voltage System
  The player operates at 3V and allows low power consumption.

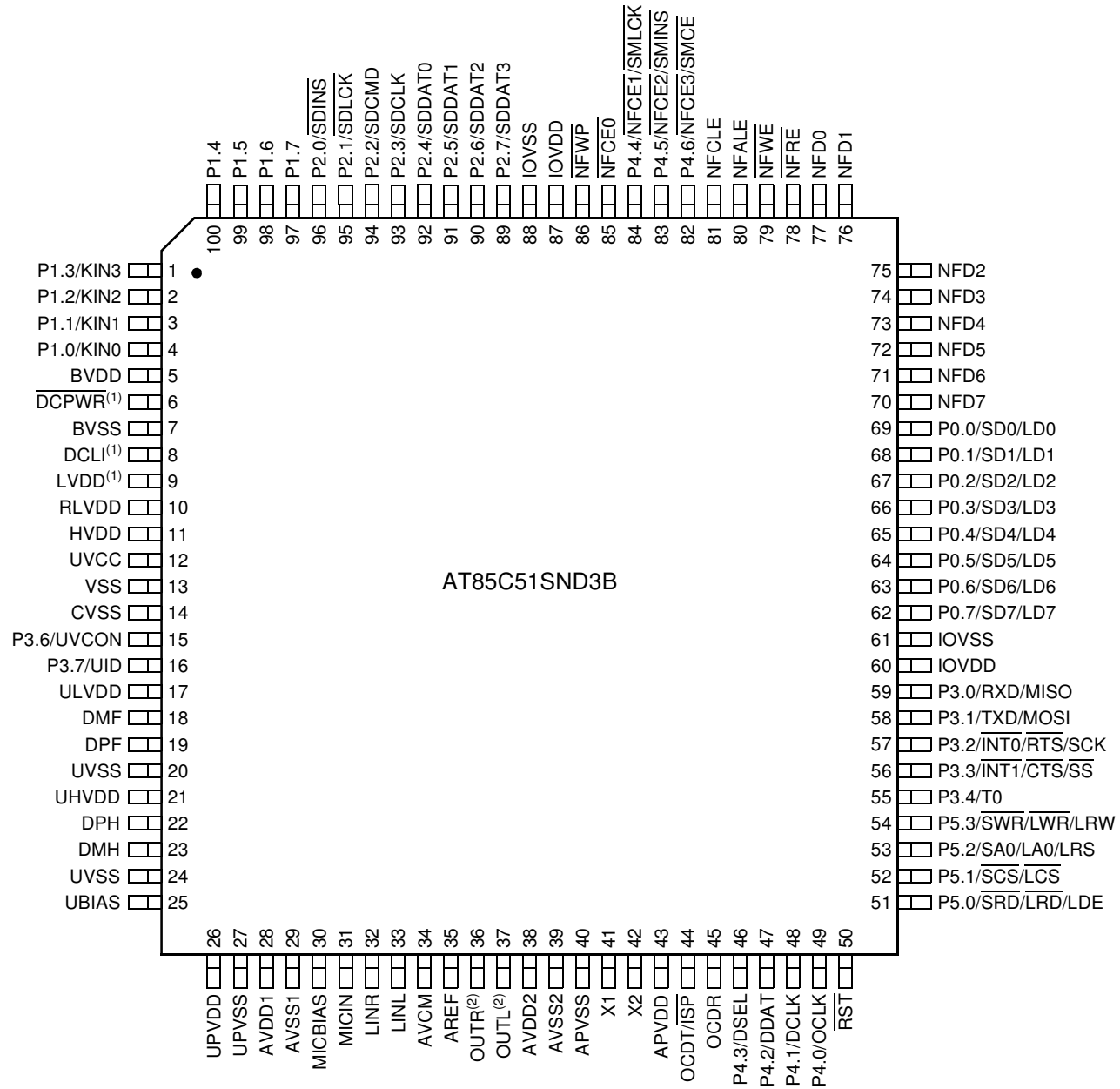
Figure 2. Typical Low Voltage 3V Application



Pin Description

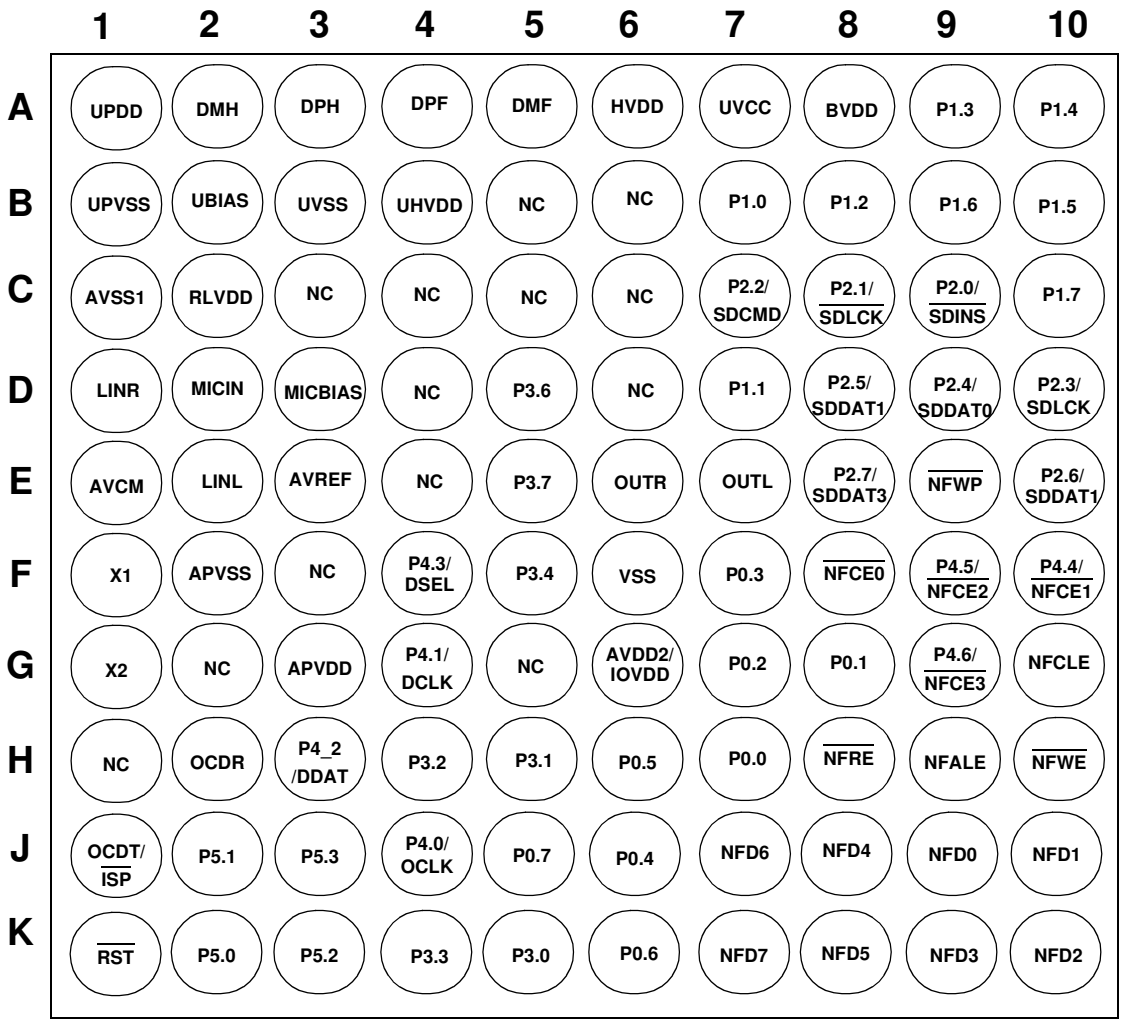
Pinouts

Figure 3. AT85C51SND3B 100-pin QFP Package



Notes: 1. Leave these pins unconnected for AT85C51SND3B0 & AT85C51SND3B1 products
2. Leave these pins unconnected for AT85C51SND3B0 product

Figure 4. AT85C51SND3B 100-pin BGA Package (no ADC)



Signals Description

System

Table 1. System Signal Description

Signal Name	Type	Description	Alternate Function
$\overline{RST}$	I/O	**Reset Input** Holding this pin low for 64 oscillator periods while the oscillator is running resets the device. The Port pins are driven to their reset conditions when a voltage lower than V_{IL} is applied, whether or not the oscillator is running. This pin has an internal pull-up resistor (R_{RST}) which allows the device to be reset by connecting a capacitor between this pin and V_{SS}. Asserting $\overline{RST}$ when the chip is in Idle mode or Power-Down mode returns the chip to normal operation. In order to reset external components connected to the $\overline{RST}$ line a low level 96-clock period pulse is generated when the watchdog timer reaches its time-out period.	-
$\overline{ISP}$	I	**In System Programming** Assert this pin during reset phase to enter the in system programming mode.	OCDT

Table 2. Ports Signal Description

Signal Name	Type	Description	Alternate Function
P0.7:0	I/O	**Port 0** P0 is an 8-bit bidirectional I/O port with internal pull-ups.	LD7:0
P1.7:0	I/O	**Port 1** P1 is an 8-bit bidirectional I/O port with internal pull-ups.	KIN3:0
P2.7:0	I/O	**Port 2** P2 is an 8-bit bidirectional I/O port with internal pull-ups.	$\overline{SDINS}$ $\overline{SDLCK}$ SDCMD SDCLK SDDAT3:0
P3.4:0 P3.7:6	I/O	**Port 3** P3 is a 7-bit bidirectional I/O port with internal pull-ups.	RXD MISO TXD MOSI $\overline{INT0}$ $\overline{RTS}$ SCK $\overline{INT1}$ $\overline{CTS}$ $\overline{SS}$ T0 UVCON UID

Signal Name	Type	Description	Alternate Function
P4.6:0	I/O	**Port 4** P4 is a 7-bit bidirectional I/O port with internal pull-ups.	OCLK DCLK DDAT DSEL $\overline{\text{NFCE1}}$/$\overline{\text{SMLCK}}$ $\overline{\text{NFCE2}}$/$\overline{\text{SMINS}}$ $\overline{\text{NFCE3}}$/$\overline{\text{SMCE}}$
P5.3:0	I/O	**Port 5** P5 is a 4-bit bidirectional I/O port with internal pull-ups.	$\overline{\text{LRD}}$/LDE $\overline{\text{SDR}}$ $\overline{\text{LCS}}$ $\overline{\text{SCS}}$ LA0/LRS $\overline{\text{SA0}}$ $\overline{\text{LWR}}$/LRW $\overline{\text{SWR}}$

Table 3. Timer 0 and Timer 1 Signal Description

Signal Name	Type	Description	Alternate Function
$\overline{\text{INT0}}$	I	**Timer 0 Gate Input** $\overline{\text{INT0}}$ serves as external run control for timer 0, when selected by GATE0 bit in TCON register. **External Interrupt 0** $\overline{\text{INT0}}$ input sets IE0 in the TCON register. If bit IT0 in this register is set, bit IE0 is set by a falling edge on $\overline{\text{INT0}}$. If bit IT0 is cleared, bit IE0 is set by a low level on $\overline{\text{INT0}}$.	P3.2 $\overline{\text{RTS}}$ SCK
$\overline{\text{INT1}}$	I	**Timer 1 Gate Input** $\overline{\text{INT1}}$ serves as external run control for timer 1, when selected by GATE1 bit in TCON register. **External Interrupt 1** $\overline{\text{INT1}}$ input sets IE1 in the TCON register. If bit IT1 in this register is set, bit IE1 is set by a falling edge on $\overline{\text{INT1}}$. If bit IT1 is cleared, bit IE1 is set by a low level on $\overline{\text{INT1}}$.	P3.3 $\overline{\text{CTS}}$ $\overline{\text{SS}}$
T0	I	**Timer 0 External Clock Input** When timer 0 operates as a counter, a falling edge on the T0 pin increments the count.	P3.4

Clock Controller

Table 4. Clock Signal Description

Signal Name	Type	Description	Alternate Function
X1	I	**Input of the on-chip inverting oscillator amplifier** To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, its output is connected to this pin. X1 is the clock source for internal timing.	-
X2	O	**Output of the on-chip inverting oscillator amplifier** To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, leave X2 unconnected.	-
UPVDD	PWR	**USB PLL Supply voltage** Connect this pin to LVDD pin.	-
UPVSS	GND	**USB PLL Circuit Ground** Connect this pin to LVSS pin.	-
APVDD	PWR	**Audio PLL / Oscillator Supply voltage** Connect this pin to LVDD pin.	-
APVSS	GND	**Audio PLL / Oscillator Circuit Ground** Connect this pin to LVSS pin.	-

Memory Controllers

Table 5. Secure Digital Card / MutiMediaCard Controller Signal Description

Signal Name	Type	Description	Alternate Function
SDCLK	O	**SD/MMC Clock** Data or command clock transfer.	P2.3
SDCMD	I/O	**SD/MMC Command Line** Bidirectional command line used for commands and responses transfer.	P2.2
SDDAT3:0	I/O	**SD/MMC Data Lines** Bidirectional data lines. In 1-bit mode configuration SDDAT0 is the DAT signal and SDDAT3:1 are not used and can be reused as I/O ports.	P2.7:4
$\overline{\text{SDINS}}$	I	**SD/MMC Card Insertion Signal** $\overline{\text{SDINS}}$ is the card presence signal. A low level on this input indicates the card is present in its slot. Note: This signal is generated by the SD/MMC card connector.	P2.0
$\overline{\text{SDLCK}}$	I	**SD Card Write Lock Signal** $\overline{\text{SDLCK}}$ is the SD Card write protected input. A low level on this pin indicates the card is write protected. Note: This signal is generated by the SD/MMC card connector.	P2.1

Table 6. Nand Flash / SmartMedia Card Controller Signal Description

Signal Name	Type	Description	Alternate Function
NFD7:0	I/O	**Memory Data Bus** 8-bit bidirectional data bus.	-
NFALE	O	**Address Latch Enable Signal** Asserted high during address write cycle.	-

Signal Name	Type	Description	Alternate Function
NFCLE	O	**Command Latch Enable Signal** Asserted high during command write cycle.	-
$\overline{\text{NFRE}}$	O	**Read Enable Signal** Read signal asserted low during NF/SMC read operation.	-
$\overline{\text{NFWE}}$	O	**Write Enable Signal** Write signal asserted low during NF/SMC write operation.	-
$\overline{\text{NFCE0}}$	O	**Nand Flash 0 Chip Enable** $\overline{\text{NFCE0}}$ is active low and is asserted by the nand flash controller each time it makes access to the device 0.	-
$\overline{\text{NFCE1}}$ $\overline{\text{SMLCK}}$	O I	**Nand Flash 1 Chip Enable** $\overline{\text{NFCE1}}$ is active low and is asserted by the nand flash controller each time it makes access to the selected device. **SmartMediaCard/xD-Picture Card Write Lock Signal** $\overline{\text{SMLCK}}$ is the card write protected input. A low level on this pin indicates the card is write protected. Note: When used as $\overline{\text{SMLCK}}$ input, pad has internal pull-up.	P4.4
$\overline{\text{NFCE2}}$ $\overline{\text{SMINS}}$	O I	**Nand Flash 2 Chip Enable** $\overline{\text{NFCE2}}$ is active low and is asserted by the nand flash controller each time it makes access to the selected device. **SmartMediaCard/xD-Picture Card Insertion Signal** $\overline{\text{SMINS}}$ is the card presence signal. A low level on this input indicates the card is present in its slot. Note: When used as $\overline{\text{SMINS}}$ input, pad has internal pull-up.	P4.5
$\overline{\text{NFCE3}}$ $\overline{\text{SMCE}}$	O	**Nand Flash 3 Chip Enable** $\overline{\text{NFCE3}}$ is active low and is asserted by the nand flash controller each time it makes access to the selected device. **SmartMediaCard/xD-Picture Card Chip Enable** $\overline{\text{SMCE}}$ is active low and is asserted by the nand flash controller each time it makes access to the card.	P4.6
$\overline{\text{NFWP}}$	O	**Write Protect Signal** $\overline{\text{NFWP}}$ is the Nand Flash / SmartMediaCard/xD-Picture Card write protect signal. This signal is active low and is set to low during reset in order to protect the memory against parasitic writes.	-

USB Controller

Table 7. USB Controller Signal Description

Signal Name	Type	Description	Alternate Function
DPF	I/O	**USB Full Speed Positive Data Upstream Port**	-
DMF	I/O	**USB Full Speed Minus Data Upstream Port**	-
DPH	I/O	**USB High Speed Plus Data Upstream Port**	-
DMH	I/O	**USB High Speed Minus Data Upstream Port**	-
UVCON	O	**USB VBUS Control line** UVCON is used to control the external VBUS power supply ON or OFF. Note: This output is requested for OTG mode.	P3.6

Signal Name	Type	Description	Alternate Function
UID	I	**USB OTG Identifier Input** This pin monitors the function of the OTG device. Note: This input is requested for OTG mode.	P3.7
UVCC	PWR	**USB Supply Voltage** Connect this pin to USB V_{BUS} power line.	-
ULVDD	PWR	**USB Pad Low Voltage** Connect this pin to LVDD pin.	-
UHVDD	PWR	**USB Pad High Voltage** Connect this pin to HVDD pin.	-
UVSS	GND	**USB Ground**	-
UBIAS	O	**USB Bias** Connect this pin to external resistor and capacitor.	

Audio Processor

Table 8. I2S Output Description

Signal Name	Type	Description	Alternate Function
OCLK	O	**Over-sampling Clock Line**	P4.0
DCLK	O	**Data Clock Line**	P4.1
DDAT	O	**Data Lines**	P4.2
DSEL	O	**Data Channel Selection Line**	P4.3

Table 9. Audio Codec Description

Signal Name	Type	Description	Alternate Function
LINR	I	**Right Channel Analog Input**	-
LINL	I	**Left Channel Analog Input**	-
MICIN	I	**Electret Microphone Analog Input**	-
MICBIAS	O	**Electret Microphone Bias Output**	-
OUTR	O	**Right Channel Output** Do not connect on AT85C51SND3B0 product	-
OUTL	O	**Left Channel Output** Do not connect on AT85C51SND3B0 product	-
AVCM	I	**Analog Common Mode Voltage** Connect this pin to external decoupling capacitor.	-
AREF	O	**Analog Reference Voltage** Connect this pin to external decoupling capacitor.	-
AVDD1	PWR	**Analog Power Supply 1** Connect this pin to LVDD pin.	-
AVSS1	GND	**Analog Ground 1** Connect this pin to LVSS pin.	-

Signal Name	Type	Description	Alternate Function
AVDD2	PWR	**Analog Power Supply 2** Low Voltage system: connect this pin to LVDD pin. High voltage system: connect this pin to external +3V power supply.	-
AVSS2	GND	**Analog Ground 2** Low Voltage system: connect this pin to LVSS pin. High voltage system: connect this pin to external +3V ground.	-

Parallel Slave Interface

Table 10. PSI Signal Description

Signal Name	Type	Description	Alternate Function
SD7:0	I/O	**Slave Data Bus** 8-bit bidirectional data bus.	P0.7:0 LD7:0
$\overline{SRD}$	I	**Slave Read Signal** Read signal asserted low during external host read operation.	P5.0 $\overline{LRD}$/LDE
$\overline{SWR}$	I	**Slave Write Signal** Write signal asserted low during external host write operation.	P5.3 $\overline{LWR}$/LRW
$\overline{SCS}$	I	**Slave Chip Select** Select signal asserted low during external host read or write operation.	P5.1 $\overline{LCS}$
SA0	I	**Slave Address Bit 0** Address signal asserted during external host read or write operation.	P5.2 LA0/LRS

Serial Interfaces

Table 11. SPI Controller Signal Description

Signal Name	Type	Description	Alternate Function
MISO	I/O	**SPI Master Input Slave Output Data Line** When in master mode, MISO receives data from the slave peripheral. When in slave mode, MISO outputs data to the master controller.	P3.0 RXD
MOSI	I/O	**SPI Master Output Slave Input Data Line** When in master mode, MOSI outputs data to the slave peripheral. When in slave mode, MOSI receives data from the master controller.	P3.1 TXD
SCK	I/O	**SPI Clock Line** When in master mode, SCK outputs clock to the slave peripheral. When in slave mode, SCK receives clock from the master controller.	P3.2 $\overline{INT0}$ $\overline{RTS}$
$\overline{SS}$	I	**SPI Slave Select Line** When in controlled slave mode, $\overline{SS}$ enables the slave mode.	P3.3 $\overline{INT1}$ $\overline{CTS}$

Table 12. SIO Signal Description

Signal Name	Type	Description	Alternate Function
RXD	I/O	**Receive Serial Data** RXD sends and receives data in serial I/O mode 0 and receives data in serial I/O modes 1, 2 and 3.	P3.0 MISO

Signal Name	Type	Description	Alternate Function
TXD	O	**Transmit Serial Data** TXD outputs the shift clock in serial I/O mode 0 and transmits data in serial I/O modes 1, 2 and 3.	P3.1 MOSI
$\overline{RTS}$	O	**Request To Send Hardware Handshake Line** Asserted low by hardware when SIO is ready to receive data.	P3.2 $\overline{INT0}$ SCK
$\overline{CTS}$	I	**Clear To Send Hardware Handshake Line** Asserted low by external hardware when SIO is allowed to send data.	P3.3 $\overline{INT1}$ $\overline{SS}$

MMI Interface

Table 13. Keypad Controller Signal Description

Signal Name	Type	Description	Alternate Function
KIN3:0	I	**Keypad Input lines** Holding one of these pins high or low for 24 oscillator periods triggers a keypad interrupt.	P1.3:0

Table 14. LCD Interface Signal Description

Signal Name	Type	Description	Alternate Function
LD7:0	I/O	**Display Data Bus** 8-bit bidirectional data bus.	P0.7:0 SD7:0
$\overline{LRD}$/LDE	O	**Read Signal/Enable Signal** 8080: Read signal asserted low during display read access. 6800: Enable signal asserted high during display access.	P5.0 $\overline{SRD}$
$\overline{LWR}$/LRW	O	**Write Signal/Read Write Signal** 8080: Write signal asserted low during display write access. 6800: Read/Write signal asserted low/high during display read/write access	P5.3 $\overline{SWR}$
$\overline{LCS}$	O	**Display Chip Select** Select signal asserted low during display access.	P5.1 $\overline{SCS}$
LA0/LRS	O	**Display Address Bit 0/Register Select** Address signal asserted during display access.	P5.2 SA0

Power Management

Table 15. Power Signal Description

Signal Name	Type	Description	Alternate Function
$\overline{DCPWR}$	I	**DC-DC Power ON Input** Connect $\overline{DCPWR}$ to V_{SS} to start the DC-DC converter.	-
DCLI	PWR	**DC-DC Inductance Input** Connect low ESR inductance to DCLI and BVDD.	
BVDD	PWR	**Battery Supply Voltage** Connect this pin to the positive pin of the battery.	-

Signal Name	Type	Description	Alternate Function
BVSS	GND	**Battery Ground** Connect this pin to the negative pin of the battery.	-
LVDD	PWR	**Low Voltage DC-DC Power Supply output** This pin outputs +1.8V typ. from internal DC-DC (battery powered).	-
RLVDD	PWR	**Low Voltage Regulator Power Supply Output** This pin outputs +1.8V typ. from internal regulator (USB powered or +3V external power supply). Connect this pin to LVDD incase of internal DC-DC usage.	-
HVDD	PWR	**High Voltage Power Supply** This pin outputs +3V typ. from internal regulator (USB powered). Connect this pin to +3V external power supply.	-
VSS	GND	**Power Ground** Connect this pin to the system ground.	-
CVSS	GND	**Core Ground** Connect this pin to VSS pin.	-
IOVDD	PWR	**Input/Output Supply voltage** Connect this pin to LVDD or HVDD pin.	-
IOVSS	GND	**Input/Output Circuit Ground** Connect this pin to VSS pin.	-

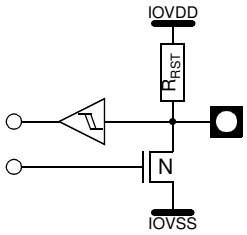
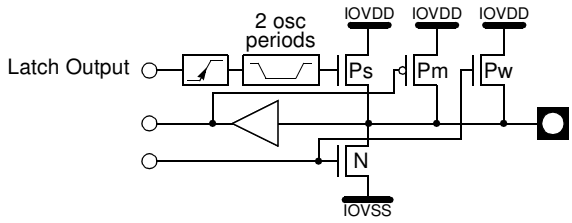
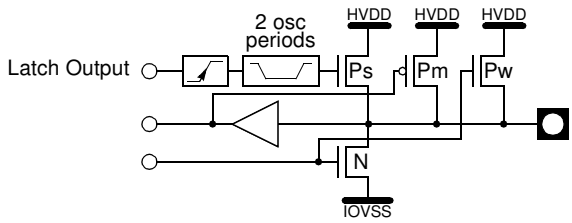
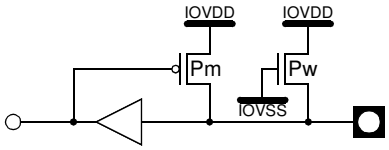
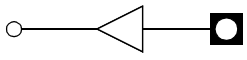
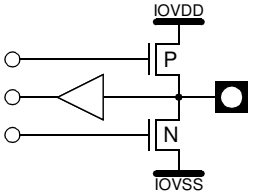
OCD Interface

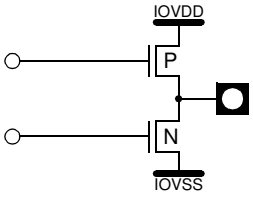
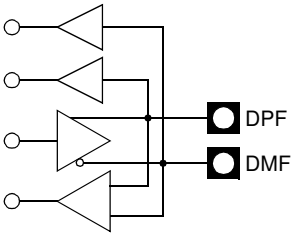
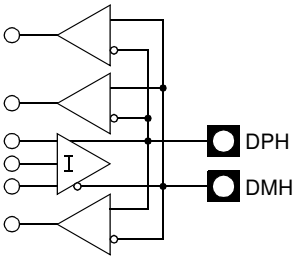
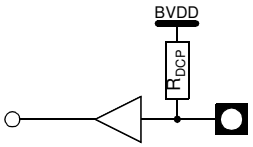
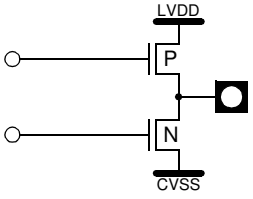
Table 16. OCD Signal Description

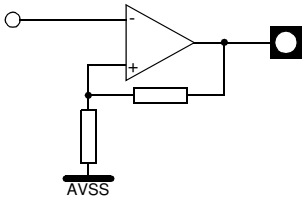
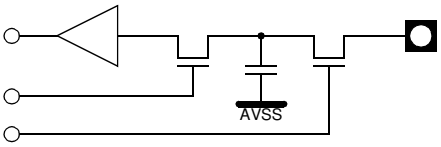
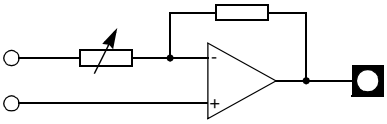
Signal Name	Type	Description	Alternate Function
OCDR	I	**On Chip Debug Receive Input** OCDR receives data.	-
OCDT	I/O	**On Chip Debug Transmit Output** OCDT transmits data.	$\overline{\text{ISP}}$

Internal Pin Structure

Table 17. Detailed Internal Pin Structure

Circuit[1]	Type	Pins
	Input/Output	$\overline{RST}$
	Input/Output	P0.7:0 P1.7:0 P2.7:0 P3.5:0 P4.6:0 P5.3:0 OCDT
	Input/Output	P3.7:6
	Input	KIN3:0 $\overline{SDINS}$ $\overline{SDLCK}$ $\overline{SMINS}$ $\overline{SMLCK}$ $\overline{TST}$ $\overline{ISP}$ UID $\overline{INT0}$ $\overline{INT1}$ T0 RXD OCDR
	Input	$\overline{SWR}$ SA0 $\overline{SRD}$ $\overline{SCS}$ $\overline{SS}$
	Input/Output	NFD7:0 SD7:0 LD7:0 SDCMD SDDAT3:0 MISO MOSI

Circuit[1]	Type	Pins
	Output	SDCLK SCK $\overline{\text{NFCE3:0}}$ NFCLE NFALE $\overline{\text{NFWE}}$ $\overline{\text{NFRE}}$ $\overline{\text{NFWP}}$ $\overline{\text{SMCE}}$ DSEL DDAT DCLK OCLK $\overline{\text{LWR}}$/LE LA0/LRS $\overline{\text{LRD}}$/LRW $\overline{\text{LCS}}$ UVCON TXD
	Input/Output	DPF DMF
	Input/Output	DPH DMH
	Input	$\overline{\text{DCPWR}}$[2]
	-	DCLI[2]

Circuit[1]	Type	Pins
	Output	MICBIAS
	Input	MICIN LINR LINL
	Output	OUTR[2] OUTL[2]

Notes:
1. For information on resistor value, input/output levels, and drive capability, refer to Section “DC Characteristics”, page 242.
2. AT85C51SND3B2 only
3. AT85C51SND3B1 & AT85C51SND3B2 only

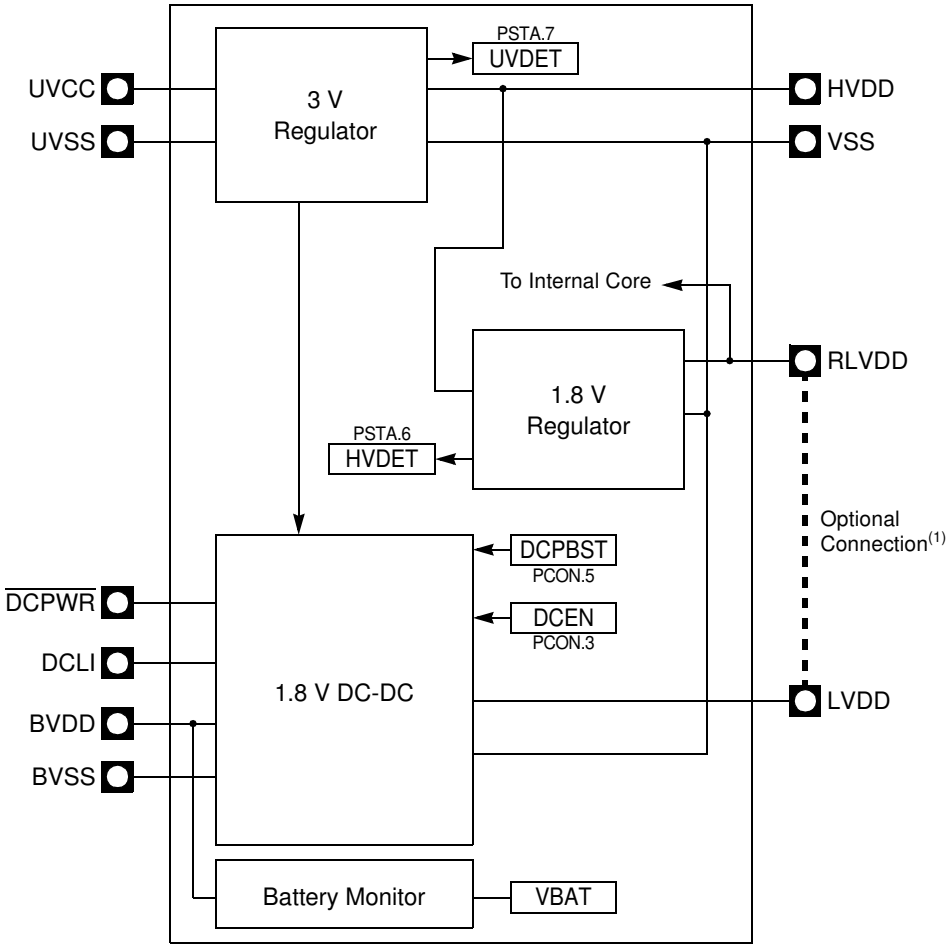
Power Management

The Power Management of AT85C51SND3B dervatives implements all the internal power circuitry (regulators, links…) as well as power failure detector and reset circuitry.

Power Supply

The AT85C51SND3B2 embeds the regulators and a DC to DC step-up convertor to be able to operate from either USB power supply (5V nominal) or from a single cell battery such as AAA battery.
The AT85C51SND3B0 and AT85C51SND3B1 embed the regulators to be able to operate from either USB power supply (5V nominal) or from an external 3 volts supply.

Figure 5. Power Supply Diagram



Note: 1. External connection mandatory when 1.8V DC-DC is used.

Regulators

The high voltage regulator supplies power to the external devices through HVDD power pin. Its nominal voltage output is 3V.
The low voltage regulator supplies power to the internal device and external devices through RLVDD power pin. Its nominal voltage output is 1.8V.
Figure 6 shows how to connect external components, capacitors value along with power characteristics are specified in the section “DC characteristics”.

Schematic

Figure 6. Regulator Connection

Note: Depending on power supply scheme, C_{LV} may replace C_{DC} capacitor (see Figure 8).

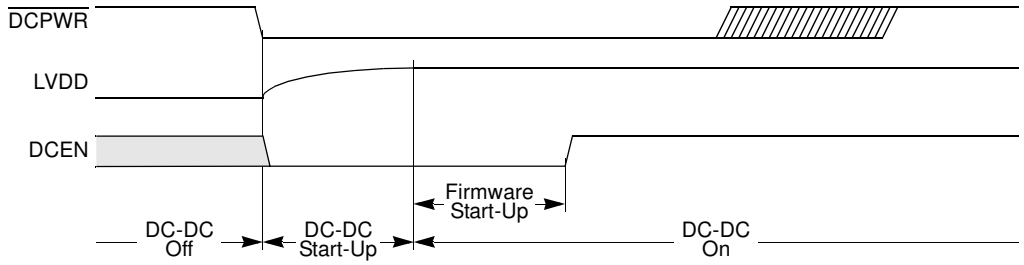
Low Voltage DC-DC in AT85C51SND3B2

The low voltage output DC-DC converter supplies power to the internal device and external devices through LVDD power pin. It operates from a single AAA battery. Its nominal voltage output is 1.8V.

DC-DC Start-Up

DC-DC start-up is done by asserting the $\overline{\text{DCPWR}}$ input until the voltage reaches its nominal value (see Section “Power Fail Detector”) and firmware starts execution and sets the DCEN bit in PCON to maintain the DC-DC enabled. $\overline{\text{DCPWR}}$ input can then be released. As shown in Figure 8 $\overline{\text{DCPWR}}$ input is asserted by pressing a key connected to BVSS.

Figure 7. DC-DC Start-Up Phase



DC-DC Shut-Down

DC-DC shut-down is done by two different ways:

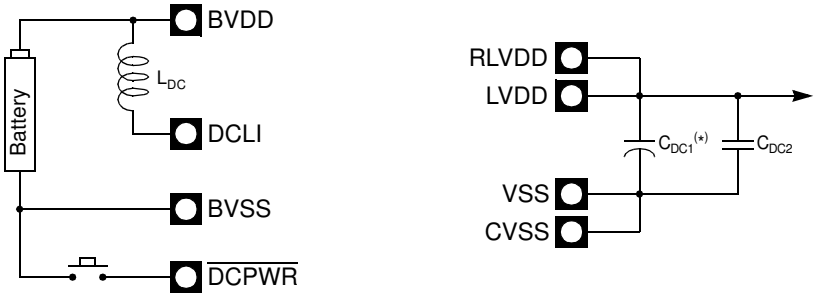
- Clearing the DCEN bit while $\overline{\text{DCPWR}}$ pin is de-asserted
- Detecting the presence of an internal or external 3V supply, e.g. when the device is connected to USB, DC-DC is disabled to save battery power(1).

Note: 1. If DCEN bit is left set, the DC-DC will restart as soon as the USB power supply disappears.

DC-DC Connection

Figure 8 shows how to connect external components, inductance and components value along with power characteristics are specified in the section “DC characteristics”.

Figure 8. Battery DC-DC Connection



Note: Depending on power supply scheme, C_{DC1} may replace C_{LV} capacitor (see Figure 6).

Battery Voltage Monitor

The battery voltage monitor is a 5-bit / 50 mV resolution A to D converter with fixed conversion range as detailed in Table 18.

Table 18. Battery Voltage Value

VB4:0	Battery Voltage (V)
00000	[0.9 - 0.95[
00001	[0.95 - 1.0[
00010	[1.0 - 1.05[
…	…
01110	[1.6 - 1.65[
01111	[1.65 - 1.7[
10000	[1.7 - 1.75[

Conversion Management

The battery voltage monitor is turned on by setting the VBPEN and VBCEN bits in PCON (see Table 20). VBPEN bit is set first and VBCEN bit is set 1 ms later. An additional delay of 16 cycles is required before lauching any conversion.
Launching a conversion is done by setting VBEN bit in VBAT (see Table 22). VBEN is automatically cleared at the end of the conversion which takes 34 clock periods. At this step two cases occur:

- Voltage is valid (inside conversion range)
  VBERR is cleared and conversion value is set in VB4:0 according to Table 18.
- Voltage is invalid (out of conversion range)
  VBERR is set and value reported by VB4:0 is indeterminate.

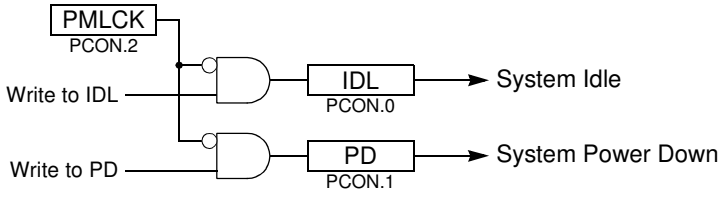
Power Reduction Mode

Two power reduction modes are implemented in the AT85C51SND3B: the Idle mode and the Power-down mode. These modes are detailed in the following sections. In addition to these power reduction modes, the clocks of the core and peripherals can be dynamically divided by 2 using the X2 mode as detailed in Section “X2 Feature”, page 31.

Lock Mode

In order to allow firmware to efficiently enter in idle mode and not to lose any events that should come from one or more interrupts, power reduction modes entry are conditioned to an hardware bit: PMLCK in PCON.
PMLCK is set by software in each ISR that needs to report an event to the system and thus disables entry in power reduction mode and allows immediate processing of this event. It is cleared by software after exiting power reduction mode.
As shown in Figure 9, when power reduction modes are disabled by setting PMLCK, IDL and PD bits in PCON can not be set and idle or power down modes are not entered.

Figure 9. Power Reduction Controller Block Diagram



Idle Mode

Idle mode is a power reduction mode that reduces the power consumption. In this mode, program execution halts. Idle mode freezes the clock to the CPU at known states while the peripherals continue to be clocked (refer to Section “System Clock Generator”, page 30). The CPU status before entering Idle mode is preserved, i.e., the program counter and program status word register retain their data for the duration of Idle mode. The contents of the SFRs and RAM are also retained.

Entering Idle Mode

To enter Idle mode, the user must set the IDL bit in PCON register while PMLCK is cleared. The AT85C51SND3B enters Idle mode upon execution of the instruction that sets IDL bit. The instruction that sets IDL bit is the last instruction executed.

Note: If IDL bit and PD bit are set simultaneously, the AT85C51SND3B enter Power-down mode. Then it does not go in Idle mode when exiting Power-down mode.

Exiting Idle Mode

There are 2 ways to exit Idle mode:

1. Generate an enabled interrupt.
   - Hardware clears IDL bit in PCON register which restores the clock to the CPU. Execution resumes with the interrupt service routine. Upon completion of the interrupt service routine, program execution resumes with the instruction immediately following the instruction that activated Idle mode. The general-purpose flags (GF1 and GF0 in PCON register) may be used to indicate whether an interrupt occurred during normal operation or during Idle mode. When Idle mode is exited by an interrupt, the interrupt service routine may examine GF1 and GF0.
2. Generate a reset.
   - A logic high on the RST pin clears IDL bit in PCON register directly and asynchronously. This restores the clock to the CPU. Program execution momentarily resumes with the instruction immediately following the instruction that activated the Idle mode and may continue for a number of clock cycles before the internal reset algorithm takes control. Reset initializes the AT85C51SND3B and vectors the CPU to address 0000h.

Note: During the time that execution resumes, the internal RAM cannot be accessed; however, it is possible for the Port pins to be accessed. To avoid unexpected outputs at the Port pins, the instruction immediately following the instruction that activated Idle mode should not write to a Port pin or to the external RAM.

Power-down Mode

The Power-down mode places the AT85C51SND3B in a very low power state. Power-down mode stops the oscillator and freezes all clocks at known states (refer to the Section “Oscillator”, page 28). The CPU status prior to entering Power-down mode is preserved, i.e., the program counter, program status word register retain their data for the duration of Power-down mode. In addition, the SFRs and RAM contents are preserved.

Entering Power-down Mode

To enter Power-down mode, set PD bit in PCON register while PMLCK is cleared. The AT85C51SND3B enters the Power-down mode upon execution of the instruction that sets PD bit. The instruction that sets PD bit is the last instruction executed.

Exiting Power-down Mode

There are 2 ways to exit the Power-down mode:

1. Generate an enabled external interrupt.
   - The AT85C51SND3B provides capability to exit from Power-down using $\overline{\text{INT0}}$, $\overline{\text{INT1}}$, and KIN3:0 inputs. In addition, using KIN input provides high or low level exit capability (see Section “Keyboard Interface”, page 240).
     Hardware clears PD bit in PCON register which starts the oscillator and restores

the clocks to the CPU and peripherals. Using $\overline{INTn}$ input, execution resumes when the input is released (see Figure 10) while using KINx input, execution resumes after counting 1024 clock ensuring the oscillator is restarted properly (see Figure 11). This behavior is necessary for decoding the key while it is still pressed. In both cases, execution resumes with the interrupt service routine. Upon completion of the interrupt service routine, program execution resumes with the instruction immediately following the instruction that activated Power-down mode.

Note: 1. The external interrupt used to exit Power-down mode must be configured as level sensitive ($\overline{INT0}$ and $\overline{INT1}$) and must be assigned the highest priority. In addition, the duration of the interrupt must be long enough to allow the oscillator to stabilize. The execution will only resume when the interrupt is de-asserted.

2. Exit from power-down by external interrupt does not affect the SFRs nor the internal RAM content.

Figure 10. Power-down Exit Waveform Using $\overline{INT1:0}$

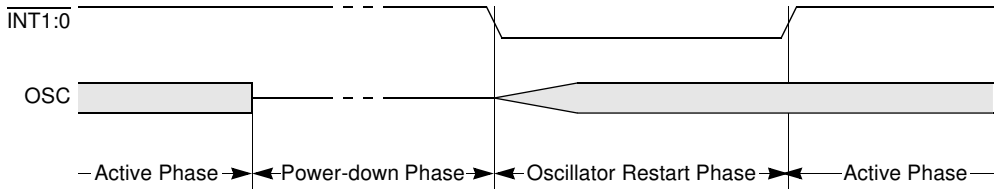
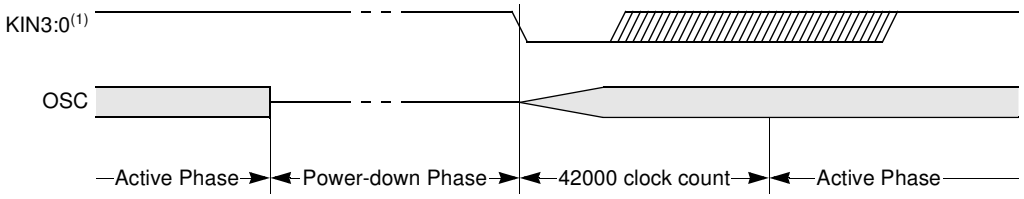


Figure 11. Power-down Exit Waveform Using KIN3:0



Note: 1. KIN3:0 can be high or low-level triggered.

2. Generate a reset.
   – A logic high on the RST pin clears PD bit in PCON register directly and asynchronously. This starts the oscillator and restores the clock to the CPU and peripherals. Program execution momentarily resumes with the instruction immediately following the instruction that activated Power-down mode and may continue for a number of clock cycles before the internal reset algorithm takes control. Reset initializes the AT85C51SND3B and vectors the CPU to address 0000h.

Notes: 1. During the time that execution resumes, the internal RAM cannot be accessed; however, it is possible for the Port pins to be accessed. To avoid unexpected outputs at the Port pins, the instruction immediately following the instruction that activated the Power-down mode should not write to a Port pin or to the external RAM.

2. Exit from power-down by reset redefines all the SFRs, but does not affect the internal RAM content.

Reset

In order to secure the product functionality while in power-up or power-down phase or while in running phase, a number of internal mechanisms have been implemented. These mechanisms are listed below and detailed in the following paragraphs.

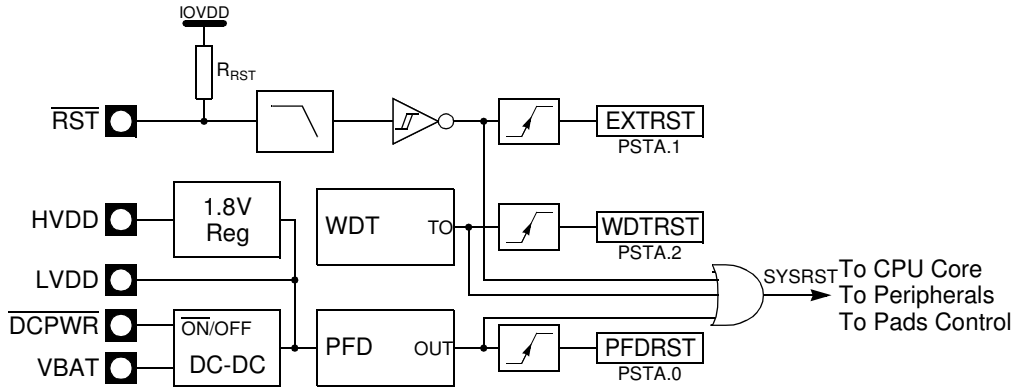
- External $\overline{RST}$ input
- Power Fail Detector (brown-out)
- Watchdog timer
- Pads control

Figure 12 details the internal reset circuitry.

Reset Source Reporting

In order for the firmware to take specific actions depending on the source which has currently reset the device, activated reset source is reported to the CPU by EXTRST, WDTRST, and PFDRST flags in PSTA register.

Figure 12. Internal Reset Circuitry



Pads Level Control

As soon as one reset source is asserted, the pads go to their reset value. This ensures that pads level is steady during reset (e.g. $\overline{NFWP}$ set to low level and then protecting Nand Flash against spurious writing).
The status of the Port pins during reset is detailed in Table 19.

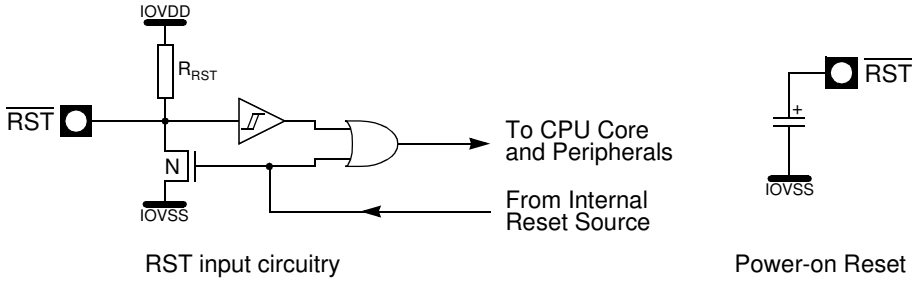
Table 19. Pin State Under Reset Condition.

Port 0	Port 1	Port 2	Port 3	Port 4	Port 5	NFD7:0	$\overline{NFWP}$	$\overline{NFCE0}$
Float	H	H	H	H	H	Float	L	H

External $\overline{RST}$ Input

In order to start-up (cold reset) or to restart (warm reset) properly the microcontroller, a low level has to be applied on the $\overline{RST}$ pin. A bad level leads to a wrong initialization of the internal registers like SFRs, Program Counter… and to unpredictable behavior of the microcontroller. A proper device reset initializes the AT85C51SND3B and vectors the CPU to address 0000h. $\overline{RST}$ input has a pull-up resistor allowing power-on reset by simply connecting an external capacitor to V_{SS} as shown in Figure 13. A warm reset can be applied either directly on the RST pin or indirectly by an internal reset source such as the watchdog timer. Resistor value and input characteristics are discussed in the Section “DC Characteristics”, page 242.

Figure 13. Reset Circuitry and Power-On Reset



Cold Reset

2 conditions are required before enabling a CPU start-up:

- V_{DD} must reach the specified V_{DD} range
- The level on X1 input pin must be outside the specification (V_{IH}, V_{IL})

If one of these 2 conditions are not met, the microcontroller does not start correctly and can execute an instruction fetch from anywhere in the program space. An active level applied on the $\overline{RST}$ pin must be asserted till both of the above conditions are met. A reset is active when the level V_{IL} is reached and when the pulse width covers the period of time where V_{DD} and the oscillator are not stabilized. 2 parameters have to be taken into account to determine the reset pulse width:

- V_{DD} rise time,
- Oscillator startup time.

To determine the capacitor value to implement, the highest value of these 2 parameters has to be chosen.

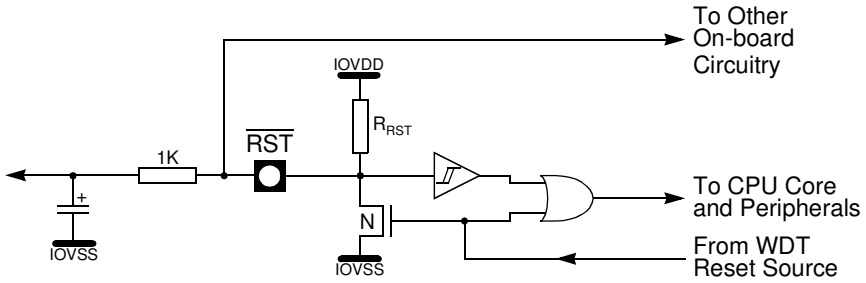
Warm Reset

To achieve a valid reset, the reset signal must be maintained for at least 2 machine cycles (24 oscillator clock periods) while the oscillator is running. The number of clock periods is mode independent (X2 or X1).

Watchdog Timer Reset

As detailed in Section "Watchdog Timer", page 75, the WDT generates a 96-clock period pulse on the $\overline{RST}$ pin. In order to properly propagate this pulse to the rest of the application in case of external capacitor or power-supply supervisor circuit, a 1 kΩ resistor must be added as shown in Figure 14.

Figure 14. Reset Circuitry for WDT Reset-out Usage



Power Fail Detector

The Power Fail Detector (PFD) ensures that whole product is in reset when internal voltage is out of its limits specification. PFD limits are detailed in the Section "DC Characteristics", page 242.