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Features

- **Multiband Transceiver: 400 MHz to 950 MHz**
- **Monochip RF Solution: Transmitter-Receiver-Synthesizer**
- **Integrated PLL and VCO: No External Coil**
- **Very Resistant to Interferers by Design**
- **Digital Channel Selection**
- **200 Hz Steps**
- **Data Rates up to 64 kbps with Data Clock and no Manchester Encoding Required**
- **High Output Power Allowing Very Low Cost Printed Antennas:**
  - **+10 dBm in the 915 MHz Frequency Band**
  - **+12 dBm in the 868 MHz Frequency Band**
  - **+14 dBm in the 433 MHz Frequency Band**
- **FSK Modulation: Integrated Modulator and Demodulator**
- **Power Savings:**
  - **Stand Alone "Sleep" Mode and "Wake-up" Procedures**
  - **8 Selectable Digital Levels for Output Power**
  - **High Data Rate and Fast Settling Time of the PLL**
  - **Oscillator Running Mode "Ready to Start"**
  - **Analog FSK Discriminator Allowing Measurement and Correction of Frequency Drifts**
- **100% Digital Interface through R/W Registers Including:**
  - **Digital RSSI**
  - **V_{CC} Readout**

Description

The AT86RF211 (aka: TRX01) is a single chip transceiver dedicated to low power wireless applications, optimized for licence-free ISM band operations from 400 MHz to 950 MHz. Its flexibility and unique level of integration make it a natural choice for any system related to telemetry, remote controls, alarms, radio modems, Automatic Meter Reading, hand held terminals, high-tech toys, etc. The AT86RF211 makes bidirectional communications affordable for applications such as secured transmissions with hand-shake procedures, new features and services, etc. The AT86RF211 can easily be configured to provide the optimal solution for the user's application: choice of external filters vs. technical requirements (bandwidth, selectivity, immunity, range, etc), and software protocol (single channel, multiple channel, FHSS). The AT86RF211 is also well adapted to battery operated systems, as it can be powered with only 2.4V. It also offers a "Wake Up" receiver feature to save power by alerting the associated microcontroller only when a valid inquiry is detected.

FSK Transceiver for ISM Radio Applications

AT86RF211 (aka: TRX01)

Smart RF

Rev. 1942C–WIRE–06/02

General Overview

General Overview of Functioning

The AT86RF211 is a microcontroller RF peripheral: all the user has to do is to write/read registers to setup the chip (i.e. frequency selection) or have information about parameters such as RSSI level, Vbattery, PLL lock state. All these operations are carried out via a three-wire serial interface.

Normal Mode

The chip is set-up by the microcontroller: frequency and mode (Rx or Tx). Then it acts like a "pipe": any data entering DATAMSG is immediately radiated (Tx) or any wanted signal collected by the aerial is demodulated, transferred to the microcontroller by the same pin DATAMSG (Rx) as reshaped bits. No data is stored or processed into the chip. See Figure 1.

Note: In Rx mode, a clock recovery DATACLK is available on the digital interface to provide the microcontroller with a synchronization signal.

Wake-up Mode

The chip is set up in a special Rx mode called sleep mode. The chip wakes up periodically thanks to its internal timer (stand alone procedure, the microcontroller is in power-down mode), waiting for an expected message previously defined. If no correct sequence is received, the periodic scan continues.

If a correct message is detected, its data field is stored into the AT86RF211 (up to 32 bits) and an interrupt is generated on the WAKEUP pin.

See Figure 2 and Figure 3.

Figure 1. Reception and Transmit Mode

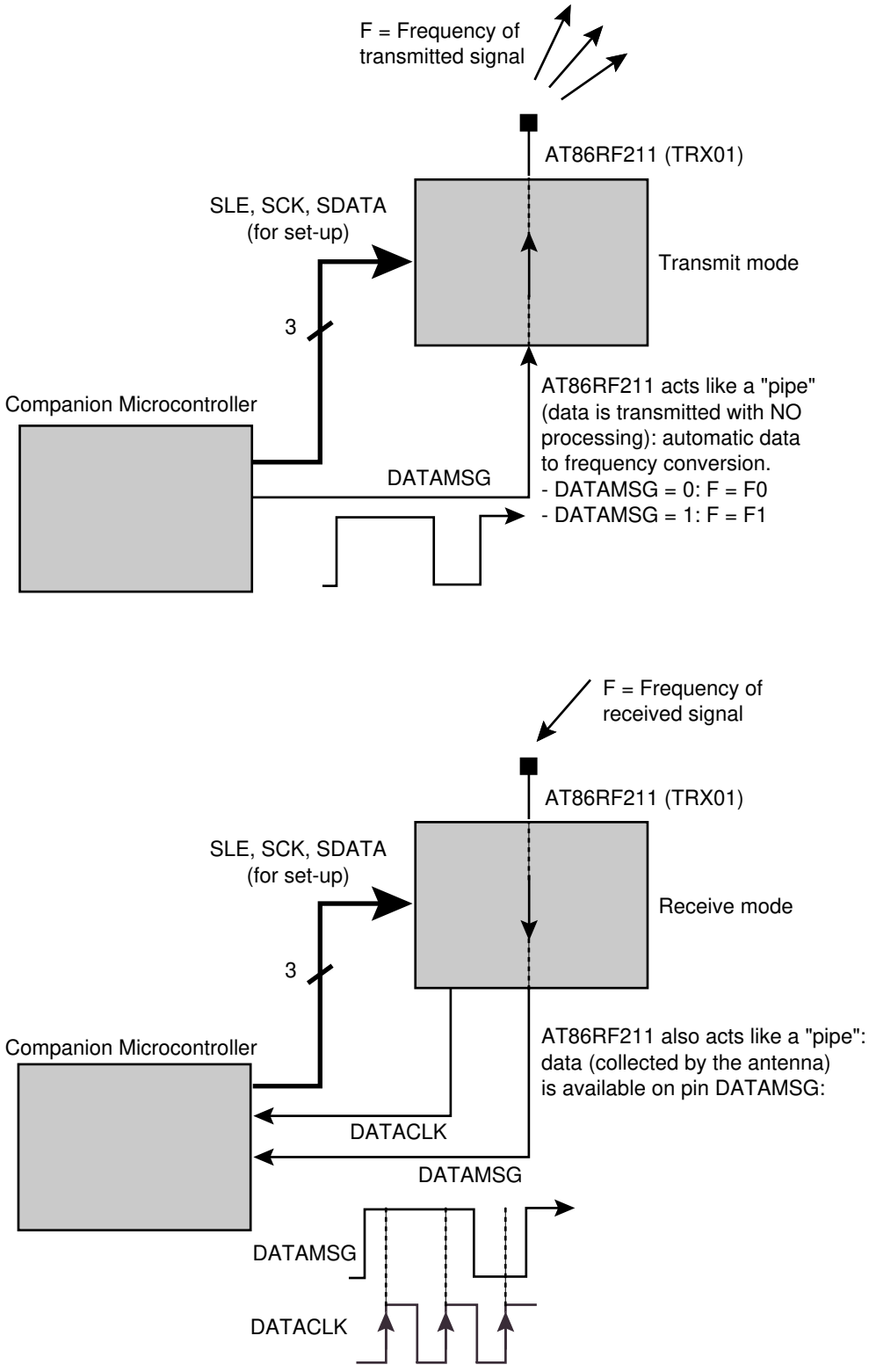


Figure 2. Wake-up Overview

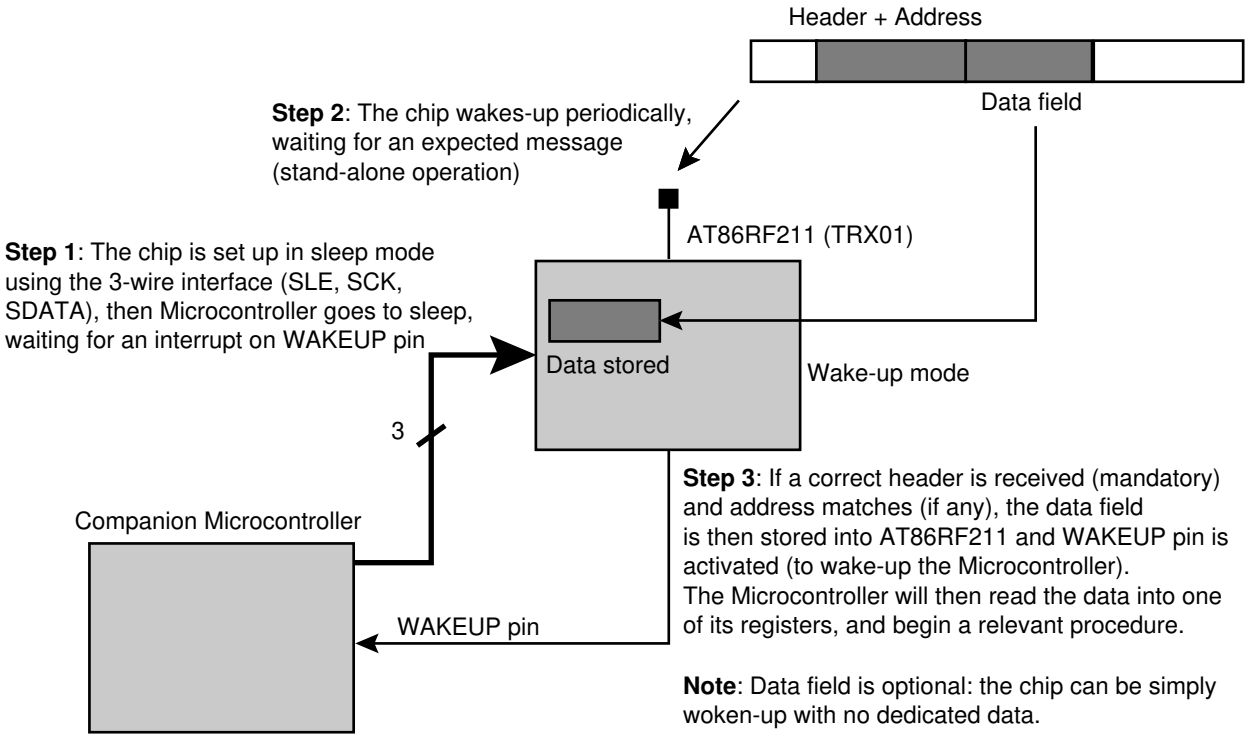
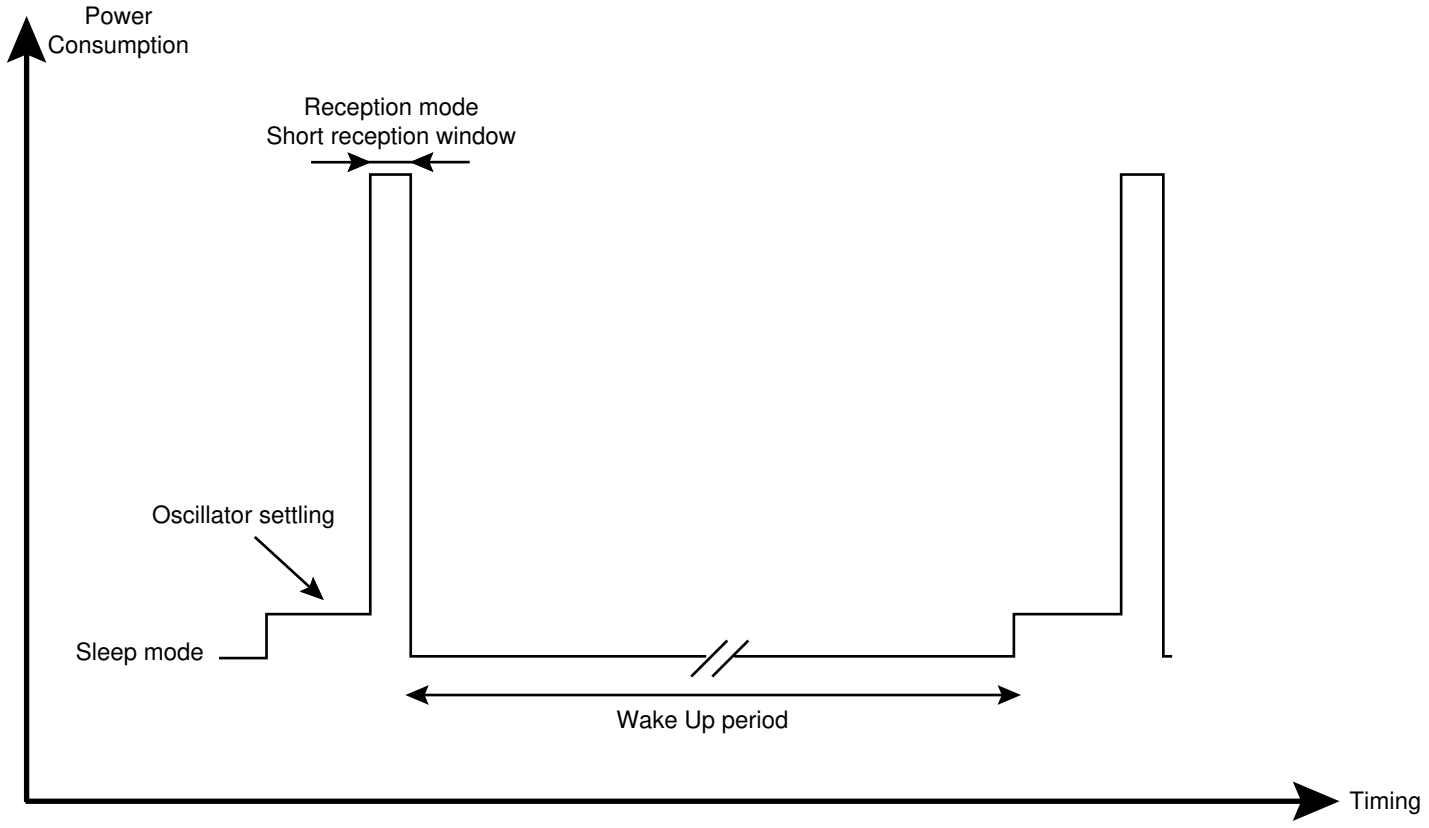
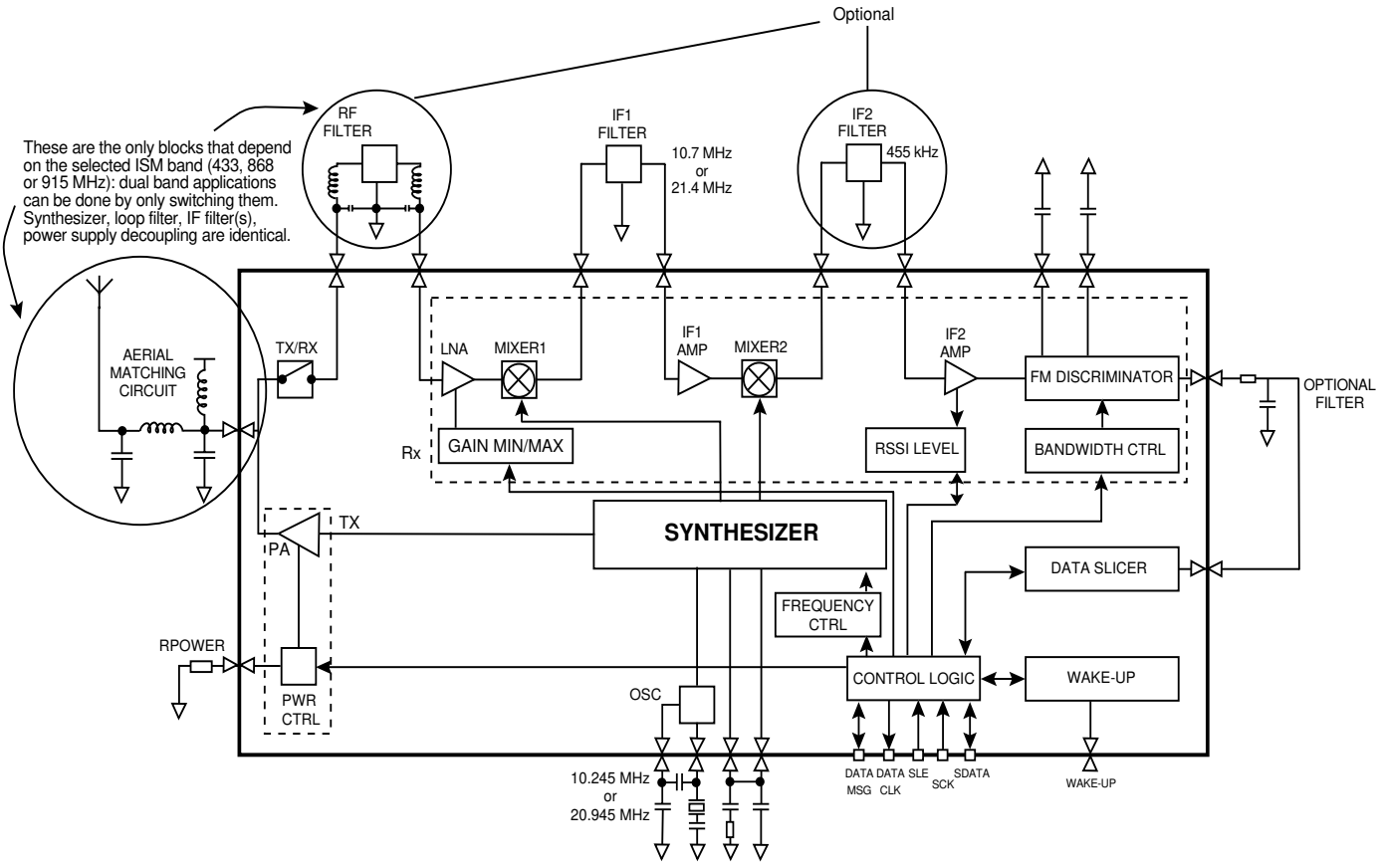


Figure 3. Periodical Scan



Block Diagram

Figure 4. AT86RF211 Block Diagram



Pin Description

Table 1. Pinout

Pin	Name	Comments	Pin	Name	Comments
1	RPOWER	Full scale output power resistor	25	SKFILT	Threshold for data slicer
2	TXGND1	GND	26	DSIN	Data slicer input
3	RF	RF input/output	27	DISCOUT	Discriminator output
4	TXGND2	GND	28	IF2VCC	VCC
5	TXGND3	GND	29	IF2GND	GND
6	TXGND4	GND	30	IF2IN	IF2 amplifier input
7	TXVCC	VCC	31	IF2DEC	2.2 nF to ground
8	TXGND5	GND	32	DISCFILT	Discriminator bypass
9	DIGND	GND	33	IF2OUT	IF2 mixer output
10	DIVCC	VCC	34	IF1DEC	4.7 nF to ground
11	DATAMSG	Input/output digital message	35	IF1IN	IF1 amplifier input
12	SLE	Serial interface enable	36	IF1OUT	IF1 mixer output
13	SCK	Serial interface clock	37	AGND	GND
14	SDATA	Serial interface data	38	AVCC	VCC
15	WAKEUP	Wake-up output	39	CVCC2	VCC
16	DATACLK	Data clock recovery	40	CGND2	GND
17	–	Test pin: do not connect	41	FILT1	Synthesizer output
18	EVCC1	VCC	42	VCOIN	Synthesizer input (VCO)
19	EGND1	GND	43	EVCC2	VCC
20	–	Test pin: do not connect	44	EGND2	GND
21	CGND1	GND	45	RXIN	LNA input from SAW filter
22	CVCC1	VCC	46	RXVCC	VCC
23	XTAL1	Crystal input	47	RXGND	GND
24	XTAL2	Crystal output	48	SWOUT	Switch output

Notes: 1. All V_{CC} pins must be connected in each functional mode (Tx, Rx, wake-up, PDN)
2. To be connected:
Rx mode only, all but: 1, 3, 17, 20, 48
Tx mode only, all but: 15 to 17, 20, 25 to 27, 30 to 36, 45, 48
3. Pin 20 must remain unconnected or connected to ground

Detailed Description

Frequency Synthesis

Crystal Reference Oscillator

The reference clock is based on a classical Colpitts architecture with three external capacitors.

An XTAL with load capacitor in the range of 10 pF - 20 pF is recommended. The bias circuitry of the oscillator is optimized to produce a low drive level for the XTAL. This reduces XTAL aging. Any standard, parallel mode 10.245 MHz or 20.945 MHz crystal can be used.

Note: The PLL is activated only when the oscillator is stabilized.

Figure 5. Crystal Oscillator Inputs

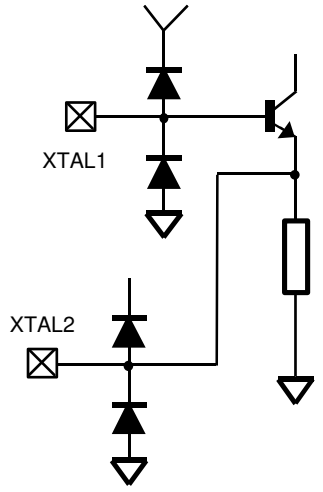
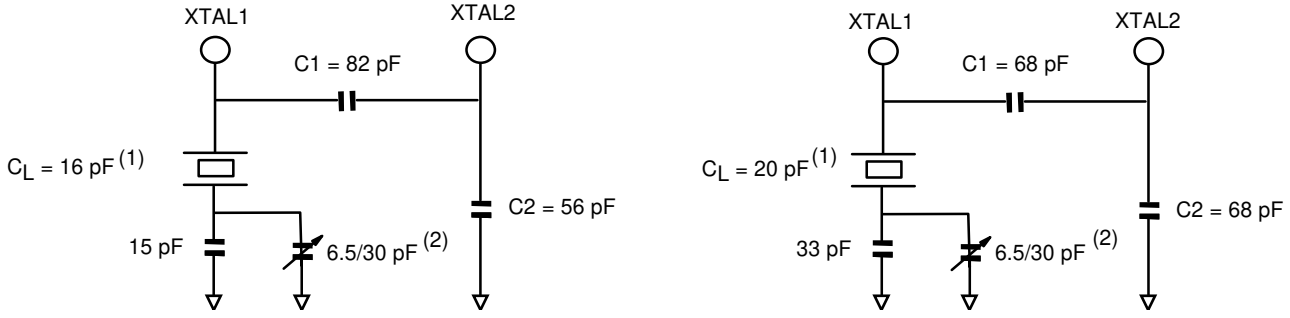


Figure 6. Typical Networks

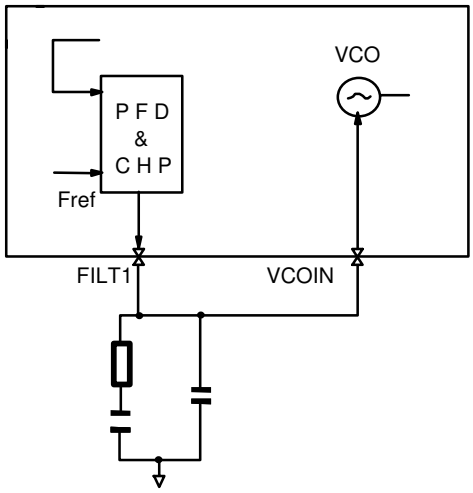


Notes:
1. Various load capacitance (C_L) crystals can be used. In case C_L differs of 16 pF or 20 pF, the surrounding network (C1, C2) must be re-calculated.
2. Thanks to the fine steps of the synthesizer (200 Hz), the trimmer capacitor can be replaced by a software adjustment.

Synthesizer

A high-speed, high-resolution multi-loop synthesizer is integrated. The synthesizer can operate within two frequency bands: 400 MHz to 480 MHz and 800 MHz to 950 MHz. All channels in these two bands can be selected through software programming (registers F0 to F3). All circuitry is on-chip with the exception of the PLL loop filter. The phase comparison is made thanks to a charge pump topology. Typical charge pump current is 225 µA.

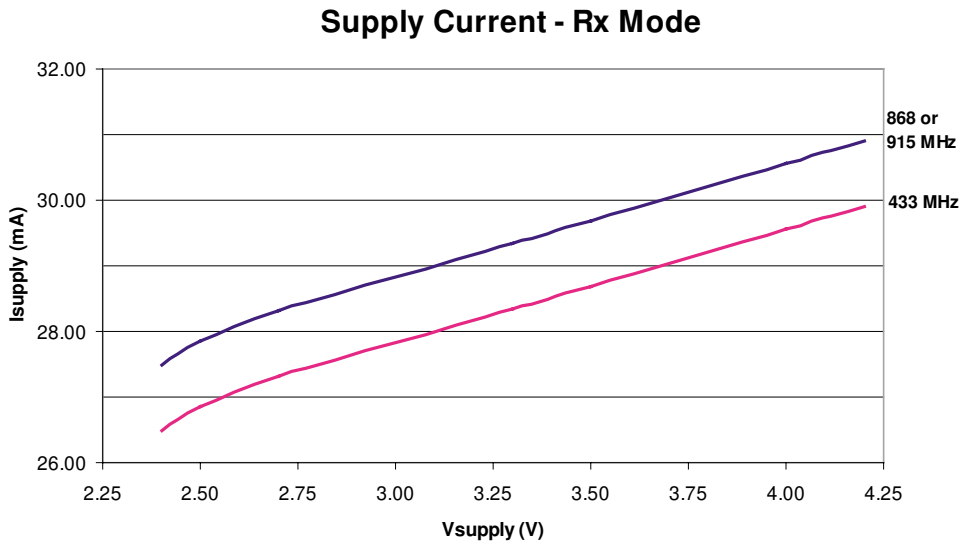
Figure 7. Synthesizer Loop Filter Schematic

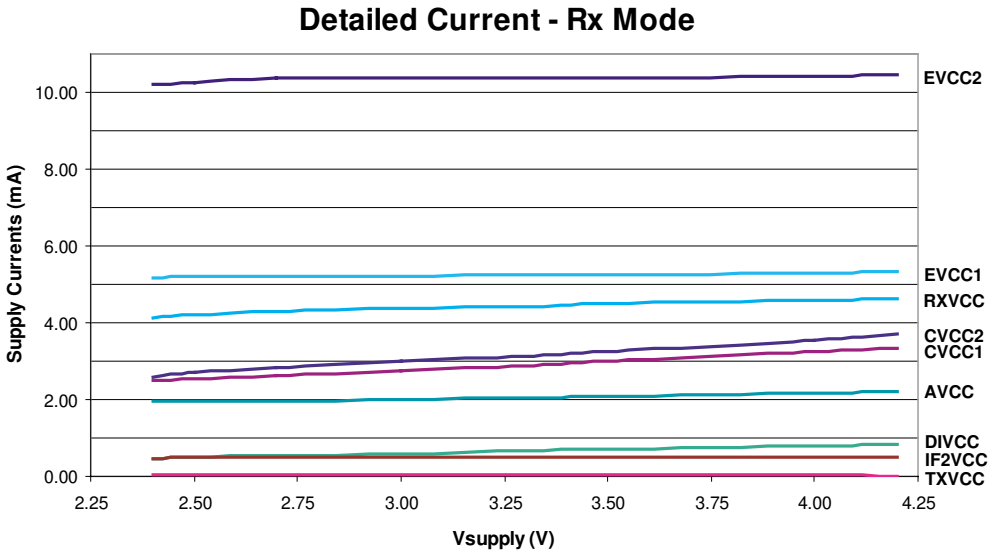


Note: The PLL loop filter can be designed to optimize the phase noise around the carrier. Three configurations can be suggested, regarding the application and channel spacing:
- Narrow band: (14.7 kΩ + 2.2 nF) // 220 pF
- Typical: (3.3 kΩ + 5.6 nF) // 560 pF
- High datarates: (10 kΩ + 1 nF) // 100 pF

Receiver Description

Figure 8. Typical Expected Currents in Rx Mode





Overview and Choice of Intermediate Frequencies

For selectivity and flexibility purpose, a classical and robust 2 IF superheterodyne architecture has been selected for the AT86RF211. In order to minimize the external components cost, the most popular IF values have been chosen. The impedances of the input/output of the mixing stages have been internally matched to the most usual ceramic filter impedances.

Two typical IF values are suggested:

- 10.7 MHz is the most popular option.
- 21.4 MHz: the image frequency is far enough from the carrier frequency to enable the use of a front-end ceramic filter instead of a SAW filter. It is also noticeable that 21.4 MHz quartz filters usually have more abrupt slopes than 10.7 MHz ceramic filters.

Rx - Tx Switch

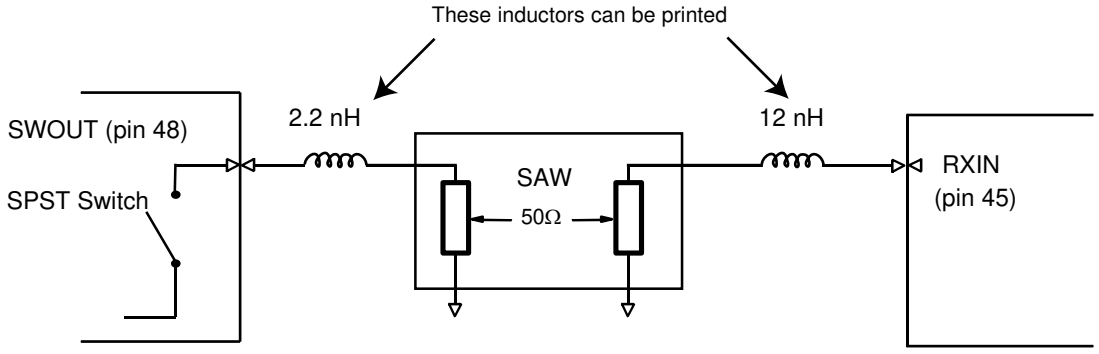
A SPST switch is integrated. In the transmission mode, it protects the LNA input from the large voltage swings of the PA output (up to several volts peak-to-peak), which is switched to a high impedance state. It is automatically turned ON or OFF by the RX/TX control bit. The insertion loss is about 2 dB and the reverse isolation about 30 dB in a 300Ω environment.

Image Rejection and RF Filter

The immunity of the AT86RF211 can be improved with an external band-pass filter.

For example, when using a SAW Filter, this device must be matched with the LNA input and the switch output. The following scheme gives the typical implementation for an 868 MHz application with a 50Ω/50Ω SAW filter.

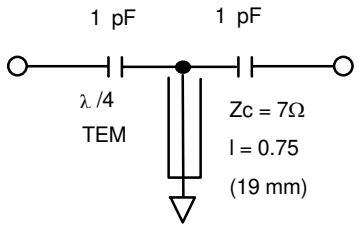
Figure 9. Typical 50Ω SAW Filter Implementation in the 868 MHz Band



See Table 2 for precise matching information.

The SAW filter can be replaced by a TEM ceramic, helicoidal or a ceramic coax λ/4 resonator designed as a narrow band-pass filter. For instance, with an IF selected at 10.7 MHz, a -3 dB bandwidth of 5 MHz, with an insertion loss of 1 dB and an image rejection of 12 dB can be achieved with the following:

Figure 10. TEM Filter



Such a filter also provides an out-of-band interference rejection greater than 20dB, 40 MHz away from 433 MHz.

First LNA/Mixer

The main characteristics of the LNA/Mixer are typically:

- Voltage gain: 17 dB for the LNA/Mixer; 11 dB if gain min. is selected
- Bandwidth: 1.2 GHz
- Noise figure of LNA alone: 3 dB at 900 MHz, best matching
- Noise figure of LNA + mixer:
  8 dB at 900 MHz, with maximum gain and best matching
  12 dB at 900 MHz, with minimum gain and best matching
- 1 dB compression point: -20 dBm at the input of LNA
- Matching:

Table 2. Matching Information

Frequency Band	RXIN(1)	SWOUT(2)
433 MHz	35 + j 170Ω	24 - j 43Ω
868 MHz	37 + j 85Ω	50 - j 42Ω
915 MHz	30 + j 85Ω	50 - j 42Ω

Notes: 1. RXIN: impedance to be seen by LNA input for NF optimization purpose
2. SWOUT: output impedance of the RF switch

The gain is programmable through bit 25 of CTRL1 register (6dB attenuation when min gain is selected). The choice for the matching between the SWITCH and the LNA depends mainly on the chosen SAW filter. Usually in/out impedance of SAW filters is 50Ω, but other ones can be implemented and the matching network recalculated thanks to the previous impedance table.

The LNA is directly coupled to the first mixer. Input and output of the LNA/Mixer must be connected through a capacitive link because of their internal DC coupling. A SAW or ceramic filter provides such a link.

Figure 11. Schematic Input of the LNA

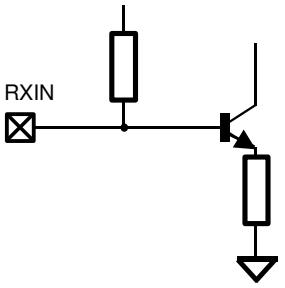
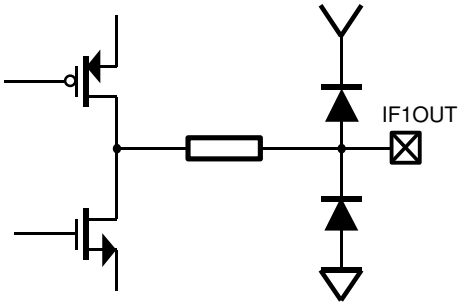


Figure 12. Schematic Output of the Mixer



The first mixer translates the input RF signal down to 10.7 MHz or 21.4 MHz as chosen by the user. The local oscillator is provided by the same synthesizer which will generate a local frequency 10.7 MHz or 21.4 MHz away from the Tx carrier frequency.

The output impedance of the mixer is 330Ω with a 20% accuracy, so that low cost, standard 10.7 MHz ceramic filters can be directly driven. Other IFs may be chosen thanks to the high bandwidth (50 MHz) of the mixer.

IF1 filtering

A popular ceramic filter is used to reject the second image frequency and provide a first level of filtering.

The IF1 filter can however be removed; it leads to a sensitivity reduction of about 3 dB (the substitution coupling capacitor should be > 100 pF).

IF1 Gain and Second Mixer

The input impedance of the IF1 amplifier is naturally 330Ω to match the input filter. The voltage gain, i.e. gain at 10.7 MHz or 21.4 MHz added to the conversion gain at 455 kHz is typically 14 dB when loaded by 1700Ω. The second mixer operates at a fixed LO frequency of 10.245 MHz or 20.945 MHz. Its output impedance is 1700Ω in parallel with 20 pF.

Figure 13. IF1 Filtering

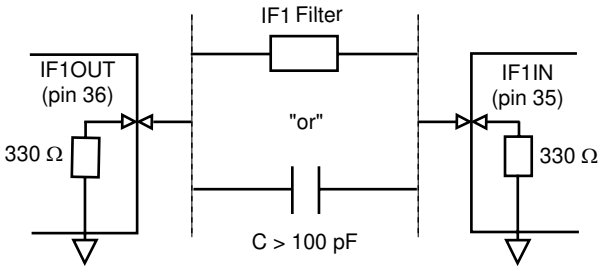


Figure 14. Schematic Input of IF1 Amplifier

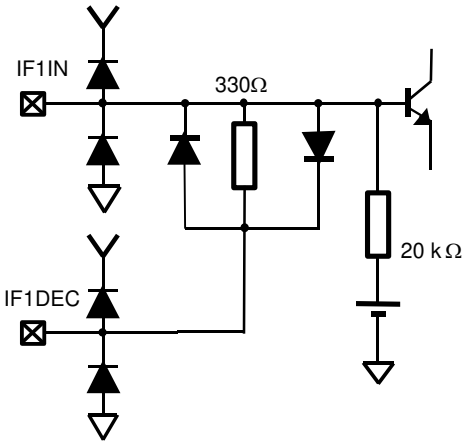
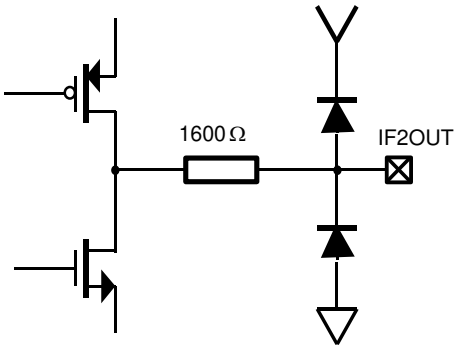


Figure 15. Schematic Output of the Second Mixer

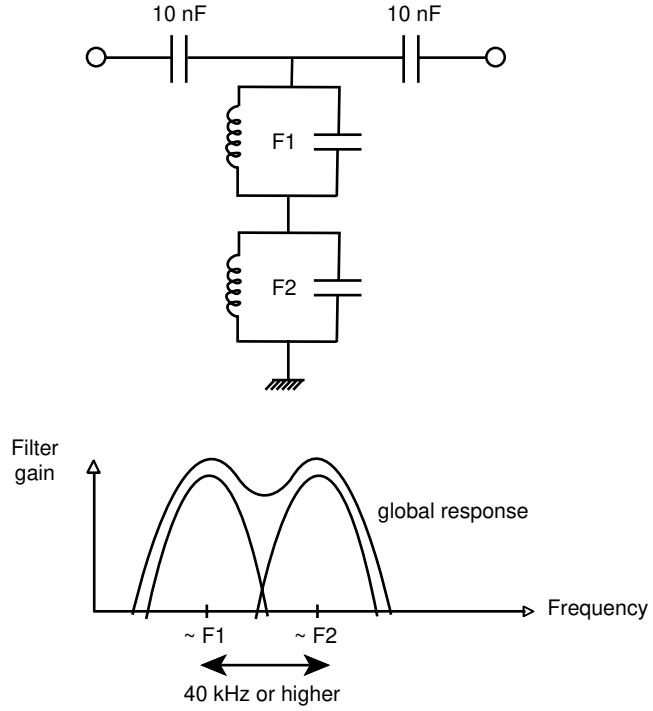


IF2 Filtering and Gain

IF2 filtering achieves a narrow channel selection. In case it is not used, it should be replaced by a > 1 nF coupling capacitor, thus the IF1 filter is the only part achieving the channel selection. Available commercial filters with a 35 kHz BW allow data rates up to 19.6 kbps if crystal temperature drifts are very low.

For faster communications and/or wider channelization, this ceramic filter can be replaced by an LC band-pass filter as proposed hereafter.

Figure 16. LC Band-pass Filter

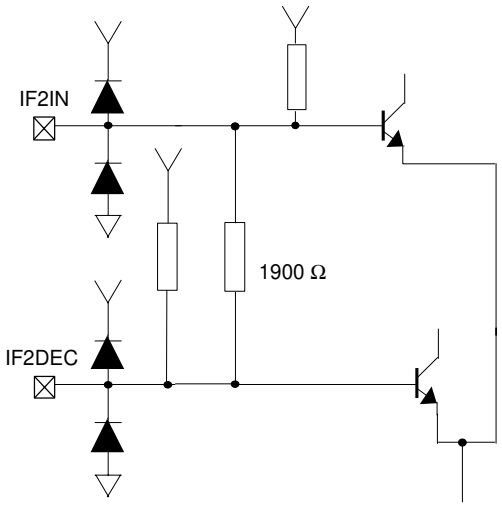


- 10 nF capacitors cut DC response forward and backward.
- The first network has the low cut-off frequency.
- The second network has the high cut-off frequency.

IF2 Amplifier Chain

The input impedance of the IF2 amplifier is 1700Ω. This value enables the use of popular filters with impedance between 1500Ω and 2000Ω. It is directly connected to the FSK demodulator. The bandwidth is internally limited to 1 MHz to minimize the noise before the discriminator. It acts like a band pass filter centered at 455 kHz with capacitive coupling between stages of amplifier and mixer. Total voltage gain is typically 86 dB. Thanks to the capacitive coupling, no slow DC feedback loop is needed enabling a fast turn on time. IF2DEC has to be decoupled with at least 2.2 nF.

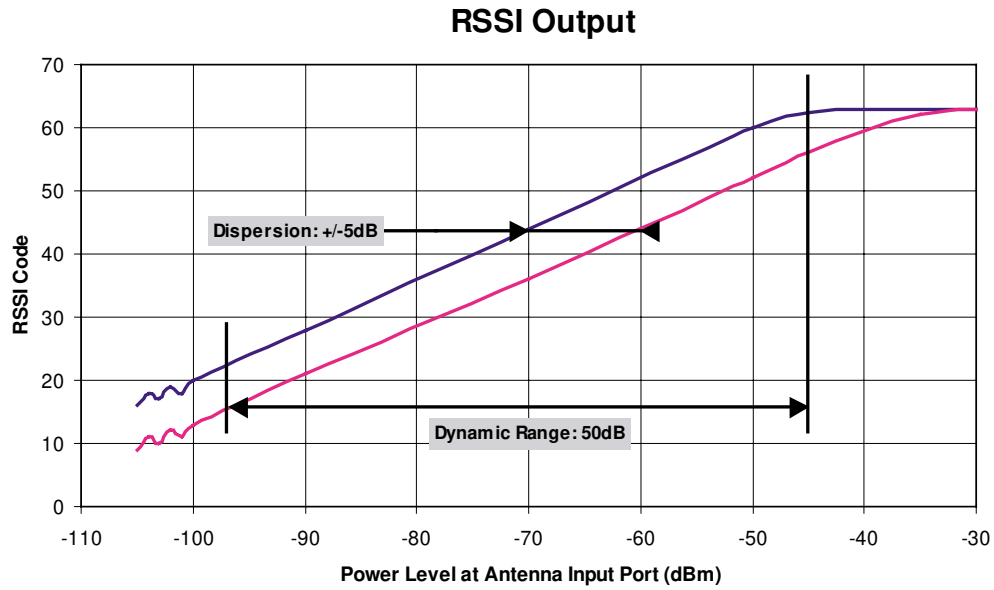
Figure 17. Input of the IF2 Amplifier Schematic



RSSI Output

The RSSI value can be read as a 6 bits word in the STATUS register. Its value is linear in dB as plotted below:

Figure 18. Typical RSSI output (board implementation, T = 25°C, V_{CC} = 3V)



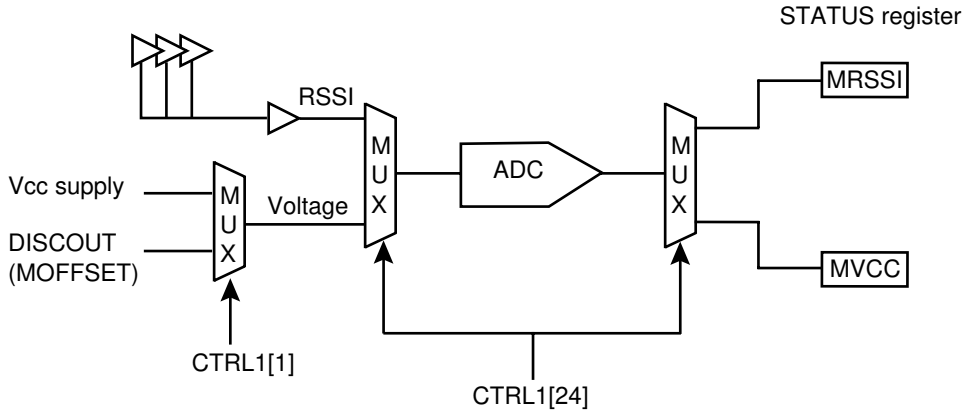
Note: Should the RSSI be required for accurate measurement purpose (precision better than 5 dB), then it is possible to measure one value with a calibrated RF source and store it into the microcontroller, during the production testing.

The RSSI dynamic range is 50 dB from -95 dBm to -45 dBm RF input signal power, over temperature and power supply ranges. The RSSI LSB's value weighs about 1.3 dB in the linear area. The RSSI value is measured from the IF2 chain.

The RSSI is periodically measured thanks to a successive approximation ADC with a 12 µs clock. Thereafter, the time needed to complete the right code depends on the power step: a 10 dB step on the aerial leads to a 10/1.3 = 8 clock cycles, i.e. 96 µs (full range from code 0 to 63 = 756 µs). Its value can be compared with a user predefined value (TRSSI), so that the demodulated data is enabled only if the RSSI value is above this threshold. Some hysteresis effect may be added (see CTRL1 register's content).

The AT86RF211 also has the possibility to measure another voltage. The ADC measuring the RSSI can be turned into voltage or discriminator output DC level measurement.

Figure 19. ADC Converter Input Selection



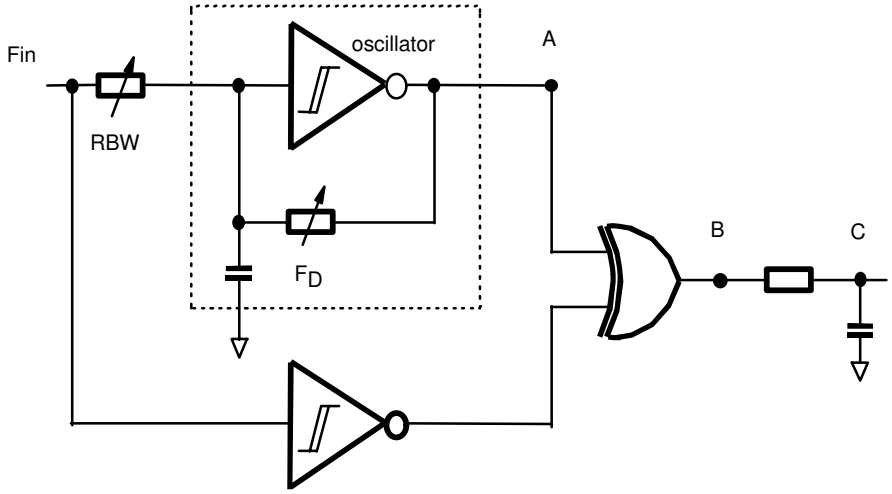
Note: For voltage measurement, the LSB weighs 85 mV and the reference voltage is 1.25V.

The ADC measuring the RSSI can be turned into voltage or discriminator output DC level measurement.

FSK Demodulator

Its structure is based on an oscillator:

Figure 20. Schematic of the FSK demodulator



The oscillator's natural frequency is F_D and it actually oscillates at the Fin frequency. The signal at the output of the oscillator (point A) is proportional to the frequency difference between Fin and F_D. The XOR function translates the difference into a pulse duty cycle (point B).Thereafter by low-pass filtering of the signal is obtained a mean voltage of the signal (point C).

The architecture of this demodulation is thereby analog and allows the transmission of continuous data stream of the same value as the output voltage is proportional to the input frequency. Thus it is not mandatory to use Manchester encoding and the first bit is correctly demodulated.

The oscillator feedback resistor controls the center frequency F_D. It is adjusted according to the output of a dummy FSK demodulator driven by a 455 kHz internal reference frequency which is a division of the reference crystal. The discrete components connected to pin 32 DISCFILT are the loop filter of the PLL stabilizing the 455 kHz signal.

The input RBW resistor controls the discriminator bandwidth. This bandwidth is selected by CTRL1[6]. The default value is "standard discriminator BW". The slope of the discriminator increases by 5 mV/kHz/V with V_{CC} and is 14 mV at 2.4V.

Example:

V_{CC} = 3V implies +17 mV/kHz sensitivity for the demodulator
V_{CC} = 3.6V implies +20 mV/kHz sensitivity for the demodulator

Data Slicer

The analog signals at the output of the discriminator (DISCOUT, pin 27) are converted into CMOS level data by a high resolution comparator called a Data Slicer.

The Data Slicer has a reference for its comparator which can be chosen thanks to CTRL1[4]. The reference sets the comparison level of the comparator. One option is to extract the average value of the demodulated signal on the SKFILT pin (25), this is the external mode. The other option is to set an absolute value for this reference (internal mode).

- External mode:

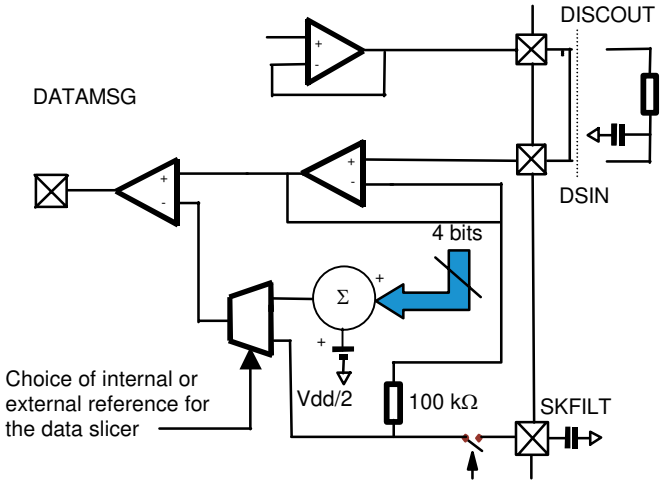
The external mode uses the average value of the demodulated signal as the comparison level for the comparator. Thus there must be enough transitions in the message to ensure that the average value remains between the "0" level and the "1" level. Manchester encoding can be used in this mode as well as DC-free encoding schemes. The choice for SKFILT capacitor is a trade-off between the maximum duration of a constant bit (whatever "0" or "1") and the max allowed settling time to charge this capacitor after powering up.

Note: The SKFILT pin is in high impedance state during the "sleep" period of the Wake Up mode, so that the level is kept constant and there is no need to charge again this tank.

- Internal mode:

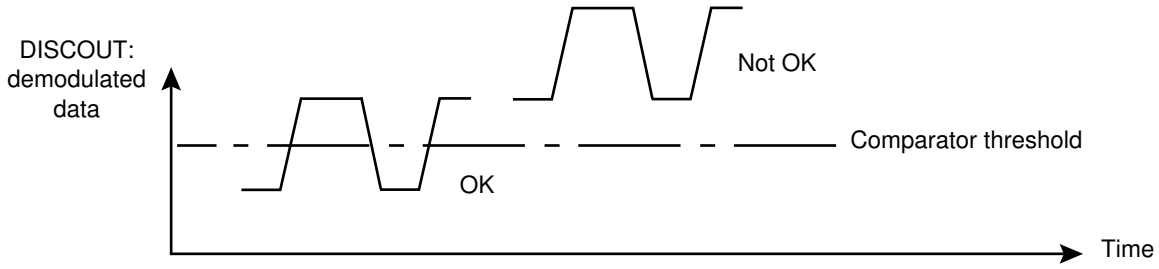
The internal mode uses the output of a DAC as the comparison level. Once this threshold has been correctly set, an "absolute" data slicing of the demodulated signal is possible: no need for DC-free modulation scheme (it is possible to send a "0" or "1" infinitely).

Figure 21. Schematic of the Data Slicer



To operate this way, the user must make sure that the "0" and "1" level at the output of the discriminator are "on both sides" of the comparison level in order for the decision to be made properly.

Figure 22. How to Set Up the Data Slicing Parameters



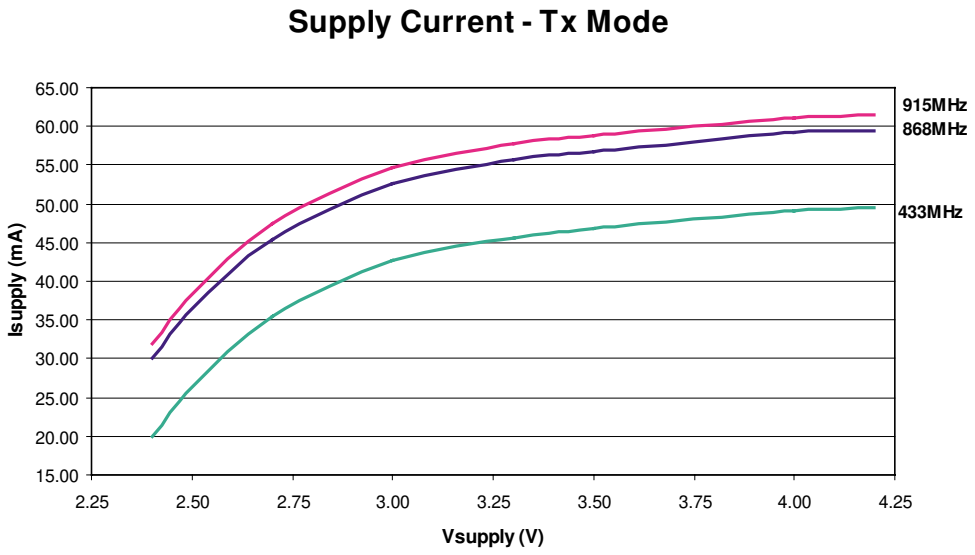
To set the discriminator and the Data Slicer accordingly:

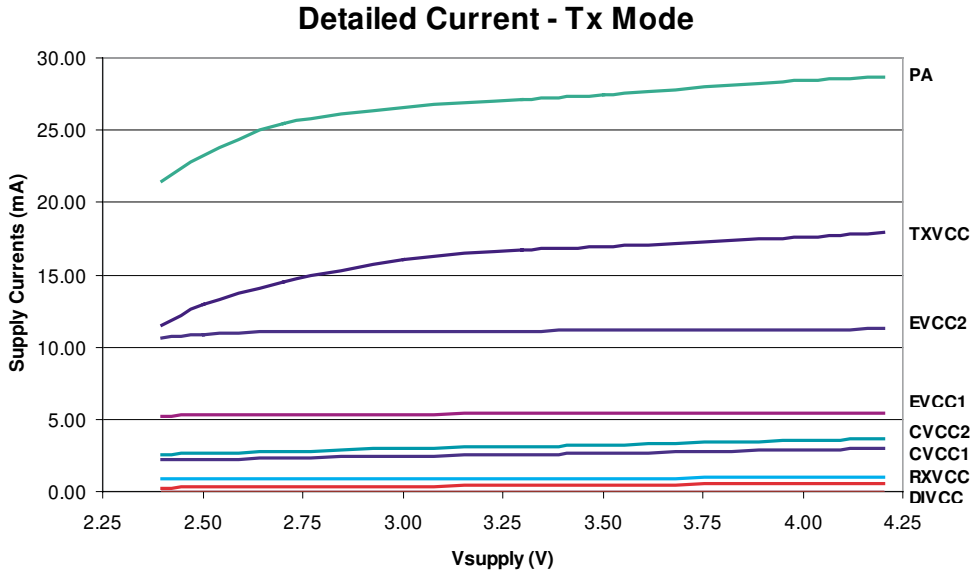
- It is possible to measure the output DC level of the discriminator DISCOUT (thanks to the A/D embedded converter)
- DTR[1:0] make it possible to shift (up or down) the DC level at the output of the discriminator :
  - DTR[1] = 1: +180 mV + 77x (V_{CC} - 2.4V)
  - DTR[0] = 1: -180 mV - 77x (V_{CC} - 2.4V)
- DTR[5:2] make it possible to tune the comparison threshold around $V_{CC}/2$. 16 levels are possible, with a LSB = 15 mV per Volt of supply voltage. $V_{CC}/2$ corresponds to DTR[5:2] = 0111, and the RESET value is 1000.

These procedures can be made automatically by software. Please refer to the application note.

Transmitter Description

Figure 23. Typical Expected Currents in Tx Mode



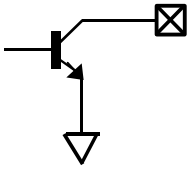


Power Amplification

The Power Amplifier has been built to deliver more than +10 dBm, i.e. 10 mW in the three popular frequency bands. This power level is intended to be measured on the aerial port with a correct output matching network. Note that a correct calculation of the matching network guarantees an optimal power efficiency.

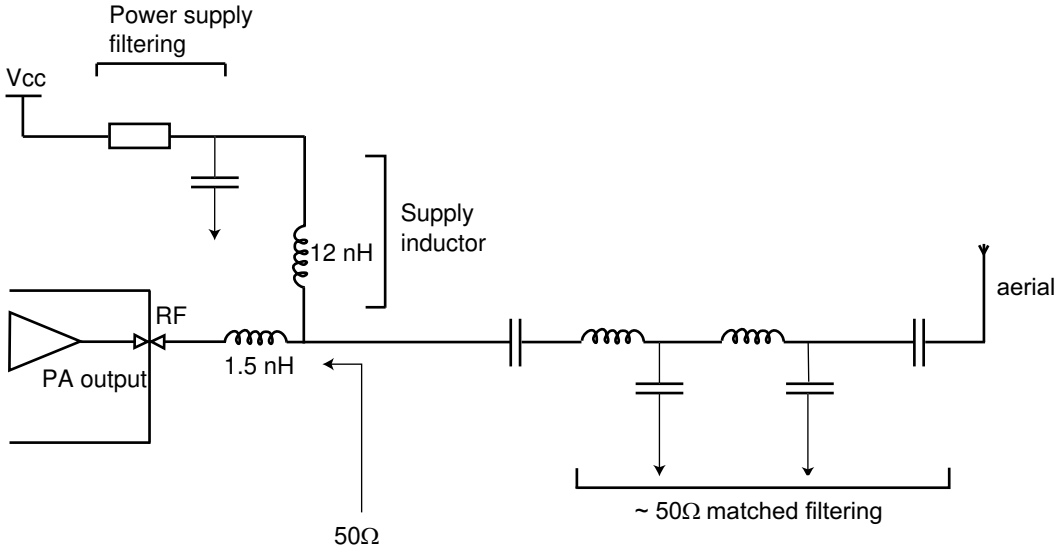
Naturally, the greater the PA output voltage swing, the better the power efficiency. As the PA output is supplied through an inductor, a swing of 2 x V_{DD} is possible. In practice, due to saturation effects, the voltage swing is limited to approximately (2 x V_{DD}) - 1V. With a power supply voltage of 3V, the PA output voltage is 5V peak-to-peak, or 1.77 V_{EFF}.

Figure 24. Output of the Power Amplifier



The PA must be correctly matched to deliver the best efficiency in terms of output power and current consumption. Here is an example of the typical recommended output network in the 868 MHz band:

Figure 25. Output Matching at 868 MHz



Note: The filter is designed to meet relevant regulations. Please refer to application note for details.

A benefit of this network is to filter the output signal harmonic levels; hence it can be designed to meet a particular regulation.

It is mandatory to implement low impedance grounding techniques. Excessive inductor values to ground will not only limit the PA output voltage swing, but may also trigger RF instability. Board design is vital to avoid parasitic loss when high output power is needed (direct short connection to a single low impedance ground plane).

An automatic level control loop (ALC) is integrated, in order to minimize the sensitivity of the PA to the temperature, process and power supply variations. For instance, at +85°C, the output power is about 2 dB less than at 25°C. At -40°C, the output power is higher than at 25°C. The ALC is controlled by a current which is generated in the following way:

Figure 26. ALC of the Power Amplifier

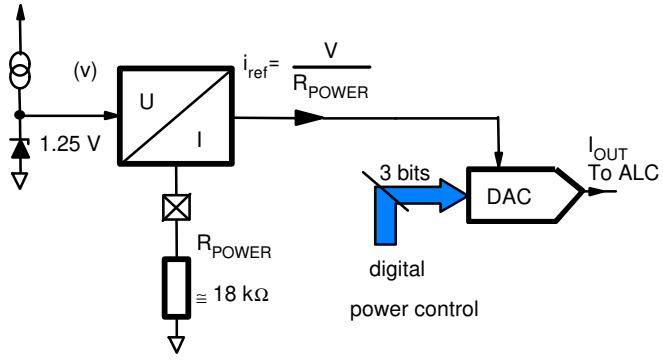
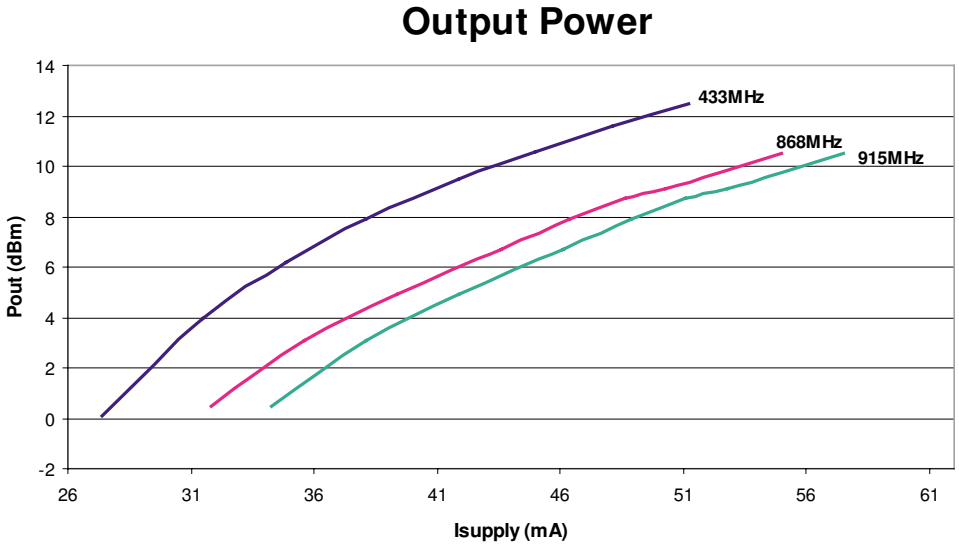


Figure 27. Typical Output Power of the PA for T = 25°C and V_{CC} = 3V

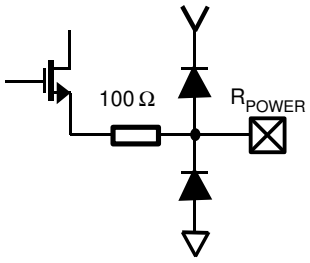


Hardware Control

The max output power is determined by R_{POWER} and the maximum output power is obtained with R_{POWER} = 10 kΩ.

18 kΩ is the nominal value for a +10 dBm output in the 868 MHz frequency band. Decreasing this value to 10 kΩ will lead to +14 dBm at 433 MHz, +12 dBm at 868 MHz, +10 dBm at 915 MHz (typical values for conducted output power).

Figure 28. R_{POWER} Input Schematic



Note: Keeping the PA output matched guarantees maximum power efficiency.

Software Control

The power can then be adjusted, from the value set by R_{POWER} down to a maximum of 12 dB below, by programming the bits 6 to 8 of the CTRL1 register. So, 8 levels are digitally selectable with a variation of the output power. The minimum regulated output power is set to -10 dBm.

Table 3. Software Control of the Power Level

TXLVL (CTRL1)	Pout at 433 MHz (dBm)	Pout at 868 MHz (dBm)	Pout at 915 MHz (dBm)
000	0	-2	-3
001	4	0	0
010	6	3	2
011	8	5	4
100	10	7	5
101	11	8	7
110	12	9	8
111	13	10	9

Note: Unless otherwise specified, typical data given for R_{POWER} = 18 kΩ, T = 25°C, V_{CC} = 3 V

Control Logic

Serial Data Interface

The application microcontroller can control and monitor the AT86RF211 through a synchronous, bidirectional, serial interface made of 3 wires:

- SLE: enable input
- SCK: clock input
- SDATA: data in/out

When SLE = ‘1’, the interface is inhibited, i.e. the SCK and SDATA (in) values are not propagated into the IC, reducing the power consumption and preventing any risk of parasitic write or read cycle.

A “read” or “write” cycle starts when SLE is set to ‘0’ and stops when SLE is set to ‘1’. Only one operation can be performed in one access cycle: only one register can be either read or written.

- **Register Interface Format**

A message is made of 3 fields:

- address A[3:0]: 4 bits (MSB first)
- R/W: read/write selection
- data D[31:0]: up to 32 bits (MSB first)

ADDRESS				R/W	DATA up to 32 bits (variable length)		
A[3]	A[2]	A[1]	A[0]	R/W	MSB	D[nbit-1:0]	LSB

Variable register length and partial read or write cycles are supported.

In case of partial read or write cycles, the first data (in or out) is always the MSB of the register.

- **WRITE Mode (R/W = 1)**

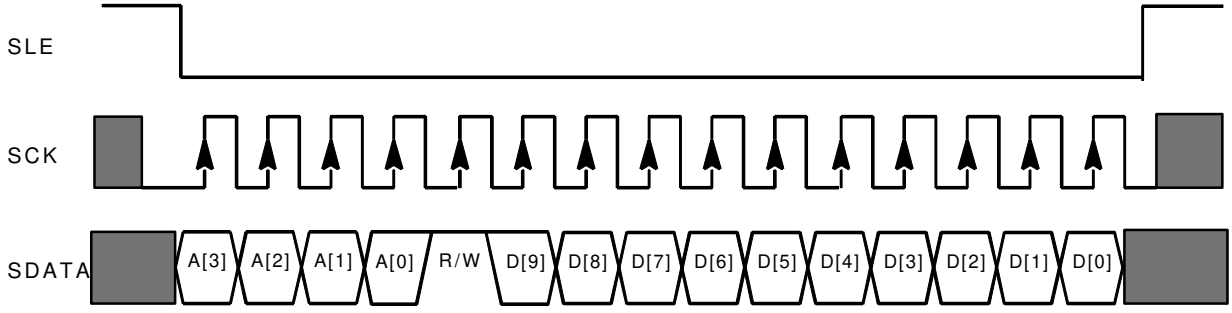
The address, R/W and data bits are clocked on the rising edge of SCK.

If the number of data bits is lower than the register capacity, the LSB bits keep their former value allowing safe partial write. If the number of data bits is greater than the register capacity, the extra bits are ignored.

The data is actually written into the register on the rising edge of SLE when the data length is less or equal to the register length.

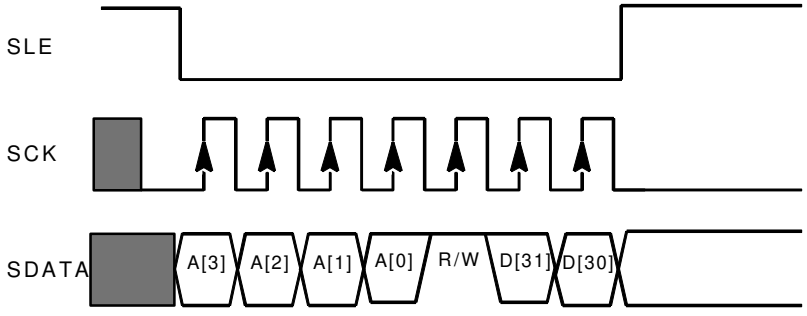
When trying to write more data than the register length, data field is written on the first extra rising clock edge regarding register length.

Figure 29. Write Chronogram: Complete Write Cycle in a 10 bits Register



The complete register of 10 bits is updated on a rising edge of SLE.

Figure 30. Write Chronogram: Partial Write Cycle, Writing 2 bits



Only the 2 MSBs are updated on the rising edge of SLE; other register bits are unchanged.

- **READ Mode (R/W = 0)**

The address and R/W bits are clocked on the rising edge of SCK.

The data bits are changed on the falling edge of SCK. The MSB of the register is the first bit read.

SDATA I/O pin is switched from input to output on the edge following the "1" clocking the R/W bit.

It is possible to stop reading a register (SLE back to “1”) at any time.

If an attempt to read more bits than the register capacity is detected, SDATA is clamped to “0”.

If the address of a register is not valid, SDATA is set to “1” during the first 32 SCK periods, then to “0” during all the extra periods.

SDATA is switched back to the input state when SLE is back to “1”.

Figure 31. Read Chronogram: Complete Read Cycle from a 10 bits Register

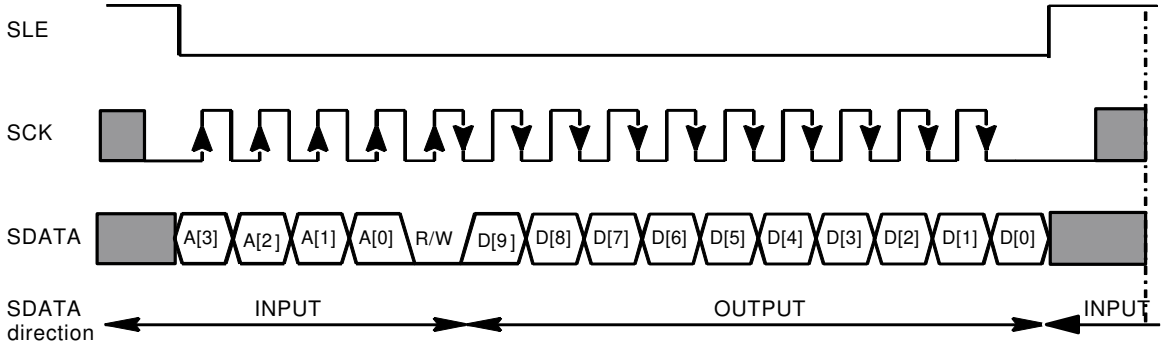


Figure 32. Read chronogram: Partial Read Cycle, Reading 2 bits

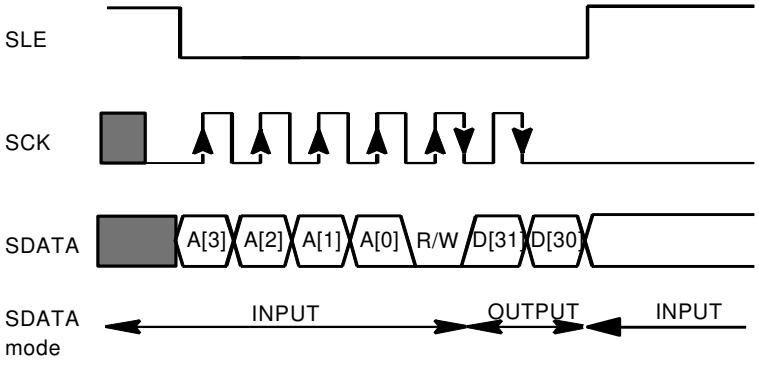
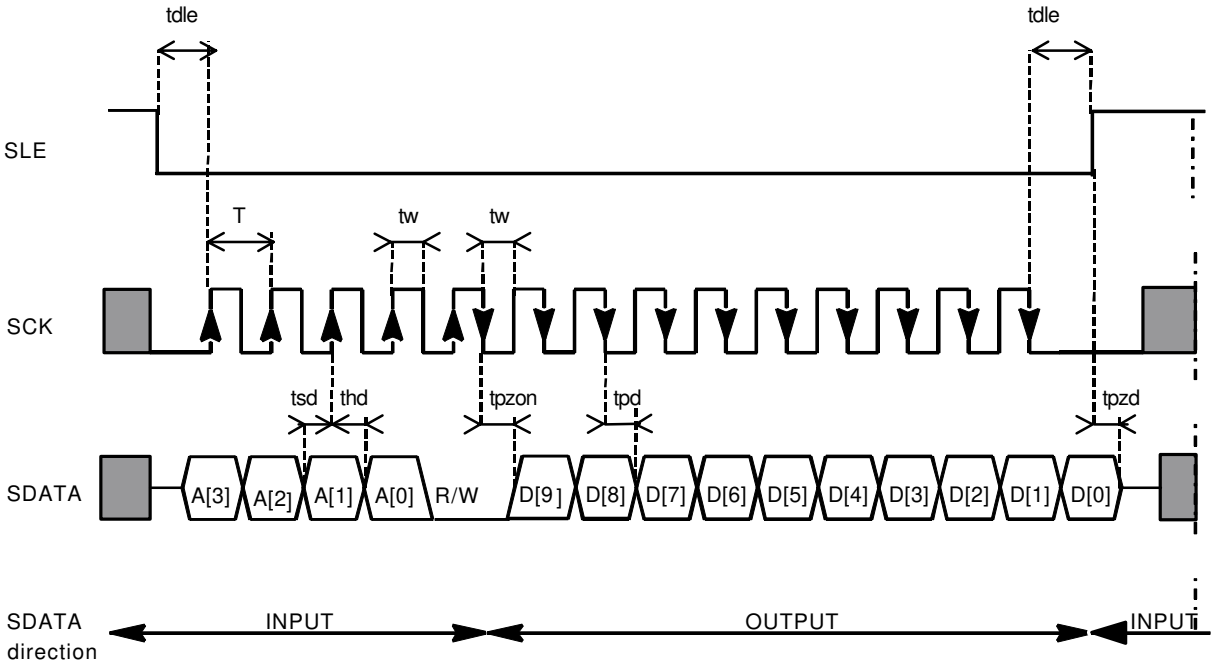


Figure 33. Chronogram with Timing



Note: For the timing specification, please refer to the timing table “Digital CMOS DC Characteristics” on page 42.

Registers

Table 4. Registers Overview

Name	Address A[3:0]	Nbits	Read-Write	Comments
F0	$(0000)_2$	32	R-W	F0 Frequency Code
F1	$(0001)_2$	32	R-W	F1 Frequency Code
F2	$(0010)_2$	32	R-W	F2 Frequency Code
F3	$(0011)_2$	32	R-W	F3 Frequency Code
CTRL1	$(0100)_2$	32	R-W	Main Control Register
STAT	$(0101)_2$	31	R	Status Register
DTR	$(0110)_2$	6	R-W	Data Slicer Reference/Discriminator offset adjusting
WUC	$(0111)_2$	32	R-W	Wake-up Control Register
WUR	$(1000)_2$	18	R-W	Wake-up Data Rate Register
WUA	$(1001)_2$	25	R-W	Wake-up Address Register
WUD	$(1010)_2$	32	R	Wake-up Data Register
RESET	$(1011)_2$	1	W	Reset
-	$(1100)_2$			Reserved
-	$(1101)_2$			Reserved
-	$(1110)_2$			Reserved
CTRL2	$(1111)_2$	32	R-W	Control Register (Lock Detect - Clock Recovery)

Note: All the registers must be reprogrammed after the voltage supply has been removed, otherwise they will be in the default state