Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Atmel AT86RF215 Device Family

Sub-1GHz/2.4GHz Transceiver and I/Q Radio for IEEE Std 802.15.4™-2015 IEEE Std 802.15.4g™-2012 ETSI TS 102 887-1

AT86RF215 / AT86RF215IQ / AT86RF215M

DATASHEET

Features AT86RF215

- Fully integrated radio transceiver covering 389.5-510MHz / 779-1020MHz / 2400-2483.5MHz including:
  - European band: 863-870MHz / 870-876MHz / 915-921MHz
  - Chinese band: 470-510MHz / 779-787MHz
  - North American band: 902-928MHz
  - Korean band: 917-923.5MHz
  - Japanese band: 920-928MHz
  - World-wide ISM band: 2400-2483.5MHz
- I/Q data interface:
  - One TX and two RX serial low voltage differential signal (LVDS) interfaces
  - 13-bit I/Q data interface with a sampling frequency of up to 4MHz
- Transceiver Control interface: SPI (serial peripheral interface)
- Supported PHYs (*proprietary)
  - MR-FSK
    - Symbol rates: 50, 100, 150, 200, 300*, 400ksymbol/s
    - Rate 1/2-FEC: RSC and NRNSC, with and without interleaving
    - Order: 2-level, 4-level
  - MR-OFDM
    - Option 1: 100, 200, 400, 800, 1200*, 1600*, 2400*kb/s
    - Option 2: 50, 100, 200, 400, 600, 800, 1200*kb/s
    - Option 3: 50, 100, 200, 300, 400, 600kb/s
    - Option 4: 50, 100, 150, 200, 300kb/s
  - MR-O-QPSK
    - 100kchip/s with 6.25, 12.5, 25, 50kb/s data rate
    - 200kchip/s with 12.5, 25*, 50*, 100*kb/s data rate
    - 1000kchip/s with 31.25, 125, 250, 500kb/s data rate
    - 2000kchip/s with 31.25, 125, 250, 500, 1000*kb/s data rate
  - O-QPSK
    - 1000kchip/s with 250kb/s and 500*kb/s data rate
    - 2000kchip/s with 250kb/s and 1000*kb/s data rate
- Bi-directional differential RF signal ports for:
  - Band I: 433/470/780/863/868/915/917/920MHz
  - Band II: 2450MHz

- Simultaneous operation of sub-1GHz and 2.4GHz transceiver
- Separate 2kbytes RX and TX frame buffer
- IEEE MAC support
  - Frame filter (IEEE Std 802.15.4-2006)
  - FCS handling
  - Automatic acknowledgement (IEEE Std 802.15.4-2006)
  - CCA with automatic transmit
- Industry leading link budget
  - Programmable TX output power up to +14.5dBm@900MHz band
  - Noise figure below 5dB for sub-1GHz and 2.4GHz transceiver
  - Receiver sensitivity down to -123dBm at 6.25kb/s MR-O-QPSK
- Radio transceiver features
  - Integrated TX/RX switch, LNA, PLL loop filter and RF frontend control
  - Fast settling PLL supporting frequency hopping
  - Automatic filter calibration
- Received signal strength indicator / energy detection
- True random number generator
- Optimized for low BOM cost and ease of production
- Low power supply voltage from 1.8V to 3.6V
- Internal voltage regulators and battery monitor
- Reduced power consumption (RPC) modes for MR-FSK and MR-OQPSK
- Low current consumption (incl. baseband processing / without I/Q interface)
  - Deep sleep 30nA
  - RX listen 6..28mA (RPC mode dependent)
  - RX active 28mA
  - TX 62mA @14dBm output power
- Industrial temperature range from –40°C to +85°C
- 48-pin low-profile lead-free plastic QFN package

1. Description

The AT86RF215 is a multi-band radio transceiver for various sub-1GHz bands and the 2.4GHz band specially designed for smart metering and applications implementing IEEE Std 802.15.4g™-2012 [3], ETSI TS 102 887-1 [5], IEEE Std 802.15.4™-2015 [7].

The device is comprised of two independent transceivers, each with its own baseband and I/Q data interface. The AT86RF215 incorporates two transceivers and two baseband cores forming two independent radio systems. The transceivers are highly integrated minimizing the number of external components required on the printed circuit board (PCB). The supply voltage ranges from 1.8V to 3.6V. A 26MHz temperature controlled oscillator (TCXO) or a crystal oscillator (XTAL) is used as a reference clock.

The AT86RF215 allows simultaneous independent reception in the sub-1GHz and 2.4GHz bands. Each radio frequency (RF) port is accessed with balanced differential signal pairs. Optimal sensitivity and output power are achieved with 50Ω differential load. The device offers a high link budget with maximum TX output power of 14.5dBm@900MHz and sensitivity down to -123dBm@MR-OQPSK-6.25kb/s.

The device is controlled via a fast serial peripheral interface (SPI). Dedicated MAC hardware, random number generator and on-board battery monitoring improve overall system efficiency and timing.

The AT86RF215 can be operated with an external microcontroller (e.g. Atmel SAM4 Family) and/or an external baseband processor.

1.1 Device Family

1.1.1 Overview

Table 1-1. Device Family Overview

Device	Description
AT86RF215	• Dual band transceiver and I/Q radio • Embedded baseband supporting MR-FSK, MR-OFDM, MR-O-QPSK, and O-QPSK • Compliant to IEEE Std 802.15.4g™-2012 [3]; IEEE Std 802.15.4™-2011 [2]; ETSI TS 102 887-1 [5], IEEE Std 802.15.4™-2015 [7]
AT86RF215IQ	• I/Q radio (13-bit I/Q low voltage differential signal (LVDS) interface)
AT86RF215M	• Sub-1GHz Transceiver and I/Q radio • Embedded baseband supporting MR-FSK, MR-OFDM, MR-O-QPSK, and O-QPSK • Compliant to IEEE Std 802.15.4g™-2012 [3]; ETSI TS 102 887-1 [5]

Note: For operation of the AT86RF215M see "Basic Operation of AT86RF215M" on page 42.

1.1.2 Device Identification

The device identifier can be read from the register RF_PN. The version number of the device can be read from the register RF_VN.

1.1.3 Register Description

1.1.3.1 RF_PN – Device Part Number

The register contains the part number of the device.

Bit	7	6	5	4	3	2	1	0	
(0x000D)	PN								RF_PN
Read/Write	R	R	R	R	R	R	R	R	

- **Bit 7:0 – RF_PN.PN: Device Part Number**

The register contains the part number of the device.

Table 1-2. PN

Sub-register	Value	Description
PN	0x34	AT86RF215
	0x35	AT86RF215IQ
	0x36	AT86RF215M

1.1.3.2 RF_VN – Device Version Number

The register contains the version number of the device.

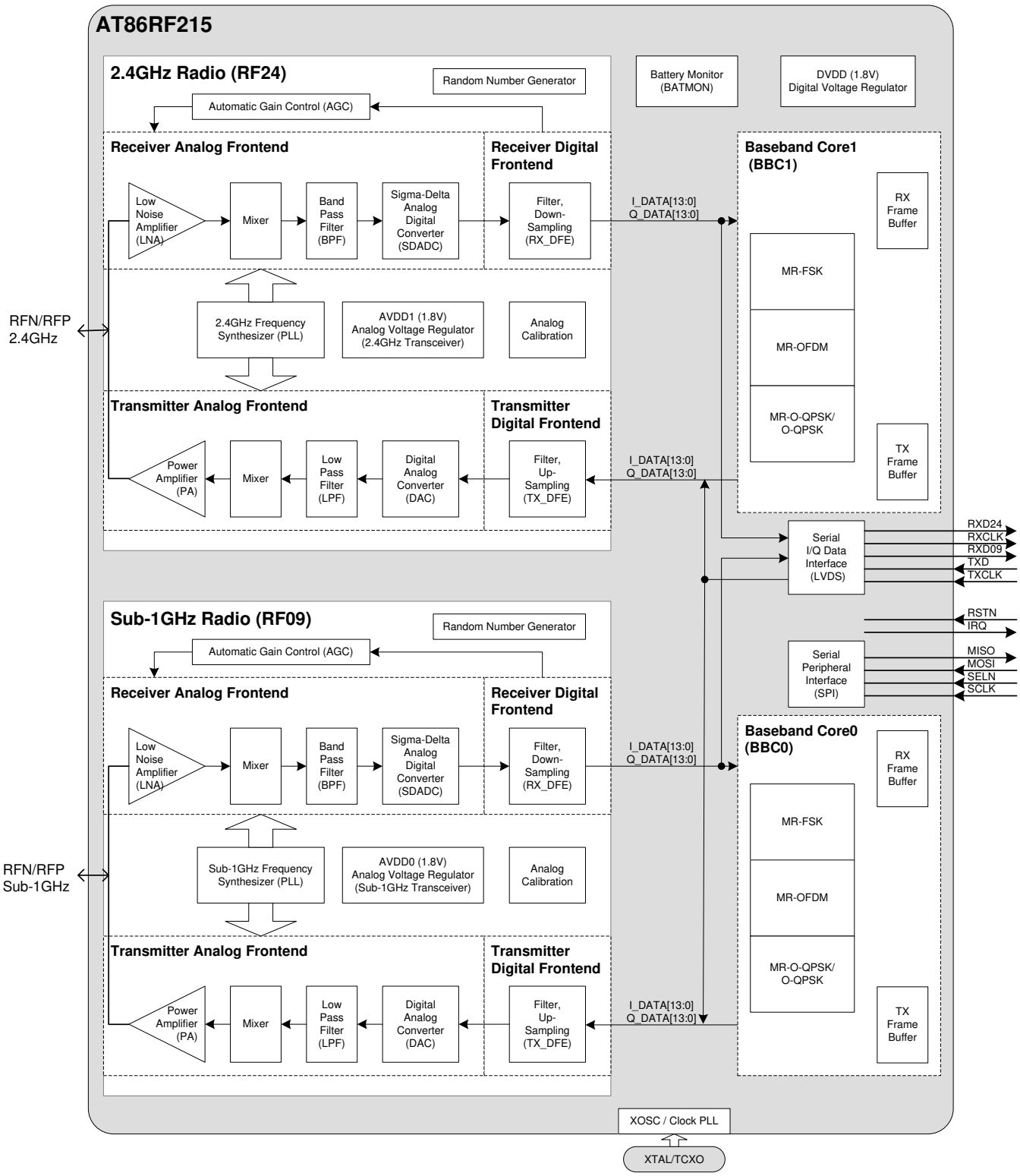
Bit	7	6	5	4	3	2	1	0	
(0x000E)	VN								RF_VN
Read/Write	R	R	R	R	R	R	R	R	
Initial Value v.1	0	0	0	0	0	0	0	1	
Initial Value v.3	0	0	0	0	0	0	1	1	

1.2 Block Diagram

The device features two independent radio systems. It contains one sub-1GHz transceiver and one 2.4GHz transceiver. Each transceiver is paired with a baseband core optimized to demodulate signals commonly used in the associated band, thus providing complete RF-to-Baseband operation. The internal baseband cores support MR-FSK, O-QPSK/MR-O-QPSK and MR-OFDM modulation schemes. Alternatively users can route the I/Q data stream directly to an external processor for advanced signal processing using the 13-bit LVDS interface.

The AT86RF215 block diagram is shown in Figure 1-1.

Figure 1-1. AT86RF215 Block Diagram



Notes: 1. Baseband Core0/1 are not available at AT86RF215IQ

2. 2.4GHz Radio (RF24) and Baseband Core1 (BBC1) are not available at AT86RF215M

1.3 Control Logic and Naming Conventions

Both radio and baseband cores have separate register blocks. The sub-1GHz radio register names are prefixed by “RF09_”. The 2.4GHz radio transceiver register names are prefixed by “RF24_”. The register descriptions, including sub-register descriptions, for both radios and their respective basebands are identical. In rare cases where a register is only valid for one specific radio (or baseband), the register for the other radio (or baseband) is ignored.

The baseband processor Core0 is connected to the sub-1GHz radio and Core1 is connected to the 2.4GHz radio.

The baseband registers of Core0 are prefixed by “BBC0_”. The baseband register of Core1 are prefixed by “BBC1_”. The general reference for both core registers is prefixed by “BBCn_”. Both cores are identical and have separate register spaces.

Common registers of the AT86RF215 which are not specific for the radio or baseband are prefixed by “RF_”.

Note, the datasheet refers to the naming convention of IEEE Std 802.15.4g™-2012 [3] in regards to multi rate and multi regional frequency (MR) PHYs. The IEEE Std 802.15.4™-2015 [7] names the PHYs SUN, i.e. smart metering utility network.

2. Pin-out Diagram and Description

2.1 Pin-out Diagram

The pin-out of the AT86RF215 is shown in Figure 2-1.

Figure 2-1. Pin-out

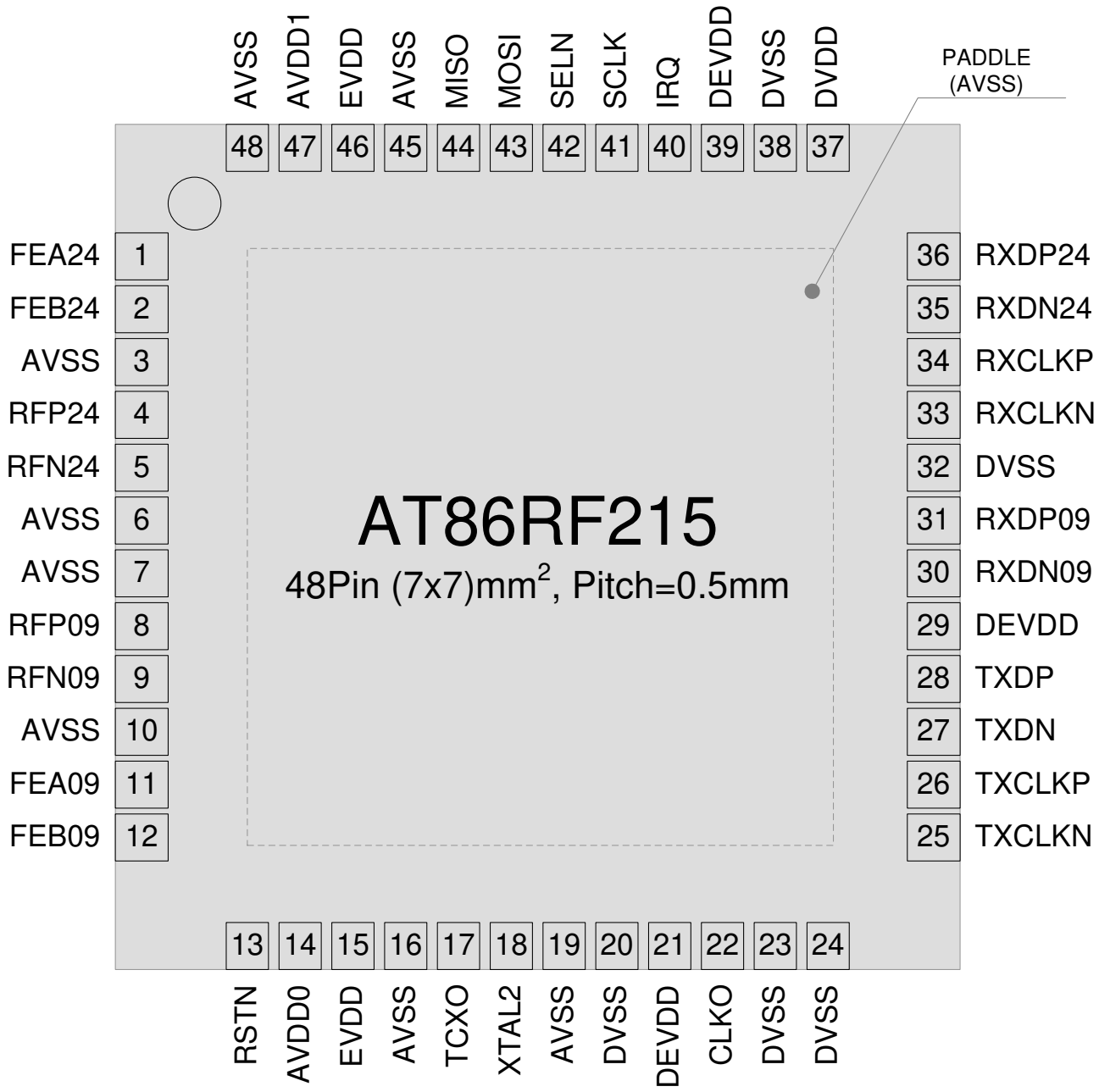


Table 2-1. Pin Description

# Pin	Name	Type	Description
1	FEA24	Output	RF frontend control; digital output for the 2.4GHz transceiver
2	FEB24	Output	RF frontend control; digital output for the 2.4GHz transceiver
3	AVSS	In/Out	Analog ground (RF)
4	RFP24	In/Out	Differential RF input/output 2.4GHz (positive)
5	RFN24	In/Out	Differential RF input/output 2.4GHz (negative)
6	AVSS	In/Out	Analog ground (RF)
7	AVSS	In/Out	Analog ground (RF)
8	RFP09	In/Out	Differential RF input/output for sub-1GHz transceiver (positive)
9	RFN09	In/Out	Differential RF input/output for sub-1GHz transceiver (negative)
10	AVSS	In/Out	Analog ground (RF)
11	FEA09	Output	RF frontend control; digital output for the sub-1GHz transceiver
12	FEB09	Output	RF frontend control; digital output for the sub-1GHz transceiver
13	RSTN	Input	Reset input (active low)
14	AVDD0	In/Out	Internal regulated analog 1.8V supply output voltage (internally generated) for analog circuitry of the sub-1GHz transceiver
15	EVDD	Input	External analog supply voltage (V_{DD}); 3.0V typical
16	AVSS	In/out	Analog ground
17	TCXO	Input	TCXO or crystal oscillator (26MHz) input
18	XTAL2	Output	Crystal oscillator
19	AVSS	In/Out	Analog ground
20	DVSS	In/Out	Digital ground
21	DEVDD	Input	External digital supply voltage (V_{DD}); 3.0V typical
22	CLKO	Output	Clock output
23	DVSS	In/Out	Digital ground
24	DVSS	In/Out	Digital ground
25	TXCLKN	Input	Differential TX I/Q clock interface input (negative)
26	TXCLKP	Input	Differential TX I/Q clock interface input (positive)
27	TXDN	Input	Differential TX I/Q data interface input (negative)
28	TXDP	Input	Differential TX I/Q data interface input (positive)
29	DEVDD	Input	External digital supply voltage (V_{DD}); 3.0V typical
30	RXDN09	Output	Differential RX I/Q data interface output sub-1GHz transceiver (negative)
31	RXDP09	Output	Differential RX I/Q data interface output sub-1GHz transceiver (positive)
32	DVSS	In/Out	Digital ground
33	RXCLKN	Output	Differential RX I/Q clock interface output (negative)
34	RXCLKP	Output	Differential RX I/Q clock interface output (positive)
35	RXDN24	Output	Differential RX I/Q data interface output 2.4GHz transceiver (negative)
36	RXDP24	Output	Differential RX I/Q data interface output 2.4GHz transceiver (positive)
37	DVDD	In/Out	Internal regulated supply output voltage (internally generated) for digital circuitry
38	DVSS	In/Out	Digital ground

# Pin	Name	Type	Description
39	DEVDD	Output	External digital supply voltage (V_{DD}); 3.0V typical
40	IRQ	Output	Interrupt output
41	SCLK	Input	SPI interface clock input
42	SELN	Input	SPI select input (active low)
43	MOSI	Input	SPI data input
44	MISO	Output	SPI data output
45	AVSS	In/Out	Analog ground
46	EVDD	Input	External analog supply voltage (V_{DD}); 3.0V typical
47	AVDD1	In/Out	Internal regulated analog 1.8V supply output voltage (internally generated) for analog circuitry for the 2.4GHz transceiver
48	AVSS	In/Out	Analog ground

2.2 Pin Description

2.2.1 RFP09/RFN09, RFP24/RFN24

The differential RF pins (RFP09/RFN09; RFP24/RFN24) provide common-mode rejection to suppress the switching noise of the internal and external digital signal processing blocks.

A 50Ω differential load at the RF ports ensures high sensitivity and output power. A DC path between the RF pins is supported; a DC path to ground or supply voltage is not supported. When connecting an RF load providing a DC path to the power supply or ground, AC coupling is required.

The pins RFP24/RFN24 of AT86RF215M are shortened to AVSS internally and may not be connected.

2.2.2 EVDD, DEVDD (V_{DD})

EVDD is the external analog supply voltage. DEVDD is the external digital supply voltage. External decoupling capacitors must be placed close to these device pins. EVDD and DEVDD must be shorted at board level and should always have the same potential.

2.2.3 AVDD0, AVDD1

AVDD0 and AVDD1 are internally generated/regulated analog supply voltages. External compensation capacitors must be placed close to these device pins. These supplies are activated, and de-activated, by the sleep-mode logic. Do not use these signals as references or power supplies. AVDD0 and AVDD1 must not be shorted. For further information about the analog supply voltages are described in section "Voltage Regulator" on page 75.

An external compensation capacitor at the pin AVDD1 is not required for AT86RF215M, the pin can have no connections.

2.2.4 DVDD

DVDD is an internally generated/regulated digital supply voltage. An external compensation capacitor must be placed close to this device pin. For further information about the digital supply voltage are described in section "Voltage Regulator" on page 75.

2.2.5 AVSS, DVSS

AVSS is the analog ground; DVSS is the digital ground voltage. The analog and the digital grounds should be separated on the PCB and only connected at a single point on the PCB.

2.2.6 MISO, MOSI, SCLK, SELN

Pins MISO, MOSI, SCLK and SELN are SPI specific pins which provide register read/write access for device operation. For further information about the control interface see section "SPI Transceiver Control Interface" on page 16.

2.2.7 RXDN09/RXDP09, RXDN24/RXDP24, RXCLKP/RXCLKN, TXDP/TXDN, TXCLKP/TXCLKN

Pins RXDN09/RXDP09, RXDN24/RXDP24, RXCLKP/RXCLKN, TXDP/TXDN and TXCLKP/TXCLKN are low voltage differential signal (LVDS) I/Q data interface pins. For further information see section "Serial I/Q Data Interface" on page 22.

The pins RXDN24/RXDP24 are not supported for AT86RF215M, the pins shall have no connections.

2.2.8 IRQ

Pin IRQ is the interrupt pin from the transceiver to the microcontroller and is controlled by both radios and basebands. The interrupt source can be detected by reading the interrupt status registers using the device control interface (SPI). For further information about IRQ configuration see section "Interrupt Signalling" on page 19.

2.2.9 RSTN

Pin RSTN is the active low reset pin. For further information see section "Reset Modes " on page 13.

2.2.10 FEA09/FEB09, FEA24/FEB24

The digital output pins FEAnn and FEBnn can control an external RF analog frontend device, in general external LNA, PA. For each transceiver band two frontend control pins are specified. The pins are not differential. For further information see section "External Frontend Control" on page 70.

The pins FEA24/FEB24 are not supported for AT86RF215M, the pins shall have no connections.

2.2.11 TCXO/XTAL2

Pin TCXO (Temperature Controlled Crystal Oscillator) is the input pin of a 26MHz clock from a TCXO device. Pin XTAL2 must be grounded if operating the device with a TCXO.

Alternatively, the device can be operated with a 26MHz Crystal (XTAL) which must be connected between pin TCXO and pin XTAL2. For further information see section "Crystal Oscillator and TCXO" on page 67.

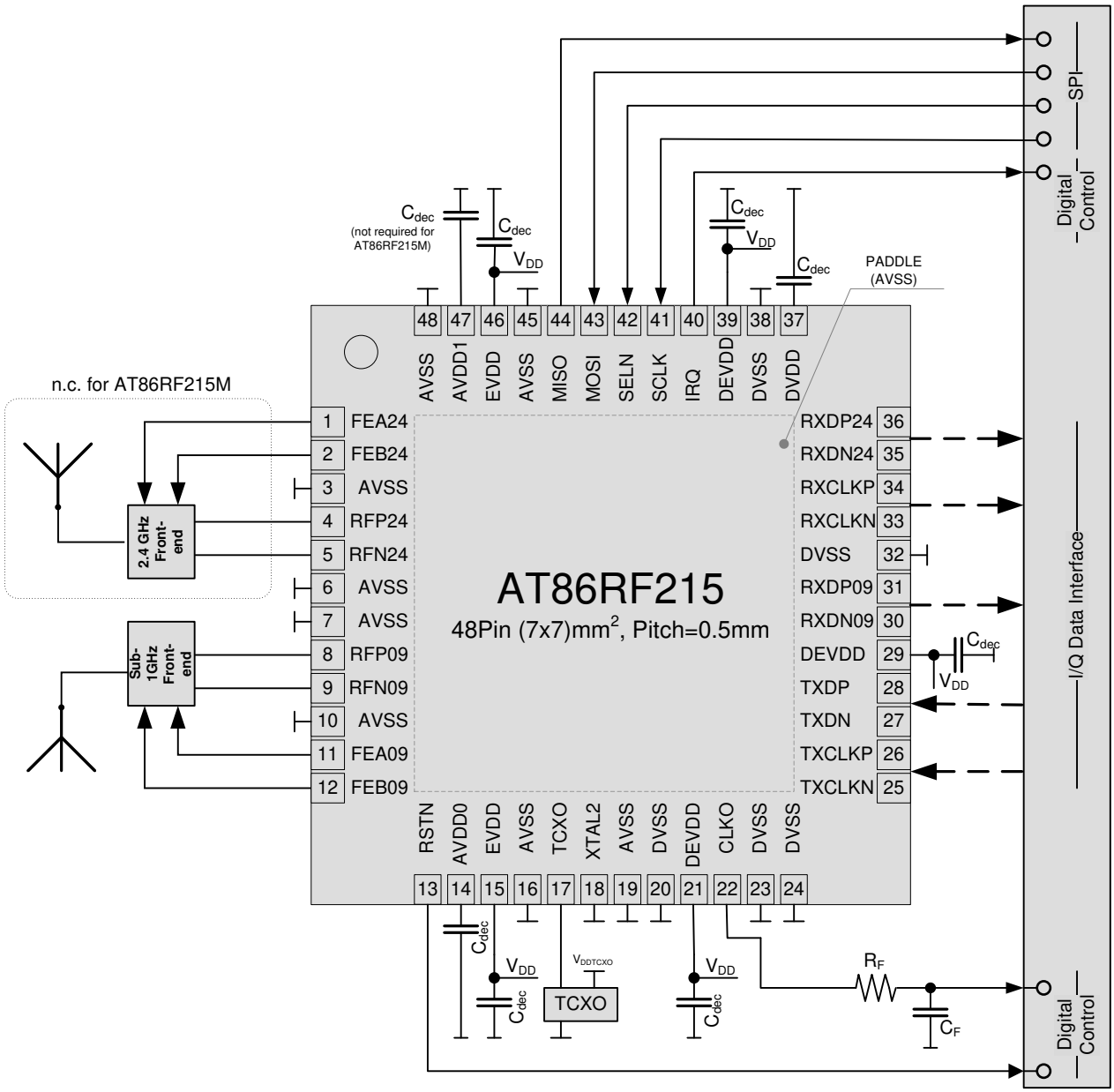
2.2.12 CLKO

Pin CLKO provides a clock output signal. An external microcontroller can use this clock signal as an input clock source. For further information about the clock output configuration see "Clock Output" on page 20.

3. Application Schematic

A basic application schematic of the AT86RF215 is shown in Figure 3-1. The RF ports require a 50Ω differential load for best RF performance. The transceiver is operated with a 26MHz TCXO.

Figure 3-1. Basic Application Schematic



The external analog power supply EVDD, the external digital power supply DEVDD and the integrated voltage regulators outputs AVDD0, DVDD and AVDD1 must be decoupled by a capacitor (C_{dec}). All decoupling capacitors should be placed as close as possible to the pins and should have low-resistance and low-inductance connection to ground. EVDD and DEVDD must be shorted at PCB level and should always have the same potential (V_{DD}).

A low-pass filter (C_F, R_F) should be placed close to pin CLKO to reduce the emission of CLKO signal harmonics. This is not needed if pin CLKO is not used as a microcontroller clock source. In this case, clock output signal should be disabled during device initialization, see register RF_CLKO.

The pins RFP24/RFN24 of the AT86RF215M are connected to AVSS and must not be connected. The pins RXDP24/RXDN24 are not supported for the AT86RF215M and can be left opened.

4. Control and Data Interfaces

4.1 Reset Modes

4.1.1 Summary Reset Modes

The AT86RF215 can be reset by the following conditions:

- Power-on reset or voltage drop, see section "Power-on Reset" below
- Chip Reset command, see section "Chip Reset" on page 14
- Chip Reset via pulse at pin RSTN, see section "Chip Reset" on page 14
- Transceiver Reset, see section "Transceiver Reset" on page 14
- State SLEEP, see section "State SLEEP" on page 34
- State DEEP_SLEEP, see section "State DEEP_SLEEP and Wake-up Procedure" on page 34

The AT86RF215 registers can be classified into register groups for common chip functionality, for the I/Q data interface, for the sub-1GHz transceiver and for the 2.4GHz transceiver. Table 4-1 shows which register groups are reset by which reset source.

Table 4-1. AT86RF215 Reset Modes

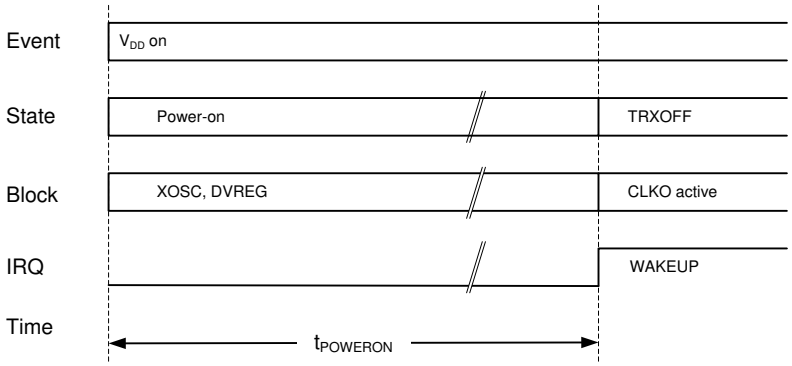
Reset Source	Common Chip Register	I/Q Data Interface Register	Sub-1GHz Transceiver Register	2.4GHz Transceiver Register
	RF_CFG, RF_XOC, RF_CLKO and RF_BMDVC	RF_IQIFC0 and RF_IQIFC1	RF09_* and BBC0_*	RF24_* and BBC1_*
Power-On Reset	reset	reset	reset	reset
Chip Reset	reset	reset	reset	reset
Sub-1GHz Transceiver Reset			reset	
2.4GHz Transceiver Reset				reset
Sub-1GHz Transceiver SLEEP			reset	
2.4GHz Transceiver SLEEP				reset
DEEP_SLEEP		reset	reset	reset

4.1.2 Power-on Reset

A power-on reset is initiated if the supply voltage drops below the operating range of the voltage regulator (see section "Voltage Regulator" on page 75) and returns back to the supported range again. For further information about the operation range see section "Operating Range" on page 187.

The power-on procedure is shown in Figure 4-1.

Figure 4-1. Power-on Procedure



When the external supply voltage (V_{DD}) is initially supplied to the AT86RF215, the device enables the crystal oscillator (XOSC) and the internal 1.8V voltage regulator for the digital domain (DVREG). After $t_{POWERON}$ the output clock signal is available at pin CLKO at default clock rate of 26MHz. During the power-on procedure, all registers are set to their default values. As soon as the state TRXOFF is reached, the SPI is enabled and it can be used to control the device. At the same time, the interrupt IRQS.WAKEUP at both transceivers is set to 1 and the pin IRQ is asserted high.

4.1.3 Chip Reset

The Chip Reset procedure resets the entire device (i.e. both radios, sub-1GHz and 2.4GHz and both baseband cores), all registers are set to their default values.

The Chip Reset is triggered by the pin RSTN or by writing the Chip Reset command. The Chip Reset is triggered by pulling the pin RSTN to low, keeping it low for t_{RST} and to release it to high again; for further timing information see section "Power-on Reset Characteristics" on page 188. To trigger the Chip Reset via the Chip Reset command, the value 0x07 needs to be written to the sub-register RF_RST.CMD.

After initiating the Chip Reset procedure, the device enters the internal state RESET. After the reset procedure is completed, the state RESET is left and the state TRXOFF is reached. The completion of the reset procedure is indicated by the interrupt IRQS.WAKEUP for both transceivers.

For further information about state changes see section "State Machine" on page 33.

4.1.4 Transceiver Reset

While the Chip Reset procedure resets the entire device (sub-1GHz/BBC0 *and* 2.4GHz/BBC1), the Transceiver Reset is used to reset only a single transceiver (RF09/BBC0 *or* RF24/BBC1). The Transceiver Reset is initiated by writing the command RESET to the register RFn_CMD of the corresponding transceiver. During the reset procedure the corresponding transceiver state machine is reset and the corresponding transceiver (RFn_*) and baseband registers (BBCn_*) are set to their default values. The common device registers (RF_*) are not reset.

Once the reset procedure is completed, the state TRXOFF is reached and the interrupt IRQS.WAKEUP is issued for the corresponding transceiver.

4.1.5 Register Description

4.1.5.1 RF_RST – Chip Reset

The register RF_RST allows resetting the entire device via an SPI command.

Bit	7	6	5	4	3	2	1	0	
(0x0005)	–	–	–	–	–	CMD			RF_RST
Read/Write	R	R	R	R	R	RW	RW	RW	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 2:0 – RF_RST.CMD: Chip Reset Command**

Writing the value 0x7 to the sub-register CMD triggers the reset procedure of the entire device; the values 0x0 to 0x6 have no effect.

Table 4-2. CMD

Sub-register	Name	Value	Description
CMD	RF_RESET	0x7	CHIP RESET

4.2 SPI Transceiver Control Interface

4.2.1 Introduction

The control interface comprises an SPI slave and provides access to registers and frame buffers of the AT86RF215.

Table 4-3 shows the SPI signals.

Table 4-3. SPI Signals

SPI Signal	Direction	Description
SCLK	Input	SPI clock signal
SELN	Input	SPI select signal, active low
MOSI	Input	SPI data master output, slave input signal
MISO	Output	SPI data master input, slave output signal

The SPI is byte-oriented with bi-directional communication between master and slave. Each byte is transferred with the MSB first. The SPI select signal SELN is active low. The number of clocks at SCLK must be a multiple of eight. The AT86RF215 SPI provides register and frame buffer access in a linear address space. The access mode is configured by the address in the COMMAND bytes.

4.2.2 SPI Protocol

Each SPI sequence starts by setting SELN to low and finishes by releasing SELN to high. After setting SELN to low, the two COMMAND bytes are transferred from the SPI master via pin MOSI followed by SPI clock signals to read or to write data. The two COMMAND bytes define the SPI access mode (read or write access) and the 14-bit address (see Table 4-4).

Table 4-4. SPI COMMAND Definition

Bit[15] MODE[1]	Bit[14] MODE[0]	Bit[13:8] ADDRESS[13:8]	Bit[7:0] ADDRESS[7:0]	SPI Access Mode
COMMAND[15:8]			**COMMAND[7:0]**	
0	0	ADDRESS[13:8]	ADDRESS[7:0]	Read
1	0	ADDRESS[13:8]	ADDRESS[7:0]	Write
0	1	ADDRESS[13:8]	ADDRESS[7:0]	Reserved
1	1	ADDRESS[13:8]	ADDRESS[7:0]	Reserved

The SPI can be operated in single or block access mode. The single access mode (see section 4.2.4) is used to read or to write a single register value. The block access mode (see section 4.2.4) is used to read or to write a block of data with a variable number of data bytes.

4.2.3 Single Access Mode

The single access mode is a three byte operation. First the two COMMAND bytes are transferred on MOSI. If MODE indicates a write access, then the third byte contains the value that is written to the selected address (see Figure 4-2). If MODE indicates a read access, then the content of the selected address is returned with the third byte on pin MISO (see Figure 4-3).

Figure 4-2. SPI Single Write Access

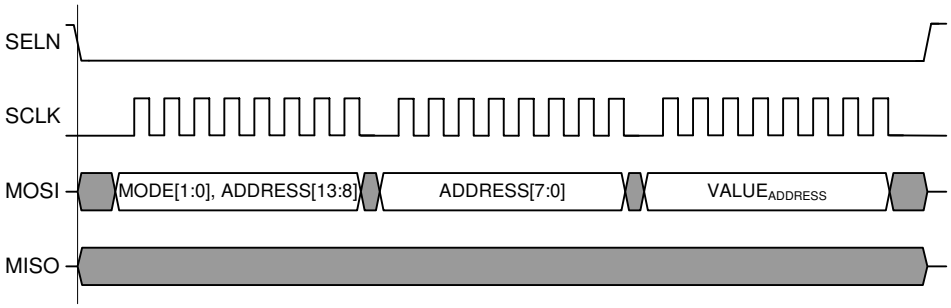
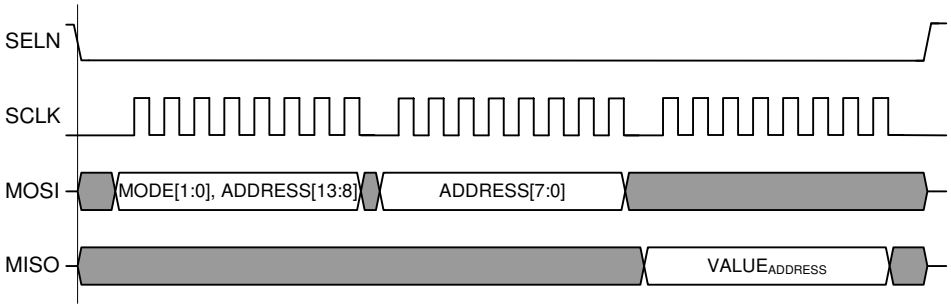


Figure 4-3. SPI Single Read Access



4.2.4 Block Access Mode

The block access mode is entered when SELN remains low after the third byte of the single access mode. During block write access the fourth byte on MOSI is written to the next address (ADDRESS+1) and so on. The same procedure applies to the block read access, where the content of the next address (ADDRESS+1) is returned with the fourth byte on pin MISO. The block mode can access the whole address space (see Figure 4-4 and Figure 4-5).

Figure 4-4. SPI Block Write Access

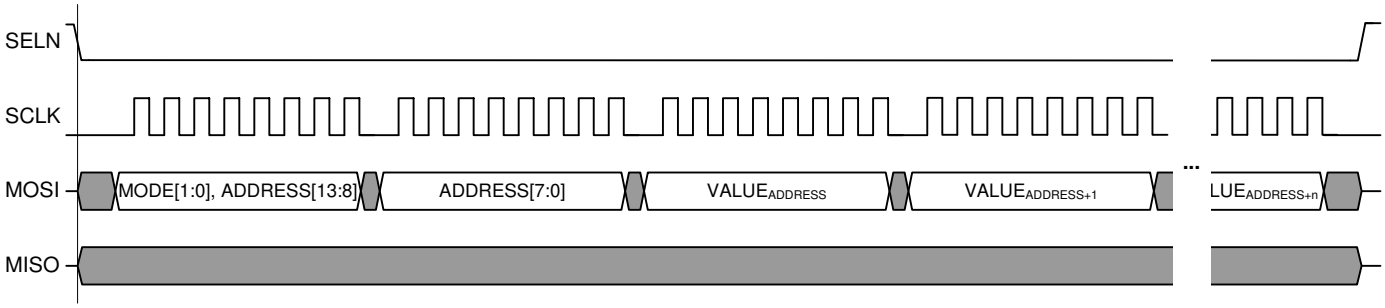
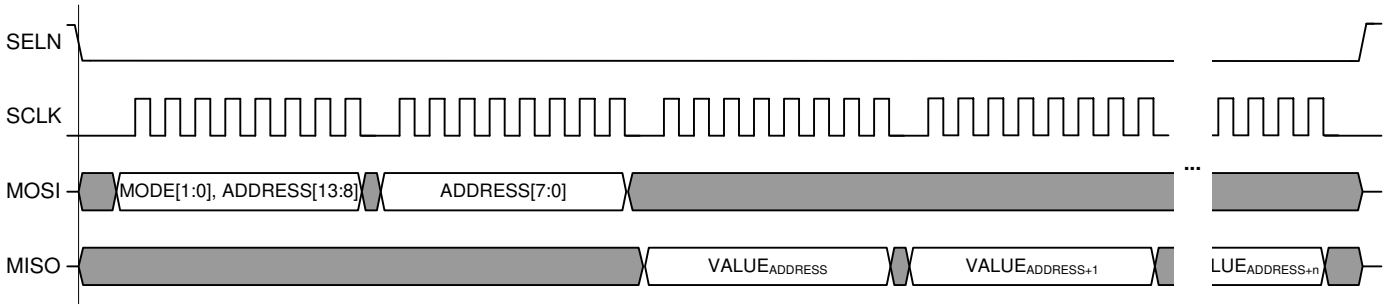


Figure 4-5. SPI Block Read Access



4.2.5 SPI Timing

Figure 4-6 and Figure 4-7 illustrate the SPI timing and its parameters. The corresponding timing parameter values t_{SPI_0} - t_{SPI_9} are defined in section "SPI Timing Characteristics" on page 204.

Figure 4-6. SPI Timing, Definition of Timing Parameters t_{SPI_0}, t_{SPI_5}, t_{SPI_6}, t_{SPI_8}, t_{SPI_9}.

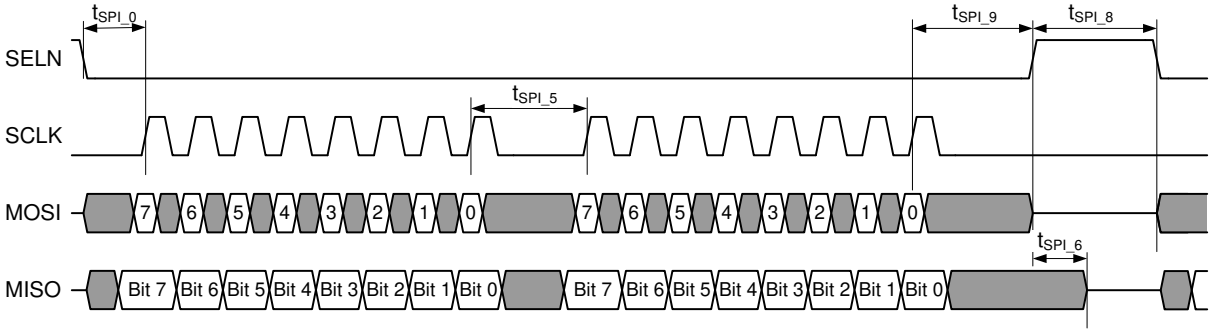
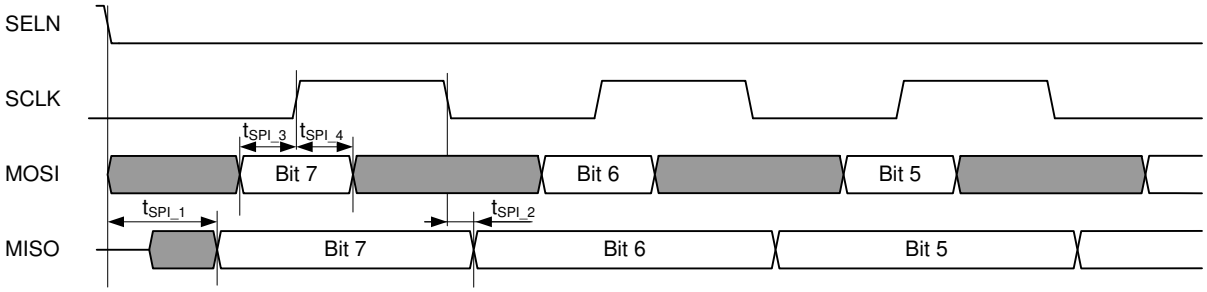


Figure 4-7. SPI Timing, Definition of Timing Parameters t_{SPI_1} to t_{SPI_4}.



SELN low enables the MISO output driver of the AT86RF215. The MSB of values transferred via MISO is valid after t_{SPI_1} and is updated at each falling edge of SCLK. If the MISO driver is disabled (during inactive SPI periods), no internal pull-up circuitry is connected to it. Driving the appropriate signal level must be ensured by the master device or an external pull-up resistor.

Referring to Figure 4-6 and Figure 4-7, the AT86RF215 MOSI is sampled at the rising edge of the SCLK signal. The signal MOSI must be stable before and after the rising edge of SCLK as specified by t_{SPI_3} and t_{SPI_4}. The output (MISO) is initiated at the falling edge of SCLK.

The SPI command is processed at the last rising clock edge of SCLK.

4.3 Interrupt Signalling

The radios and the basebands of the AT86RF215 generate interrupt events. All enabled interrupt events are logically OR'd to form the single external interrupt signal at pin IRQ.

The IRQ behavior and the pad driver strength can be configured by the register RF_CFG. The register RF_CFG content is maintained during state DEEP_SLEEP and is cleared during RESET.

The active polarity of pin IRQ can be configured by sub-register RF_CFG.IRQP. After a reset procedure the polarity is set to active high.

For further information see section "Interrupts" on page 38.

4.3.1 Register Description

4.3.1.1 RF_CFG – IRQ Configuration

The register RF_CFG contains bits to configure the IRQ behavior.

Bit	7	6	5	4	3	2	1	0	
(0x0006)	–	–	–	–	**IRQMM**	**IRQP**	**DRV**		**RF_CFG**
Read/Write	R	R	R	R	RW	RW	RW	RW	
Initial Value	0	0	0	0	1	0	0	1	

- **Bit 3 – RF_CFG.IRQMM: IRQ Mask Mode**

The bit IRQMM configures the IRQ mask mode.

Table 4-5. IRQMM

Sub-register	Value	Description
IRQMM	0x0	Masked IRQ reasons do not appear in IRQS register
	0x1	Masked IRQ reasons do appear in IRQS register

- **Bit 2 – RF_CFG.IRQP: IRQ Polarity**

The bit IRQP configures the IRQ pin polarity.

Table 4-6. IRQP

Sub-register	Value	Description
IRQP	0x0	Active high
	0x1	Active low

- **Bit 1:0 – RF_CFG.DRV: Output Driver Strength of Pads**

The bits DRV configure the pads driver strength of the pins IRQ, MISO, and the frontend control (i.e. FEA09, FEB09, FEA24, FEB24) pins.

Table 4-7. DRV

Sub-register	Name	Value	Description
DRV	RF_DRV2	0x0	2mA
	RF_DRV4	0x1	4mA
	RF_DRV6	0x2	6mA
	RF_DRV8	0x3	8mA

4.4 Clock Output

The AT86RF215 provides a clock output signal at pin CLKO.

The clock output signal is generated by the oscillator module using the external crystal or TCXO; see section "Crystal Oscillator and TCXO" on page 67 for further information about the oscillator configuration.

After reset or power-on the clock output signal is enabled and set to the default clock rate value of 26MHz. The signal's driver strength and the clock frequency can be configured by register RF_CLKO.

Resetting AT86RF215 via Chip Reset causes the register RF_CLKO to be reset to its default value.

In state DEEP_SLEEP the clock output signal is paused. If the device is woken up by writing command TRXOFF to one of the transceiver command registers, the clock output signal continues after $t_{DEEP\_SLEEP\_TRXOFF}$ with the configuration that has been set before entering state DEEP_SLEEP.

If the clock output signal is not used, it is recommended to switch it off. The output signal can be switched off by the sub-register RF_CLKO.OS.

For electrical parameter of the clock output signal see section "Clock Output – pin CLKO" on page 189 and "General Transceiver Specifications" on page 188.

4.4.1 Register Description

4.4.1.1 RF_CLKO – Clock Output

The register RF_CLKO contains configuration bits for the clock output signal. The register setting is maintained during state DEEP_SLEEP.

Bit	7	6	5	4	3	2	1	0	
(0x0007)	–	–	–	DRV			OS		RF_CLKO
Read/Write	R	R	R	RW	RW	RW	RW	RW	
Initial Value	0	0	0	0	1	0	0	1	

- **Bit 4:3 – RF_CLKO.DRV: Output Driver Strength CLKO**

The bit DRV configures the CLKO pad driver strength.

Table 4-8. DRV

Sub-register	Name	Value	Description
DRV	RF_DRVCLKO2	0x0	2mA
	RF_DRVCLKO4	0x1	4mA
	RF_DRVCLKO6	0x2	6mA
	RF_DRVCLKO8	0x3	8mA

- **Bit 2:0 – RF_CLKO.OS: Clock Output Selection**

The bit OS configures the clock output frequency of the CLKO output signal. The change of the clock output frequency occurs immediately and spike free.

Table 4-9. OS

Sub-register	Value	Description
OS	0x0	OFF
	0x1	26MHz
	0x2	32MHz
	0x3	16MHz
	0x4	8MHz
	0x5	4MHz
	0x6	2MHz
	0x7	1MHz

4.5 Serial I/Q Data Interface

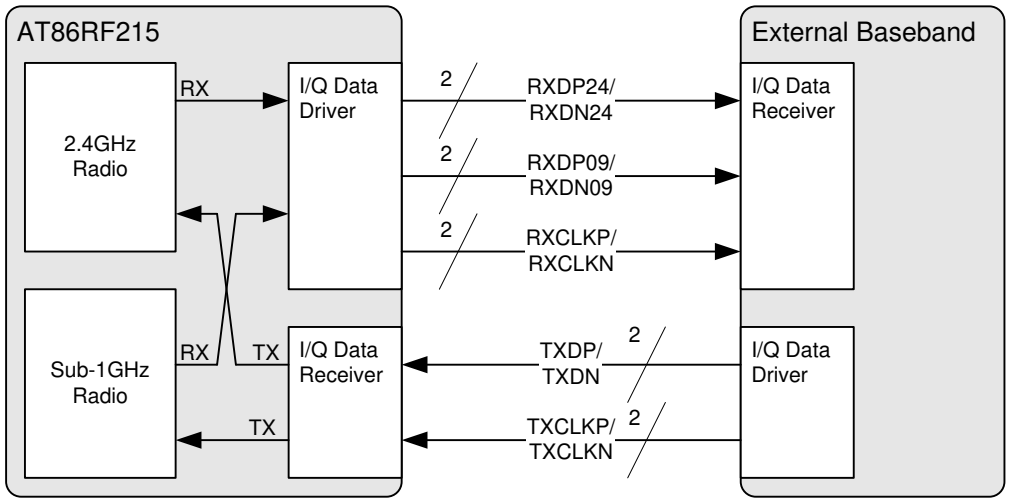
4.5.1 Introduction

A point-to-point, low voltage differential signalling (LVDS) interface is used for the data transfer between the AT86RF215 and an external baseband processor. The implemented interface is based on the IEEE standard 1596.3-1996 (see [4]). The specific interface of the AT86RF215 has a data rate of 128Mb/s composed of 16 data bits at 4MHz for each of the I and Q data streams from the device. The LVDS clock frequency is 64MHz. The interface uses double data rate (DDR). A new data bit is received and transmitted at both the falling and rising edge of the LVDS clock.

In order to decrease current consumption, a proprietary scalable LVDS (SLVDS) interface is implemented in addition to the IEEE standard functionality.

The AT86RF215 data interface consists of two receive and one transmit signal paths. The interface signals are all implemented as differential pairs. Two receive pairs and one clock pair form the LVDS driver. One transmit pair and one clock pair form the LVDS receiver. Within this document the terminologies of I/Q data *driver* and *receiver* are used with reference to the external baseband processor, see Figure 4-8.

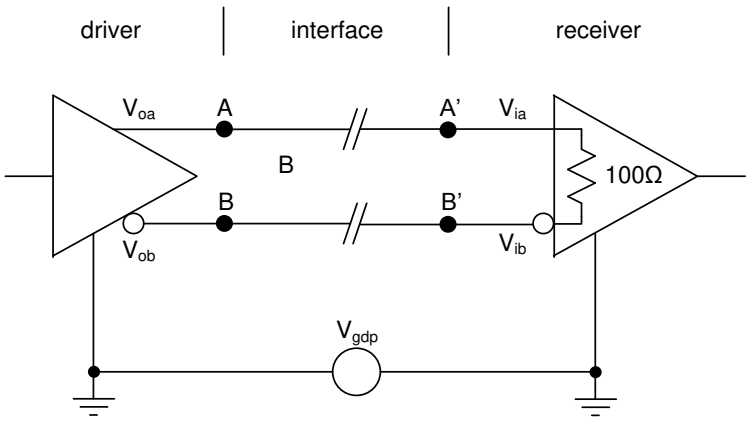
Figure 4-8. I/Q Data Interface



The TXCLK must have the same frequency as the RXCLK signal. There is no requirement on the phase alignment. The RXCLK driver is also enabled while transmitting data, so that the external baseband can derive the TXCLK from the RXCLK, see Table 10-34 on page 206 and Table 10-35 on page 207 for the required phase relation between clock and data.

The driver and receiver should be on the same printed circuit board (PCB) and have a small ground potential V_{gdb} (see Figure 4-9 on page 23) difference. The length of the PCB wires between the devices is expected to be short and their differential impedance should be 100Ω.

Figure 4-9. I/Q Data Interface Structure (Refer to [4])



4.5.2 Configuration

The proprietary SLVDS link has a low voltage swing of 200mV with a common mode offset voltage of 200mV. The differential lines must be terminated with a 100Ω differential impedance. This termination is included in the I/Q data receiver of the AT86RF215. Voltage swing and offset can be adjusted with sub-registers IQIFC0.DRV and IQIFC0.CMV. Note that a higher voltage swing also increases the current consumption.

The I/Q data interface can also be operated with a common mode voltage of 1.2V. In this way the AT86RF215 can communicate with common LVDS interfaces compliant to the IEEE standard 1596.3-1996 [4]. The higher common mode voltage is selected if bit IQIFC0.CMV1V2 is set to 1. If it is set to 1, the sub-register IQIFC0.CMV has no function.

The I/Q data interface receivers operate over a wide input common mode range. They have a differential input hysteresis and a fail safe circuit. The hysteresis avoids amplifying small signal noise at zero input voltages. Input voltages can be zero when receiver inputs are open or the connected drivers are powered down. The hysteresis means that an input signal must change by more than Vhyst (see Table 10-32 on page 206) to toggle the receiver output. If no driver circuit is connected to the inputs, the fail safe circuit sets the sub-register IQIFC1.FAILSF to 1 and the internal pull-ups force the open inputs to DEVDD.

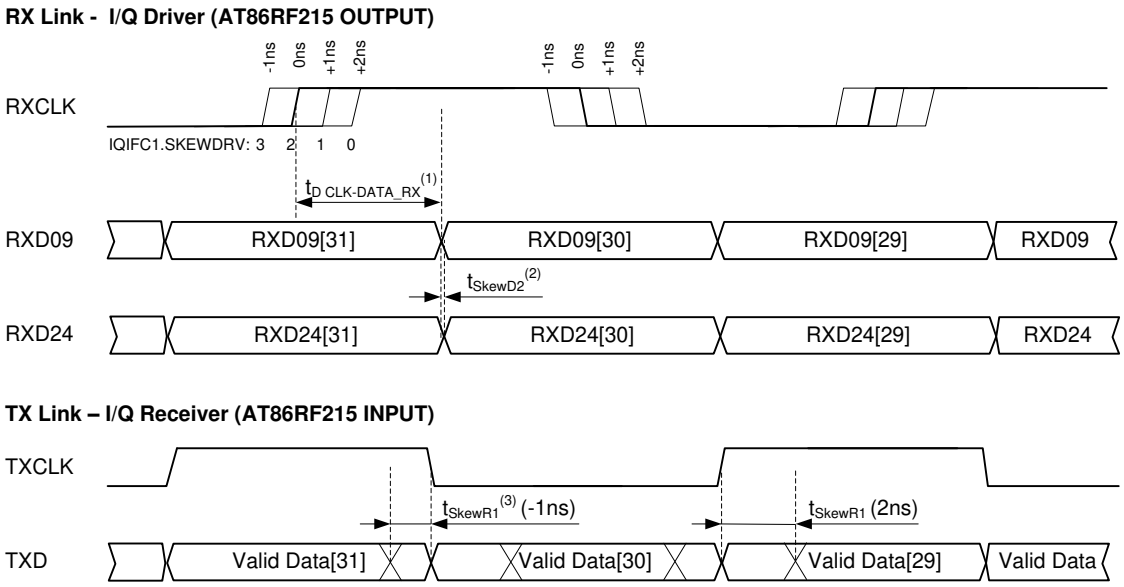
Refer to chapter "Electrical Characteristics" on page 187 for a complete list of all DC and AC characteristics of the LVDS interface.

4.5.3 Characteristics and Timing

Double data rate is implemented to clock the data using both negative and positive clock edges. The data sent by the AT86RF215 (transceiver state RX) is center aligned. The data received from an external baseband processor (transceiver TX) must be edge aligned. Uneven data bits are related to the rising clock edge. Even data bits are related to the falling clock edge (see Figure 4-10 on page 24).

The skew between RX clock and data can be adjusted to match the timing requirement of the LVDS input of an external baseband processor. The skew alignment parameter is set by the sub-register IQIFC1.SKEWDRV. Figure 4-10 shows the functionality of the skew alignment. The skew settings must only be altered when the LVDS interface is off (for example in state TRXOFF).

Figure 4-10. Clock to Data Timing Alignment



Notes:
1. Programmable clock to data delay at the I/Q data interface driver (for details refer to register IQIFC1.SKEWDRV on page 28 and section "I/Q Data Interface Driver AC Specification" on page 206)
2. LVDS data channel to LVDS data channel skew (see section "I/Q Data Interface Driver AC Specification" on page 206)
3. Skew tolerable at receiver input to meet setup and hold time requirements (see section "I/Q Data Interface Receiver AC Specification" on page 207)

The data sampling rate f_s ranges from 400ksample/s to 4Msample/s and is defined by the registers RFn_TXDFE and RFn_RXDFE. The interface transfers the I/Q data in 32-bit data words with a fixed rate of 4Mword/s. This results in a fixed rate of 128Mb/s with a double data rate clock frequency of 64MHz at the interface.

An IDLE period must be inserted between each 32-bit data word if a lower sampling rate f_s is used. During the IDLE period zero words are transmitted. A zero word consists of 32 zero bits.

The interface must be DC coupled, because the bit stream is not DC balanced.

4.5.4 Word Format

The I/Q data interface is based on serializing/de-serializing a 32-bit word. The 32-bit word is composed of a two bit I synchronization pattern followed by a 14-bit I data word and a two bit Q synchronization pattern followed by a 14-bit Q data word (see Table 4-10 below).

Table 4-10. I/Q Data Interface Word Frame Format

Bit[31:30]	Bit[29:16]	Bit[15:14]	Bit[13:0]
I_SYNC = 0b10	I_DATA[13:0]	Q_SYNC = 0b01	Q_DATA[13:0]

The actual baseband signal data is contained in sub-fields I_DATA[13:1] and Q_DATA[13:1], each interpreted as 13-bit 2's complement signed values with {I,Q}_DATA[13] being the sign bit and {I,Q}_DATA[1] being the least significant bit.

For the transmit I/Q data (pin TXD) TX control information can be embedded in the bit I_DATA[0]. In this case, embedded TX control must be enabled in the register IQIFC0.EEC and the bit Q_DATA[0] must be zero. If embedded TX control is not enabled, the bits {I,Q}_DATA[0] are not interpreted.

For the receive I/Q data (pin RXD09/24) the bits {I,Q}_DATA[0] are not used and always equal to 0.

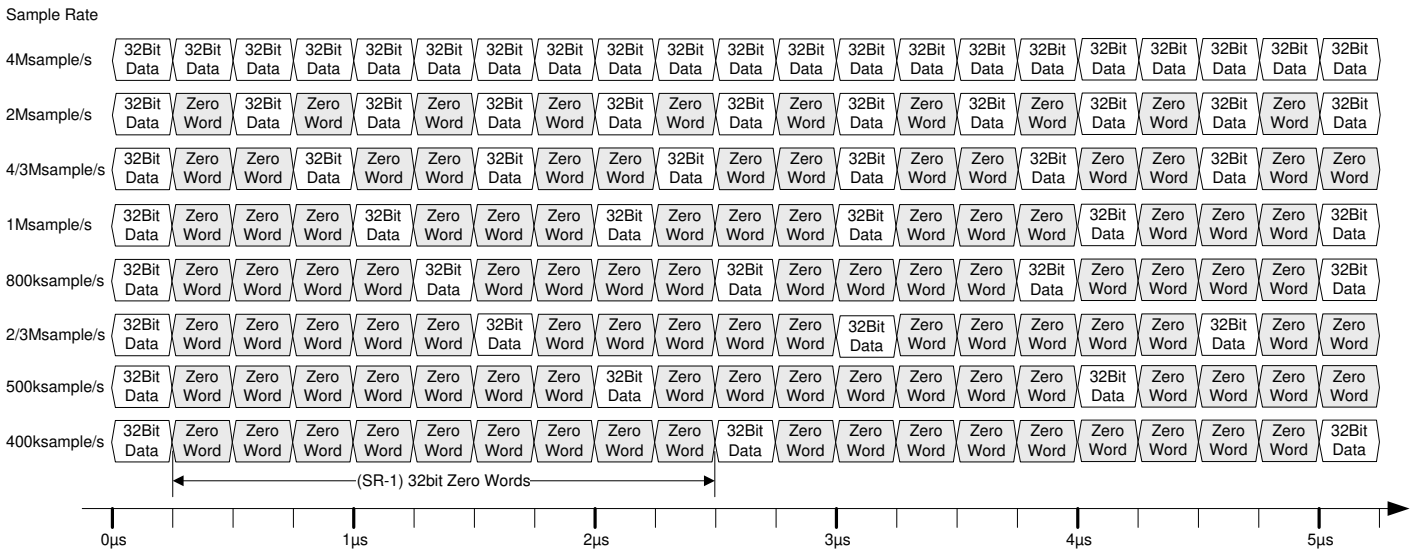
For details on the I/Q data processing refer to section "Transmitter Digital Frontend" on page 43 and "Receiver Digital Frontend" on page 53. Embedded TX control is described in section "Transmit Control" on page 46.

4.5.5 Sample Rate

The sample rate (SR) of the I/Q data stream at TXD must be the same as the transmit sample rate configured in register TXDFE.SR. A number of m = TXDFE.SR-1 zero words must be inserted between the data carrying 32-bit words (refer to Figure 4-11 below).

The sample rate of the I/Q data stream at RXD09 and RXD24 is the same as the receive sample rate configured in register RXDFE.SR. Zero words are inserted in the same format as for the TXD stream.

Figure 4-11. I/Q Data at Different Sample Rates



4.5.6 Operation and Synchronization

If the AT86RF215 operates in I/Q radio mode, it automatically enables the required I/Q data interface driver and receiver. The TX link (TXD and TXCLK receiver) is enabled in the states TXPREP and TX. In addition, the RXCLK driver is activated because the AT86RF215 operates as I/Q data interface clock master. The RX link is enabled in state RX and incorporates the RXCLK and RXD09 or RXD24 driver for the sub-1GHz or 2.4GHz transceiver, respectively. For details about the transceiver operating modes and states refer to chapter "Basic Operation " on page 30

After enabling the TX link, the TXD and TXCLK driver require a start-up time (see section "I/Q Data Interface Driver DC and Startup Specification" on page 205). The start-up phase is followed by the initial synchronization. If the I_SYNC pattern is detected after 32 or more zero bits, the de-serialization of the I/Q data is started. The synchronization of the TX link is validated at each expected I_SYNC and Q_SYNC pattern. An I_SYNC pattern is expected either 16 bits after a Q_SYNC pattern or 32 or more zero bits after a 32-bit data word. A Q_SYNC pattern is expected 16 bits after an I_SYNC pattern. Figure 4-12 on page 26 shows the start-up phase and initial synchronization of the TX link.

The successful reception of a I/Q data word is indicated by the synchronization status bit IQIFC2.SYNC. The bit is cleared at each read access and set again at the reception of the next I/Q data word.