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Features

- High Performance RF-CMOS 2.4 GHz Radio Transceiver Targeted for IEEE 802.15.4™, ZigBee®, 6LoWPAN, RF4CE, SP100, WirelessHART™ and ISM Applications
- Industry Leading Link Budget (104 dB):
  - Programmable Output Power from -17 dBm up to 3 dBm
  - Receiver Sensitivity -101 dBm
- Ultra-Low Power Consumption:
  - SLEEP: 20 nA
  - RX: 15.5 mA
  - TX: 16.5 mA (at max Transmit Power of 3 dBm)
- Ultra-Low Supply Voltage (1.8V to 3.6V) with Internal Regulator
- Optimized for Low BoM Cost and Ease of Production:
  - Few External Components Necessary (Crystal, Capacitors and Antenna)
- Excellent ESD Robustness
- Easy to Use Interface:
  - Registers and Frame Buffer Accessible through Fast SPI
  - Only Two Microcontroller GPIO Lines Necessary
  - One Interrupt Pin from Radio Transceiver
  - Clock Output with Prescaler from Radio Transceiver
- Radio Transceiver Features:
  - 128-byte SRAM for Data Buffering
  - Programmable Clock Output to Clock the Host Microcontroller or as Timer Reference
  - Integrated TX/RX Switch
  - Fully Integrated PLL with on-chip Loop Filter
  - Fast PLL Settling Time
  - Battery Monitor
  - Fast Power-Up Time < 1 ms
- Special IEEE 802.15.4-2003 Hardware Support:
  - FCS Computation
  - Clear Channel Assessment
  - Energy Detection / RSSI Computation
  - Automatic CSMA-CA
  - Automatic Frame Retransmission
  - Automatic Frame Acknowledgement
  - Automatic Address Filtering
- Industrial Temperature Range:
  - -40° C to 85° C
- I/O and Packages:
  - 32-pin Low-Profile QFN
  - RoHS/Fully Green
- Compliant to EN 300 328/440, FCC-CFR-47 Part 15, ARIB STD-66, RSS-210
- Compliant to IEEE 802.15.4-2003

AVR®

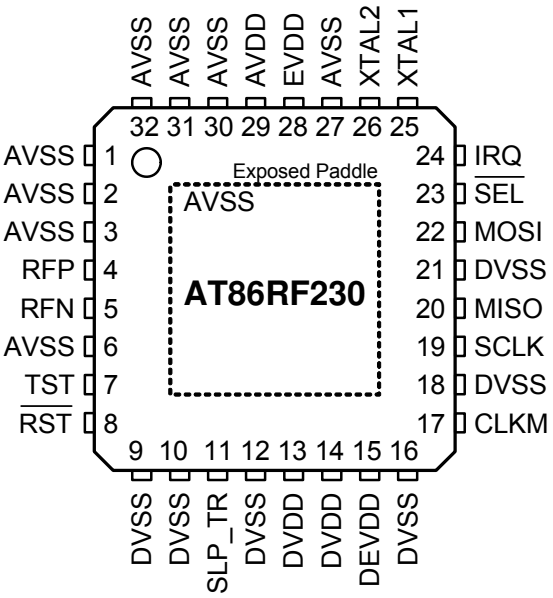
Low Power 2.4 GHz Transceiver for ZigBee, IEEE 802.15.4, 6LoWPAN, RF4CE and ISM Applications

AT86RF230

5131E-MCU Wireless-02/09

1 Pin-out Diagram

Figure 1-1. AT86RF230 Pin-Out Diagram



Note: The exposed paddle is electrically connected to the die inside the package. It shall be soldered to the board to ensure electrical and thermal contact and good mechanical stability.

Disclaimer

Typical values contained in this datasheet are based on simulations and testing. Min and Max values will be available when the radio transceiver has been fully characterized.

2 Overview

The AT86RF230 is a low-power 2.4 GHz radio transceiver especially designed for ZigBee/IEEE 802.15.4 applications. The AT86RF230 is a true SPI-to-antenna solution. All RF-critical components except the antenna, crystal and de-coupling capacitors are integrated on-chip. Therefore, the AT86RF230 is particularly suitable for applications like:

- 2.4 GHz IEEE 802.15.4 and ZigBee systems
- 6LoWPAN and RF4CE systems
- Wireless sensor networks
- Industrial control, sensing and automation (SP100, WirelessHART)
- Home and building automation
- Consumer electronics
- PC peripherals

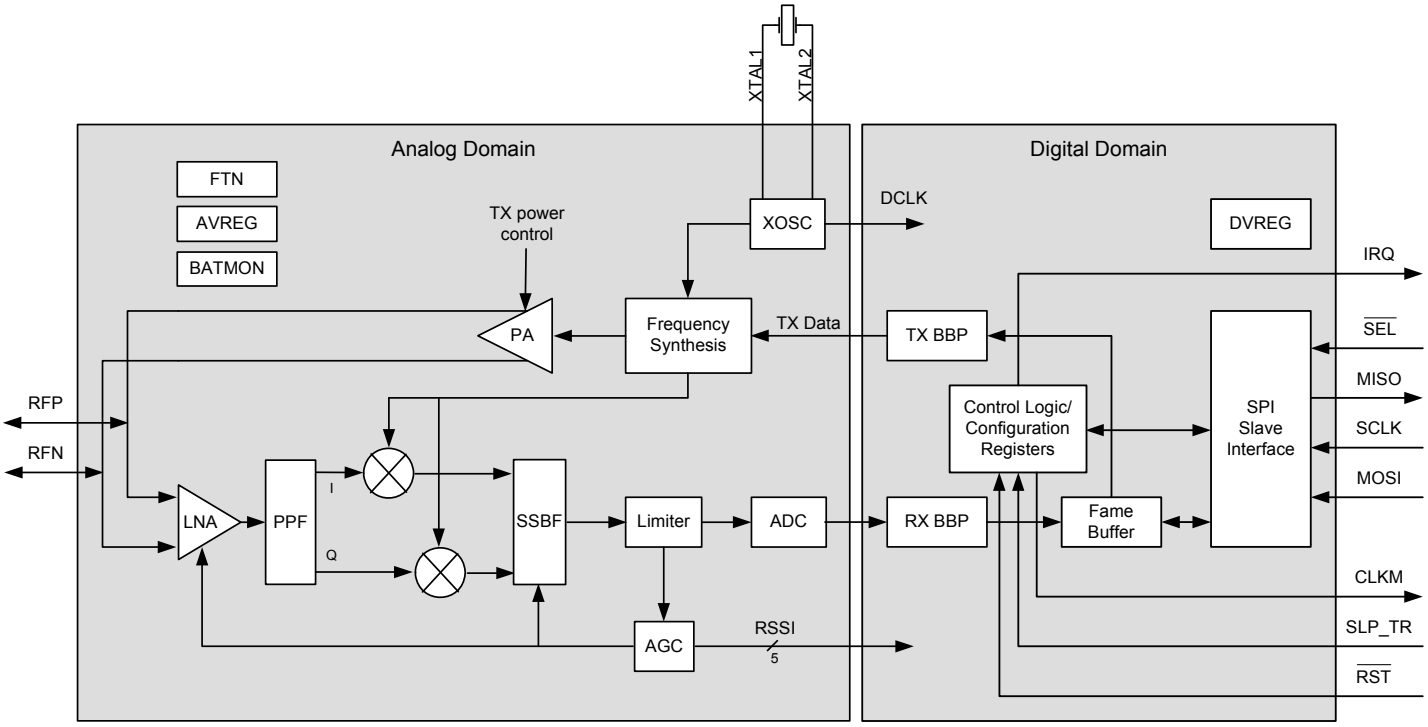
The AT86RF230 can be operated by using an external microcontroller like ATMEL's AVR microcontrollers. A comprehensive software programming description can be found in the application note AVR2009 "AT86RF230 – Software Programming Model".

3 General Circuit Description

This single-chip radio transceiver provides a complete radio transceiver interface between the antenna and the microcontroller. It comprises the analog radio transceiver and the digital demodulation including time and frequency synchronization, and data buffering. The number of external components is minimized such that only an antenna, a crystal and four decoupling capacitors are required. The bidirectional differential antenna pins are used for transmission and reception, so that no external antenna switch is needed.

The AT86RF230 block diagram is shown in Figure 3-1.

Figure 3-1. Block Diagram of the AT86RF230



The received RF signal at pins RFN and RFP is differentially fed through the low-noise amplifier (LNA) to the RF filter (PPF) to generate a complex signal. This signal is converted down by mixers to an intermediate frequency and fed to the integrated channel filter (SSBF). The limiting amplifier provides sufficient gain to drive the succeeding analog-to-digital converter (ADC) and generates a digital RSSI signal with 3 dB granularity. The ADC output signal is sampled by the digital base band receiver (RX BBP).

The transmit modulation scheme is offset-QPSK (O-QPSK) with half-sine pulse shaping and 32-length block coding (spreading) according to [1]. The modulation signal is generated in the digital transmitter (TX BBP) and applied to the fractional-N frequency synthesis (PLL) generating a coherent phase modulation required for demodulation of O-QPSK signals. The frequency-modulated RF signal is fed to the power amplifier (PA).

An internal 128 byte RAM for RX and TX (Frame Buffer) buffers the data to be transmitted or the received data. Two on chip low dropout (LDO) voltage regulators provide the internal analog and digital 1.8V supply.

4 Pin Description

Table 4-1. AT86RF230 Pin List

Number	Name	Type	Description
1	AVSS	Ground	Analog ground
2	AVSS	Ground	Analog ground
3	AVSS	Ground	Ground for RF signals
4	RFP	RF I/O	Differential RF signal
5	RFN	RF I/O	Differential RF signal
6	AVSS	Ground	Ground for RF signals
7	TST	Digital input	Enables Continuous Transmission Test Mode; active high
8	$\overline{\text{RST}}$	Digital input	Chip reset; active low
9	DVSS	Ground	Digital ground
10	DVSS	Ground	Digital ground
11	SLP_TR	Digital input	Controls sleep, transmit start and receive states; active high
12	DVSS	Ground	Digital ground
13	DVDD	Supply	Regulated 1.8V supply voltage; digital domain
14	DVDD	Supply	Regulated 1.8V supply voltage; digital domain
15	DEVDD	Supply	External supply voltage; digital domain
16	DVSS	Ground	Digital ground
17	CLKM	Digital output	Master clock signal output
18	DVSS	Ground	Digital ground
19	SCLK	Digital input	SPI clock
20	MISO	Digital output	SPI data output (master input slave output)
21	DVSS	Ground	Digital ground
22	MOSI	Digital input	SPI data input (master output slave input)
23	$\overline{\text{SEL}}$	Digital input	SPI select; active low
24	IRQ	Digital output	Interrupt request signal; active high
25	XTAL1	Analog input	Crystal pin or external clock supply
26	XTAL2	Analog input	Crystal pin
27	AVSS	Ground	Analog ground
28	EVDD	Supply	External supply voltage; analog domain
29	AVDD	Supply	Regulated 1.8V supply voltage; analog domain
30	AVSS	Ground	Analog ground
31	AVSS	Ground	Analog ground
32	AVSS	Ground	Analog ground
Paddle	AVSS	Ground	Analog ground; Exposed Paddle of QFN package

4.1 Supply and Ground Pins

EVDD, DEVDD

EVDD and DEVDD are analog and digital supply voltage pins of the AT86RF230 radio transceiver.

AVDD, DVDD

AVDD and DVDD are outputs of the internal 1.8V voltage regulators. The voltage regulators are controlled independently by the radio transceivers state machine and are activated depending on the current radio transceiver state. The voltage regulators can be configured for external supply. For details refer to section 9.4.

AVSS, DVSS

AVSS and DVSS are analog and digital ground pins respectively.

The analog and digital power domains should be separated on the PCB, for further details see application note AVR2005 "Design Considerations for the AT86RF230".

4.2 Analog and RF Pins

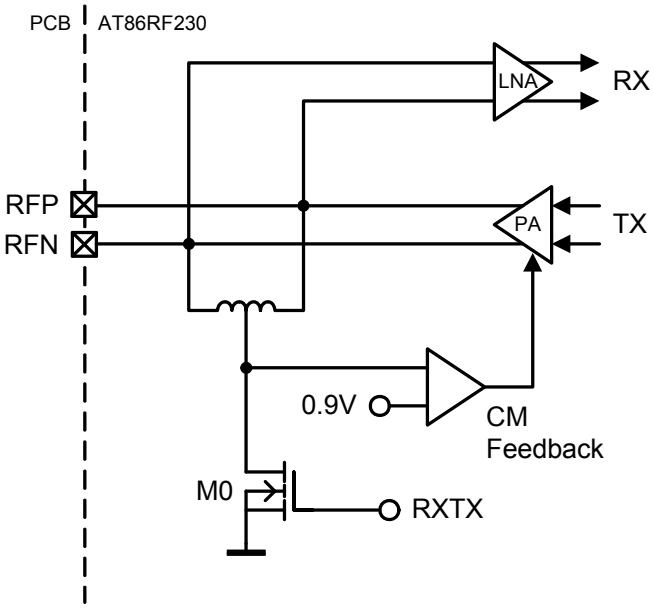
RFP, RFN

A differential RF port (RFP/RFN) provides common-mode rejection to suppress the switching noise of the internal digital signal processing blocks. At the board-level, the differential RF layout ensures high receiver sensitivity by rejecting any spurious interspersions originating from other digital ICs such as a microcontroller.

The RF port is designed for a 100Ω differential load. A DC path between the RF pins is allowed. A DC path to ground or supply voltage is not allowed. Therefore, when connecting a RF-load providing a DC path to the power supply or to ground, capacitive coupling is required as indicated in Table 4-2.

A simplified schematic of the RF front end is shown in Figure 4-1.

Figure 4-1. Simplified RF Front-End Schematic



RF port DC values depend on the operating mode. In TRX_OFF state (see section 7.1.2), when the analog front end is disabled, the RF pins are pulled to ground, preventing a floating voltage.

In receive mode, the RF input provides a low-impedance path to ground when transistor M0 (see Figure 4-1) pulls the inductor center tap to ground. A DC voltage drop of 20 mV across the on-chip inductor can be measured at the RF pins.

In transmit mode, a control loop provides a common-mode voltage of 0.9V. Transistor M0 is off, allowing the PA to set the common-mode voltage. The common-mode capacitance at each pin to ground shall be < 30 pF to ensure the stability of this common-mode feedback loop.

XTAL1, XTAL2

The pin XTAL1 is the input of the reference oscillator amplifier (XOSC), XTAL2 is the output. A detailed description of the crystal oscillator setup and the related XTAL1/XTAL2 pin configuration can be found in section 9.6.

When using an external clock reference signal, XTAL1 shall be used as input pin. For further details refer to section 9.6.3.

Table 4-2. Comments on Analog and RF Pins

Pin	Condition	Recommendation/Comment
RFP/RFN	VDC = 0.9V (TX) VDC = 20 mV (RX) at both pins	AC-coupling is required if an antenna with a DC path to ground is used. Serial capacitance must be < 30 pF.
XTAL1/XTAL2	CPAR = 3 pF VDC = 0.9V at both pins	Parasitic capacitance (CPAR) of the pins must be considered as additional load capacitance to the crystal.

4.3 Digital Pins

The digital interface of the AT86RF230 compromises pins $\overline{\text{SEL}}$, SCLK, MOSI and MISO forming the serial peripheral interface (SPI) and pins CLKM, IRQ, SLP_TR and $\overline{\text{RST}}$ used as additional control signal between radio transceiver and microcontroller. The digital radio transceiver interface is described in detail in section 6.

4.3.1 Driver Strength Settings of Digital Output Pins

The driver strength of the digital output pins (MISO, IRQ) and CLKM pin can be configured by register 0x03 (TRX_CTRL_0) as described in Table 4-3.

The capacitive load should be as small as possible and not larger than 50 pF when using the 2 mA minimum driver strength setting. Generally, the output driver strength should be adjusted to the lowest possible value in order to keep the current consumption and the emission of digital signal harmonics low.

Table 4-3. Digital Output Driver Configuration

Pin	Default Driver Strength	Comment
MISO, IRQ	2 mA	Adjustable to 2 mA, 4 mA, 6 mA and 8 mA
CLKM	4 mA	Adjustable to 2 mA, 4 mA, 6 mA and 8 mA

4.3.2 Pull-up and Pull-down Configuration of Digital Input Pins

Pulling resistors are internally connected to all digital input pins in radio transceiver state P_ON (see section 7.1.2). Table 4-4 summarizes the pull-up and pull-down configuration.

Table 4-4 Pull-Up/Pull-Down Configuration of Digital Input Pins in P_ON State

Pin	H ≙ pull-up, L ≙ pull-down
$\overline{\text{RST}}$	H
$\overline{\text{SEL}}$	H
SCLK	L
MOSI	L
SLP_TR	L

In all other radio transceiver states, no pull-up or pull-down resistors are connected to any of the digital input pins.

4.3.3 Register Description

Register 0x03 (TRX_CTRL_0)

The TRX_CTRL_0 register controls the drive current of the digital output pads and the CLKM clock rate.

Bit	7	6	5	4	
0x03	PAD_IO		PAD_IO_CLKM		TRX_CTRL_0
Read/Write	R/W	R/W	R/W	R/W	
Reset value	0	0	0	1	

Bit	3	2	1	0	
0x03	CLKM_SHA_SEL	CLKM_CTRL			TRX_CTRL_0
Read/Write	R/W	R/W	R/W	R/W	
Reset value	1	0	0	1	

- **Bit [7:6] – PAD_IO**

The register bits PAD_IO set the output driver current of digital output pads MISO and IRQ.

Table 4-5. Digital Output Driver Strength

Register Bit	Value	Description
PAD_IO	0[1]	2 mA
	1	4 mA
	2	6 mA
	3	8 mA
Notes:	1. Reset values of register bits are underlined characterized in the document.	

- **Bit [5:6] – PAD_IO_CLKM**

The register bits PAD_IO_CLKM set the output driver current of pin CLKM.

Table 4-6. CLKM Driver Strength

Register Bit	Value	Description
PAD_IO_CLKM	0	2 mA
	1	4 mA
	2	6 mA
	3	8 mA

- **Bit 3 – CLKM_SHA_SEL**

Refer to section 9.6.5.

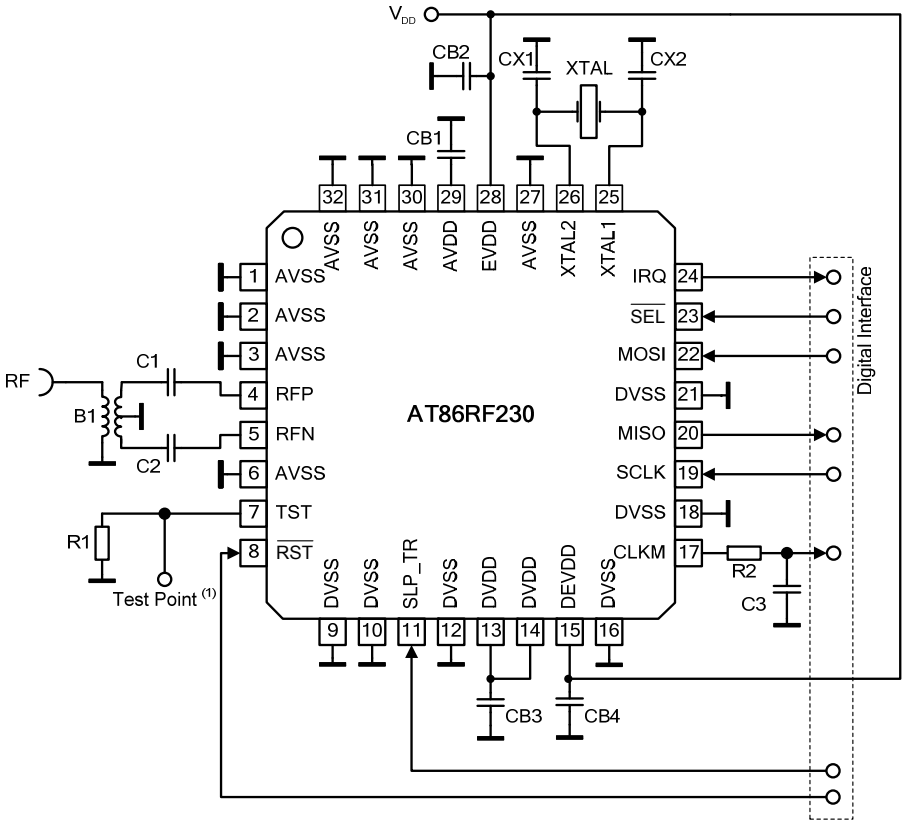
- **Bit [2:0] – CLKM_CTRL**

Refer to section 9.6.5.

5 Application Circuit

An application circuit of the AT86RF230 radio transceiver with a single-ended RF connector is shown in Figure 5-1. The balun B1 transforms the 100Ω differential RF port (RFP/RFN) to a 50Ω single-ended RF port. The capacitors C1 and C2 provide AC coupling of the RF signals to the RF pins.

Figure 5-1. Application Circuit Schematic



Note: (1) For further details refer to „Appendix A – Continuous Transmission Test Mode“

The power supply decoupling capacitors (CB2, CB4) are connected to the external analog supply pin (EVDD, pin 28) and the external digital supply pin (DEVDD, pin 15).

Capacitors CB1 and CB3 are bypass capacitors for the integrated analog and digital voltage regulators to ensure stable operation (1 µF recommended value). All decoupling and bypass capacitors should be placed as close as possible to the AT86RF230 pins and should have a low-resistance and low-inductance connection to ground to achieve the best performance.

The crystal (XTAL), the two load capacitors (CX1, CX2), and the internal circuitry connected to pins XTAL1 and XTAL2 form the crystal oscillator. To achieve the best accuracy and stability of the reference frequency, large parasitic capacitances should be avoided. Crystal lines should be routed as short as possible and not in proximity of digital I/O signals.

Crosstalk from digital signals on the crystal pins or the RF pins can degrade the system performance. Therefore, a low-pass filter (C3, R2) is placed close to the CLKM output pin to reduce the radiation of signal harmonics. This is not needed if the CLKM pin is not used. Then the output should be turned off during device initialization.

The application board ground plane should be separated into four independent fragments, the analog, the digital, the antenna and the XTAL ground plane. The exposed paddle shall act as reference of the individual grounds.

For further details see application note AVR2005 "Design Considerations for the AT86RF230".

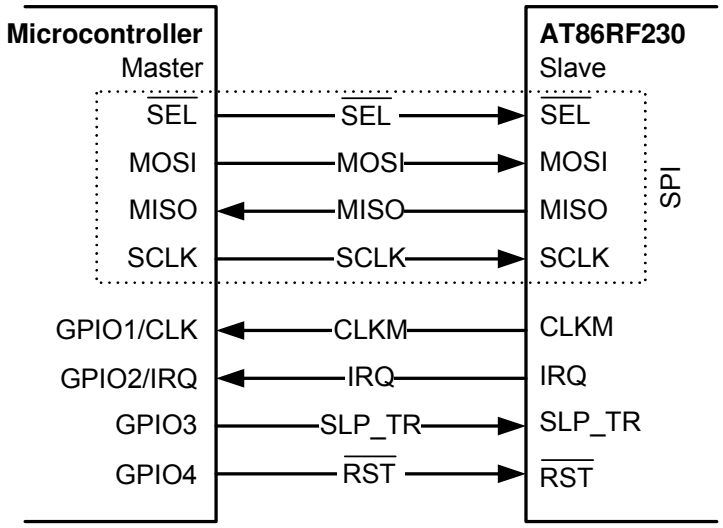
Table 5-1. Example Bill of Materials

Designator	Description	Value	Manufacturer	Part Number	Comment
B1	SMD balun	2.45 GHz	Wuerth	748421245	2.45 GHz Balun
B1 (alternatively)	SMD balun / filter	2.45 GHz	Johanson Technology	2450FB15L0001	2.45 GHz Balun / Filter
CB1	LDO VREG bypass capacitor	1 µF	AVX Murata	0603YD105KAT2A GRM188R61C105KA12D	X5R 10% 16V (0603)
CB2	Power supply decoupling	1 µF			
CB3	LDO VREG bypass capacitor	1 µF			
CB4	Power supply decoupling	1 µF			
CX1	Crystal load capacitor	12 pF	AVX Murata	06035A120JA GRP1886C1H120JA01	COG 5% 50V (0603)
CX2	Crystal load capacitor	12 pF			
C1	RF coupling capacitor	22 pF	Epcos Epcos AVX	B37930 B37920 06035A220JAT2A	C0G 5% 50V (0402 or 0603)
C2	RF coupling capacitor	22 pF			
C3	CLKM low-pass filter capacitor	2.2 pF	AVX Murata	06035A229DA GRP1886C1H2R0DA01	COG ±0.5 pF 50V (0603) Designed for f_{CLKM} = 1 MHz
R1	Pull-down resistor	10 kΩ			Recommended 0Ω, if continuous transmission is not required
R2	CLKM low-pass filter resistor	680Ω			Designed for f_{CLKM} = 1 MHz
XTAL	Crystal	CX-4025 16 MHz SX-4025 16 MHz	ACAL Taitjen Siward	XWBBPL-F-1 A207-011	

6 Microcontroller Interface

This section describes the AT86RF230 to microcontroller interface. The interface comprises a slave SPI and additional control signals, see Figure 6-1. The SPI timing and protocol are described.

Figure 6-1. Microcontroller to AT86RF230 Interface



Microcontrollers with a master SPI, such as Atmel's AVR family, interface directly to the AT86RF230. The SPI is used for Frame Buffer and register access. The additional control signals are connected to the GPIO/IRQ interface of the microcontroller. Table 6-1 introduces the radio transceiver I/O signals and their functionality.

Table 6-1. Signal Description of Microcontroller Interface

Signal	Description
$\overline{\text{SEL}}$	SPI select signal, active low
MOSI	SPI data (master output slave input) signal
MISO	SPI data (master input slave output) signal
SCLK	SPI clock signal
CLKM	AT86RF230 clock output, usable as: - Microcontroller clock source - High precision timing reference
IRQ	AT86RF230 interrupt request signal
SLP_TR	AT86RF230 multi purpose control signal (functionality is state-depended): - Sleep/Wakeup - TX start - Controls CLKM output
$\overline{\text{RST}}$	AT86RF230 reset signal, active low

6.1 SPI Timing Description

The SPI is designed to work in synchronous or asynchronous mode.

In synchronous mode, the CLKM output of the radio transceiver is used as the master clock of the microcontroller. In this case the maximum SPI clock frequency is 8 MHz.

In asynchronous mode, the SPI master clock (SCLK) is generated by the microcontroller itself. The maximum SPI clock rate is limited to 7.5 MHz using this operating mode. If the clock signal from the radio transceiver pin CLKM is not required, it may be disabled.

Figure 6-2 and Figure 6-3 illustrate the SPI timing and introduce its parameters. The corresponding timing parameter definition is given in Table 11-4.

Figure 6-2. SPI Timing, Global Map and Definition of Timing Parameters t_5, t_6, t_8 and t_9

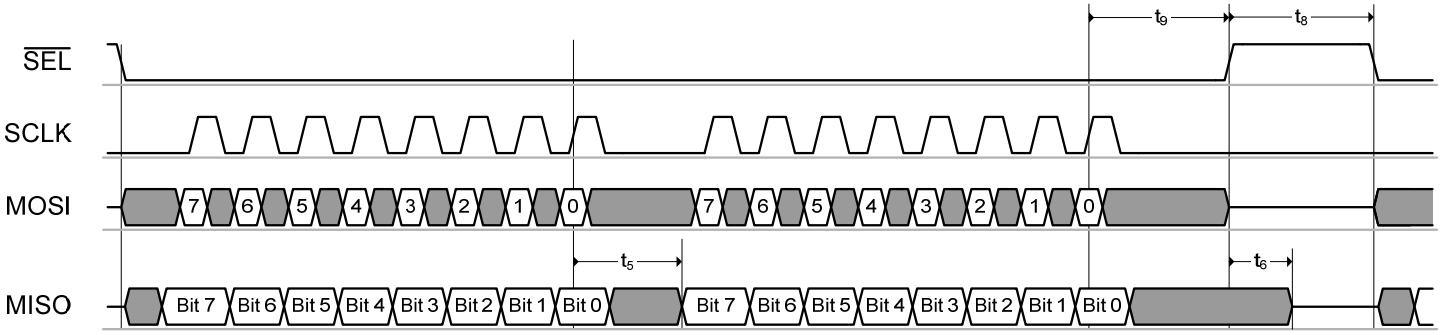
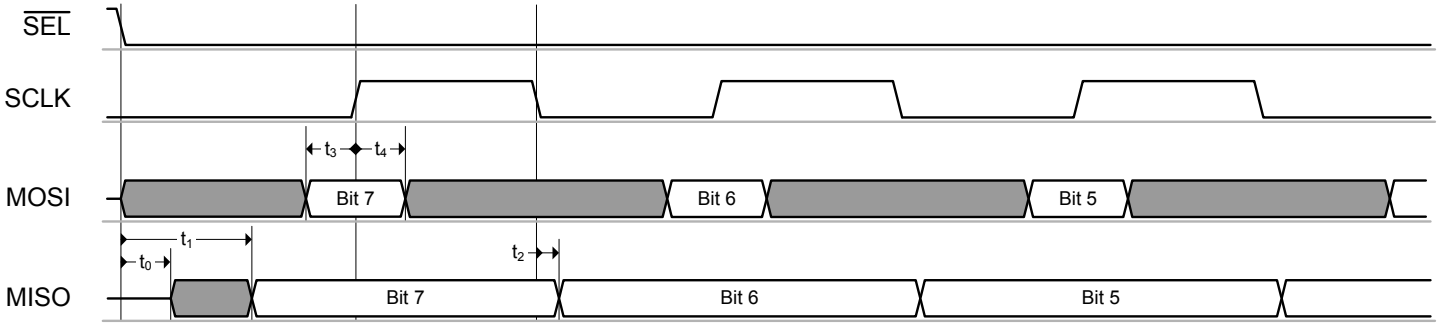


Figure 6-3. SPI Timing, Detailed View and Definition of Timing Parameters t_0 to t_4



The SPI is based on a byte-oriented protocol and is always a bidirectional communication between master and slave. The SPI master starts the transfer by asserting $\overline{SEL}$ = L. Then the master generates eight SPI clock cycles to transfer a byte to the radio transceiver (via MOSI). At the same time the slave transmits one byte to the master (via MISO). When the master wants to receive one byte of data from the slave it must also transmit one byte to the slave. All bytes are transferred MSB first. An SPI transaction is finished by releasing $\overline{SEL}$ = H.

A SPI register access consists of two bytes, a Frame Buffer or SRAM access of two or more bytes, as described in section 6.2.

$\overline{SEL}$ = L enables the MISO output driver of the radio transceiver. The MSB of MISO is valid after t_1 (see section 11.4 parameter 11.4.3) and is updated at each falling edge of SCLK. If the MISO output driver is disabled, there is no internal pull-up resistor connected to the output. Driving the appropriate signal level must be ensured by the

master device or an external pull-up resistor. Note, when both $\overline{SEL}$ and $\overline{RST}$ are active, the MISO output driver is also enabled.

The MOSI line is sampled by the radio transceiver at the rising edge of SCLK. The signal must be stable before and after the rising edge of SCLK as specified by t_3 and t_4, refer to section 11.4 parameters 11.4.5 and 11.4.6.

This mode of SPI operation is commonly called “SPI Mode 0”.

6.2 SPI Protocol

Each transfer sequence starts with transferring a command byte from SPI master via MOSI (see Table 6-2) with MSB first. This command byte defines the access mode and additional mode-dependent information.

Table 6-2. SPI Command Byte Definition

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Mode
1	0	Register address [5:0]						Register Access Mode – Read Access
1	1	Register address [5:0]						Register Access Mode – Write Access
0	0	1	Reserved					Frame Buffer Access Mode – Read Access
0	1	1	Reserved					Frame Buffer Access Mode – Write Access
0	0	0	Reserved					SRAM Access Mode – Read Access
0	1	0	Reserved					SRAM Access Mode – Write Access

The different access modes are described within the following sections.

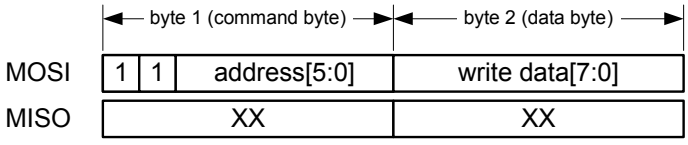
In Figure 6-4 to Figure 6-14 logic values stated with X on MOSI are ignored by the radio transceiver, but need to have a valid level. Return values on MISO stated as X shall be ignored by the microcontroller.

6.2.1 Register Access Mode

The Register access mode is a two-byte read/write operation and is initiated by setting $\overline{SEL}$ = L. The first transferred byte on MOSI is the command byte and must indicate a register access (see Table 6-2) and a register address (see Table 12-1).

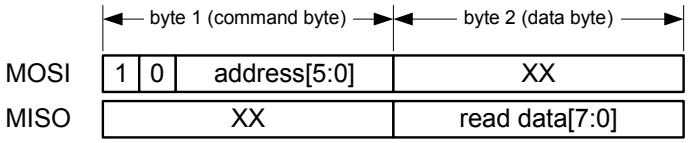
On write access the second byte transferred on MOSI contains the write data to the selected address (see Figure 6-4).

Figure 6-4. Packet Structure – Register Write Access



On read access the content of the selected register address is returned in the second byte on MISO (see Figure 6-5).

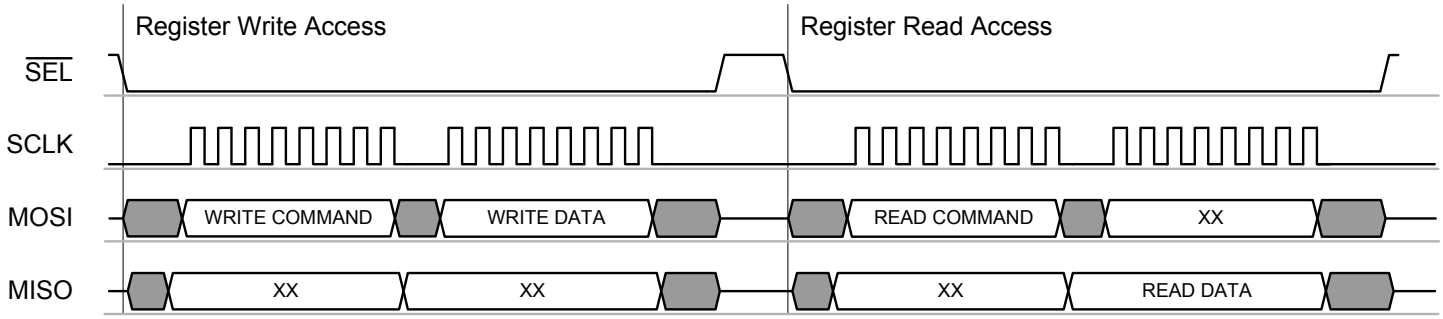
Figure 6-5. Packet Structure – Register Read Access



Each register access must be terminated by setting $\overline{SEL}$ = H.

Figure 6-6 illustrates a typical SPI sequence for a register access sequence for write and read respectively.

Figure 6-6. Example SPI Sequence - Register Access Mode



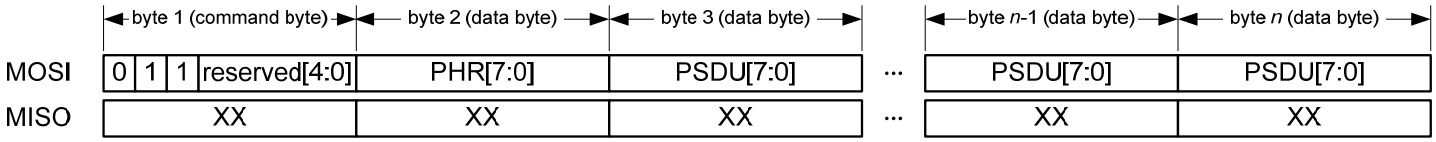
6.2.2 Frame Buffer Access Modes

The Frame Buffer read access and the Frame Buffer write access are used to upload or download frames to the microcontroller.

Each access starts by setting $\overline{SEL}$ = L. The first byte transferred on MOSI is the command byte and must indicate a Frame Buffer access mode according to the definition in Table 6-2.

On Frame Buffer write access the second byte transferred on MOSI contains the frame length (PHR field) followed by the payload data (PSDU) as shown by Figure 6-7.

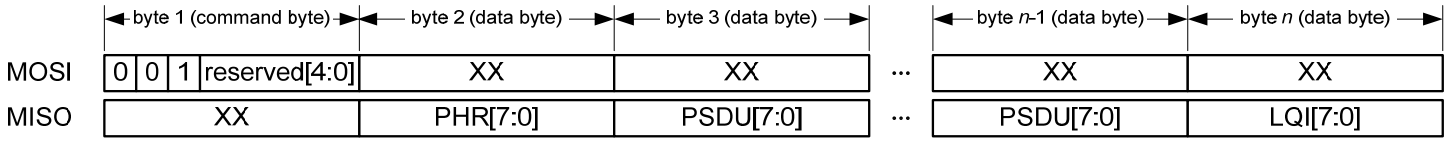
Figure 6-7. Packet Structure - Frame Buffer Write Access



On Frame Buffer read access PHR and PSDU are transferred via MISO starting with the second byte. After the PSDU data bytes one more byte can be transferred containing the link quality indication (LQI) value of the received frame, for details refer to section 8.5. Figure 6-8 illustrates the packet structure of a Frame Buffer read access.

Note, the Frame Buffer read access can be terminated at any time without any consequences by setting $\overline{SEL}$ = H, e.g. after reading the frame length byte only.

Figure 6-8. Packet Structure - Frame Buffer Read Access



The number of bytes *n* for one Frame Buffer access is calculated as follow:

Receive: *n* = 3 + *frame_length*

[command byte, frame length byte, PSDU data, LQI byte]

Transmit: *n* = 2 + *frame_length*

[command byte, frame length byte, PSDU data]

The maximum value of *frame_length* is 127 bytes. That means that *n* ≤ 130 for Frame Buffer read access and *n* ≤ 129 for Frame Buffer write access. Each read or write of a data byte increments automatically the address counter of the Frame Buffer until the access is terminated by setting $\overline{SEL}$ = H.

Figure 6-9 and Figure 6-10 illustrate an example SPI sequence of a Frame Buffer access to write and read a frame with 4-byte PSDU respectively.

Figure 6-9. Example SPI Sequence - Frame Buffer Write Sequence of a Frame with 4-byte PSDU

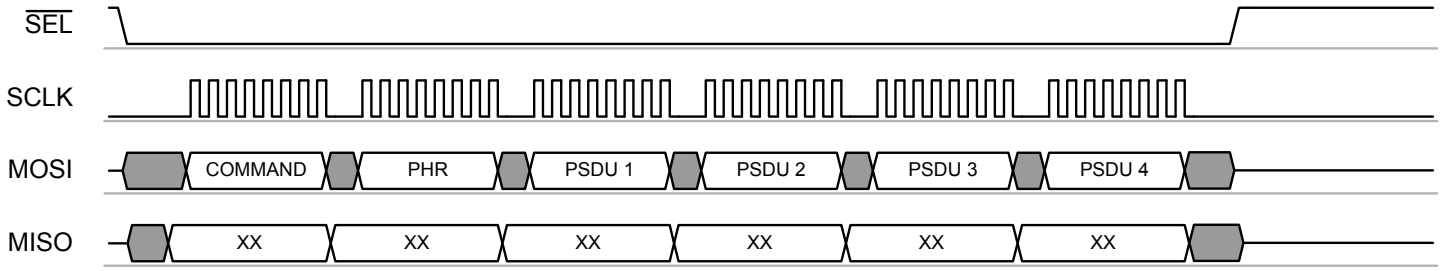
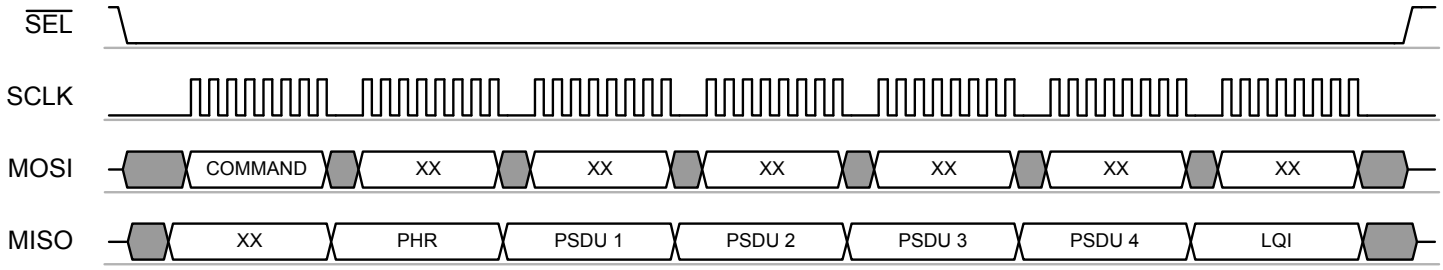


Figure 6-10. Example SPI Sequence - Frame Buffer Read Sequence of a Frame with 4-byte PSDU



Access violations during a Frame Buffer write or read access are indicated by a TRX_UR interrupt. For further details refer to section 9.3.3.

6.2.3 SRAM Access Mode

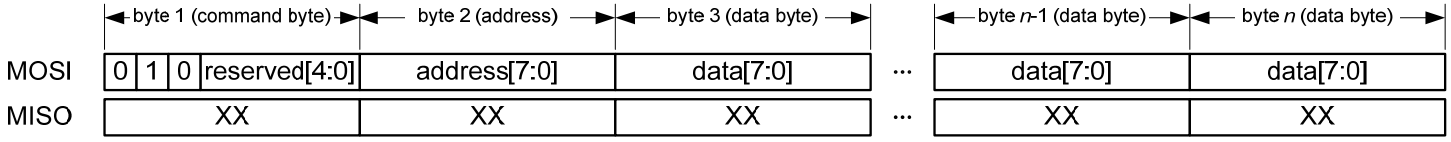
The SRAM access mode allows access to certain bytes within the Frame Buffer. This may reduce SPI traffic.

The SRAM access mode is useful, for instance, if a transmit frame is already stored in the Frame Buffer and certain bytes (e.g. sequence number or address field) need to be replaced before retransmitting the frame. Furthermore, it can be used to access only the LQI value after frame reception. A detailed description of the user accessible frame content can be found in section 9.3.2.

Each access starts by setting $\overline{SEL}$ = L. The first transferred byte on MOSI shall be the command byte and must indicate a SRAM access mode according to the definition in Table 6-2. The following byte indicates the start address of the write or read access. The address space is 0x00 to 0x7F. The microcontroller software has to ensure to access only to the valid address space.

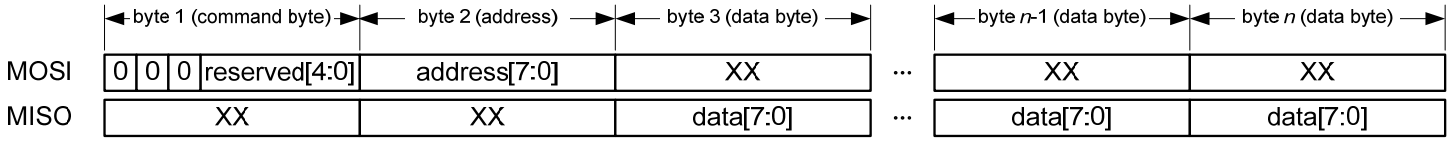
On SRAM write access, one or more bytes of write data are transferred on MOSI starting with the third byte of the access sequence (see Figure 6-11).

Figure 6-11. Packet Structure - SRAM Write Access



On SRAM read access, one or more bytes of read data are transferred on MISO starting with the third byte of the access sequence (see Figure 6-12).

Figure 6-12. Packet Structure - SRAM Read Access



As long as $\overline{SEL}$ is logic low, every subsequent byte read or write increments the address counter of the Frame Buffer until the SRAM access is terminated by setting $\overline{SEL}$ = H.

Figure 6-13 and Figure 6-14 illustrate an example SPI sequence of a SRAM access to write and read a data package of 5 byte length respectively.

Figure 6-13. Example SPI Sequence – SRAM Write Access Sequence of a 5 byte Data Package

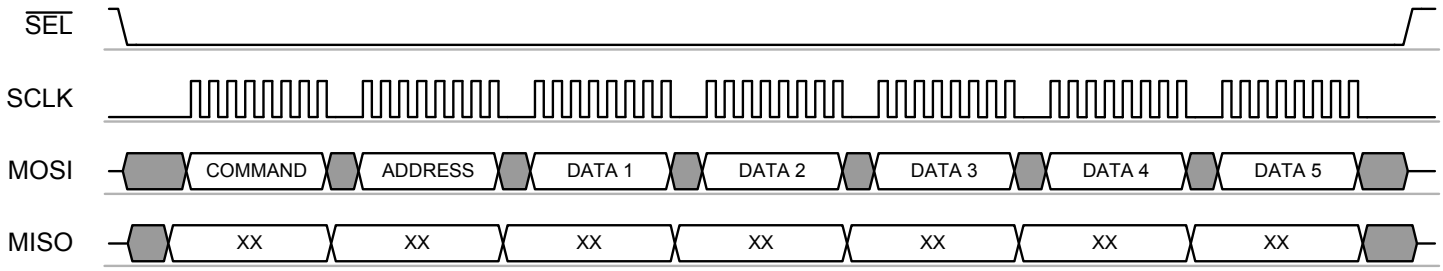
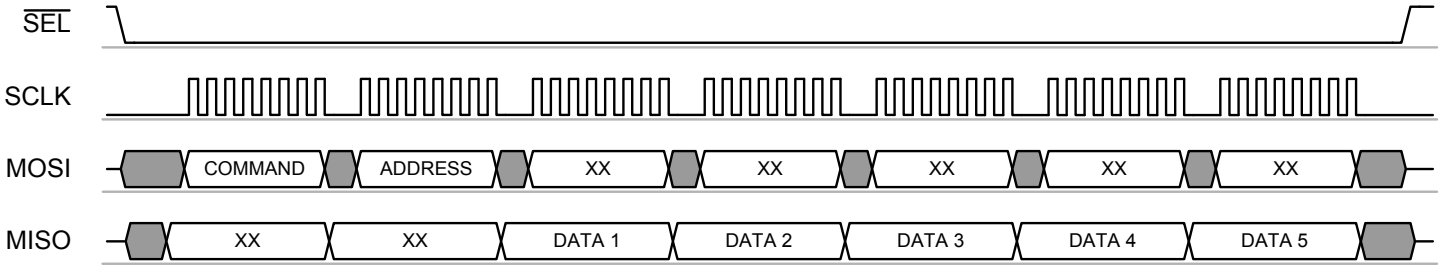


Figure 6-14. Example SPI Sequence – SRAM Read Access Sequence of a 5 byte Data Package



Notes:

- Because the Frame Buffer is shared between TX and RX, the frame data are overwritten by new incoming frames. If the TX frame data is to be retransmitted, it must be ensured that no frame was received meanwhile.
- If the SRAM access mode is used to upload received frames, the Frame Buffer contains all frame data except the frame length byte. The frame length information can be accessed only using the Frame Buffer read access.
- It is not possible to transmit received frames without a Frame Buffer read and write operation by the microcontroller.
- Frame Buffer access violations are not indicated by a TXR_UR interrupt when using the SRAM access mode (see section 9.3.3)

6.3 Radio Transceiver Identification

The AT86RF230 can be identified by four registers. One register contains an unique part number and one register the corresponding version number. Additional two registers contain the JEDEC manufacturer ID.

6.3.1 Register Description

Register 0x1C (PART_NUM)

Bit	7	6	5	4	3	2	1	0	
0x1C	PART_NUM								PART_NUM
Read/Write	R	R	R	R	R	R	R	R	
Reset value	0	0	0	0	0	0	1	0	

- **Bit [7:0] – PART_NUM**

This register bits PART_NUM contain the radio transceiver part number.

Table 6-3. Radio Transceiver Part Number

Register Bits	Value[7:0]	Description
PART_NUM	2	AT86RF230 part number

Register 0x1D (VERSION_NUM)

Bit	7	6	5	4	3	2	1	0	
0x1D	VERSION_NUM								VERSION_NUM
Read/Write	R	R	R	R	R	R	R	R	
Reset value	0	0	0	0	0	0	1	0	

- **Bit [7:0] – VERSION_NUM**

This register bits VERSION_NUM contain the radio transceiver version number.

Table 6-4. Radio Transceiver Version Number

Register Bits	Value[7:0]	Description
VERSION_NUM	1	AT86RF230 Revision A
	2	AT86RF230 Revision B

Register 0x1E (MAN_ID_0)

Bit	7	6	5	4	3	2	1	0	
0x1E	MAN_ID_0								MAN_ID_0
Read/Write	R	R	R	R	R	R	R	R	
Reset value	0	0	0	1	1	1	1	1	

- **Bit [7:0] – MAN_ID_0**

Bits [7:0] of the 32 bit JEDEC manufacturer ID are stored in register bits MAN_ID_0. Bits [15:8] are stored in register 0x1F (MAN_ID_1). The highest 16 bits of the ID are not stored in registers.

Table 6-5. JEDEC Manufacturer ID – Bits [7:0]

Register Bits	Value[7:0]	Description
MAN_ID_0	0x1F	Atmel JEDEC manufacturer ID Bits [7:0] of 32 bit manufacturer ID: 00 00 00 1F

Register 0x1F (MAN_ID_1)

Bit	7	6	5	4	3	2	1	0	
0x1F	MAN_ID_1								MAN_ID_1
Read/Write	R	R	R	R	R	R	R	R	
Reset value	0	0	0	0	0	0	0	0	

- **Bit [7:0] – MAN_ID_1**

Bits [15:8] of the 32 bit JEDEC manufacturer ID are stored in register bits MAN_ID_1. Bits [7:0] are stored in register 0x1E (MAN_ID_0). The upper 16 bits of the ID are not stored in registers.

Table 6-6. JEDEC Manufacturer ID – Bits [15:8]

Register Bits	Value[7:0]	Description
MAN_ID_1	0x00	Atmel JEDEC manufacturer ID Bits [15:8] of 32 bit manufacturer ID: 00 00 00 1F

6.4 Sleep/Wake-up and Transmit Signal (SLP_TR)

The SLP_TR signal is a multi-functional pin. Its function relates to the current state of the AT86RF230 and is summarized in Table 6-7. The radio transceiver states are explained in detail in section 7.

Table 6-7. SLP_TR Multi-Functional Pin

Radio Transceiver Status	Function	Transition	Description
TRX_OFF	Sleep	L → H	Takes the radio transceiver into SLEEP state
SLEEP	Wakeup	H → L	Takes the radio transceiver into TRX_OFF state
RX_ON	Disable CLKM	L → H	Takes the radio transceiver into RX_ON_NOCLK state and disables CLKM
RX_ON_NOCLK	Enables CLKM	H → L	Takes the radio transceiver into RX_ON state and enables CLKM
RX_AACK_ON	Disable CLKM	L → H	Takes the radio transceiver into RX_AACK_ON_NOCLK state and disables CLKM
RX_AACK_ON_NOCLK	Enables CLKM	H → L	Takes the radio transceiver into RX_AACK_ON state and enables CLKM
PLL_ON	TX start	L → H	Starts frame transmission
TX_ARET_ON	TX start	L → H	Starts TX_ARET transaction

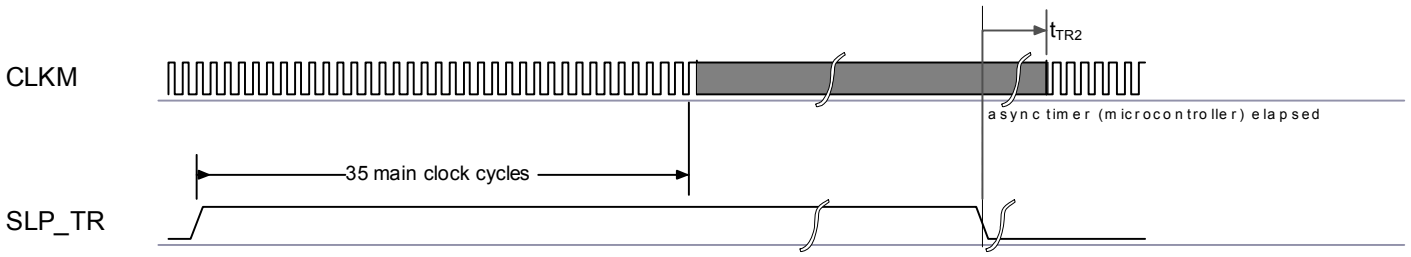
In states PLL_ON and TX_ARET_ON, the SLP_TR pin is used as trigger input to initiate a TX transaction. Here pin SLP_TR is sensitive on rising edge only.

After initiating a state change by a rising edge at pin SLP_TR in radio transceiver states TRX_OFF, RX_ON or RX_AACK_ON the radio transceiver remains in the new state as long as the pin is logical high and returns to the preceding state with the falling edge.

The SLEEP state is used when radio transceiver functionality is not required, and thus the AT86RF230 can be powered down to reduce the overall power consumption.

A power-down scenario is shown in Figure 6-15. When the radio transceiver is in TRX_OFF state the microcontroller force the AT86RF230 to SLEEP by setting SLP_TR = H. If the CLKM output provides a clock to the microcontroller this clock is switched off after 35 clock cycles. This enables a microcontroller in a synchronous system to complete its power-down routine and prevent dead-lock situations. The AT86RF230 awakes when the microcontroller releases pin SLP_TR. This concept provides the lowest possible power consumption.

Figure 6-15. Sleep and Wake-up Initiated by Asynchronous Microcontroller Timer Output (for Timing Information see Table 7-1)



For synchronous systems, where CLKM is used as a microcontroller clock source and the SPI master clock (SCLK) is directly derived from CLKM, the AT86RF230 supports an additional power-down mode for receive operating states RX_ON and RX_AACK_ON.

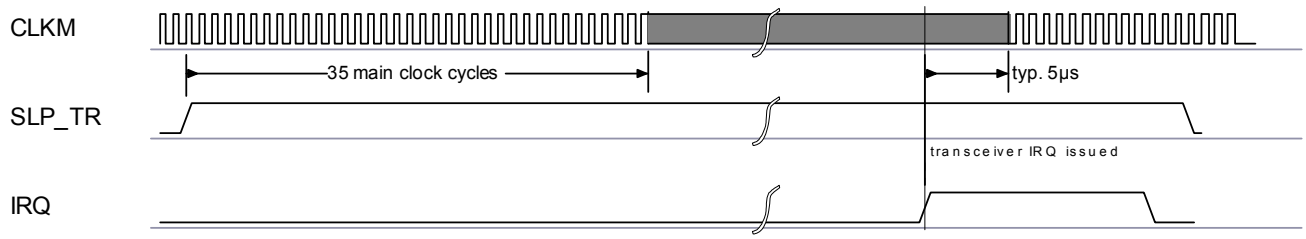
If an incoming frame is expected and no other applications are running on the microcontroller, it can be powered down without missing incoming frames.

This can be achieved by a rising edge on pin SLP_TR which turns off the CLKM output 35 clock cycles afterwards. The radio transceiver state changes from RX_ON or RX_AACK_ON to RX_ON_NOCLK or RX_AACK_ON_NOCLK respectively.

In case that a frame is received the radio transceiver enters the state BUSY_RX/BUSY_RX_AACK and the clock output CLKM is automatically switched on again. This scenario is shown in Figure 6-16.

The power consumption of the radio transceiver is similar in state RX_ON_NOCLK/RX_AACK_ON_NOCLK and state RX_ON, because only the CLKM output is switched off.

Figure 6-16. Wake-Up Initiated by Radio Transceiver Interrupt



6.5 Interrupt Logic

6.5.1 Overview

The AT86RF230 differentiates between six interrupt events. Each interrupt is enabled or disabled by writing the corresponding bit to the interrupt mask register 0x0E (IRQ_MASK). Internally, each interrupt is stored as a separate bit of the interrupt status register. All interrupt lines are combined via logical “OR” to one external interrupt line (IRQ). If the IRQ pin issues, the microcontroller shall read the interrupt status register 0x0F (IRQ_STATUS) to determine the reason for the interrupt. A read access to this register clears the interrupt status register and the IRQ pin, too. Interrupts are not cleared automatically when the event that caused them is not valid anymore. Exception: the PLL_LOCK IRQ clears the PLL_UNLOCK IRQ and vice versa. The supported interrupts for the Basic Operating Mode (see section 7.1) are summarized in Table 6-8.

Table 6-8. Interrupt Description in Basic Operating Mode

IRQ Name	Comments	Details
IRQ_7: BAT_LOW	Indicates a supply voltage below the programmed threshold.	Section 9.5.3
IRQ_6: TRX_UR	Indicates a Frame Buffer access violation (under run).	Section 9.3.3
IRQ_3: TRX_END	RX: Indicates the completion of a frame reception. TX: Indicates the completion of a frame transmission.	Section 7.1.3 Section 7.1.3
IRQ_2: RX_START	Indicates a SFD detection. The TRX_STATE changes to BUSY_RX.	Section 7.1.3
IRQ_1: PLL_UNLOCK	Indicates PLL unlock. The PA is turned off immediately, if the radio transceiver is in BUSY_TX/BUSY_TX_ARET state.	Section 9.7.4
IRQ_0: PLL_LOCK	Indicates PLL lock	Section 9.7.4

Using the Extended Operating Mode, the interrupts are handled in a slightly different way. A detailed description can be found in section 7.2.4.

6.5.2 Register Description

Register 0x0E (IRQ_MASK)

The IRQ_MASK register is used to enable (set register bit to 1) or disable (set register bit to 0) interrupt events by writing the corresponding bit to the interrupt mask register.

Bit	7	6	5	4	
0x0E	MASK_BAT_LOW	MASK_TRX_UR	Reserved		IRQ_MASK
Read/Write	R/W	R/W	R/W	R/W	
Reset value	1	1	1	1	

Bit	3	2	1	0	
0x0E	MASK_TRX_END	MASK_RX_START	MASK_PLL_UNLOCK	MASK_PLL_LOCK	IRQ_MASK
Read/Write	R/W	R/W	R/W	R/W	
Reset value	1	1	1	1	

If an interrupt will be enabled or disabled, it is recommended to read the interrupt status register 0x0F (IRQ_STATUS) first to clear the history.

Register 0x0F (IRQ_STATUS)

The IRQ_STATUS register contains the status of the individual interrupts. A read access to this register resets all interrupt bits.

Bit	7	6	5	4	
0x0F	BAT_LOW	TRX_UR	Reserved		IRQ_STATUS
Read/Write	R	R	R	R	
Reset value	0	0	0	0	

Bit	3	2	1	0	
0x0F	TRX_END	RX_START	PLL_UNLOCK	PLL_LOCK	IRQ_STATUS
Read/Write	R	R	R	R	
Reset value	0	0	0	0	

By reading the register after an interrupt is signaled at IRQ pin, the reason for the interrupt can be identified.

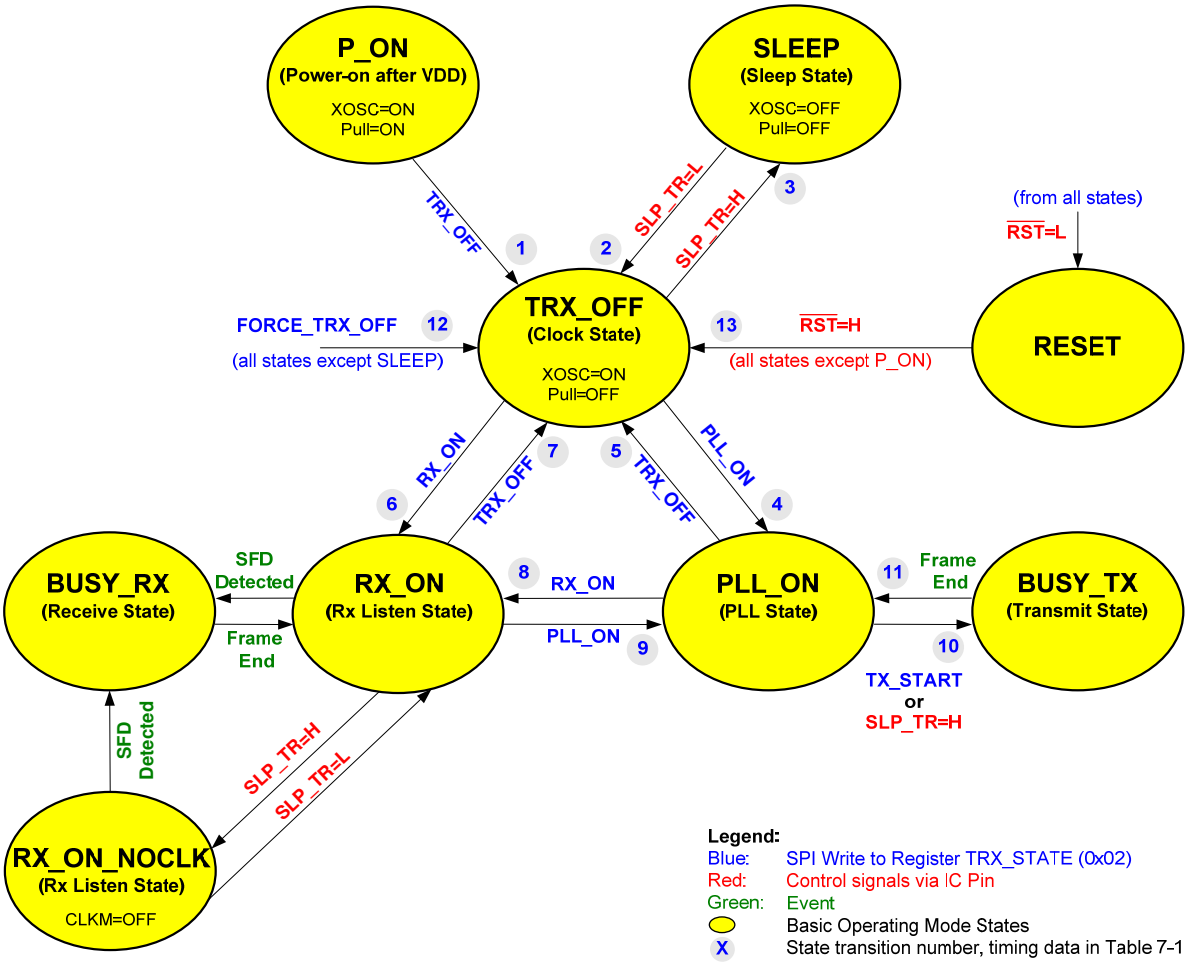
A detailed description of the individual interrupts can be found in Table 6-8.

7 Operating Modes

7.1 Basic Operating Mode

This section summarizes all states to provide the basic functionality of the AT86RF230, such as receiving and transmitting frames, and powering up and down. The Basic Operating Mode is designed for IEEE 802.15.4 applications; the corresponding radio transceiver states are shown in Figure 7-1.

Figure 7-1. Basic Operating Mode State Diagram (for State Transition Timing Data Refer to Table 7-1)



7.1.1 State Control

The radio transceiver state is controlled by two signal pins (SLP_TR, $\overline{\text{RST}}$) and the register 0x02 (TRX_STATE). A successful state change shall be confirmed by reading the radio transceiver status from register 0x01 (TRX_STATUS).

If TRX_STATUS = 0x1F (STATE_TRANSITION_IN_PROGRESS) the AT86RF230 is on a state transition. Do not try to initiate a further state change while the radio transceiver is in STATE_TRANSITION_IN_PROGRESS.

The pin SLP_TR is a multifunctional pin. Depending on radio transceiver state the rising edge of SLP_TR causes the following state transitions:

- TRX_OFF → SLEEP
- RX_ON → RX_ON_NOCLK
- PLL_ON → BUSY_TX

For further details to the functionality of pin SLP_TR refer to section 6.4.

The pin $\overline{\text{RST}}$ causes a reset of all registers (register bits CLKM_SHA_SEL and CLKM_CTRL are shadowed, for details refer to section 9.6.4) and forces the radio transceiver into TRX_OFF state. However, if the device is in the P_ON state it remains in the P_ON state.

For all states, the state change commands FORCE_TRX_OFF or TRX_OFF lead to a transition into TRX_OFF state. If the radio transceiver is in the BUSY_RX or BUSY_TX state, the command FORCE_TRX_OFF interrupts the active receiving or transmitting process, and forces an immediate transition. In contrast to that the TRX_OFF command is stored until a currently ongoing frame reception or transmission has finished. After the end of the frame, the transition to TRX_OFF is performed.

The completion of each requested state change shall always be confirmed by reading the register 0x01 (TRX_STATUS).

7.1.2 Basic Operating Mode Description

7.1.2.1 P_ON - Power-on after V_{DD}

When the external supply voltage (V_{DD}) is firstly applied to the radio transceiver, the system goes into the P_ON state. An on-chip reset is performed. The crystal oscillator gets activated and the master clock is provided to the CLKM pin after the crystal oscillator has stabilized. CLKM can be used as a clock source to the microcontroller.

The on-chip power-on-reset sets all registers to their default values. A dedicated reset signal from the microcontroller at the pin $\overline{\text{RST}}$ is not necessary, but recommended for hardware/software synchronization reasons. The reset impulse should have a minimum length as specified in section 11.4, see parameter 11.4.12.

All digital inputs have pull-up or pull-down resistors (see Table 4-4). This is necessary to support microcontrollers where GPIO signals are floating after reset. The input pull-up and pull-down resistors are disabled when the radio transceiver leaves the P_ON state.

Prior to leaving P_ON, the microcontroller must set all digital input pins (MOSI, $\overline{\text{RST}}$, SCLK, $\overline{\text{SEL}}$, SLP_TR) to their default operating values.

Once the supply voltage has stabilized and the crystal oscillator has settled (see section 11.5, parameter 11.5.5), a SPI write access to the register 0x02 (TRX_STATE) with the command TRX_OFF or FORCE_TRX_OFF initiates a state change from P_ON to TRX_OFF.

7.1.2.2 SLEEP – Sleep State

In SLEEP state, the entire radio transceiver is disabled. No circuitry is operating. The AT86RF230 current consumption is reduced to leakage current only.

This state can only be entered from state TRX_OFF by setting the pin SLP_TR = H. If CLKM is enabled, the SLEEP state is entered 35 CLKM cycles after the rising edge. At that time CLKM is turned off. If the CLKM output is turned off (bits CLKM_CTRL = 0 in register 0x03), the SLEEP state is entered immediately.

Setting SLP_TR = L returns the radio transceiver to the TRX_OFF state. It is recommended that pin SLP_TR should be active for a minimum of 40 CLKM cycles to completely power down the radio transceiver.

During SLEEP state, the register contents remain valid while the content of the Frame Buffer is cleared.

7.1.2.3 TRX_OFF – Clock State

In TRX_OFF state the SPI interface and the crystal oscillator are enabled. The digital voltage regulator (DVREG) is enabled and provides 1.8V to the digital core to make the Frame Buffer available (see section 9.1). The microcontroller can access all digital functions and if enabled, the CLKM output supplies a clock. The pin SLP_TR is enabled for state control.

7.1.2.4 PLL_ON – PLL State

Entering the PLL_ON state from TRX_OFF state enables the analog voltage regulator (AVREG) first. After the voltage regulator has been settled, the PLL frequency synthesizer is enabled. When the PLL has been settled at the receive frequency, a successful PLL lock is indicated by issuing a PLL_LOCK interrupt.

If an RX_ON command is issued in PLL_ON state, the receiver is immediately enabled. If the PLL has not been settled before, actual frame reception can only happen once the PLL has locked.

The PLL_ON state corresponds to the TX_ON state in IEEE 802.15.4.

7.1.2.5 RX_ON and BUSY_RX – RX Listen and Receive State

In RX_ON state the receiver blocks and the PLL frequency synthesizer are enabled.

The AT86RF230 receive mode is internally divided into RX_ON state and BUSY_RX state. There is no difference between these states with respect to the analog radio transceiver circuitry, which is always turned on. During RX_ON state, only the preamble detection of the digital signal processing is running. When a preamble and a valid SFD are detected, also the digital receiver is turned on. The radio transceiver enters the BUSY_RX state and a RX_START interrupt is generated.

During the frame reception frame data are stored continuously in the Frame Buffer until the last byte was received. The completion of the frame reception is indicated by a TRX_END interrupt and the radio transceiver reenters the state RX_ON. At the same time the register bit RX_CRC_VALID (register 0x06) is updated with the result of the FCS check (see section 8.2).

Note, settings of address registers 0x20 to 0x2B do not affect the frame reception in Basic Operating Mode. Frame address filtering is only applied when using the Extended Operating Mode (see section 7.2).

7.1.2.6 RX_ON_NOCLK – RX Listen State without CLKM

If the radio transceiver is listening for an incoming frame and the microcontroller is not running an application, the microcontroller can be powered down to decrease the total system power consumption. This special power-down scenario for systems running in clock synchronous mode (see section 6.4) is supported by the AT86RF230 using the state RX_ON_NOCLK.

This state can only be entered by setting SLP_TR = H while the AT86RF230 is in the RX_ON state. The CLKM pin is disabled 35 clock cycles after the rising edge at the SLP_TR pin. This allows the microcontroller to complete its power-down sequence. The

reception of a frame is indicated to the microcontroller by a RX_START interrupt. CLKM is turned on again, and the radio transceiver enters the BUSY_RX state (see section 6.4, Figure 6-16).

The end of the transaction is indicated to the microcontroller by a TRX_END interrupt. After the transaction has been completed, the radio transceiver enters the RX_ON state. The radio transceiver only reenters the RX_ON_NOCLK state, when the next rising edge at pin SLP_TR occurs.

If the radio transceiver is in the RX_ON_NOCLK state, and the SLP_TR pin is reset to logic low, it enters the RX_ON state, and it starts to supply clock on the CLKM pin again.

In states RX_ON_NOCLK and RX_ON, the current consumption is about the same, because only the CLKM output is switched off in state RX_ON_NOCLK.

7.1.2.7 BUSY_TX – Transmit State

A transmission can only be started in state PLL_ON. There are two ways to start a transmission:

- Rising edge of SLP_TR
- TX_START command to register 0x02 (TRX_STATE).

Either of these causes the AT86RF230 to enter the BUSY_TX state.

During the transition to BUSY_TX state, the PLL frequency shifts to the transmit frequency. Transmission of the first data chip of the preamble starts after 16 µs to allow PLL settling and PA ramping, see Figure 7-2. After transmission of the preamble and the SFD, the Frame Buffer content is transmitted.

The last two bytes to be transmitted are the FCS (see Figure 8-2). The radio transceiver can be configured to autonomously compute the FCS bytes and append it to the transmit data. The register bit TX_AUTO_CRC_ON in register 0x05 (PHY_TX_PWR) needs to be set to 1 to enable this feature. For further details refer to section 8.2.When the frame transmission is completed, the radio transceiver automatically turns off the power amplifier, generates a TRX_END interrupt and returns to PLL_ON state.

Note that in case the PHR indicates a frame length of zero, the transmission is aborted.

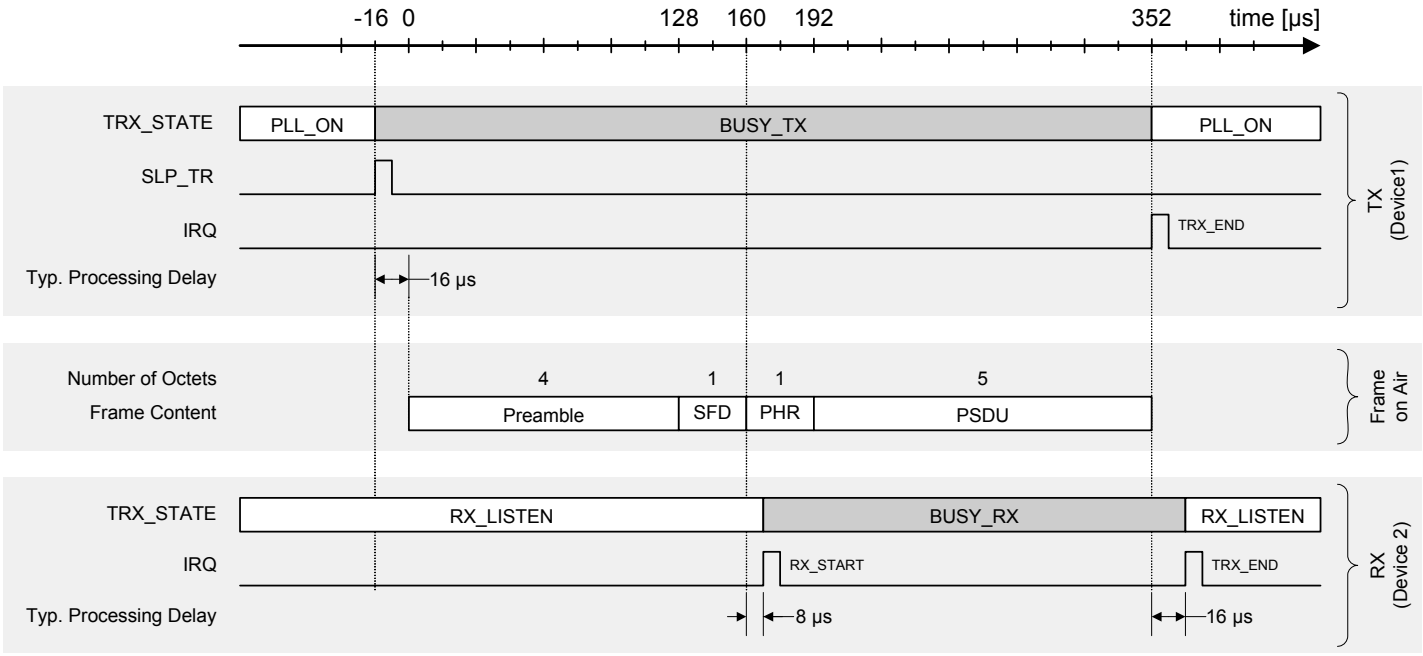
7.1.3 Interrupt Handling in Basic Operating Mode

All interrupts of the AT86RF230 (see Table 6-8) are supported during operation in Basic Operating Mode.

Two interrupts are used to support RX and TX operation of the radio transceiver. On receive the RX_START interrupt indicates the detection of a valid SFD. The TRX_END interrupt indicates the completion of the frame reception or frame transmission.

Figure 7-2 shows a receive/transmit transaction and the related interrupt events in Basic Operating Mode. One device is assumed to operate as transmitter (device 1), the second one as receiver (device 2). Processing delays are typical values.

Figure 7-2. Timing of RX_START and TRX_END Interrupts in Basic Operating Mode (see register 0x0F)



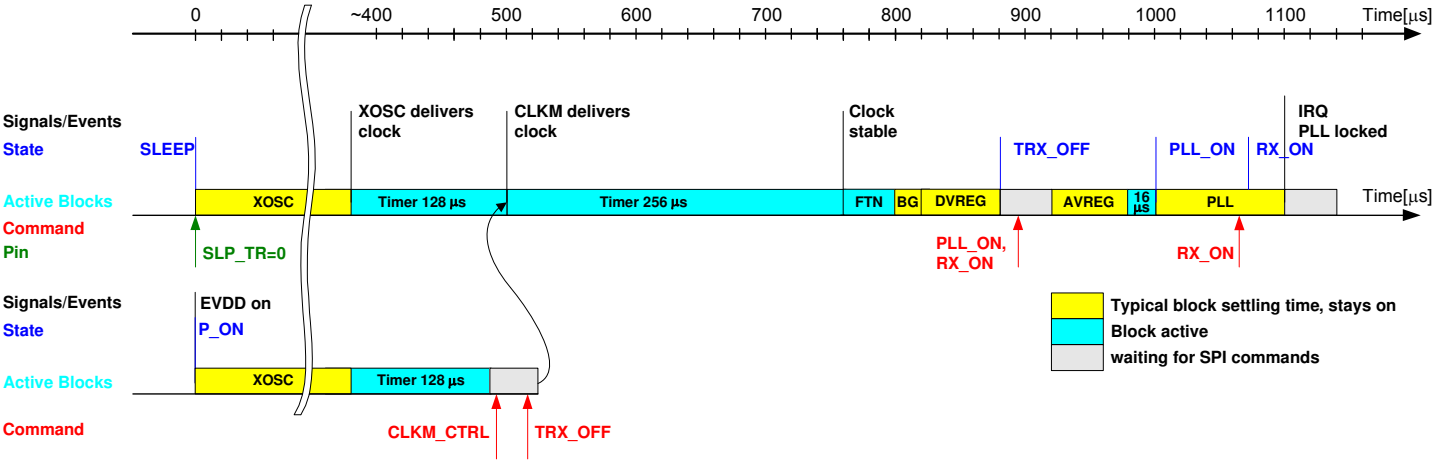
7.1.4 Basic Mode Timing

The following paragraphs depict the transitions between states and their timing.

7.1.4.1 Power-on and Wake-up Procedure

The power-on sequence and the wake-up procedure is shown in Figure 7-3.

Figure 7-3. Wake-Up Procedure from SLEEP and P_ON to RX_ON (PLL Locked)



Setting pin SLP_TR = L in SLEEP state enables the crystal oscillator. After 0.4 ms (typ.), the internal clock signal is available. After another 128 µs the clock signal is provided at the CLKM pin if enabled. An additional 256 µs timer ensures that frequency stability is sufficient to drive filter tuning (FTN) and the PLL. After the digital voltage regulator has been settled, the radio transceiver enters the TRX_OFF state and waits for further commands.