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  - Receiver Sensitivity -101 dBm
  - Programmable Output Power from -17 dBm up to +3 dBm
- Ultra-Low Current Consumption:
  - SLEEP = 0.02 µA
  - TRX_OFF = 0.4 mA
  - RX_ON = 12.3 mA
  - BUSY_TX = 14 mA (at max. Transmit Power of +3 dBm)
- Ultra-Low Supply Voltage (1.8V to 3.6V) with Internal Regulator
- Optimized for Low BoM Cost and Ease of Production:
  - Few External Components Necessary (Crystal, Capacitors and Antenna)
  - Excellent ESD Robustness
- Easy to Use Interface:
  - Registers, Frame Buffer and AES Accessible through Fast SPI
  - Only Two Microcontroller GPIO Lines Necessary
  - One Interrupt Pin from Radio Transceiver
  - Clock Output with Prescaler from Radio Transceiver
- Radio Transceiver Features:
  - 128-byte FIFO (SRAM) for Data Buffering
  - Programmable Clock Output, to Clock the Host Microcontroller or as Timer Reference
  - Integrated RX/TX Switch
  - Fully Integrated, Fast Settling PLL to support Frequency Hopping
  - Battery Monitor
  - Fast Wake-Up Time < 0.4 msec
- Special IEEE 802.15.4-2006 Hardware Support:
  - FCS Computation and Clear Channel Assessment
  - RSSI Measurement, Energy Detection and Link Quality Indication
- MAC Hardware Accelerator:
  - Automated Acknowledgement, CSMA-CA and Retransmission
  - Automatic Address Filtering
  - Automated FCS Check
- Extended Feature Set Hardware Support:
  - AES 128-bit Hardware Accelerator
  - RX/TX Indication (external RF Front-End Control)
  - RX Antenna Diversity
  - Supported PSDU data rates: 250 kb/s, 500 kb/s, 1 Mb/s and 2 Mb/s
  - True Random Number Generation for Security Application
- Industrial and Extended Temperature Range:
  - -40°C to +85°C and -40°C to +125°C
- I/O and Packages:
  - 32-pin Low-Profile QFN Package 5 x 5 x 0.9 mm³
  - RoHS/Fully Green
- Compliant to IEEE 802.15.4-2006 and IEEE 802.15.4-2003
- Compliant to EN 300 328/440, FCC-CFR-47 Part 15, ARIB STD-T66, RSS-210

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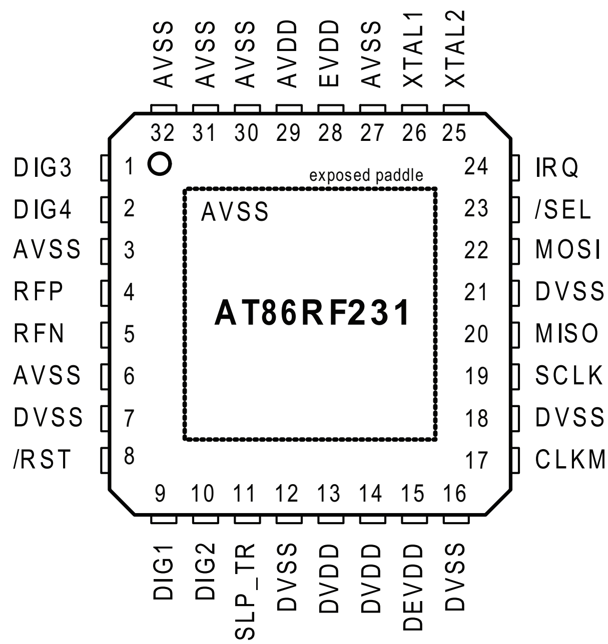
AT86RF231-ZU
AT86RF231-ZF

8111C–MCU Wireless–09/09

1. Pin-out Diagram

Figure 1-1. AT86RF231 Pin-out Diagram



Note: The exposed paddle is electrically connected to the die inside the package. It shall be soldered to the board to ensure electrical and thermal contact and good mechanical stability.

1.1 Pin Descriptions

Table 1-1. Pin Description AT86RF231

Pins	Name	Type	Description
1	DIG3	Digital output (Ground)	1. RX/TX Indicator, see Section 11.5 2. If disabled, pull-down enabled (AVSS)
2	DIG4	Digital output (Ground)	1. RX/TX indicator (DIG3 inverted), see Section 11.5 2. If disabled, pull-down enabled (AVSS)
3	AVSS	Ground	Ground for RF signals
4	RFP	RF I/O	Differential RF signal
5	RFN	RF I/O	Differential RF signal
6	AVSS	Ground	Ground for RF signals
7	DVSS	Ground	Digital ground
8	/RST	Digital input	Chip reset; active low
9	DIG1	Digital output (Ground)	1. Antenna Diversity RF switch control, see Section 11.4 2. If disabled, pull-down enabled (DVSS)
10	DIG2	Digital output (Ground)	1. Antenna Diversity RF switch control (DIG1 inverted), see Section 11.4 2. Signal IRQ_2 (RX_START) for RX Frame Time Stamping, see Section 11.6 3. If functions disabled, pull-down enabled (DVSS)
11	SLP_TR	Digital input	Controls sleep, transmit start, receive states; active high, see Section 6.5
12	DVSS	Ground	Digital ground
13	DVDD	Supply	Regulated 1.8V voltage regulator; digital domain, see Section 9.4
14	DVDD	Supply	Regulated 1.8V voltage regulator; digital domain, see Section 9.4
15	DEVDD	Supply	External supply voltage; digital domain
16	DVSS	Ground	Digital ground
17	CLKM	Digital output	Master clock signal output; low if disabled, see Section 9.6
18	DVSS	Ground	Digital ground
19	SCLK	Digital input	SPI clock
20	MISO	Digital output	SPI data output (Master Input Slave Output)
21	DVSS	Ground	Digital ground
22	MOSI	Digital input	SPI data input (Master Output Slave Input)
23	/SEL	Digital input	SPI select, active low
24	IRQ	Digital output	1. Interrupt request signal; active high or active low; configurable 2. Frame Buffer Empty Indicator; active high, see Section 11.7
25	XTAL2	Analog input	Crystal pin, see Section 9.6
26	XTAL1	Analog input	Crystal pin or external clock supply, see Section 9.6
27	AVSS	Ground	Analog ground
28	EVDD	Supply	External supply voltage, analog domain

Table 1-1. Pin Description AT86RF231 (Continued)

Pins	Name	Type	Description
29	AVDD	Supply	Regulated 1.8V voltage regulator; analog domain, see Section 9.4
30	AVSS	Ground	Analog ground
31	AVSS	Ground	Analog ground
32	AVSS	Ground	Analog ground
Paddle	AVSS	Ground	Analog ground; Exposed paddle of QFN package

1.2 Analog and RF Pins

1.2.1 Supply and Ground Pins

EVDD, DEVDD

EVDD and DEVDD are analog and digital supply voltage pins of the AT86RF231 radio transceiver.

AVDD, DVDD

AVDD and DVDD are outputs of the internal 1.8V voltage regulators. The voltage regulators are controlled independently by the radio transceivers state machine and are activated dependent on the current radio transceiver state. The voltage regulators can be configured for external supply.

For details, refer to Section 9.4 "Voltage Regulators (AVREG, DVREG)" on page 110.

AVSS, DVSS

AVSS and DVSS are analog and digital ground pins respectively. The analog and digital power domains should be separated on the PCB.

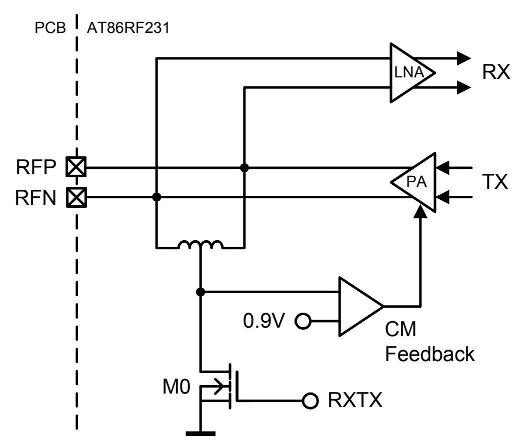
1.2.2 RF Pins

RFN, RFP

A differential RF port (RFP/RFN) provides common-mode rejection to suppress the switching noise of the internal digital signal processing blocks. At board-level, the differential RF layout ensures high receiver sensitivity by rejecting any spurious emissions originated from other digital ICs such as a microcontroller.

A simplified schematic of the RF front end is shown in Figure 1-2 on page 5.

Figure 1-2. Simplified RF Front-end Schematic



The RF port is designed for a 100Ω differential load. A DC path between the RF pins is allowed. A DC path to ground or supply voltage is not allowed. Therefore, when connecting an RF-load providing a DC path to the power supply or ground, AC-coupling is required as indicated in Table 1-2 on page 6.

The RF port DC values depend on the operating state, refer to Section 7. “Operating Modes” on page 33. In TRX_OFF state, when the analog front-end is disabled (see Section 7.1.2.3 “TRX_OFF - Clock State” on page 35), the RF pins are pulled to ground, preventing a floating voltage.

In transmit mode, a control loop provides a common-mode voltage of 0.9V. Transistor M0 is off, allowing the PA to set the common-mode voltage. The common-mode capacitance at each pin to ground shall be < 30 pF to ensure the stability of this common-mode feedback loop.

In receive mode, the RF port provides a low-impedance path to ground when transistor M0, see Figure 1-2 on page 5, pulls the inductor center tap to ground. A DC voltage drop of 20 mV across the on-chip inductor can be measured at the RF pins.

1.2.3 Crystal Oscillator Pins

XTAL1, XTAL2

The pin XTAL1 is the input of the reference oscillator amplifier (XOSC), XTAL2 is the output. A detailed description of the crystal oscillator setup and the related XTAL1/XTAL2 pin configuration can be found in Section 9.6 “Crystal Oscillator (XOSC)” on page 116.

When using an external clock reference signal, XTAL1 shall be used as input pin.

For further details, refer to Section 9.6.3 “External Reference Frequency Setup” on page 117.

1.2.4 Analog Pin Summary

Table 1-2. Analog Pin Behavior - DC values

Pin	Values and Conditions	Comments
RFP/RFN	V_{DC} = 0.9V (BUSY_TX) V_{DC} = 20 mV (receive states) V_{DC} = 0 mV (otherwise)	DC level at pins RFP/RFN for various transceiver states AC coupling is required if an antenna with a DC path to ground is used. Serial capacitance and capacitance of each pin to ground must be < 30 pF.
XTAL1/ XTAL2	V_{DC} = 0.9V at both pins C_{PAR} = 3 pF	DC level at pins XTAL1/XTAL2 for various transceiver states Parasitic capacitance (C_{PAR}) of the pins must be considered as additional load capacitance to the crystal.
DVDD	V_{DC} = 1.8V (all states, except SLEEP) V_{DC} = 0 mV (otherwise)	DC level at pin DVDD for various transceiver states Supply pins (voltage regulator output) for the digital 1.8V voltage domain, recommended bypass capacitor 1 µF.
AVDD	V_{DC} = 1.8V (all states, except P_ON, SLEEP, RESET, and TRX_OFF) V_{DC} = 0 mV (otherwise)	DC level at pin AVDD for various transceiver states Supply pin (voltage regulator output) for the analog 1.8V voltage domain, recommended bypass capacitor 1 µF.

1.3 Digital Pins

The AT86RF231 provides a digital microcontroller interface. The interface comprises a slave SPI (/SEL, SCLK, MOSI and MISO) and additional control signals (CLKM, IRQ, SLP_TR, /RST and DIG2). The microcontroller interface is described in detail in Section 6. "Microcontroller Interface" on page 16.

Additional digital output signals DIG1...DIG4 are provided to control external blocks, i.e. for Antenna Diversity RF switch control or as an RX/TX Indicator, see Section 11.4 "Antenna Diversity" on page 142 and Section 11.5 "RX/TX Indicator" on page 147. After reset, these pins are pulled-down to digital ground (DIG1/DIG2) or analog ground (DIG3/DIG4).

1.3.1 Driver Strength Settings

The driver strength of all digital output pins (MISO, IRQ, DIG1, DIG2, DIG3, DIG4) and CLKM pin can be configured using register 0x03 (TRX_CTRL_0), see Table 1-3 on page 7.

Table 1-3. Digital Output Driver Configuration

Pins	Default Driver Strength	Recommendation/Comment
MISO, IRQ, DIG1,..., DIG4	2 mA	Adjustable to 2 mA, 4 mA, 6 mA and 8 mA
CLKM	4 mA	Adjustable to 2 mA, 4 mA, 6 mA and 8 mA

The capacitive load should be as small as possible as, not larger than 50 pF when using the 2 mA minimum driver strength setting. Generally, the output driver strength should be adjusted to the lowest possible value in order to keep the current consumption and the emission of digital signal harmonics low.

1.3.2 Pull-Up and Pull-Down Configuration

All digital input pins are internally pulled-up or pulled-down in radio transceiver state P_ON, see Section 7.1.2.1 "P_ON - Power-On after VDD" on page 34. Table 1-4 on page 7 summarizes the pull-up and pull-down configuration.

Table 1-4. Pull-Up / Pull-Down Configuration of Digital Input Pins in P_ON State

Pins	H $\hat{=}$ pull-up, L $\hat{=}$ pull-down
/RST	H
/SEL	H
SCLK	L
MOSI	L
SLP_TR	L

In all other radio transceiver states, no pull-up or pull-down circuitry is connected to any of the digital input pins mentioned in Table 1-4 on page 7. In RESET state, the pull-up / pull-down configuration is disabled.

1.3.3 Register Description

Register 0x03 (TRX_CTRL_0):

The TRX_CTRL_0 register controls the drive current of the digital output pads and the CLKM clock rate.

Bit	7	6	5	4	3	2	1	0	
0x03	PAD_IO		PAD_IO_CLKM		CLKM_SHA_SEL	CLKM_CTRL			TRX_CTRL_0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	1	1	0	0	1	

- **Bit [7:6] - PAD_IO**

The register bits set the output driver current of all digital output pads, except CLKM.

Table 1-5. Digital Output Driver Strength

Register Bit	Value	Description
PAD_IO	0[(1)]	2 mA
	1	4 mA
	2	6 mA
	3	8 mA

Note: 1. Reset values of register bits are underlined characterized in the document.

- **Bit [5:4] - PAD_IO_CLKM**

The register bits set the output driver current of pin CLKM. Refer also to Section 9.6 “Crystal Oscillator (XOSC)” on page 116.

Table 1-6. CLKM Driver Strength

Register Bit	Value	Description
PAD_IO_CLKM	0	2 mA
	1	4 mA
	2	6 mA
	3	8 mA

- **Bit 3 - CLKM_SHA_SEL**

Refer to Section 9.6 “Crystal Oscillator (XOSC)” on page 116.

- **Bit [2:0] - CLKM_CTRL**

Refer to Section 9.6 “Crystal Oscillator (XOSC)” on page 116.

2. Disclaimer

Typical values contained in this datasheet are based on simulations and testing. Min and Max values are available when the radio transceiver has been fully characterized.

3. Overview

The AT86RF231 is a feature rich, low-power 2.4 GHz radio transceiver designed for industrial and consumer ZigBee/IEEE 802.15.4, 6LoWPAN, RF4CE and high data rate 2.4 GHz ISM band applications. The radio transceiver is a true SPI-to-antenna solution. All RF-critical components except the antenna, crystal and de-coupling capacitors are integrated on-chip. Therefore, the AT86RF231 is particularly suitable for applications like:

- 2.4 GHz IEEE 802.15.4 and ZigBee systems
- 6LoWPAN and RF4CE systems
- Wireless sensor networks
- Industrial control, sensing and automation (SP100, WirelessHART)
- Residential and commercial automation
- Health care
- Consumer electronics
- PC peripherals

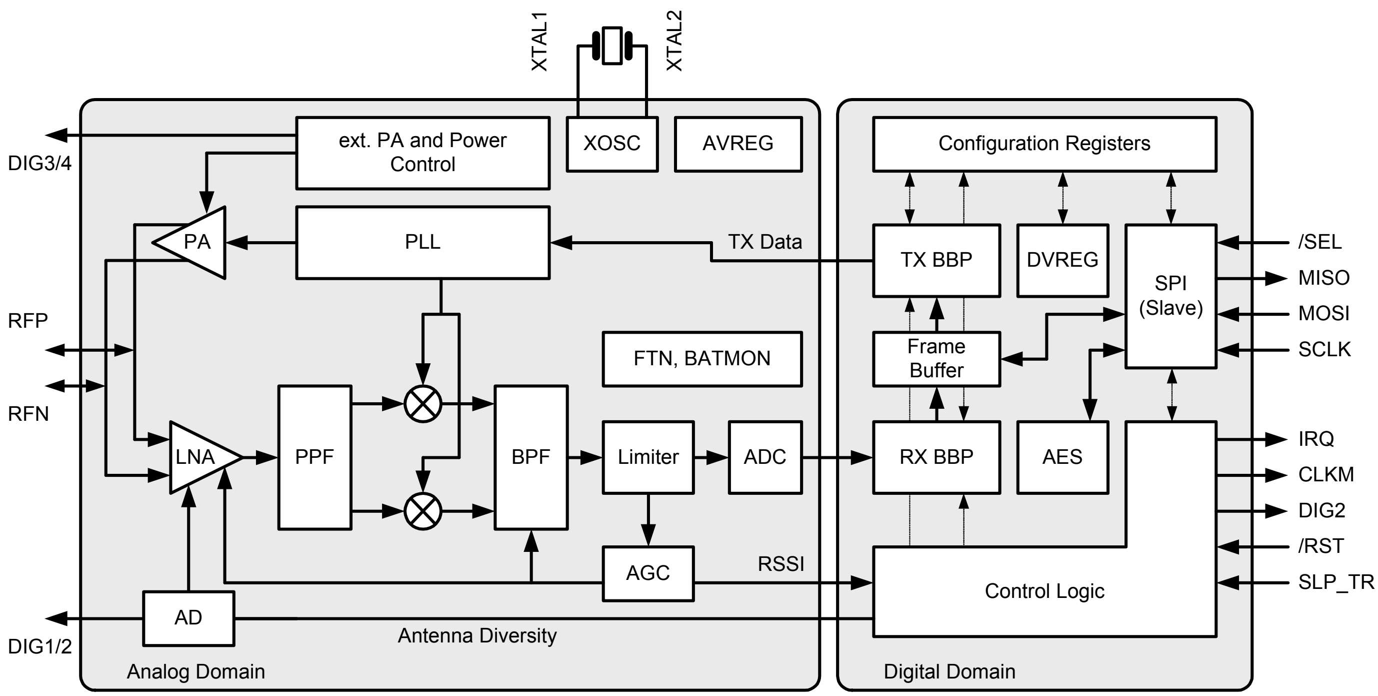
The AT86RF231 can be operated by using an external microcontroller like Atmel's AVR microcontrollers. A comprehensive software programming description can be found in reference [6], AT86RF231 Software Programming Model.

4. General Circuit Description

This single-chip radio transceiver provides a complete radio transceiver interface between an antenna and a microcontroller. It comprises the analog radio, digital modulation and demodulation including time and frequency synchronization and data buffering. The number of external components is minimized such that only the antenna, the crystal and decoupling capacitors are required. The bidirectional differential antenna pins (RFP, RFN) are used for transmission and reception, thus no external antenna switch is needed.

The AT86RF231 block diagram is shown in Figure 4-1 on page 10.

Figure 4-1. AT86RF231 Block Diagram



The received RF signal at pins RFN and RFP is differentially fed through the low-noise amplifier (LNA) to the RF filter (PPF) to generate a complex signal, driving the integrated channel filter (BPF). The limiting amplifier provides sufficient gain to drive the succeeding analog-to-digital converter (ADC) and generates a digital RSSI signal. The ADC output signal is sampled by the digital base band receiver (RX BBP).

The transmit modulation scheme is offset-QPSK (O-QPSK) with half-sine pulse shaping and 32-length block coding (spreading) according to [1] and [2]. The modulation signal is generated in the digital transmitter (TX BBP) and applied to the fractional-N frequency synthesis (PLL), to ensure the coherent phase modulation required for demodulation of O-QPSK signals. The frequency-modulated signal is fed to the power amplifier (PA).

A differential pin pair DIG3/DIG4 can be enabled to control an external RF front-end.

Two on-chip low-dropout voltage regulators (A|DVREG) provide the analog and digital 1.8V supply.

An internal 128-byte RAM for RX and TX (Frame Buffer) buffers the data to be transmitted or the received data.

The configuration of the AT86RF231, reading and writing of Frame Buffer is controlled by the SPI interface and additional control lines.

The AT86RF231 further contains comprehensive hardware-MAC support (Extended Operating Mode) and a security engine (AES) to improve the overall system power efficiency and timing. The stand-alone 128-bit AES engine can be accessed in parallel to all PHY operational transactions and states using the SPI interface, except during SLEEP state.

For applications not necessarily targeting IEEE 802.15.4 compliant networks, the radio transceiver also supports alternative data rates up to 2 Mb/s.

For long-range applications or to improve the reliability of an RF connection the RF performance can further be improved by using an external RF front-end or Antenna Diversity. Both operation modes are supported by the AT86RF231 with dedicated control pins without the interaction of the microcontroller.

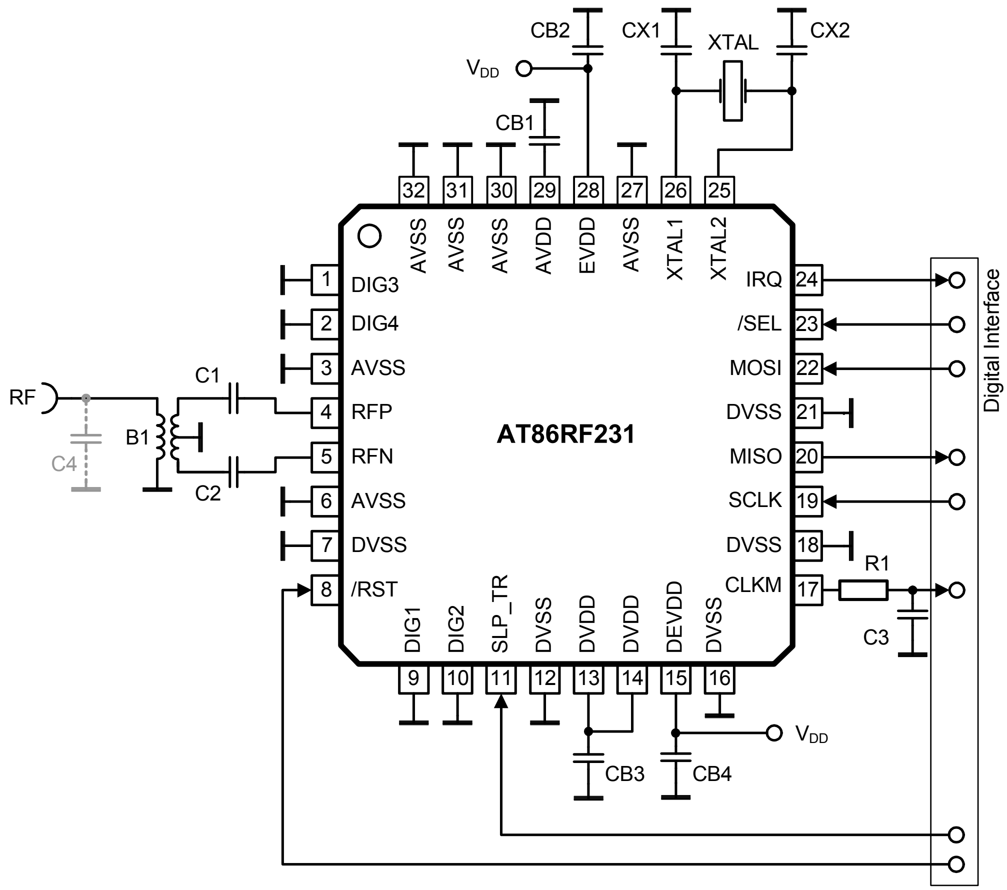
Additional features of the Extended Feature Set, see Section 11. “AT86RF231 Extended Feature Set” on page 128, are provided to simplify the interaction between radio transceiver and microcontroller.

5. Application Circuits

5.1 Basic Application Schematic

A basic application schematic of the AT86RF231 with a single-ended RF connector is shown in Figure 5-1 on page 12. The 50Ω single-ended RF input is transformed to the 100Ω differential RF port impedance using balun B1. The capacitors C1 and C2 provide AC coupling of the RF input to the RF port, optional capacitor C4 improves matching if required.

Figure 5-1. Basic Application Schematic



The power supply decoupling capacitors (CB2, CB4) are connected to the external analog supply pin (EVDD, pin 28) and external digital supply pin (DEVDD, pin 15). Capacitors CB1 and CB3 are bypass capacitors for the integrated analog and digital voltage regulators to ensure stable operation. All decoupling and bypass capacitors should be placed as close as possible to the pins and should have a low-resistance and low-inductance connection to ground to achieve the best performance.

The crystal (XTAL), the two load capacitors (CX1, CX2), and the internal circuitry connected to pins XTAL1 and XTAL2 form the crystal oscillator. To achieve the best accuracy and stability of the reference frequency, large parasitic capacitances should be avoided. Crystal lines should be routed as short as possible and not in proximity of digital I/O signals. This is especially required for the High Data Rate Modes, refer to Section 11.3 "High Data Rate Modes" on page 137.

Crosstalk from digital signals on the crystal pins or the RF pins can degrade the system performance. Therefore, a low-pass filter (C3, R1) is placed close to the CLKM output pin to reduce the emission of CLKM signal harmonics. This is not needed if the CLKM pin is not used as a microcontroller clock source. In that case, the output should be turned off during device initialization.

The ground plane of the application board should be separated into four independent fragments, the analog, the digital, the antenna and the XTAL ground plane. The exposed paddle shall act as the reference point of the individual grounds.

Table 5-1. Example Bill of Materials (BoM) for Basic Application Schematic

<table>
<tr><th>Designator</th><th>Description</th><th>Value</th><th>Manufacture</th><th>Part Number</th><th colspan="3">Comment</th></tr>
<tr><td>B1</td><td>SMD balun</td><td>2.45 GHz</td><td>Wuerth</td><td>748421245</td><td colspan="3">2.45 GHz Balun</td></tr>
<tr><td>B1
(alternatively)</td><td>SMD balun / filter</td><td>2.45 GHz</td><td>Johanson
Technology</td><td>2450FB15L0001</td><td colspan="3">2.45 GHz Balun / Filter</td></tr>
<tr><td>CB1
CB3</td><td>LDO VREG
bypass capacitor</td><td rowspan="2">1 µF</td><td rowspan="2">AVX
Murata</td><td rowspan="2">0603YD105KAT2A
GRM188R61C105KA12D</td><td rowspan="2">X5R
(0603)</td><td rowspan="2">10%</td><td rowspan="2">16V</td></tr>
<tr><td>CB2
CB4</td><td>Power Supply decoupling</td></tr>
<tr><td>CX1, CX2</td><td>Crystal load capacitor</td><td>12 pF</td><td>AVX
Murata</td><td>06035A120JA
GRP1886C1H120JA01</td><td>COG
(0603)</td><td>5%</td><td rowspan="4">50V</td></tr>
<tr><td rowspan="2">C1, C2</td><td rowspan="2">RF coupling capacitor</td><td rowspan="2">22 pF</td><td rowspan="2">Epcos
Epcos
AVX</td><td rowspan="2">B37930
B37920
06035A220JAT2A</td><td>COG</td><td>5%</td></tr>
<tr><td colspan="2">(0402 or 0603)</td></tr>
<tr><td rowspan="2">C3</td><td rowspan="2">CLKM low-pass
filter capacitor</td><td rowspan="2">2.2 pF</td><td rowspan="2">AVX
Murata</td><td rowspan="2">06035A229DA
GRP1886C1H2R0DA01</td><td>COG
(0603)</td><td>±0.5 pF</td></tr>
<tr><td colspan="3">Designed for f_{CLKM}=1 MHz</td></tr>
<tr><td>C4 (optional)</td><td>RF matching</td><td>0.47 pF</td><td></td><td></td><td colspan="3">Depends on final PCB implementation</td></tr>
<tr><td>R1</td><td>CLKM low-pass
filter resistor</td><td>680Ω</td><td></td><td></td><td colspan="3">Designed for f_{CLKM}=1 MHz</td></tr>
<tr><td>XTAL</td><td>Crystal</td><td>CX-4025 16 MHz
SX-4025 16 MHz</td><td>ACAL Taitjen
Siward</td><td>XWBBPL-F-1
A207-011</td><td></td><td></td><td></td></tr>
</table>

Note: Please note that pins DIG1...4 are connected to the ground in the Basic Application Schematic, refer to Figure 5-1 on page 12. Special programming of these pins require a different schematic, refer to "Extended Feature Set Application Schematic" on page 14.

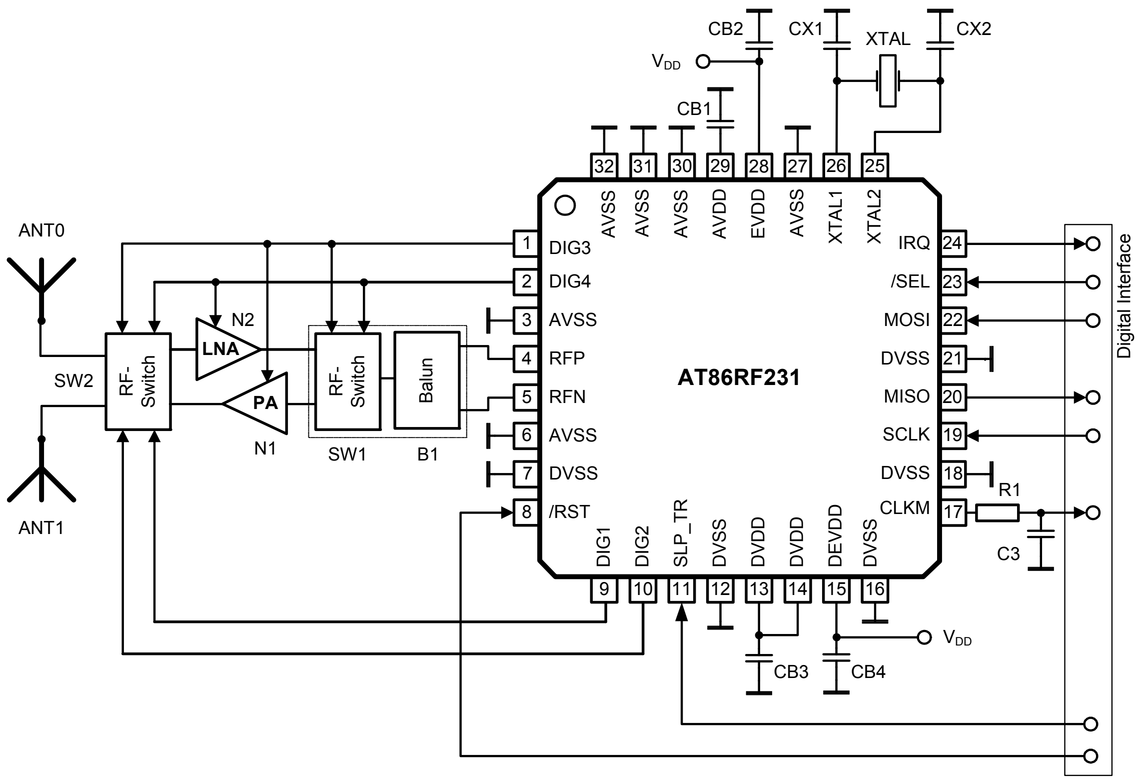
5.2 Extended Feature Set Application Schematic

The AT86RF231 supports additional features like:

• Security Module (AES)		see Section 11.1
• High Data Rate Mode		see Section 11.3
• Antenna Diversity	uses pins DIG1/2	see Section 11.4
• RX/TX indicator	uses pins DIG3/4	see Section 11.5
• RX Frame Time Stamp	uses pin DIG2	see Section 11.6

An extended feature set application schematic illustrating the use of the AT86RF231 Extended Feature Set, see Section 11. "AT86RF231 Extended Feature Set" on page 128, is shown in Figure 5-2 on page 14. Although this example shows all additional hardware features combined, it is possible to use all features separately or in various combinations.

Figure 5-2. Extended Feature Application Schematic



In this example, a balun (B1) transforms the differential RF signal at the radio transceiver RF pins (RFP/RFN) to a single ended RF signal, similar to the Basic Application Schematic; refer to Figure 5-1 on page 12. The RF-Switches (SW1, SW2) separate between receive and transmit path in an external RF front-end.

These switches are controlled by the RX/TX Indicator, represented by the differential pin pair DIG3/DIG4, refer to Section 11.5 "RX/TX Indicator" on page 147.

During receive the radio transceiver searches for the most reliable RF signal path using the Antenna Diversity algorithm. One antenna is selected (SW2) by the Antenna Diversity RF switch control pins DIG1/DIG2, the RF signal is amplified by an optional low-noise amplifier (N2) and fed to the radio transceiver using the second RX/TX switch (SW1).

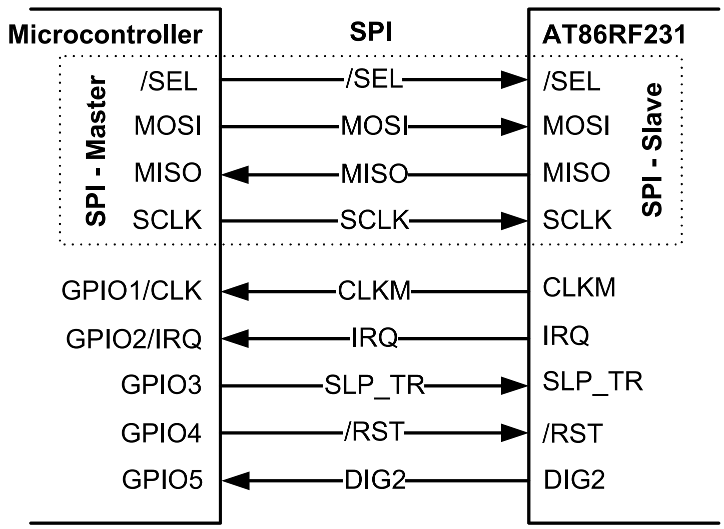
During transmit the AT86RF231 TX signal is amplified using an external PA (N1) and fed to the antennas via an RF switch (SW2). In this example RF switch SW2 further supports Antenna Diversity controlled by the differential pin pair DIG1/DIG2.

The security engine (AES) and High Data Rate Modes do not require specific circuitry to operate. The security engine (AES) has to be configured in advance, for details refer to Section 11.1 "Security Module (AES)" on page 128. The High Data Rate Modes are enabled by register bits OQPSK_DATA_RATE (register 0x0C, TRX_CTRL_2), for details refer to Section 11.3 "High Data Rate Modes" on page 137.

6. Microcontroller Interface

This section describes the AT86RF231 to microcontroller interface. The interface comprises a slave SPI and additional control signals; see Figure 6-1 on page 16. The SPI timing and protocol are described below.

Figure 6-1. Microcontroller to AT86RF231 Interface



Microcontrollers with a master SPI such as Atmel's AVR family interface directly to the AT86RF231. The SPI is used for register, Frame Buffer, SRAM and AES access. The additional control signals are connected to the GPIO/IRQ interface of the microcontroller.

Table 6-1 on page 16 introduces the radio transceiver I/O signals and their functionality.

Table 6-1. Signal Description of Microcontroller Interface

Signal	Description
/SEL	SPI select signal, active low
MOSI	SPI data (master output slave input) signal
MISO	SPI data (master input slave output) signal
SCLK	SPI clock signal
CLKM	Clock output, refer to Section 9.6.4 usable as: -microcontroller clock source -high precision timing reference -MAC timer reference
IRQ	Interrupt request signal, further used as: -Frame Buffer Empty Indicator, refer to Section 11.7

Table 6-1. Signal Description of Microcontroller Interface (Continued)

SLP_TR	Multipurpose control signal (functionality is state dependent, see Section 6.5): -Sleep/Wakeup enable/disable SLEEP state -TX start BUSY_TX_(ARET) state -disable/enable CLKM RX_(AACK)_ON state
/RST	AT86RF231 reset signal, active low
DIG2	Optional, IRQ_2 (RX_START) for RX Frame Time Stamping, see Section 11.6

6.1 SPI Timing Description

Pin 17 (CLKM) can be used as a microcontroller master clock source. If the microcontroller derives the SPI master clock (SCLK) directly from CLKM, the SPI operates in synchronous mode, otherwise in asynchronous mode.

In synchronous mode, the maximum SCLK frequency is 8 MHz.

In asynchronous mode, the maximum SCLK frequency is limited to 7.5 MHz. The signal at pin CLKM is not required to derive SCLK and may be disabled to reduce power consumption and spurious emissions.

Figure 6-2 on page 17 and Figure 6-3 on page 17 illustrate the SPI timing and introduces its parameters. The corresponding timing parameter definitions t_1 - t_9 are defined in Section 12.4 "Digital Interface Timing Characteristics" on page 157.

Figure 6-2. SPI Timing, Global Map and Definition of Timing Parameters t_5, t_6, t_8 and t_9

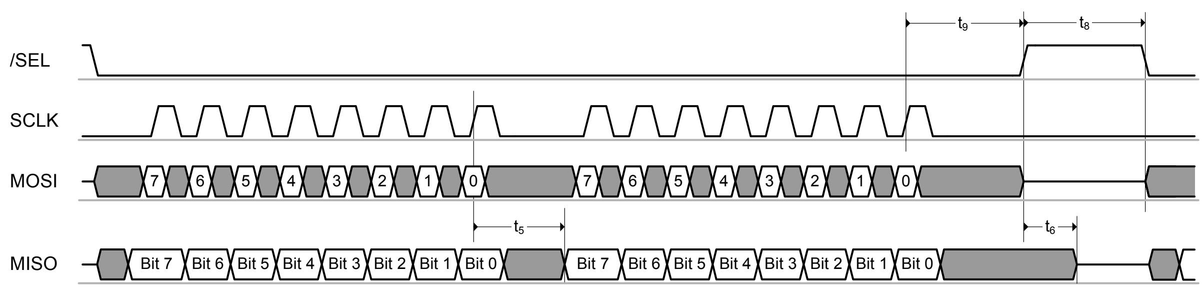
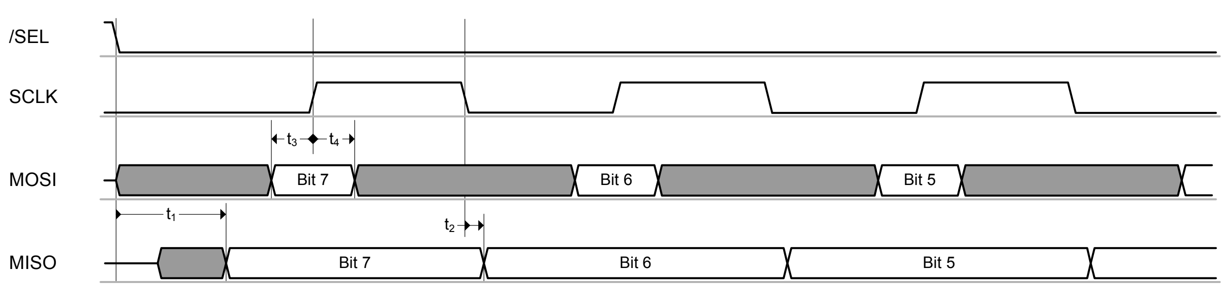


Figure 6-3. SPI Timing, Detailed Drawing of Timing Parameter t_1 to t_4



The SPI is based on a byte-oriented protocol and is always a bidirectional communication between master and slave. The SPI master starts the transfer by asserting /SEL = L. Then the master generates eight SPI clock cycles to transfer one byte to the radio transceiver (via MOSI). At the same time, the slave transmits one byte to the master (via MISO). When the master wants to receive one byte of data from the slave it must also transmit one byte to the slave. All bytes are transferred with MSB first. An SPI transaction is finished by releasing /SEL = H.

An SPI register access consists of two bytes, a Frame Buffer or SRAM access of at least two or more bytes as described in Section 6.2 “SPI Protocol” on page 19.

/SEL = L enables the MISO output driver of the AT86RF231. The MSB of MISO is valid after t1 (see Section 12.4 “Digital Interface Timing Characteristics” on page 157 parameter 12.4.3) and is updated at each falling edge of SCLK. If the driver is disabled, there is no internal pull-up circuitry connected to it. Driving the appropriate signal level must be ensured by the master device or an external pull-up resistor. Note, when both /SEL and /RST are active, the MISO output driver is also enabled.

Referring to Figure 6-2 on page 17 and Figure 6-3 on page 17 MOSI is sampled at the rising edge of the SCLK signal and the output is set at the falling edge of SCLK. The signal must be stable before and after the rising edge of SCLK as specified by t_3 and t_4, refer to Section 12.4 “Digital Interface Timing Characteristics” on page 157 parameters 12.4.5 and 12.4.6.

This SPI operational mode is commonly known as "*SPI mode 0*".

6.2 SPI Protocol

Each SPI sequence starts with transferring a command byte from the SPI master via MOSI (see Table 6-2 on page 19) with MSB first. This command byte defines the SPI access mode and additional mode-dependent information.

Table 6-2. SPI Command Byte definition

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access Mode	Access Type
1	0	Register address [5:0]						Register access	Read access
1	1	Register address [5:0]							Write access
0	0	1	Reserved					Frame Buffer access	Read access
0	1	1	Reserved						Write access
0	0	0	Reserved					SRAM access	Read access
0	1	0	Reserved						Write access

Each SPI transfer returns bytes back to the SPI master on MISO. The content of the first byte (see value "PHY_STATUS" in Figure 6-4 on page 19 to Figure 6-14 on page 23) is set to zero after reset. To transfer status information of the radio transceiver to the microcontroller, the content of the first byte can be configured with register bits SPI_CMD_MODE (register 0x04, TRX_CTRL_1). For details, refer to Section 6.3.1 "Register Description - SPI Control" on page 24.

In Figure 6-4 on page 19 to Figure 6-14 on page 23 and the following chapters logic values stated with XX on MOSI are ignored by the radio transceiver, but need to have a valid logic level. Return values on MISO stated as XX shall be ignored by the microcontroller.

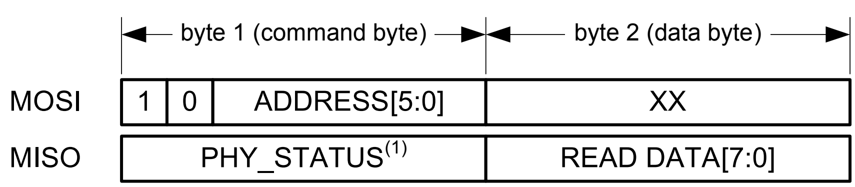
The different access modes are described within the following sections.

6.2.1 Register Access Mode

A register access mode is a two-byte read/write operation initiated by /SEL = L. The first transferred byte on MOSI is the command byte including an identifier bit (bit7 = 1), a read/write select bit (bit 6), and a 6-bit register address.

On read access, the content of the selected register address is returned in the second byte on MISO (see Figure 6-4 on page 19).

Figure 6-4. Packet Structure - Register Read Access



Note: 1. Each SPI access can be configured to return radio controller status information *(PHY_STATUS)* on MISO, for details refer to Section 6.3 "Radio Transceiver Status information" on page 24.

On write access, the second byte transferred on MOSI contains the write data to the selected address (see Figure 6-5 on page 20).

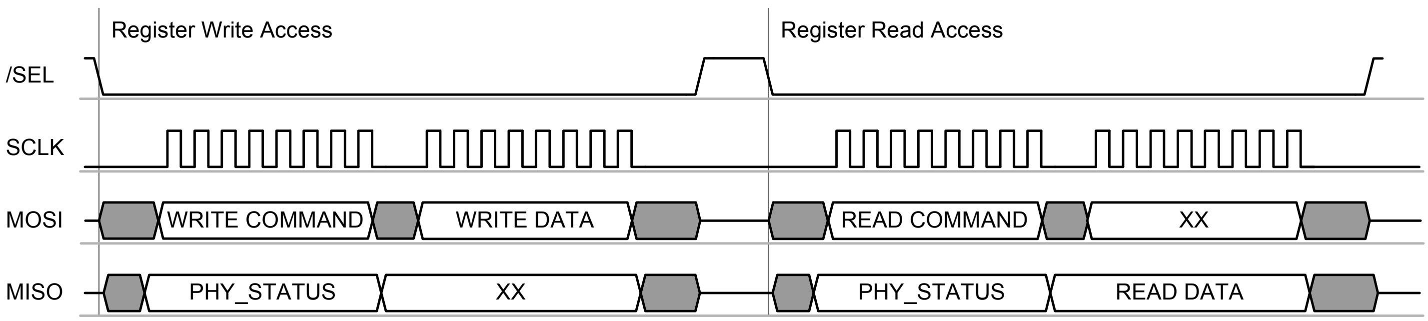
Figure 6-5. Packet Structure - Register Write Access

	byte 1 (command byte)			byte 2 (data byte)
MOSI	1	1	ADDRESS[5:0]	WRITE DATA[7:0]
MISO	PHY_STATUS			XX

Each register access must be terminated by setting /SEL = H.

Figure 6-6 on page 20 illustrates a typical SPI sequence for a register access sequence for write and read respectively.

Figure 6-6. Example SPI Sequence - Register Access Mode



6.2.2 Frame Buffer Access Mode

The 128-byte Frame Buffer can hold the PHY service data unit (PSDU) data of one IEEE 802.15.4 compliant RX or one TX frame of maximum length at a time. A detailed description of the Frame Buffer can be found in Section 9.3 “Frame Buffer” on page 107. An introduction to the IEEE 802.15.4 frame format can be found in Section 8.1 “Introduction - IEEE 802.15.4 - 2006 Frame Format” on page 79.

Frame Buffer read and write accesses are used to read or write frame data (PSDU and additional information) from or to the Frame Buffer. Each access starts with /SEL = L followed by a command byte on MOSI. If this byte indicates a frame read or write access, the next byte PHR[7:0] indicates the frame length followed by the PSDU data, see Figure 6-7 on page 20 and Figure 6-8 on page 21.

On Frame Buffer read access, PHY header (PHR) and PSDU are transferred via MISO starting with the second byte. After the PSDU data, one more byte is transferred containing the link quality indication (LQI) value of the received frame, for details refer to Section 8.6 “Link Quality Indication (LQI)” on page 99. Figure 6-7 on page 20 illustrates the packet structure of a Frame Buffer read access.

Figure 6-7. Packet Structure - Frame Read Access

	byte 1 (command byte)				byte 2 (data byte)	byte 3 (data byte)		byte *n-1* (data byte)	byte *n* (data byte)
MOSI	0	0	1	reserved[4:0]	XX	XX	...	XX	XX
MISO	PHY_STATUS				PHR[7:0]	PSDU[7:0]	...	PSDU[7:0]	LQI[7:0]

Note, the Frame Buffer read access can be terminated at any time without any consequences by setting /SEL = H, e.g. after reading the PHR byte only.

On Frame Buffer write access the second byte transferred on MOSI contains the frame length (PHR field) followed by the payload data (PSDU) as shown by Figure 6-8 on page 21.

Figure 6-8. Packet Structure - Frame Write Access

	byte 1 (command byte)	byte 2 (data byte)	byte 3 (data byte)		byte *n*-1 (data byte)	byte *n* (data byte)
MOSI	0 | 1 | 1 | reserved[4:0]	PHR[7:0]	PSDU[7:0]	...	PSDU[7:0]	PSDU[7:0]
MISO	PHY_STATUS	XX	XX	...	XX	XX

The number of bytes n for one frame access is calculated as follows:

- **Read Access:** *n = 3 + frame_length*

  [*PHY_STATUS, PHR* byte, PSDU data, and LQI byte]

- **Write Access:** *n = 2 + frame_length*

  [command byte, *PHR* byte, and PSDU data]

The maximum value of frame_length is 127 bytes. That means that $n \le 130$ for Frame Buffer read and $n \le 129$ for Frame Buffer write accesses.

Each read or write of a data byte increments automatically the address counter of the Frame Buffer until the access is terminated by setting /SEL = H. A Frame Buffer read access may be terminated (/SEL = H) at any time without affecting the Frame Buffer content. Another Frame Buffer read operation starts again at the PHR field.

The content of the Frame Buffer is only overwritten by a new received frame or a Frame Buffer write access.

Figure 6-9 on page 21 and Figure 6-10 on page 22 illustrate an example SPI sequence of a Frame Buffer access to read and write a frame with 4-byte PSDU respectively.

Figure 6-9. Example SPI Sequence - Frame Buffer Read of a Frame with 4-byte PSDU

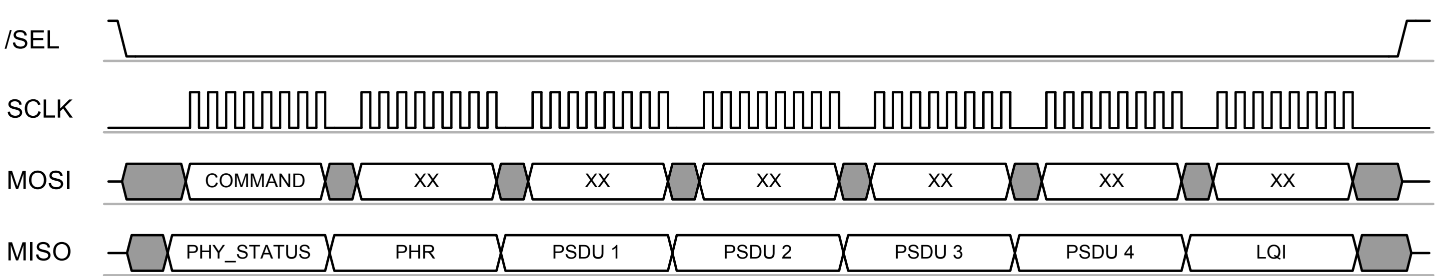
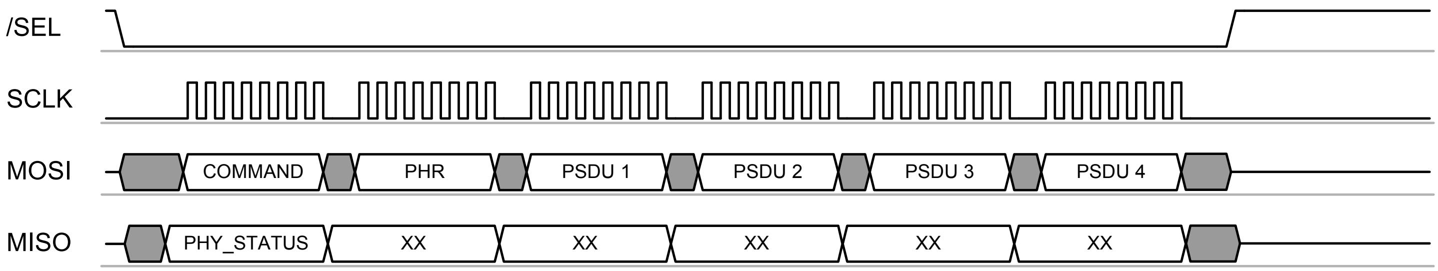


Figure 6-10. Example SPI Sequence - Frame Buffer Write of a Frame with 4 byte PSDU



Access violations during a Frame Buffer read or write access are indicated by interrupt IRQ_6 (TRX_UR). For further details, refer to Section 9.3 "Frame Buffer" on page 107.

Notes

- The Frame Buffer is shared between RX and TX; therefore, the frame data are overwritten by new incoming frames. If the TX frame data are to be retransmitted, it must be ensured that no frame was received in the meanwhile.
- To avoid overwriting during receive *Dynamic Frame Buffer Protection* can be enabled, refer to Section 11.8 "Dynamic Frame Buffer Protection" on page 154.
- It is not possible to retransmit received frames without a Frame Buffer read and write access cycle.
- For exceptions, e.g. receiving acknowledgement frames in Extended Operating Mode (TX_ARET) refer to Section 7.2.4 "TX_ARET_ON - Transmit with Automatic Retry and CSMA-CA Retry" on page 64.

6.2.3 SRAM Access Mode

The SRAM access mode allows accessing dedicated bytes within the Frame Buffer. This may reduce the SPI traffic.

The SRAM access mode is useful, for instance, if a transmit frame is already stored in the Frame Buffer and dedicated bytes (e.g. sequence number, address field) need to be replaced before retransmitting the frame. Furthermore, it can be used to access only the LQI value after frame reception. A detailed description of the user accessible frame content can be found in Section 9.3 "Frame Buffer" on page 107.

Each SRAM access starts with /SEL = L. The first transferred byte on MOSI shall be the command byte and must indicate an SRAM access mode according to the definition in Table 6-2 on page 19. The following byte indicates the start address of the write or read access. The address space is 0x00 to 0x7F for radio transceiver receive or transmit operations.

On SRAM read access, one or more bytes of read data are transferred on MISO starting with the third byte of the access sequence (see Figure 6-11 on page 22).

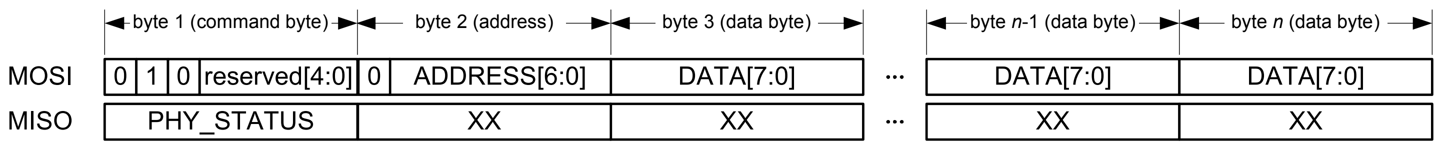
Figure 6-11. Packet Structure - SRAM Read Access

	byte 1 (command byte)	byte 2 (address)	byte 3 (data byte)		byte *n*-1 (data byte)	byte *n* (data byte)
MOSI	0 0 0 reserved[4:0]	0 ADDRESS[6:0]	XX	...	XX	XX
MISO	PHY_STATUS	XX	DATA[7:0]	...	DATA[7:0]	DATA[7:0]

On SRAM write access, one or more bytes of write data are transferred on MOSI starting with the third byte of the access sequence (see Figure 6-12 on page 23).

On SRAM read or write accesses do not attempt to read or write bytes beyond the SRAM buffer size.

Figure 6-12. Packet Structure - SRAM Write Access



As long as /SEL = L, every subsequent byte read or byte write increments the address counter of the Frame Buffer until the SRAM access is terminated by /SEL = H.

Figure 6-13 on page 23 and Figure 6-14 on page 23 illustrate an example SPI sequence of a SRAM access to read and write a data package of 5-byte length respectively.

Figure 6-13. Example SPI Sequence - SRAM Read Access of a 5 byte Data Package

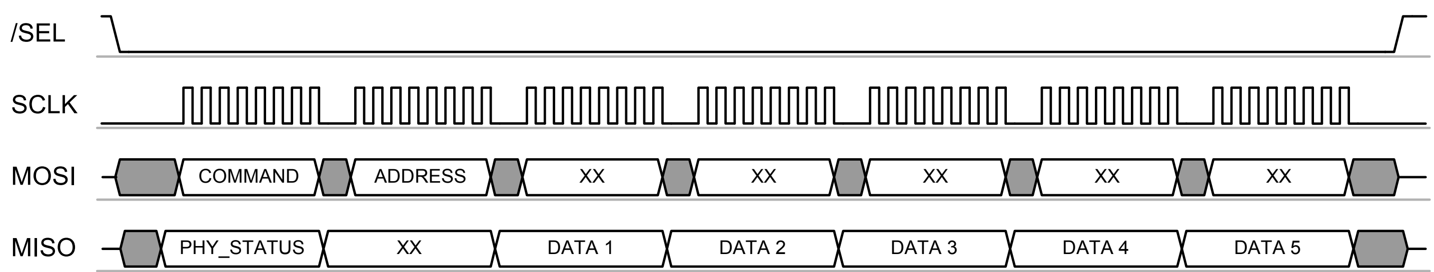
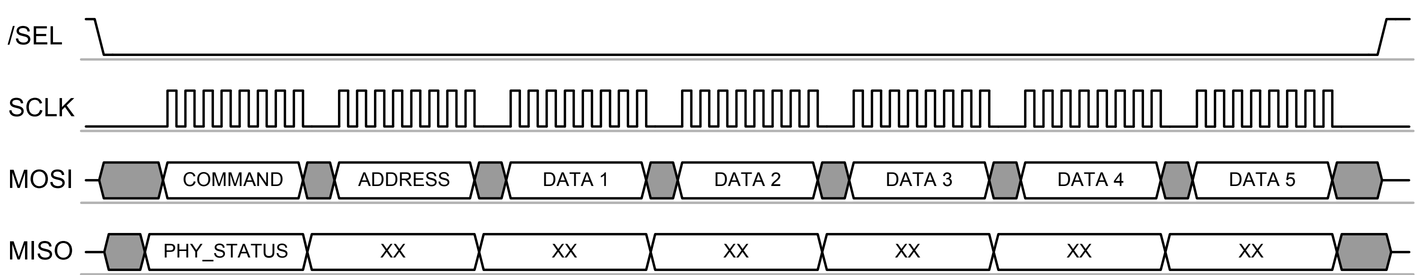


Figure 6-14. Example SPI Sequence - SRAM Write Access of a 5 byte Data Package



Notes

- The SRAM access mode is not intended to be used as an alternative to the Frame Buffer access modes (see Section 6.2.2 "Frame Buffer Access Mode" on page 20).
- If the SRAM access mode is used to read PSDU data, the Frame Buffer contains all PSDU data except the frame length byte (PHR). The frame length information can be accessed only using Frame Buffer access.
- Frame Buffer access violations are not indicated by a TRX_UR interrupt when using the SRAM access mode, for further details refer to Section 9.3.3 "Interrupt Handling" on page 109.

6.3 Radio Transceiver Status information

Each SPI access can be configured to return status information of the radio transceiver (PHY_STATUS) to the microcontroller using the first byte of the data transferred via MISO.

The content of the radio transceiver status information can be configured using register bits SPI_CMD_MODE (register 0x04, TRX_CTRL_1). After reset, the content on the first byte send on MISO to the microcontroller is set to 0x00.

6.3.1 Register Description - SPI Control

Register 0x04 (TRX_CTRL_1):

The TRX_CTRL_1 register is a multi purpose register to control various operating modes and settings of the radio transceiver.

Bit	7	6	5	4	3	2	1	0	
+0x04	PA_EXT_EN	IRQ_2_EXT_EN	TX_AUTO_CRC_ON	RX_BL_CTRL	SPI_CMD_MODE		IRQ_MASK_MODE	IRQ_POLARITY	TRX_CTRL_1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	1	0	0	0	0	0	

- **Bit 7 - PA_EXT_EN**

Refer to Section 11.5 “RX/TX Indicator” on page 147.

- **Bit 6 - IRQ_2_EXT_EN**

Refer to Section 11.6 “RX Frame Time Stamping” on page 150.

- **Bit 5 - TX_AUTO_CRC_ON**

Refer to Section 8.2 “Frame Check Sequence (FCS)” on page 85.

- **Bit 4 - RX_BL_CTRL**

Refer to Section 11.7 “Frame Buffer Empty Indicator” on page 152.

- **Bit [3:2] - SPI_CMD_MODE**

Each SPI transfer returns bytes back to the SPI master. The content of the first byte can be configured using register bits SPI_CMD_MODE. The transfer of the following status information can be configured as follows:

Table 6-3. Radio Transceiver Status Information - PHY_STATUS

Register Bit	Value	Description
SPI_CMD_MODE	0	default (empty, all bits 0x00)
	1	monitor TRX_STATUS register; see Section 7.1.5
	2	monitor PHY_RSSI register; see Section 8.3
	3	monitor IRQ_STATUS register; see Section 6.6

- **Bit 1 - IRQ_MASK_MODE**

Refer to Section 6.6 “Interrupt Logic” on page 29.

- **Bit 0 - IRQ_POLARITY**

Refer to Section 6.6 “Interrupt Logic” on page 29.

6.4 Radio Transceiver Identification

The AT86RF231 can be identified by four registers. One register contains a unique part number and one register the corresponding version number. Two additional registers contain the JEDEC manufacture ID.

6.4.1 Register Description - AT86RF231 Identification

Register 0x1C (PART_NUM):

Bit	7	6	5	4	3	2	1	0	
+0x1C	PART_NUM[7:0]								PART_NUM
Read/Write	R	R	R	R	R	R	R	R	
Reset Value	0	0	0	0	0	0	1	1	

- **Bit [7:0] - PART_NUM**

This register contains the radio transceiver part number.

Table 6-4. Radio Transceiver Part Number

Register Bit	Value	Description
PART_NUM	3	AT86RF231 part number

Register 0x1D (VERSION_NUM):

Bit	7	6	5	4	3	2	1	0	
+0x1D	VERSION_NUM[7:0]								VERSION_NUM
Read/Write	R	R	R	R	R	R	R	R	
Reset Value	0	0	0	0	0	0	1	0	

- **Bit [7:0] - VERSION_NUM**

This register contains the radio transceiver version number.

Table 6-5. Radio Transceiver Version Number

Register Bit	Value	Description
VERSION_NUM	2	Revision A

Register 0x1E (MAN_ID_0):

Bit	7	6	5	4	3	2	1	0	
+0x1E	MAN_ID_0[7:0]								MAN_ID_O
Read/Write	R	R	R	R	R	R	R	R	
Reset Value	0	0	0	1	1	1	1	1	

- **Bit [7:0] - MAN_ID_0**

Bits [7:0] of the 32-bit JEDEC manufacturer ID are stored in register bits MAN_ID_0. Bits [15:8] are stored in register 0x1F (MAN_ID_1). The highest 16 bits of the ID are not stored in registers.