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Features

- High Performance RF-CMOS 2.4GHz radio transceiver targeted for IEEE® 802.15.4, ZigBee®, RF4CE, 6LoWPAN, and ISM applications
- Industry leading link budget:
  - Receiver sensitivity -100dBm
  - Programmable output power from -17dBm up to +3dBm
- Ultra-low current consumption:
  - SLEEP = 0.4µA
  - TRX_OFF = 330µA
  - RX_ON = 11.8mA (LISTEN)
  - BUSY_TX = 13.8mA (at max. transmit power)
- Ultra-low supply voltage (1.8V to 3.6V) with internal regulator
- Support for coin cell operation
- Optimized for low BoM cost and ease of production:
  - Few external components necessary (crystal, capacitors and antenna)
- Easy to use interface:
  - Registers, frame buffer and AES accessible through fast SPI
  - Only two microcontroller GPIO lines necessary
  - One interrupt pin from radio transceiver
  - Clock output
- Radio transceiver features:
  - 128-byte FIFO (SRAM) for data buffering
  - Fully integrated, fast settling PLL to support Frequency Hopping
  - Battery monitor
  - Fast Wake-Up time < 0.4msec
- Special IEEE 802.15.4™-2011 hardware support:
  - FCS computation and Clear Channel Assessment
  - RSSI measurement, Energy Detection and Link Quality Indication
- MAC hardware accelerator:
  - Automated acknowledgement, CSMA-CA and retransmission
  - Automatic address filtering
  - Automated FCS check
- Extended feature set hardware support:
  - AES 128-bit hardware accelerator
  - Antenna Diversity
  - True Random Number Generation for security application
- Commercial temperature range:
  - 0°C to +70°C
- I/O and packages:
  - 32-pin low-profile QFN package 5 x 5 x 0.9mm³
  - RoHS/Fully Green
- Compliant to IEEE 802.15.4-2011, IEEE 802.15.4-2006 and IEEE 802.15.4-2003
- Compliant to EN 300 328/440, FCC-CFR-47 Part 15, ARIB STD-66, RSS-210

Low Power, 2.4GHz Transceiver for ZigBee, IEEE 802.15.4, 6LoWPAN, RF4CE and ISM Applications

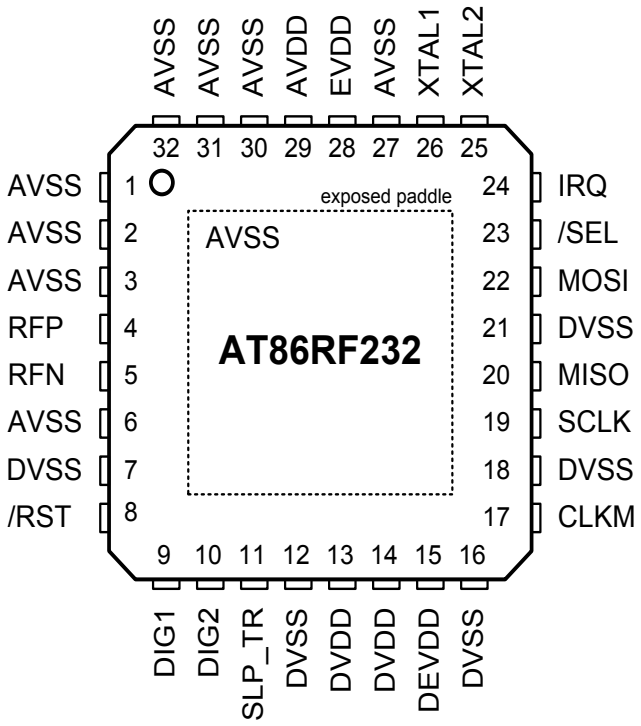
AT86RF232

PRELIMINARY

Rev. 8321A–MCU Wireless–10/11

1 Pin-out Diagram

Figure 1-1. Atmel AT86RF232 Pin-out Diagram.



Note: 1. The exposed paddle is electrically connected to the die inside the package. It shall be soldered to the board to ensure electrical and thermal contact and good mechanical stability.

1.1 Pin Descriptions

Table 1-1. Atmel AT86RF232 Pin Description.

Pins	Name	Type	Description
1	AVSS	Ground	Analog ground
2	AVSS	Ground	Analog ground
3	AVSS	Ground	Ground for RF signals
4	RFP	RF I/O	Differential RF signal
5	RFN	RF I/O	Differential RF signal
6	AVSS	Ground	Ground for RF signals
7	DVSS	Ground	Digital ground
8	/RST	Digital input	Chip reset; active low
9	DIG1	Digital output (Ground)	1. Antenna Diversity RF switch control, see Section 11.3 2. If disabled, pull-down enabled (DVSS)
10	DIG2	Digital output (Ground)	1. Antenna Diversity RF switch control (DIG1 inverted), see Section 11.3 2. RX Frame Time Stamping, see Section 11.4 3. TX Frame Time Stamping, see Section 11.4 4. If functions disabled, pull-down enabled (DVSS)
11	SLP_TR	Digital input	Controls sleep, transmit start, receive states; active high, see Section 6.5
12	DVSS	Ground	Digital ground
13, 14	DVDD	Supply	Regulated 1.8V voltage regulator; digital domain, see Section 9.4
15	DEVDD	Supply	External supply voltage; digital domain
16	DVSS	Ground	Digital ground
17	CLKM	Digital output	Master clock signal output; low if disabled, see Section 9.6
18	DVSS	Ground	Digital ground
19	SCLK	Digital input	SPI clock
20	MISO	Digital output	SPI data output (master input slave output)
21	DVSS	Ground	Digital ground
22	MOSI	Digital input	SPI data input (master output slave input)
23	/SEL	Digital input	SPI select, active low
24	IRQ	Digital output	1. Interrupt request signal; active high or active low; configurable 2. Frame Buffer Empty Indicator; active high, see Section 11.5
25	XTAL2	Analog input	Crystal pin, see Section 9.6
26	XTAL1	Analog input	Crystal pin or external clock supply, see Section 9.6
27	AVSS	Ground	Analog ground
28	EVDD	Supply	External supply voltage, analog domain
29	AVDD	Supply	Regulated 1.8V voltage regulator; analog domain, see Section 9.4
30, 31, 32	AVSS	Ground	Analog ground
Paddle	AVSS	Ground	Analog ground; Exposed paddle of QFN package

1.2 Analog and RF Pins

1.2.1 Supply and Ground Pins

EVDD, DEVDD

EVDD and DEVDD are analog and digital supply voltage pins of the Atmel® AT86RF232 radio transceiver.

AVDD, DVDD

AVDD and DVDD are outputs of the internal 1.8V voltage regulators. The voltage regulators can be configured for external supply.

For details, refer to Section 9.4.

AVSS, DVSS

AVSS and DVSS are analog and digital ground pins respectively. The analog and digital power domains should be separated on the PCB.

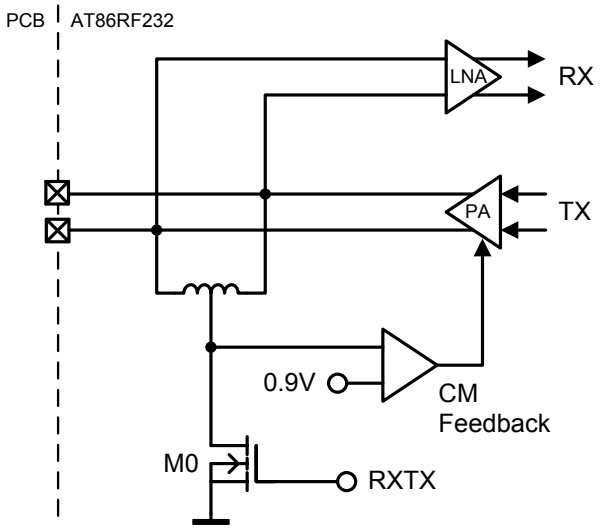
1.2.2 RF Pins

RFN, RFP

A differential RF port (RFP/RFN) provides common-mode rejection to suppress the switching noise of the internal digital signal processing blocks. At board-level, the differential RF layout ensures high receiver sensitivity by rejecting any spurious emissions originated from other digital ICs such as a microcontroller.

A simplified schematic of the RF front end is shown in Figure 1-2.

Figure 1-2. Simplified RF Front-end Schematic.



The RF port is designed for a 100Ω differential load. A DC path between the RF pins is allowed. A DC path to ground or supply voltage is not allowed.

The RF port DC values depend on the operating state, see Chapter 7. In TRX_OFF state, when the analog front-end is disabled (see Section 7.1.2.3), the RF pins are pulled to ground, preventing a floating voltage.

In transmit mode, a control loop provides a common-mode voltage of 0.9V. Transistor M0 is off, allowing the PA to set the common-mode voltage. The common-mode capacitance at each pin to ground shall be < 30pF to ensure the stability of this common-mode feedback loop.

In receive mode, the RF port provides a low-impedance path to ground when transistor M0, see Figure 1-2, pulls the inductor center tap to ground. A DC voltage drop of 20mV across the on-chip inductor can be measured at the RF pins.

1.2.3 Crystal Oscillator Pins

XTAL1, XTAL2

The pin 26 (XTAL1) of Atmel AT86RF232 is the input of the reference oscillator amplifier (XOSC), the pin 25 (XTAL2) is the output. A detailed description of the crystal oscillator setup and the related XTAL1/XTAL2 pin configuration can be found in Section 9.6.

When using an external clock reference signal, XTAL1 shall be used as input pin. For further details, refer to Section 9.6.3.

1.2.4 Analog Pin Summary

Table 1-2. Analog Pin Behavior – DC values.

Pin	Values and Conditions	Comments
RFP/RFN	V_{DC} = 0.9V (BUSY_TX) V_{DC} = 20mV (receive states) V_{DC} = 0mV (otherwise)	DC level at pins RFP/RFN for various transceiver states. AC coupling is required if a circuitry with DC path to ground or supply is used. Serial capacitance and capacitance of each pin to ground must be < 30pF.
XTAL1/XTAL2	V_{DC} = 0.9V at both pins C_{PAR} = 3pF	DC level at pins XTAL1/XTAL2 for various transceiver states. Parasitic capacitance (C_{par}) of the pins must be considered as additional load capacitance to the crystal.
DVDD	V_{DC} = 1.8V (all states, except SLEEP) V_{DC} = 0mV (otherwise)	DC level at pin DVDD for various transceiver states. Supply pins (voltage regulator output) for the digital 1.8V voltage domain, recommended bypass capacitor 100nF.
AVDD	V_{DC} = 1.8V (all states, except P_ON, SLEEP, RESET, and TRX_OFF) V_{DC} = 0mV (otherwise)	DC level at pin AVDD for various transceiver states. Supply pin (voltage regulator output) for the analog 1.8V voltage domain, recommended bypass capacitor 100nF.

1.3 Digital Pins

The Atmel AT86RF232 provides a digital microcontroller interface. The interface comprises a slave SPI (/SEL, SCLK, MOSI and MISO) and additional control signals (CLKM, IRQ, SLP_TR, /RST and DIG2). The microcontroller interface is described in detail in Chapter 6.

Additional digital output signals DIG1 and DIG2 are provided to control external blocks, that is for Antenna Diversity RF switch control, see Section 11.3.

1.3.1 Driver Strength Settings

The driver strength of all digital output pins (MISO, IRQ, DIG1, and DIG2) and CLKM pin are fixed. The capacitive load should be as small as possible as, not larger than 50pF.

1.3.2 Pull-up and Pull-down Configuration

All digital input pins are internally pulled-up or pulled-down in radio transceiver state P_ON, see Section 7.1.2.1. Table 1-3 summarizes the pull-up and pull-down configuration.

Table 1-3. Pull-up / Pull-Down Configuration of Digital Input Pins.

Pins	H $\hat{=}$ pull-up, L $\hat{=}$ pull-down
/RST	H
/SEL	H
SCLK	L
MOSI	L
SLP_TR	L

In all other radio transceiver states, no pull-up or pull-down circuitry is connected to any of the digital input pins mentioned in Table 1-3. In RESET state, the pull-up or pull-down resistors are not enabled.

If the additional digital output signals DIG1or DIG2 are not activated, these pins are pulled-down to digital ground.

2 Disclaimer

Typical values contained in this datasheet are based on simulations and testing. Minimum and maximum values are available when the radio transceiver has been fully characterized.

3 Overview

The Atmel AT86RF232 is a low-power 2.4GHz radio transceiver designed for consumer ZigBee/IEEE 802.15.4, RF4CE, 6LoWPAN, and 2.4GHz ISM band applications. The radio transceiver is a true SPI-to-antenna solution. All RF-critical components except the antenna, crystal and de-coupling capacitors are integrated on-chip. Therefore, the AT86RF232 is particularly suitable for applications like:

- 2.4GHz IEEE 802.15.4 and ZigBee systems
- RF4CE systems
- 6LoWPAN systems
- Wireless sensor networks
- Residential and commercial automation
- Health care
- Consumer electronics
- PC peripherals

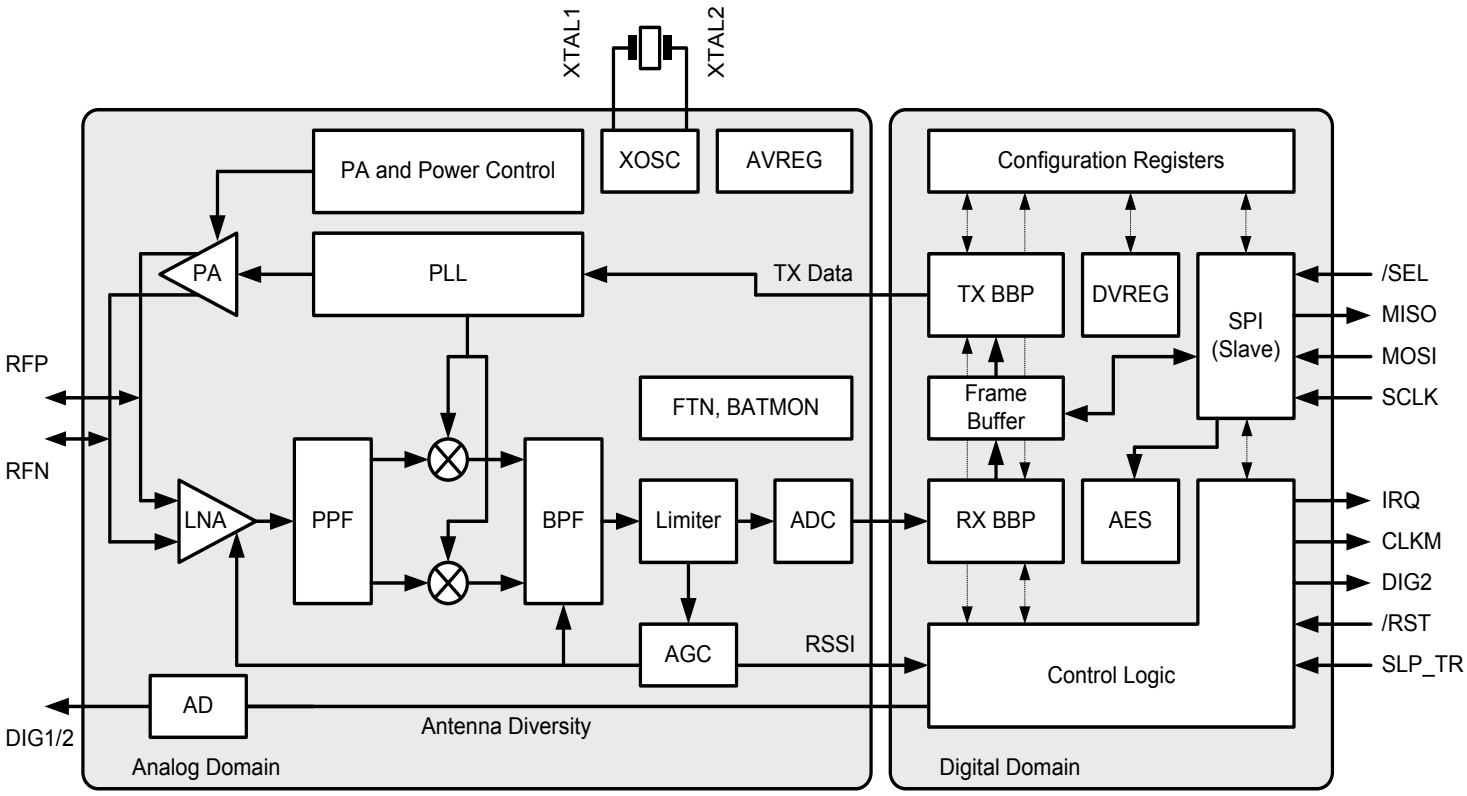
The AT86RF232 can be operated by using an external microcontroller like Atmel AVR® microcontrollers. A comprehensive software programming description can be found in reference [6], AT86RF232 Software Programming Model.

4 General Circuit Description

This single-chip radio transceiver provides a complete radio transceiver interface between an antenna and a microcontroller. It comprises the analog radio, digital modulation and demodulation including time and frequency synchronization and data buffering. The number of external components is minimized such that only the antenna, the crystal and decoupling capacitors are required. The bidirectional differential antenna pins (RFP, RFN) are used for transmission and reception, thus no external antenna switch is needed.

The Atmel AT86RF232 block diagram is shown in Figure 4-1.

Figure 4-1. AT86RF232 Block Diagram.



The received RF signal at pin 5 (RFN) and pin 6 (RFP) is differentially fed through the low-noise amplifier (LNA) to the RF filter (PPF) to generate a complex signal, driving the integrated channel filter (BPF). The limiting amplifier provides sufficient gain to drive the succeeding analog-to-digital converter (ADC) and generates a digital RSSI signal. The ADC output signal is sampled by the digital base band receiver (RX BBP).

The transmit modulation scheme is offset-QPSK (O-QPSK) with half-sine pulse shaping and 32-length block coding (spreading) according to [1] and [2]. The modulation signal is generated in the digital transmitter (TX BBP) and applied to the fractional-N frequency synthesis (PLL), to ensure the coherent phase modulation required for demodulation of O-QPSK signals. The frequency-modulated signal is fed to the power amplifier (PA).

Two on-chip low-dropout voltage regulators (A|DVREG) provide the analog and digital 1.8V supply.

An internal 128-byte RAM for RX and TX (Frame Buffer) buffers the data to be transmitted or the received data.

The configuration of the Atmel AT86RF232, reading and writing of Frame Buffer is controlled by the SPI interface and additional control lines.

The AT86RF232 further contains comprehensive hardware-MAC support (Extended Operating Mode) and a security engine (AES) to improve the overall system power efficiency and timing. The stand-alone 128-bit AES engine can be accessed in parallel to all PHY operational transactions and states using the SPI interface, except during SLEEP state.

To improve the reliability of an RF connection the RF performance can further be improved by using Antenna Diversity.

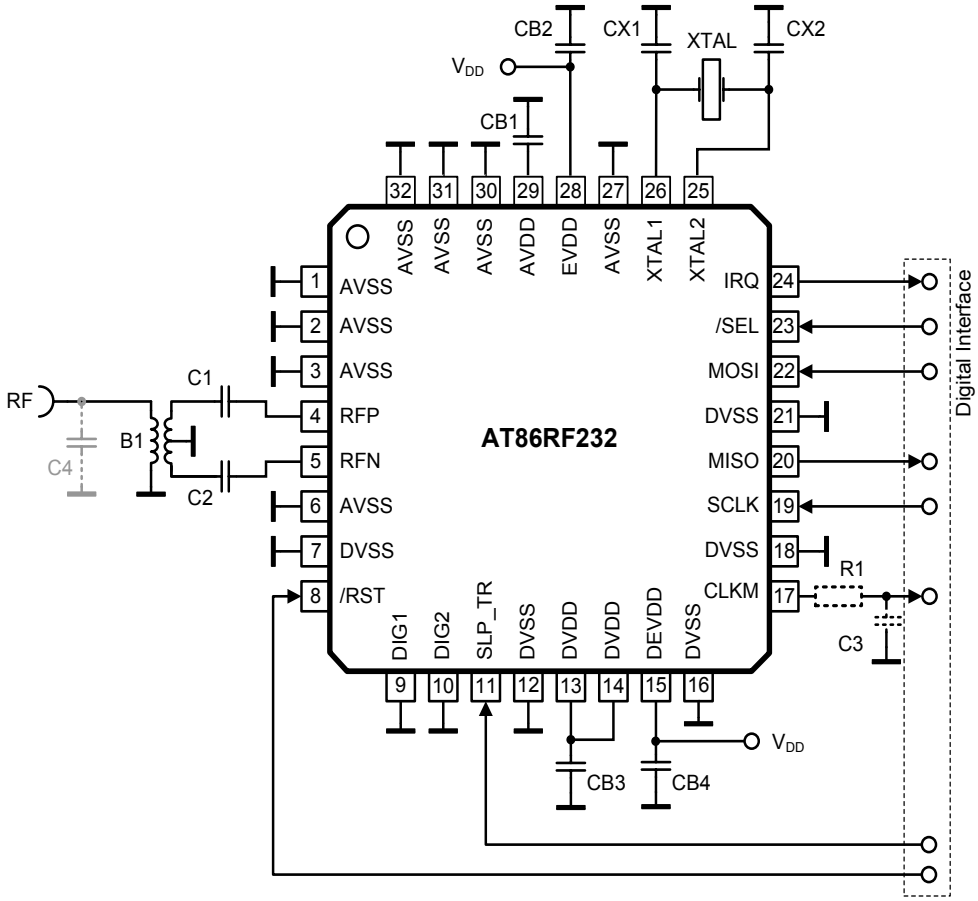
Additional features of the Extended Feature Set, see Chapter 11, are provided to simplify the interaction between radio transceiver and microcontroller.

5 Application Circuits

5.1 Basic Application Schematic

A basic application schematic of the Atmel AT86RF232 with a single-ended RF connector is shown in Figure 5-1. The 50Ω single-ended RF input is transformed to the 100Ω differential RF port impedance using balun B1. The capacitors C1 and C2 provide AC coupling of the RF input to the RF port, optional capacitor C4 improves matching if required.

Figure 5-1. Basic Application Schematic.



The power supply decoupling capacitors (CB2, CB4) are connected to the external analog supply pin 28 (EVDD) and external digital supply pin 15 (DEVDD). Capacitors CB1 and CB3 are bypass capacitors for the integrated analog and digital voltage regulators to ensure stable operation. All decoupling and bypass capacitors should be placed as close as possible to the pins and should have a low-resistance and low-inductance connection to ground to achieve the best performance.

The crystal (XTAL), the two load capacitors (CX1, CX2), and the internal circuitry connected to pins XTAL1 and XTAL2 form the crystal oscillator. To achieve the best accuracy and stability of the reference frequency, large parasitic capacitances should be avoided. Crystal lines should be routed as short as possible and not in proximity of digital I/O signals.

Crosstalk from digital signals on the crystal pins or the RF pins can degrade the system performance. Therefore, a low-pass filter (C3, R1) is placed close to the Atmel AT86RF232 CLKM output pin to reduce the emission of CLKM signal harmonics. This is not needed if the pin 17 (CLKM) is not used as a microcontroller clock source. In that case, the output should be turned off during device initialization.

The ground plane of the application board should be separated into four independent fragments, the analog, the digital, the antenna and the XTAL ground plane. The exposed paddle shall act as the reference point of the individual grounds.

Table 5-1. Example Bill of Materials (BoM) for Basic Application Schematic.

Designator	Description	Value	Manufacturer	Part Number	Comment
B1	SMD balun	2.45GHz	Wuerth	748421245	2.45GHz Balun
B1 (alternatively)	SMD balun / filter	2.45GHz	Johanson Technology	2450FB15L0001	2.45GHz Balun / Filter
CB1 CB3	LDO VREG bypass capacitor	100nF	Generic		X7R 10% 16V (0402)
CB2 CB4	Power supply decoupling	1µF	AVX Murata	0603YD105KAT2A GRM188R61C105KA12D	X5R 10% 16V (0603)
CX1, CX2	Crystal load capacitor	12pF	AVX Murata	06035A120JA GRM1555C1H120JA01D	COG 5% 50V (0402)
C1, C2	RF coupling capacitor	22pF	Murata Epcos AVX	GRM1555C1H220JA01J B37920 06035A220JAT2A	C0G 5% 50V (0402 or 0603)
C3	CLKM low-pass filter capacitor	2.2pF	AVX Murata	06035A229DA GRP1886C1H2R0DA01	COG ±0.5pF 50V (0603) Designed for f_{CLKM} = 1MHz
C4 (optional)	RF matching				Value depends on final PCB implementation
R1	CLKM low-pass filter resistor	680Ω			Designed for f_{CLKM} = 1MHz
XTAL	Crystal	CX-4025 16MHz SX-4025 16MHz	ACAL Taitjen Siward	XWBBPL-F-1 A207-011	

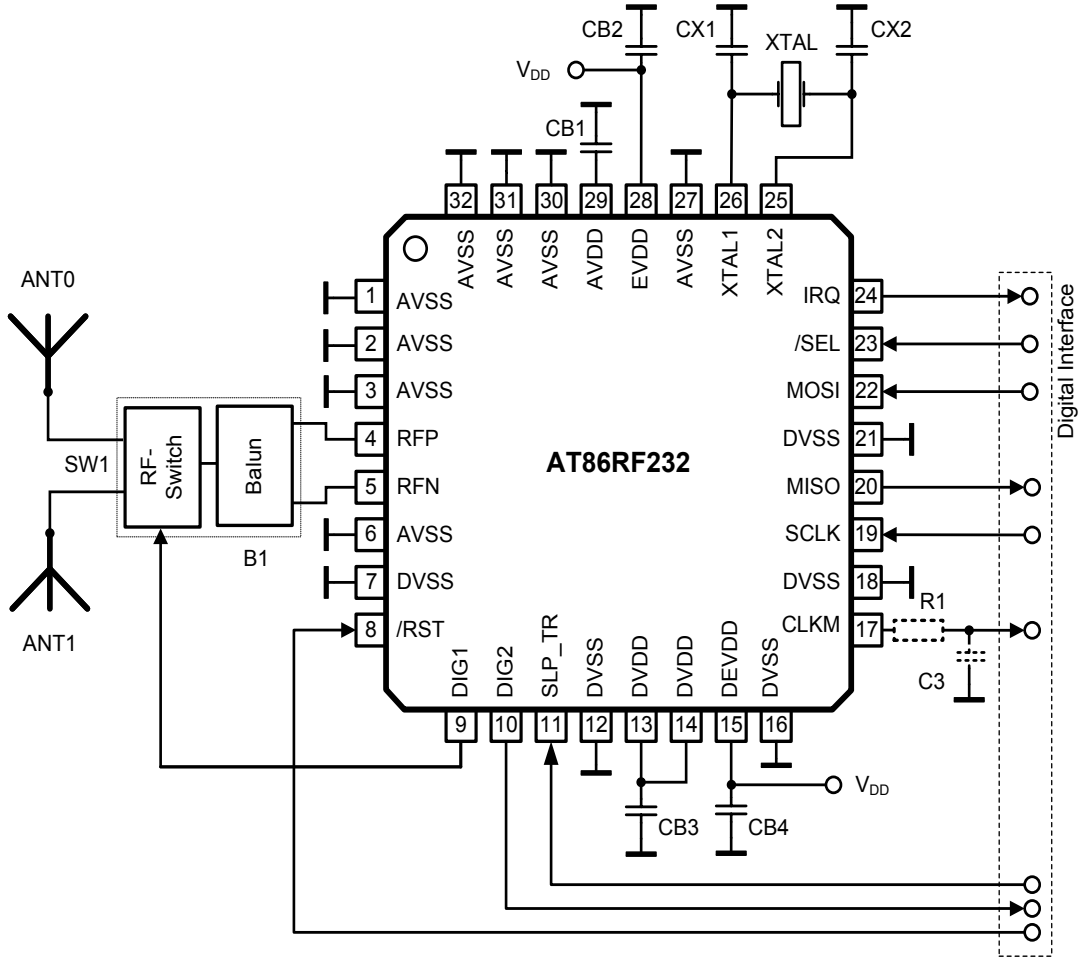
5.2 Extended Feature Set Application Schematic

The Atmel AT86RF232 supports additional features like:

- Security Module (AES) — Section 11.1
- Random Number Generator — Section 11.2
- Antenna Diversity — uses pins DIG1(/2) — Section 11.3
- RX and TX Frame Time Stamping (TX_ARET) — uses pin DIG2 — Section 11.4
- Frame Buffer Empty Indicator — uses pin IRQ — Section 11.5
- Dynamic Frame Buffer Protection — Section 11.6

An extended feature set application schematic illustrating the use of the AT86RF232 Extended Feature Set, see Chapter 11, is shown in Figure 5-2 Although this example shows all additional hardware features combined, it is possible to use all features separately or in various combinations.

Figure 5-2. Extended Feature Application Schematic.



In this example, a balun (B1) transforms the differential RF signal at the Atmel AT86RF232 radio transceiver RF pins (RFP/RFN) to a single ended RF signal, similar to the Basic Application Schematic; refer to Figure 5-1. During receive mode the radio transceiver searches for the most reliable RF signal path using the Antenna Diversity algorithm. One antenna is selected (SW2) by the Antenna Diversity RF switch control pin 9 (DIG1), refer to Section 11.3.

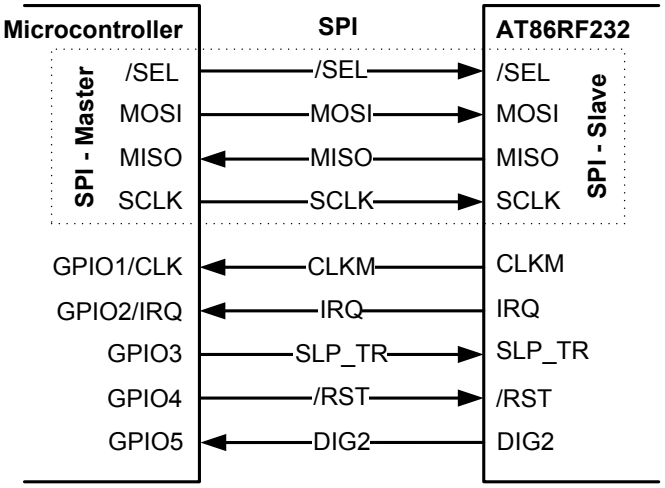
RX and TX Frame Time stamping is implemented through pin 10 (DIG2), refer to Section 11.4.

The security engine (AES) does not require specific circuitry to operate, for details refer to Section 11.1.

6 Microcontroller Interface

This section describes the Atmel AT86RF232 to microcontroller interface. The interface comprises a slave SPI and additional control signals; see Figure 6-1. The SPI timing and protocol are described below.

Figure 6-1. Microcontroller to AT86RF232 Interface.



Microcontrollers with a master SPI such as Atmel AVR family interface directly to the AT86RF232. The SPI is used for register, Frame Buffer, SRAM and AES access. The additional control signals are connected to the GPIO/IRQ interface of the microcontroller. Table 6-1 introduces the radio transceiver I/O signals and their functionality.

Table 6-1. Signal Description of Microcontroller Interface.

Signal	Description
/SEL	SPI select signal, active low
MOSI	SPI data (master output slave input) signal
MISO	SPI data (master input slave output) signal
SCLK	SPI clock signal
CLKM	Optional, Clock output, refer to Section 9.6.4, usable as: - microcontroller clock source - high precision timing reference
IRQ	Interrupt request signal, further used as: - Frame Buffer Empty indicator, refer to Section 11.5
SLP_TR	Multi purpose control signal (functionality is state dependent, see Section 6.5): - Sleep/Wakeup enable/disable SLEEP state - TX start BUSY_TX_(ARET) state
/RST	AT86RF232 reset signal, active low
DIG2	Optional, - IRQ_2 (RX_START) for RX Frame Time Stamping, see Section 11.4 - Signals frame transmit within TX_ARET mode for TX Time Stamping

6.1 SPI Timing Description

Pin 17 (CLKM) can be used as a microcontroller master clock source. If the microcontroller derives the SPI master clock (SCLK) directly from CLKM, the SPI operates in synchronous mode, otherwise in asynchronous mode.

In asynchronous mode, the maximum SCLK frequency f_{async} is limited to 7.5MHz. The signal at pin 17 (CLKM) is not required to derive SCLK and may be disabled to reduce power consumption and spurious emissions.

Figure 6-2 and Figure 6-3 illustrate the SPI timing and introduces its parameters. The corresponding timing parameter definitions t_1 – t_9 are defined in Section 12.4.

Figure 6-2. SPI Timing, Global Map and Definition of Timing Parameters t_5, t_6, t_8, t_9.

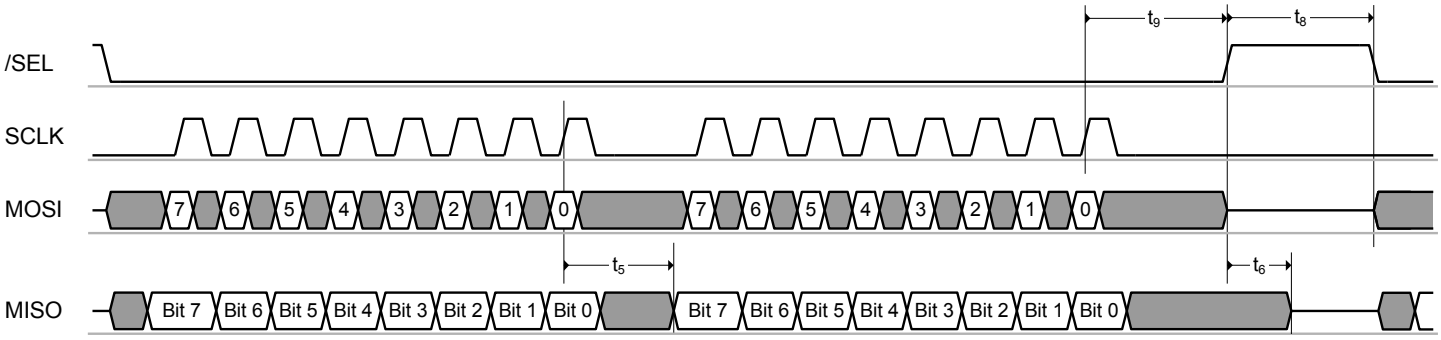
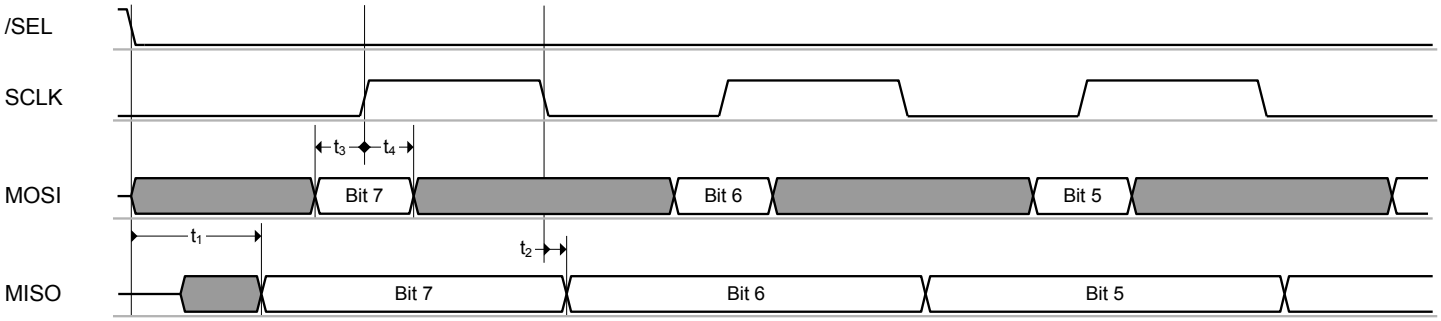


Figure 6-3. SPI Timing, Detailed Drawing of Timing Parameters t_1 to t_4.



The SPI is based on a byte-oriented protocol and is always a bidirectional communication between master and slave. The SPI master starts the transfer by asserting /SEL = L. Then the master generates eight SPI clock cycles to transfer one byte to the radio transceiver (via MOSI). At the same time, the slave transmits one byte to the master (via MISO). When the master wants to receive one byte of data from the slave it must also transmit one byte to the slave. All bytes are transferred with MSB first. An SPI transaction is finished by releasing /SEL = H.

An SPI register access consists of two bytes, a Frame Buffer or SRAM access of at least two or more bytes as described in Section 6.2.

/SEL = L enables the MISO output driver of the Atmel AT86RF232. The MSB of MISO is valid after t_1 (see Section 12.4 parameter) and is updated at each falling edge of SCLK. If the driver is disabled, there is no internal pull-up circuitry connected to it. Driving the appropriate signal level must be ensured by the master device or an external pull-up resistor.

Note: 1. When both /SEL and /RST are active, the MISO output driver is also enabled.

Referring to Figure 6-2 and Figure 6-3 Atmel AT86RF232 MOSI is sampled at the rising edge of the SCLK signal and the output is set at the falling edge of SCLK. The signal must be stable before and after the rising edge of SCLK as specified by t_3 and t_4, refer to Section 12.4 parameters.

This SPI operational mode is commonly known as "*SPI mode 0*".

6.2 SPI Protocol

Each SPI sequence starts with transferring a command byte from the SPI master via MOSI (see Table 6-2) with MSB first. This command byte defines the SPI access mode and additional mode-dependent information.

Table 6-2. SPI Command Byte Definition.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access Mode	Access Type
1	0	Register address [5:0]						Register access	Read access
1	1	Register address [5:0]							Write access
0	0	1	reserved					Frame Buffer access	Read access
0	1	1	reserved						Write access
0	0	0	reserved					SRAM access	Read access
0	1	0	reserved						Write access

Each SPI transfer returns bytes back to the SPI master on MISO. The content of the first byte (see value "*PHY_STATUS*" in Figure 6-4 to Figure 6-14) is set to zero after reset. To transfer status information of the radio transceiver to the microcontroller, the content of the first byte can be configured with register bits SPI_CMD_MODE (register 0x04, TRX_CTRL_1). For details, refer to Section 6.3.1.

In Figure 6-4 to Figure 6-14 and the following chapters logic values stated with XX on MOSI are ignored by the radio transceiver, but need to have a valid logic level. Return values on MISO stated as XX shall be ignored by the microcontroller.

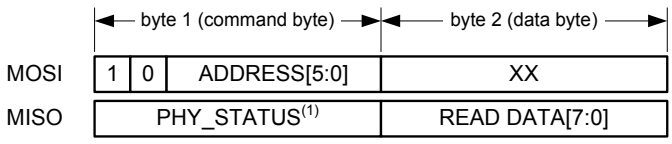
The different access modes are described within the following sections.

6.2.1 Register Access Mode

A register access mode is a two-byte read/write operation initiated by /SEL = L. The first transferred byte on MOSI is the command byte including an identifier bit (bit[7] = 1), a read/write select bit (bit[6]), and a 6-bit register address.

On read access, the content of the selected register address is returned in the second byte on MISO (see Figure 6-4).

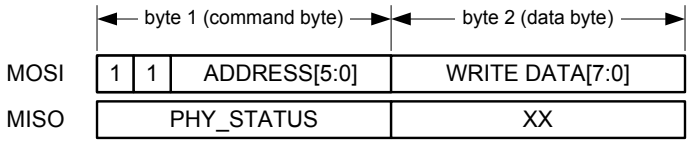
Figure 6-4. Packet Structure - Register Read Access.



Note: 1. Each SPI access can be configured to return radio controller status information (PHY_STATUS) on MISO, for details refer to Section 6.3.

On write access, the second byte transferred on MOSI contains the write data to the selected address (see Figure 6-5).

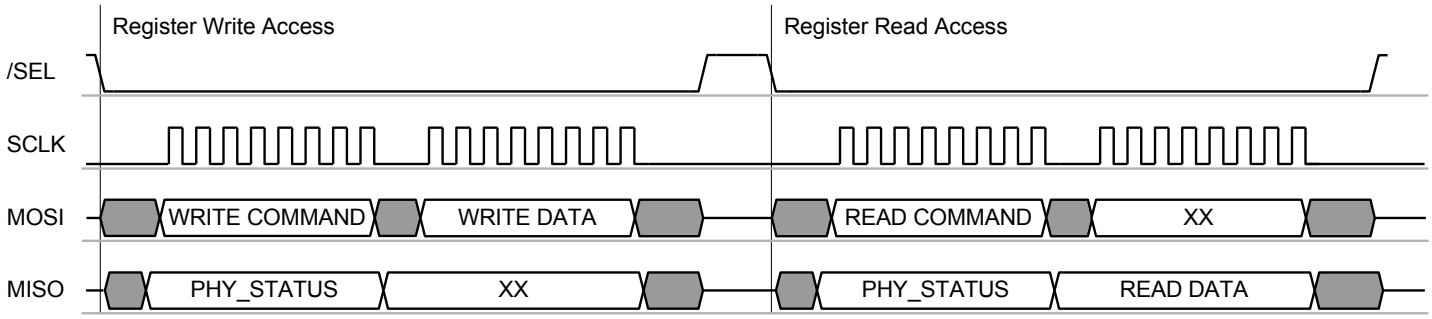
Figure 6-5. Packet Structure - Register Write Access.



Each register access must be terminated by setting /SEL = H.

Figure 6-6 illustrates a typical SPI sequence for a register access sequence for write and read respectively.

Figure 6-6. Example SPI Sequence – Register Access Mode.



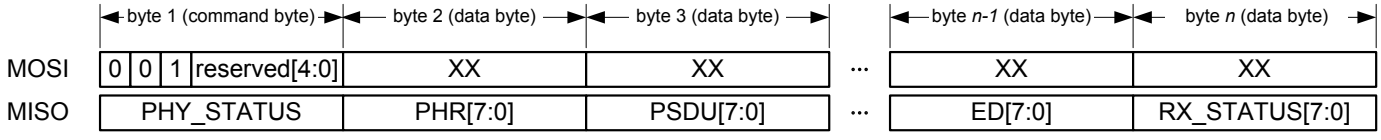
6.2.2 Frame Buffer Access Mode

The Atmel AT86RF232 128-byte Frame Buffer can hold the PHY service data unit (PSDU) data of one IEEE 802.15.4 compliant RX or one TX frame of maximum length at a time. A detailed description of the Frame Buffer can be found in Section 9.3. An introduction to the IEEE 802.15.4 frame format can be found in Section 8.1.

Frame Buffer read and write accesses are used to read or write frame data (PSDU and additional information) from or to the Frame Buffer. Each access starts with /SEL = L followed by a command byte on MOSI. If this byte indicates a frame read or write access, the next byte PHR indicates the frame length followed by the PSDU data, see Figure 6-7 and Figure 6-8.

On Frame Buffer read access, PHY header (PHR) and PSDU are transferred via MISO starting with the second byte. After the PSDU data, three more bytes are transferred containing the link quality indication (LQI) value, the energy detection (ED) value, and the status information (RX_STATUS) of the received frame, for LQI details refer to Section 8.6. The Figure 6-7 illustrates the packet structure of a Frame Buffer read access.

Figure 6-7. Packet Structure - Frame Read Access.



The structure of RX_STATUS is described in Table 6-3.

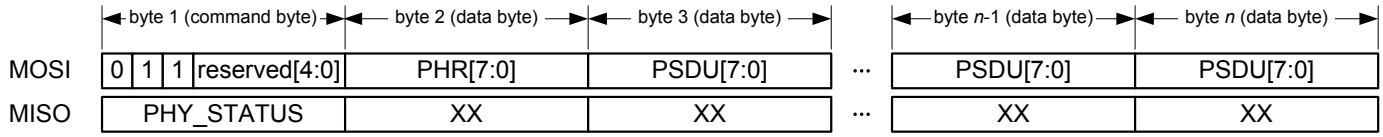
Table 6-3. Structure of RX_STATUS.

Bit	7	6	5	4	
	RX_CRC_VALID	TRAC_STATUS			RX_STATUS
Read/Write	R	R	R	R	
Reset value	0	0	0	0	
Bit	**3**	**2**	**1**	**0**	
	reserved				RX_STATUS
Read/Write	R	R	R	R	
Reset value	0	0	0	0	

Note: 1. More information to RX_CRC_VALID, see Section 8.2.5, and to TRAC_STATUS, see Section 7.2.6.

On Frame Buffer write access the second byte transferred on MOSI contains the frame length (PHR field) followed by the payload data (PSDU) as shown by Figure 6-8.

Figure 6-8. Packet Structure - Frame Write Access.



The number of bytes *n* for one frame access is calculated as follows:

Read Access: *n* = 5 + *frame_length*

[PHY_STATUS, PHR byte, PSDU data, LQI, ED, and RX_STATUS]

Write Access: *n* = 2 + *frame_length*

[command byte, PHR byte, and PSDU data]

Each read or write of a data byte automatically increments the address counter of the Frame Buffer until the access is terminated by setting /SEL = H. A Frame Buffer read access may be terminated (/SEL = H) at any time without affecting the Frame Buffer content. Another Frame Buffer read operation starts again at the PHR field.

The content of the Atmel AT86RF232 Frame Buffer is overwritten by a new received frame or a Frame Buffer write access.

Figure 6-9 and Figure 6-10 illustrate an example SPI sequence of a Frame Buffer access to read a frame with 2-byte PSDU and write a frame with 4-byte PSDU.

Figure 6-9. Example SPI Sequence - Frame Buffer Read of a Frame with 2-byte PSDU.

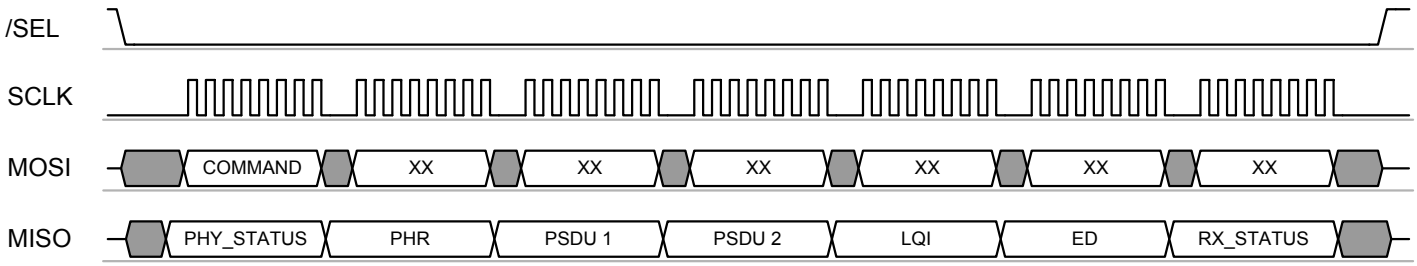
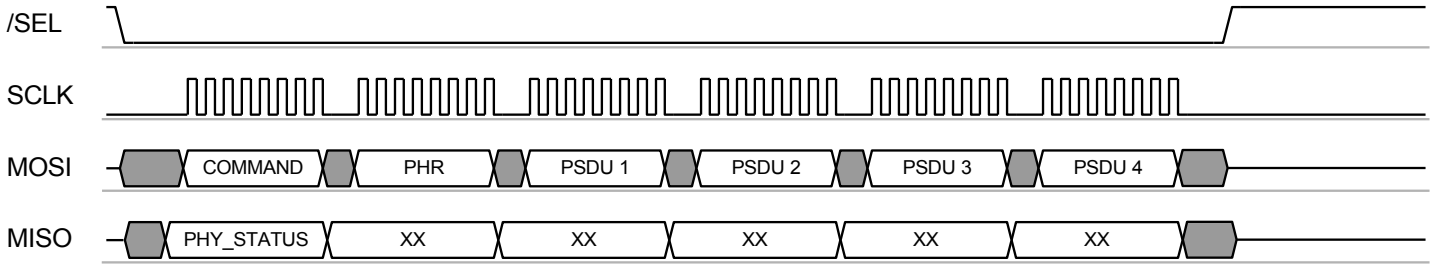


Figure 6-10. Example SPI Sequence - Frame Buffer Write of a Frame with 4-byte PSDU.



Access violations during a Frame Buffer read or write access are indicated by interrupt IRQ_6 (TRX_UR). For further details, refer to Section 9.3.

Notes:
1. The Frame Buffer is shared between RX and TX; therefore, the frame data are overwritten by new incoming frames. If the TX frame data are to be retransmitted, it must be ensured that no frame was received in the meanwhile.
2. To avoid overwriting during receive *Dynamic Frame Buffer Protection* can be enabled, refer to Section 11.6.
3. For exceptions, receiving acknowledgement frames in Extended Operating Mode (TX_ARET) refer to Section 7.2.4.

6.2.3 SRAM Access Mode

The SRAM access mode allows accessing dedicated bytes within the Atmel AT86RF232 Frame Buffer or AES address space, refer to Section 11.1.

During frame receive after occurrence of interrupt IRQ_2 (RX_START) an SRAM access can be used to upload the PHR field while preserving Dynamic Frame Buffer Protection, see Section 11.6.

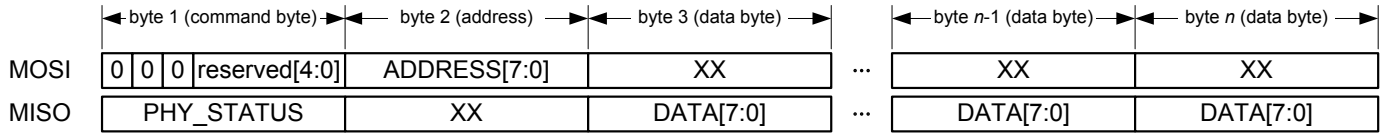
Each SRAM access starts with /SEL = L. The first transferred byte on MOSI shall be the command byte and must indicate an SRAM access mode according to the definition in Table 6-2. The following byte indicates the start address of the write or read access.

SRAM address space:

- Frame Buffer: 0x00 to 0x7F
- AES: 0x82 to 0x94

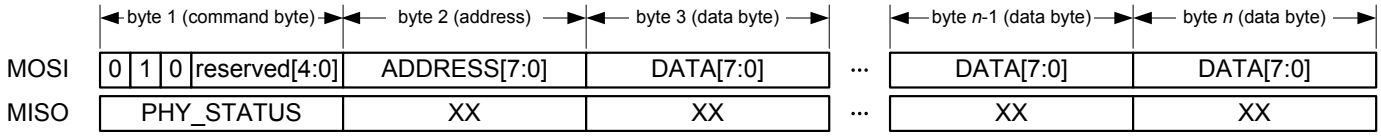
On SRAM read access, one or more bytes of read data are transferred on MISO starting with the third byte of the access sequence (see Figure 6-11).

Figure 6-11. Packet Structure – SRAM Read Access.



On SRAM write access, one or more bytes of write data are transferred on MOSI starting with the third byte of the access sequence (see Figure 6-12).

Figure 6-12. Packet Structure – SRAM Write Access.



As long as /SEL = L, every subsequent byte read or byte write increments the address counter of the Frame Buffer until the SRAM access is terminated by /SEL = H.

Figure 6-13 and Figure 6-14 illustrate an example SPI sequence of an Atmel AT86RF232 SRAM access to read and write a data package of five byte length respectively.

Figure 6-13. Example SPI Sequence – SRAM Read Access of a 5-byte Data Package.

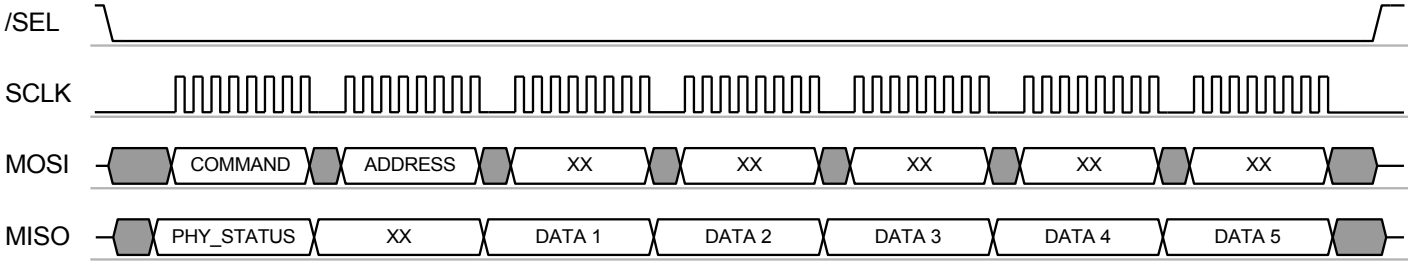
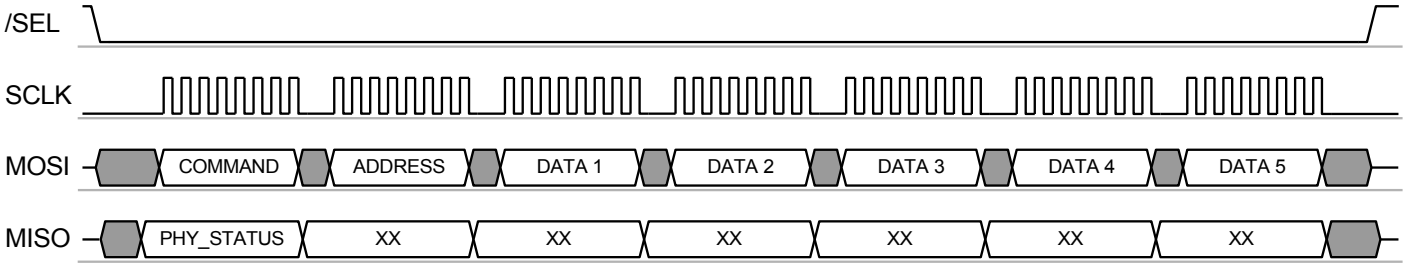


Figure 6-14. Example SPI Sequence – SRAM Write Access of a 5-byte Data Package.



Notes:
1. The SRAM access mode is not intended to be used as an alternative to the Frame Buffer access modes (see Section 6.2.2).
2. Frame Buffer access violations are not indicated by a TRX_UR interrupt when using the SRAM access mode, for further details refer to Section 9.3.3.

6.3 Radio Transceiver Status information

Each Atmel AT86RF232 SPI access can be configured to return status information of the radio transceiver (PHY_STATUS) to the microcontroller using the first byte of the data transferred via MISO.

The content of the radio transceiver status information can be configured using register bits SPI_CMD_MODE (register 0x04, TRX_CTRL_1). After reset, the content on the first byte send on MISO to the microcontroller is set to zero.

6.3.1 Register Description

Register 0x04 (TRX_CTRL_1):

The TRX_CTRL_1 register is a multi-purpose register to control various operating modes and settings of the radio transceiver.

Figure 6-15. Register TRX_CTRL_1.

Bit	7	6	5	4	
0x04	reserved	IRQ_2_EXT_EN	TX_AUTO_CRC_ON	RX_BL_CTRL	TRX_CTRL_1
Read/Write	R/W	R/W	R/W	R/W	
Reset value	0	0	1	0	

Bit	3	2	1	0	
0x04	SPI_CMD_MODE		IRQ_MASK_MODE	IRQ_POLARITY	TRX_CTRL_1
Read/Write	R/W	R/W	R/W	R/W	
Reset value	0	0	1	0	

- **Bit 3:2 - SPI_CMD_MODE**

Each SPI transfer returns bytes back to the SPI master. The content of the first byte (PHY_STATUS) can be configured using register bits SPI_CMD_MODE.

Table 6-4. SPI_CMD_MODE.

Register Bits	Value	Description
SPI_CMD_MODE	0	Default (empty, all bits zero)
	1	Monitor TRX_STATUS register
	2	Monitor PHY_RSSI register
	3	Monitor IRQ_STATUS register

Note: 1. More information to register TRX_STATUS, see Section 7.1.5, to register PHY_RSSI, see Section 8.3, and to register IRQ_STATUS, see Section 6.6.

6.4 Radio Transceiver Identification

The Atmel AT86RF232 can be identified by four registers. One register contains a unique part number and one register the corresponding version number. Two additional registers contain the JEDEC manufacture ID.

6.4.1 Register Description

Register 0x1C (PART_NUM):

The register PART_NUM can be used for the radio transceiver identification and includes the device part number.

Figure 6-16. Register PART_NUM.

Bit	7	6	5	4	
0x1C	PART_NUM				PART_NUM
Read/Write	R	R	R	R	
Reset value	0	0	0	0	

Bit	3	2	1	0	
0x1C	PART_NUM				PART_NUM
Read/Write	R	R	R	R	
Reset value	1	0	1	0	

- **Bit 7:0 - PART_NUM**

Table 6-5. PART_NUM.

Register Bits	Value	Description
PART_NUM	0x0A	AT86RF232 part number

Register 0x1D (VERSION_NUM):

The register VERSION_NUM can be used for the radio transceiver identification and includes the device version number.

Figure 6-17. Register VERSION_NUM.

Bit	7	6	5	4	
0x1D	VERSION_NUM				VERSION_NUM
Read/Write	R	R	R	R	
Reset value	0	0	0	0	

Bit	3	2	1	0	
0x1D	VERSION_NUM				VERSION_NUM
Read/Write	R	R	R	R	
Reset value	0	0	1	0	

- **Bit 7:0 - VERSION_NUM**

Table 6-6. VERSION_NUM.

Register Bits	Value	Description
VERSION_NUM	0x02	Revision A

Register 0x1E (MAN_ID_0):

Part one of the JEDEC manufacturer ID.

Figure 6-18. Register MAN_ID_0.

Bit	7	6	5	4	
0x1E	MAN_ID_0				MAN_ID_0
Read/Write	R	R	R	R	
Reset value	0	0	0	1	
Bit	3	2	1	0	
0x1E	MAN_ID_0				MAN_ID_0
Read/Write	R	R	R	R	
Reset value	1	1	1	1	

- **Bit 7:0 - MAN_ID_0**

Table 6-7. MAN_ID_0.

Register Bits	Value	Description
MAN_ID_0	0x1F	Atmel JEDEC manufacturer ID, bits[7:0] of the 32-bit JEDEC manufacturer ID are stored in register bits MAN_ID_0. Bits [15:8] are stored in register 0x1F (MAN_ID_1). The higher 16 bits of the ID are not stored in registers.

Register 0x1F (MAN_ID_1):

Part two of the JEDEC manufacturer ID.

Figure 6-19. Register MAN_ID_1.

Bit	7	6	5	4	
0x1F	MAN_ID_1				MAN_ID_1
Read/Write	R	R	R	R	
Reset value	0	0	0	0	
Bit	3	2	1	0	
0x1F	MAN_ID_1				MAN_ID_1
Read/Write	R	R	R	R	
Reset value	0	0	0	0	

- **Bit 7:0 - MAN_ID_1**

Table 6-8. MAN_ID_1.

Register Bits	Value	Description
MAN_ID_1	0x00	Atmel JEDEC manufacturer ID, bits[15:8] of the 32-bit JEDEC manufacturer ID are stored in register bits MAN_ID_1. Bits [7:0] are stored in register 0x1E (MAN_ID_0). The higher 16 bits of the ID are not stored in registers.

6.5 Sleep/Wake-up and Transmit Signal (SLP_TR)

Pin 11 (SLP_TR) is a multi-functional pin. Its function relates to the current state of the Atmel AT86RF232 and is summarized in Table 6-9. The radio transceiver states are explained in detail in Chapter 7.

Table 6-9. SLP_TR Multi-functional Pin.

Transceiver Status	Function	Transition	Description
PLL_ON	TX start	L ⇨ H	Starts frame transmission
TX_ARET_ON	TX start	L ⇨ H	Starts TX_ARET transaction
TRX_OFF	Sleep	L ⇨ H	Takes the radio transceiver into SLEEP state, CLKM disabled
SLEEP	Wakeup	H ⇨ L	Takes the radio transceiver back into TRX_OFF state, level sensitive

In states PLL_ON and TX_ARET_ON, pin 11 (SLP_TR) is used as trigger input to initiate a TX transaction. Here SLP_TR is sensitive on rising edge only.

After initiating a state change by a rising edge at pin 11 (SLP_TR) in radio transceiver state TRX_OFF, the radio transceiver remains in the new state as long as the pin is logical high and returns to the preceding state with the falling edge.

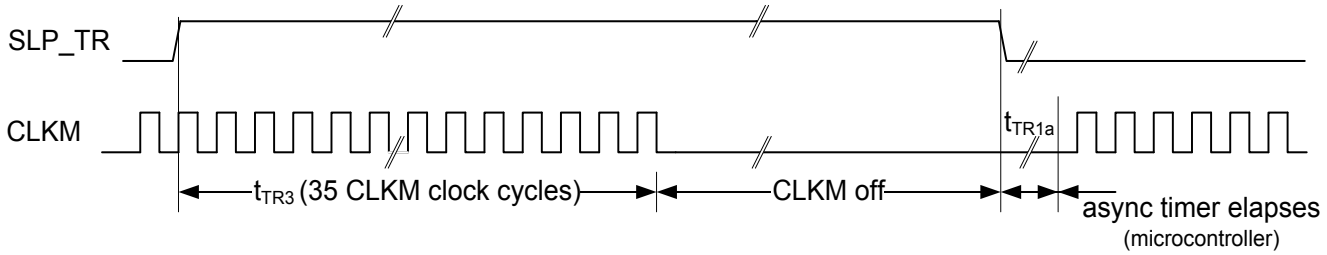
SLEEP state

The SLEEP state is used when radio transceiver functionality is not required, and thus the AT86RF232 can be powered down to reduce the overall power consumption.

A power-down scenario is shown in Figure 6-20. When the radio transceiver is in TRX_OFF state the microcontroller forces the AT86RF232 to SLEEP by setting SLP_TR = H. If pin 17 (CLKM) provides a clock to the microcontroller this clock is switched off after 35 CLKM cycles. The AT86RF232 awakes when the microcontroller releases pin 11 (SLP_TR).

The CLKM clock frequency setting for 62.5kHz are not intended to directly clock the microcontroller. When using these clock rates, CLKM is turned off immediately when entering SLEEP state.

Figure 6-20. Sleep and Wake-up Initiated by Asynchronous Microcontroller Timer.



Note: 1. Timing figures t_{TR3} and t_{TR1a} refer to Table 7-1.

6.6 Interrupt Logic

6.6.1 Overview

The Atmel AT86RF232 differentiates between nine interrupt events (eight physical interrupt registers, one shared by two functions). Each interrupt is enabled by setting the corresponding bit in the interrupt mask register 0x0E (IRQ_MASK). Internally, each pending interrupt is stored in a separate bit of the interrupt status register. All interrupt events are OR-combined to a single external interrupt signal (IRQ pin). If an interrupt is issued, pin 24 (IRQ) = H, the microcontroller shall read the interrupt status register 0x0F (IRQ_STATUS) to determine the source of the interrupt. A read access to this register clears the interrupt status register and thus the IRQ pin, too.

Interrupts are not cleared automatically when the event that caused them vanishes. Exceptions are IRQ_0 (PLL_LOCK) and IRQ_1 (PLL_UNLOCK) because the occurrence of one clears the other.

The supported interrupts for the Basic Operating Mode are summarized in Table 6-10.

Table 6-10. Interrupt Description in Basic Operating Mode.

IRQ Name	Description	Section
IRQ_7 (BAT_LOW)	Indicates a supply voltage below the programmed threshold.	9.5.4
IRQ_6 (TRX_UR)	Indicates a Frame Buffer access violation.	9.3.3
IRQ_5 (AMI)	Indicates an address match.	7.2.3.4
IRQ_4 (CCA_ED_DONE)	Multi-functional interrupt: 1. AWAKE_END: • Indicates finished transition to TRX_OFF state from P_ON, SLEEP, or RESET state. 2. CCA_ED_DONE: • Indicates the end of a CCA or ED measurement.	 7.1.2.3 8.4.4 8.5.4
IRQ_3 (TRX_END)	RX: Indicates the completion of a frame reception. TX: Indicates the completion of a frame transmission.	7.1.3 7.1.3
IRQ_2 (RX_START)	Indicates the start of a PSDU reception. Register bits TRX_STATUS changes to BUSY_RX, the PHR is valid to be read from Frame Buffer.	7.1.3
IRQ_1 (PLL_UNLOCK)	Indicates PLL unlock. If the radio transceiver is in BUSY_TX / BUSY_TX_ARET state, the PA is turned off immediately.	9.7.5
IRQ_0 (PLL_LOCK)	Indicates PLL lock.	9.7.5

Note: 1. The IRQ_4 (AWAKE_END) interrupt can usually not be seen when the transceiver enters TRX_OFF state after P_ON, or RESET, because register 0x0E (IRQ_MASK) is reset to mask all interrupts. It is recommended to enable IRQ_4 (AWAKE_END) to be notified once the TRX_OFF state is entered.

The interrupt handling in Extended Operating Mode is described in Section 7.2.5.