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Atmel®

AT86RF233

Low Power, 2.4GHz Transceiver for ZigBee, RF4CE, IEEE 802.15.4, 6LoWPAN, and ISM Applications

PRELIMINARY DATASHEET

Features

- High Performance RF-CMOS 2.4GHz radio transceiver targeted for IEEE[®] 802.15.4, ZigBee[®], RF4CE, 6LoWPAN, and ISM applications
- Industry leading link budget:
  - Receiver sensitivity -101dBm
  - Programmable TX output power from -17dBm up to +4dBm
- Ultra-low current consumption:
  - DEEP_SLEEP = 0.02µA
  - TRX_OFF = 300µA
  - RX_ON = 11.8mA (LISTEN)
    - Smart Receiving Techniques enable further current reduction in LISTEN mode between 10 to 50% from 11.8mA
    - Desensitation will enable further reduction up to 1mA
  - BUSY_TX = 13.8mA (at max. transmit power)
- Ultra-low supply voltage (1.8V to 3.6V) with internal regulator
- Support for coin cell operation
- Optimized for low BoM Cost and ease of production:
  - Few external components necessary (crystal, capacitors and antenna)
- Easy to use interface:
  - Registers, frame buffer, and AES accessible through fast SPI
  - Only two microcontroller GPIO lines necessary
  - One interrupt pin from radio transceiver
  - Clock output with prescaler from radio transceiver
- Radio transceiver features:
  - 128-byte FIFO (SRAM) for data buffering
  - Fully integrated, fast settling PLL to support Frequency Hopping
  - Supports 500kHz channel spacing
  - Battery monitor and Fast Wake-Up Time < 0.4msec
- Special IEEE 802.15.4™ 2011 hardware support:
  - FCS computation and Clear Channel Assessment
  - RSSI measurement, Energy Detection and Link Quality Indication
- MAC hardware accelerator:
  - Automated acknowledgement, CSMA-CA and retransmission
  - Automatic address filtering
  - Automated FCS check
- Extended feature set hardware support:
  - AES 128-bit hardware accelerator
  - Antenna Diversity and RX/TX indication
  - Supported PSDU data rates: 250kb/s, 500kb/s, 1000kb/s and 2000kb/s
  - True Random Number Generation for security application
  - Reduced Power Consumption modes
  - Time and phase measurement support
- Industrial and extended temperature range:
  - -40°C to +85°C and -40°C to +125°C
- I/O and packages:
  - 32-pin Low-Profile QFN Package 5 x 5 x 0.9mm³
  - RoHS/Fully Green
- Compliant to EN 300 328/440, FCC-CFR-47 Part 15, ARIB STD-66, RSS-210
- Compliant to IEEE 802.15.4 2003/2006/2011

Table of Contents

1 Pin-out Diagram

Figure 1-1. Atmel AT86RF233 Pin-out Diagram.

Note: 1. The exposed paddle is electrically connected to the die inside the package. It shall be soldered to the board to ensure electrical and thermal contact and good mechanical stability.

1.1 Pin Descriptions

Table 1-1. Atmel AT86RF233 Pin Description.

Pins	Name	Type	Description
1	DIG3	Digital output (Ground)	1. RX/TX Indicator, see Section 11.5 2. If disabled, pull-down enabled (AVSS)
2	DIG4	Digital output (Ground)	1. RX/TX Indicator (DIG3 inverted), see Section 11.5 2. If disabled, pull-down enabled (AVSS)
3	AVSS	Ground	Ground for RF signals
4	RFP	RF I/O	Differential RF signal
5	RFN	RF I/O	Differential RF signal
6	AVSS	Ground	Ground for RF signals
7	DVSS	Ground	Digital ground
8	/RST	Digital input	Chip reset; active low
9	DIG1	Digital output (Ground)	1. Antenna Diversity RF switch control, see Section 11.4 2. If disabled, pull-down enabled (DVSS)
10	DIG2	Digital output (Ground)	1. Antenna Diversity RF switch control (DIG1 inverted), see Section 11.4 2. RX Frame Time Stamping, see Section 11.6 3. TX Frame Time Stamping, see Section 11.6 4. If functions disabled, pull-down enabled (DVSS)
11	SLP_TR	Digital input	Controls sleep, deep sleep, transmit start, receive states; active high, see Section 6.6
12	DVSS	Ground	Digital ground
13, 14	DVDD	Supply	Regulated 1.8V voltage regulator output or regulated voltage input; digital domain, see Section 9.4
15	DEVDD	Supply	External supply voltage; digital domain
16	DVSS	Ground	Digital ground
17	CLKM	Digital output	Master clock signal output; low if disabled, see Section 9.6
18	DVSS	Ground	Digital ground
19	SCLK	Digital input	SPI clock
20	MISO	Digital output	SPI data output (master input slave output)
21	DVSS	Ground	Digital ground
22	MOSI	Digital input	SPI data input (master output slave input)
23	/SEL	Digital input	SPI select, active low
24	IRQ	Digital output	1. Interrupt request signal; active high or active low; configurable, see Section 6.7 2. Frame Buffer Empty Indicator; active high, see Section 11.7
25	XTAL2	Analog input	Crystal pin, see Section 9.6
26	XTAL1	Analog input	Crystal pin or external clock supply, see Section 9.6
27	AVSS	Ground	Analog ground
28	EVDD	Supply	External supply voltage, analog domain
29	AVDD	Supply	Regulated 1.8V voltage regulator; analog domain, see Section 9.4
30, 31, 32	AVSS	Ground	Analog ground
Paddle	AVSS	Ground	Analog ground; Exposed paddle of QFN package

1.2 Analog and RF Pins

1.2.1 Supply and Ground Pins

EVDD, DEVDD

EVDD and DEVDD are analog and digital supply voltage pins of the Atmel® AT86RF233 radio transceiver.

AVDD, DVDD

AVDD and DVDD are outputs of the internal voltage regulators and require bypass capacitors for stable operation. The voltage regulators are controlled independently by the radio transceivers state machine and are activated depending on the current radio transceiver state. The voltage regulators can be configured for external supply; for details, refer to Section 9.4.

AVSS, DVSS

AVSS and DVSS are analog and digital ground pins respectively. The analog and digital power domains should be separated on the PCB.

1.2.2 RF Pins
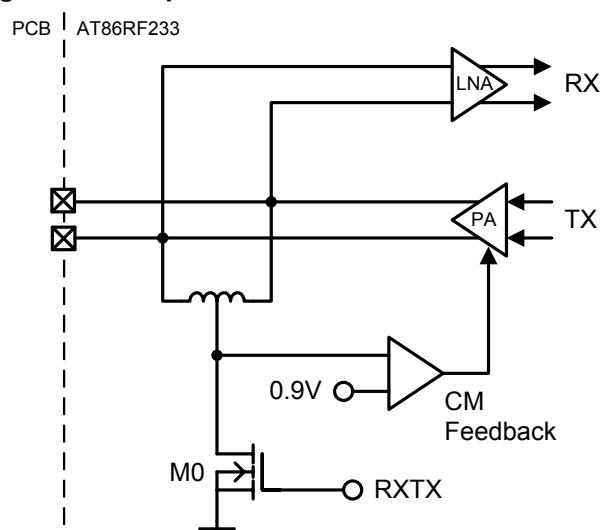
RFN, RFP

A differential RF port (RFP/RFN) provides common-mode rejection to suppress the switching noise of the internal digital signal processing blocks. At board-level, the differential RF layout ensures high receiver sensitivity by reducing spurious emissions originated from other digital ICs such as a microcontroller.

The RF port is designed for a 100Ω differential load. A DC path between the RF pins is allowed; a DC path to ground or supply voltage is not allowed.

A simplified schematic of the RF front end is shown in Figure 1-2.

Figure 1-2. Simplified RF Front-end Schematic.

The RF port DC values depend on the operating state; refer to Chapter 7. In TRX_OFF state, when the analog front-end is disabled (see Section 7.1.2.5), the RF pins are pulled to ground, preventing a floating voltage larger than 1.8V which is not allowed for the internal circuitry.

In transmit mode, a control loop provides a common-mode voltage of 0.9V. Transistor M0 is off, allowing the PA to set the common-mode voltage. The common-mode capacitance at each pin to ground shall be < 30pF to ensure the stability of this common-mode feedback loop.

In receive mode, the RF port provides a low-impedance path to ground when transistor M0, (see Figure 1-2) pulls the inductor center tap to ground. A DC voltage drop of 20mV across the on-chip inductor can be measured at the RF pins.

1.2.3 Crystal Oscillator Pins

XTAL1, XTAL2

The pin 26 (XTAL1) of Atmel AT86RF233 is the input of the reference oscillator amplifier (XOSC), the pin 25 (XTAL2) is the output. A detailed description of the crystal oscillator setup and the related XTAL1/XTAL2 pin configuration can be found in Section 9.6.

When using an external clock reference signal, XTAL1 shall be used as input pin. For further details, refer to Section 9.6.3.

1.2.4 Analog Pin Summary

Table 1-2. Analog Pin Behavior – DC values.

Pin	Values and Conditions	Comments
RFP/RFN	V_{DC} = 0.9V (BUSY_TX) V_{DC} = 20mV (receive states) V_{DC} = 0mV (otherwise)	DC level at pins RFP/RFN for various transceiver states. AC coupling is required if a circuitry with a DC path to ground or supply is used. Serial capacitance and capacitance of each pin to ground must be < 30pF.
XTAL1/XTAL2	V_{DC} = 0.9V at both pins C_{PAR} = 3pF	DC level at pins XTAL1/XTAL2 for various transceiver states. Parasitic capacitance (C_{PAR}) of the pins must be considered as additional load capacitance to the crystal.
DVDD	V_{DC} = 1.8V (all states, except SLEEP and DEEP_SLEEP) V_{DC} = 0mV (otherwise)	DC level at pin DVDD for various transceiver states. Supply pins (voltage regulator output) for the digital 1.8V voltage domain. The outputs shall be bypassed by 100nF.
AVDD	V_{DC} = 1.8V (all states, except P_ON, SLEEP, DEEP_SLEEP, RESET, and TRX_OFF) V_{DC} = 0mV (otherwise)	DC level at pin AVDD for various transceiver states. Supply pin (voltage regulator output) for the analog 1.8V voltage domain. The outputs shall be bypassed by 100nF.

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1.3 Digital Pins

The Atmel AT86RF233 provides a digital microcontroller interface. The interface comprises a slave SPI (/SEL, SCLK, MOSI, and MISO) and additional control signals (CLKM, IRQ, SLP_TR, /RST, and DIG2). The microcontroller interface is described in detail in Chapter 6.

Additional digital output signals DIG1, …, DIG4 are provided to control external blocks, that is for Antenna Diversity RF switch control or as an RX/TX Indicator, see Section 11.4 and Section 11.5 respectively.

1.3.1 Driver Strength Settings

The driver strength of all digital output pins (MISO, IRQ, DIG1, …, DIG4) and CLKM pin are fixed. The capacitive load should be as small as possible as, not larger than 50pF.

1.3.2 Pull-up and Pull-down Configuration

Pulling transistors are internally connected to all digital input pins in radio transceiver states P_ON (including reset during P_ON) and DEEP_SLEEP, refer to Section 7.1.2.1 and Section 7.1.2.4.

Table 1-3 summarizes the pull-up and pull-down configuration.

Table 1-3. Pull-Up / Pull-Down Configuration of Digital Input Pins.

Pin	H $\triangleq$ pull-up, L $\triangleq$ pull-down
/RST	H
/SEL	H
SCLK	L
MOSI	L
SLP_TR[1]	L

Note: 1.   Except SLP_TR pin for DEEP_SLEEP state.

In all other radio transceiver states, including RESET, no pull-up or pull-down transistors are connected to any of the digital input pins mentioned in Table 1-3.

Note: 2.   In all other states, external circuitry should guaranty defined levels at all input pins. Floating input pins may cause unexpected functionality and increased power consumption, for example in SLEEP state.

If the additional digital output signals DIG1, …, DIG4 are not activated, these pins are pulled-down to digital ground (DIG1/DIG2) or analog ground (DIG3/DIG4).

2 Disclaimer

Typical values contained in this datasheet are based on simulations and testing. Minimum and maximum values are available when the radio transceiver has been fully characterized.

3 Overview

The Atmel AT86RF233 is a feature rich, extremely low-power 2.4GHz radio transceiver designed for industrial and consumer ZigBee/IEEE 802.15.4, RF4CE, 6LoWPAN, and high data rate 2.4GHz ISM band applications.

The AT86RF233 is a true SPI-to-antenna solution. All RF-critical components except the antenna, crystal, and de-coupling capacitors are integrated on-chip. MAC and AES hardware accelerators improve overall system power efficiency and timing. Therefore, the AT86RF233 is particularly suitable for applications like:

- 2.4GHz IEEE 802.15.4 and ZigBee systems
- RF4CE systems
- Energy Harvesting systems
- 6LoWPAN systems
- Wireless sensor networks
- Industrial Control
- Residential and commercial automation
- Health care
- Consumer electronics
- PC peripherals
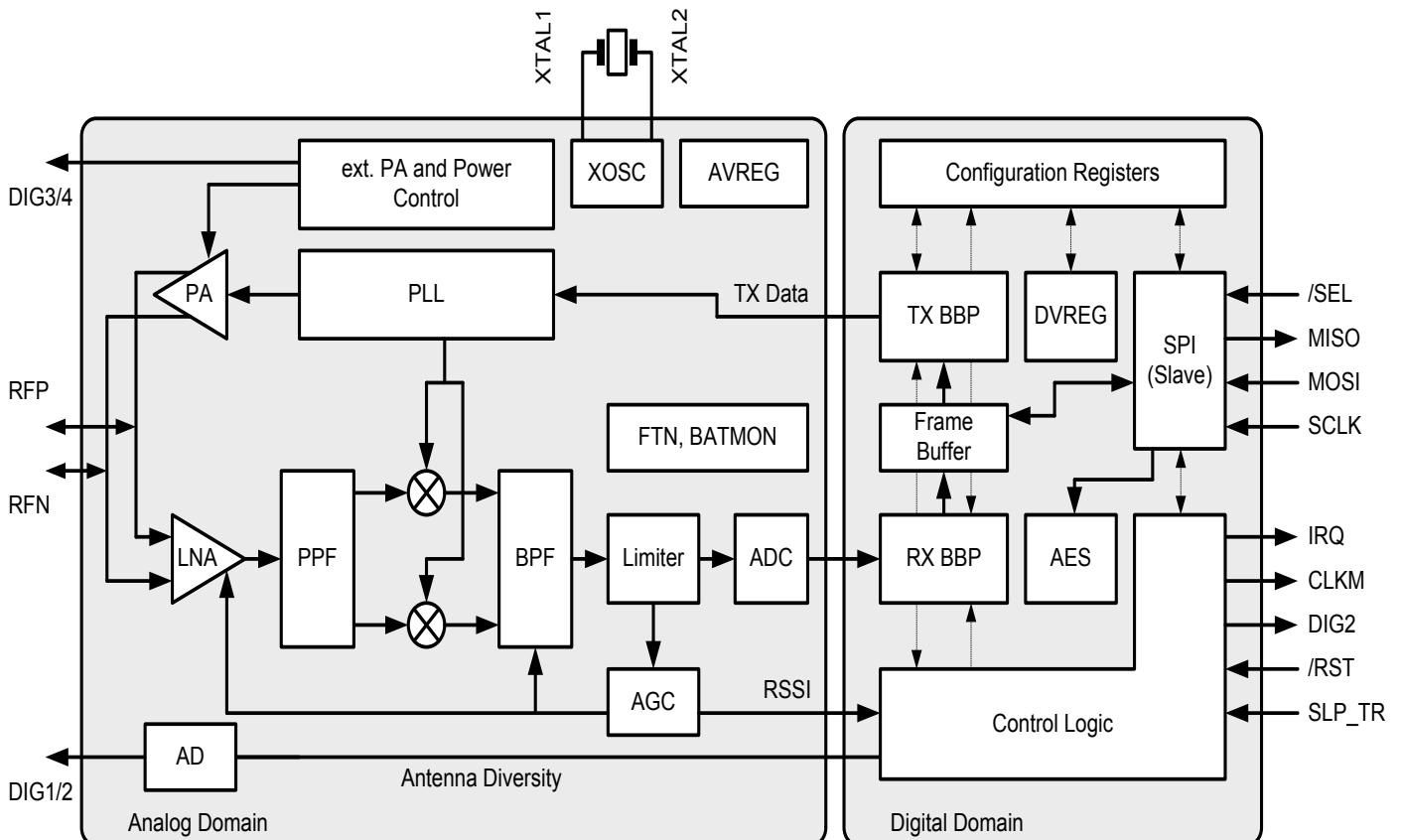
The AT86RF233 can be operated by using an external microcontroller like Atmel AVR® microcontrollers. A comprehensive software programming description can be found in reference [7].

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4 General Circuit Description

The Atmel AT86RF233 single-chip radio transceiver provides a complete radio transceiver interface between an antenna and a microcontroller. It comprises the analog radio, digital modulation and demodulation including time and frequency synchronization, as well as data buffering. A single 128-byte TRX buffer stores receive or transmit data. Communication between transmitter and receiver is based on direct sequence spread spectrum with different modulation schemes and spreading codes.

The AT86RF233 block diagram is shown in Figure 4-1.

Figure 4-1. AT86RF233 Block Diagram.

The number of external components is minimized such that only the antenna, the crystal and decoupling capacitors are required. The bidirectional differential antenna pins (RFP, RFN) are used for transmission and reception, thus no external antenna switch is needed. Control of an external power amplifier is supported by two digital control signals (differential operation).

The received RF signal at pin 5 (RFN) and pin 6 (RFP) is differentially fed through the low-noise amplifier (LNA) to the RF filter (PPF) to generate a complex signal, driving the integrated channel filter (BPF). The limiting amplifier provides sufficient gain to drive the succeeding analog-to-digital converter (ADC) and generates a digital RSSI signal. The ADC output signal is sampled by the digital base band receiver (RX BBP).

The transmit modulation scheme is offset-QPSK (O-QPSK) with half-sine pulse shaping and 32-length block coding (spreading) according to [1], [2] and [3]. The modulation signal is generated in the digital transmitter (TX BBP) and applied to the fractional-N frequency synthesis (PLL), to ensure the coherent phase modulation required for

demodulation of O-QPSK signals. The frequency-modulated signal is fed to the power amplifier (PA).

Two on-chip low-dropout voltage regulators (A|DVREG) provide regulated analog and digital 1.8V supply outputs.

An internal 128-byte RAM for RX and TX (Frame Buffer) buffers the data to be transmitted or the received data.

The configuration of the Atmel AT86RF233, reading and writing of Frame Buffer is controlled by the SPI interface and additional control lines.

The AT86RF233 further contains comprehensive hardware-MAC support (Extended Operating Mode) and a security engine (AES) to improve the overall system power efficiency and timing. The stand-alone 128-bit AES engine can be accessed in parallel to all PHY operational transactions and states using the SPI interface, except during SLEEP and DEEP_SLEEP states.

For applications not necessarily targeting IEEE 802.15.4 compliant networks, the radio transceiver also supports alternative data rates up to 2000kb/s.

For long-range applications or to improve the reliability of a RF connection the RF performance can further be improved by using an external RF front-end or Antenna Diversity. Both operation modes are supported by the AT86RF233 with dedicated control pins DIG1, …, DIG4 without the interaction of the microcontroller.
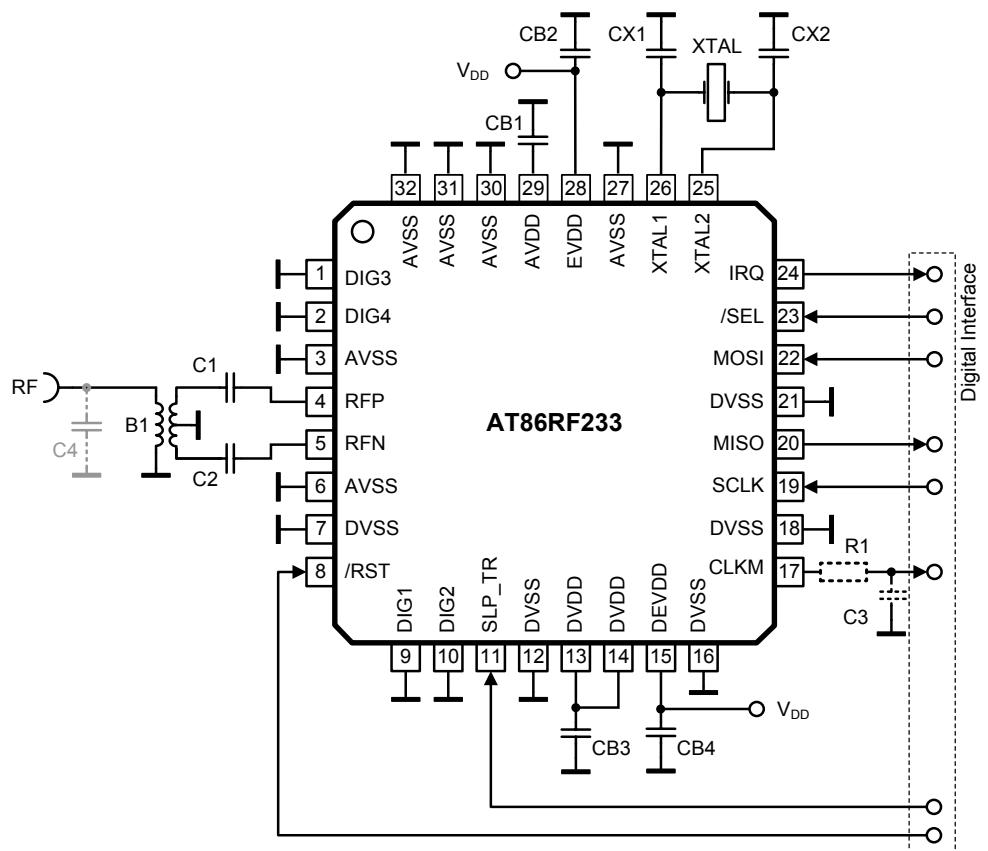
Additional features of the Extended Feature Set, see Chapter 11, are provided to simplify the interaction between radio transceiver and microcontroller.

5 Application Schematic

5.1 Basic Application Schematic

A basic application schematic of the Atmel AT86RF233 with a single-ended RF connector is shown in Figure 5-1. The 50Ω single-ended RF input is transformed to the 100Ω differential RF port impedance using balun B1. The capacitors C1 and C2 provide AC coupling of the RF input to the RF port, optional capacitor C4 improves matching if required.

Figure 5-1. Basic Application Schematic.

The power supply decoupling capacitors (CB2, CB4) are connected to the external analog supply pin 28 (EVDD) and external digital supply pin 15 (DEVDD). Capacitors CB1 and CB3 are bypass capacitors for the integrated analog and digital voltage regulators to ensure stable operation. All bypass capacitors should be placed as close as possible to the pins and should have a low-resistance and low-inductance connection to ground to achieve the best performance.

The crystal (XTAL), the two load capacitors (CX1, CX2), and the internal circuitry connected to pins XTAL1 and XTAL2 form the crystal oscillator. To achieve the best accuracy and stability of the reference frequency, large parasitic capacitances should be avoided. Crystal lines should be routed as short as possible and not in proximity of digital I/O signals. This is especially required for the High Data Rate Modes; refer to Section 11.3.

Crosstalk from digital signals on the crystal pins or the RF pins can degrade the system performance. Therefore, a low-pass filter (C3, R1) is placed close to the Atmel AT86RF233 CLKM output pin to reduce the emission of CLKM signal harmonics.

This is not needed if pin 17 (CLKM) is not used as a microcontroller clock source. In this case, pin 17 (CLKM) output should be disabled during device initialization.

The ground plane of the application board should be separated into four independent fragments: the analog, the digital, the antenna, and the XTAL ground plane. The exposed paddle shall act as the reference point of the individual grounds.

Note: 1. The pins DIG1, DIG2, DIG3, and DIG4 are connected to ground in the Basic Application Schematic; refer to Figure 5-1. Special programming of these pins requires a different schematic; refer to Section 5.2.

Table 5-1. Exemplary Bill of Materials (BoM) for Basic Application Schematic.

Symbol	Description	Value	Manufacturer	Part Number	Comment
B1	SMD balun	2.45GHz	Wuerth	748421245	2.45GHz Balun
B1 (alternatively)	SMD balun / filter	2.45GHz	Johanson Technology	2450BM15A0015	2.45GHz Balun / Filter
CB1 CB3	LDO VREG bypass capacitor	100nF	Generic		X7R 10% 16V (0402)
CB2 CB4	Power supply decoupling	1µF	AVX Murata	0603YD105KAT2A GRM188R61C105KA12D	X5R 10% 16V (0603)
CX1, CX2	Crystal load capacitor	12pF	AVX Murata	06035A120JA GRM1555C1H120JA01D	COG 5% 50V (0402)
C1, C2	RF coupling capacitor	22pF	Murata Epcos AVX	GRM1555C1H220JA01J B37920 06035A220JAT2A	C0G 5% 50V (0402 or 0603)
C3	CLKM low-pass filter capacitor	2.2pF	AVX Murata	06035A229DA GRP1886C1H2R0DA01	COG ±0.5pF 50V (0603) Designed for f_{CLKM} = 1MHz
C4 (optional)	RF matching				Value depends on final PCB implementation
R1	CLKM low-pass filter resistor	680Ω			Designed for f_{CLKM} = 1MHz
XTAL	Crystal	CX-4025 16MHz SX-4025 16MHz	ACAL Taitjen Siward	XWBBPL-F-1 A207-011	
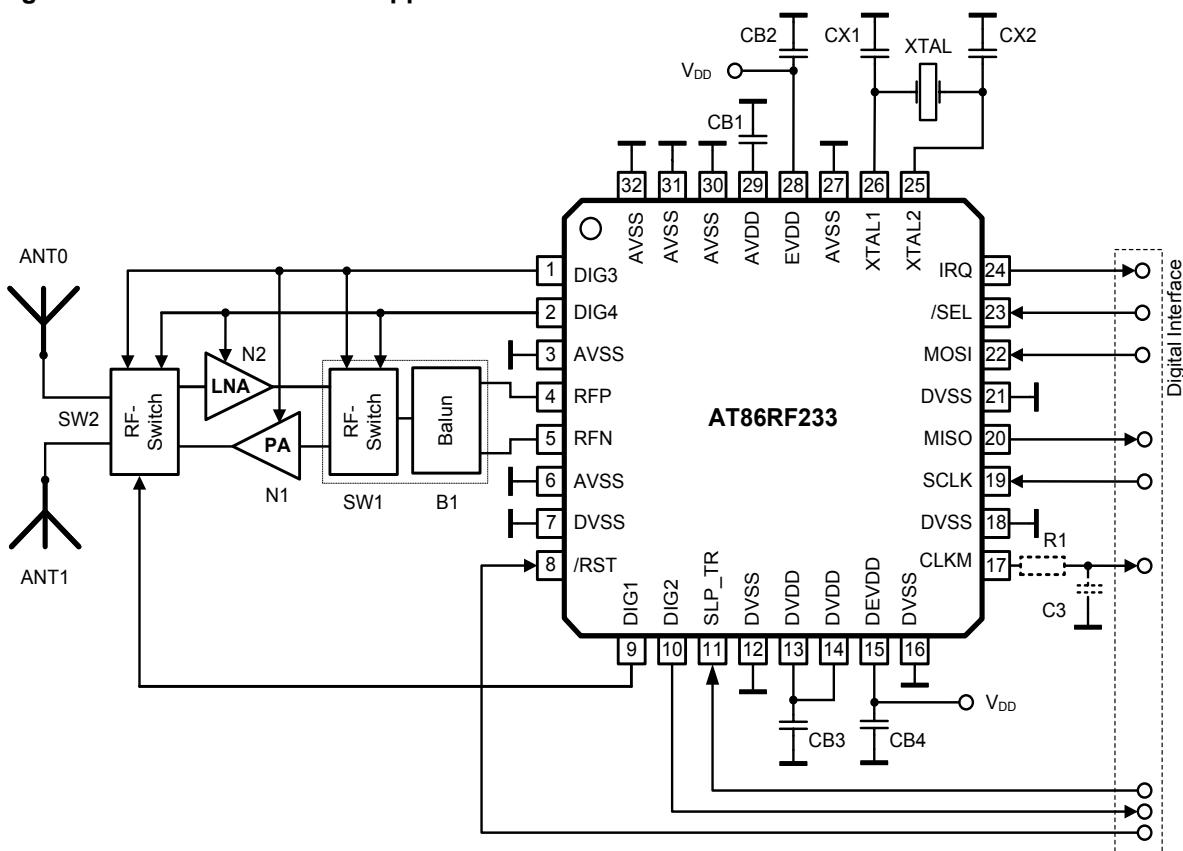
5.2 Extended Feature Set Application Schematic

The Atmel AT86RF233 supports additional features like:

- Security Module (AES)   Section 11.1
- Random Number Generator   Section 11.2
- High Data Rate Modes   Section 11.3
- Antenna Diversity   uses pins DIG1(/2)   Section 11.4
- RX/TX Indicator   uses pins DIG3/4   Section 11.5
- RX and TX Frame Time Stamping (TX_ARET)
                                     uses pin DIG2   Section 11.6
- Frame Buffer Empty Indicator   uses pin IRQ   Section 11.7
- Dynamic Frame Buffer Protection   Section 11.8
- Alternate Start-Of-Frame Delimiter   Section 11.9
- Reduced Power Consumption Mode (RPC)   Section 11.10
- TOM Measurements   Section 11.11
- Phase Difference Measurement   Section 11.12

An extended feature set application schematic illustrating the use of the AT86RF233 Extended Feature Set, see Chapter 11, is shown in Figure 5-2. Although this example shows all additional hardware features combined, it is possible to use all features separately or in various combinations.

Figure 5-2. Extended Feature Application Schematic.

In this example, a balun (B1) transforms the differential RF signal at the Atmel AT86RF233 radio transceiver RF pins (RFP/RFN) to a single ended RF signal, similar to the Basic Application Schematic; refer to Figure 5-1. During receive mode the radio transceiver searches for the most reliable RF signal path using the Antenna Diversity algorithm. One antenna is selected (SW2) by the Antenna Diversity RF switch control pin 9 (DIG1), refer to Section 11.4.

The RX signal is amplified by an optional low-noise amplifier (N2) and fed to the radio transceiver using the RX/TX switch (SW1). During transmit mode the AT86RF233 TX signal is amplified using an external PA (N1) and fed to the antennas via an RF switch (SW2). These switches are controlled by the RX/TX Indicator, represented by the differential pin pair DIG3/DIG4, refer to Section 11.5.

RX and TX Frame Time stamping is implemented through pin 10 (DIG2), refer to Section 11.6.
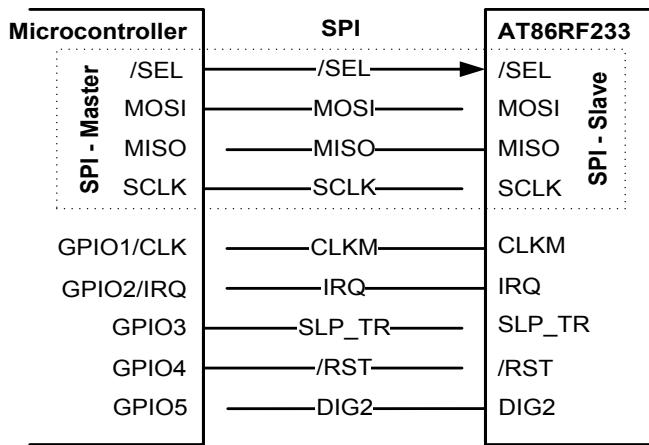
The Security Module (AES), Random Number Generator, High Data Rate Modes, Frame Buffer Empty Indicator, Dynamic Frame Buffer Protection, Alternate Start-Of-Frame Delimiter or Reduced Power Consumption Mode (RPC) do not require specific circuitry to operate, for details refer to Section 11.1, Section 11.2, Section 11.3, Section 11.7, Section 11.8, Section 11.9 and Section 11.10.

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6 Microcontroller Interface

6.1 Overview

This section describes the Atmel AT86RF233 to microcontroller interface. The interface comprises a slave SPI and additional control signals; see Figure 6-1. The SPI timing and protocol are described below.

Figure 6-1. Microcontroller to AT86RF233 Interface.

Microcontrollers with a master SPI such as Atmel AVR family interface directly to the AT86RF233. The SPI is used for register, Frame Buffer, SRAM and AES access. The additional control signals are connected to the GPIO/IRQ interface of the microcontroller. Table 6-1 introduces the radio transceiver I/O signals and their functionality.

Table 6-1. Signal Description of Microcontroller Interface.

Signal	Description
/SEL	SPI select signal, active low
MOSI	SPI data (master output slave input) signal
MISO	SPI data (master input slave output) signal
SCLK	SPI clock signal
CLKM	Optional, Clock output, refer to Section 9.6.4, usable as: - microcontroller clock source and/or MAC timer reference - high precision timing reference
IRQ	Interrupt request signal, further used as: - Frame Buffer Empty indicator, refer to Section 11.7
SLP_TR	Multi purpose control signal (functionality is state dependent, see Section 6.6): - Sleep/Wakeup enable/disable SLEEP state - Sleep/Wakeup enable/disable DEEP_SLEEP state - TX start BUSY_TX_(ARET) state
/RST	AT86RF233 reset signal, active low
DIG2	Optional, - IRQ_2 (RX_START) for RX Frame Time Stamping, see Section 11.6 - Signals frame transmit within TX_ARET mode for TX Time Stamping

6.2 SPI Timing Description

Pin 17 (CLKM) can be used as a microcontroller master clock source. If the microcontroller derives the SPI master clock (SCLK) directly from CLKM, the SPI operates in synchronous mode, otherwise in asynchronous mode.

In asynchronous mode, the maximum SCLK frequency f_{async} is limited to 7.5MHz. The signal at pin 17 (CLKM) is not required to derive SCLK and may be disabled to reduced power consumption and spurious emissions.

Figure 6-2 and Figure 6-3 illustrate the SPI timing and introduces its parameters. The corresponding timing parameter definitions $t_1 - t_9$ are defined in Section 12.4.

Figure 6-2. SPI Timing, Global Map and Definition of Timing Parameters t_5, t_6, t_8, t_9.
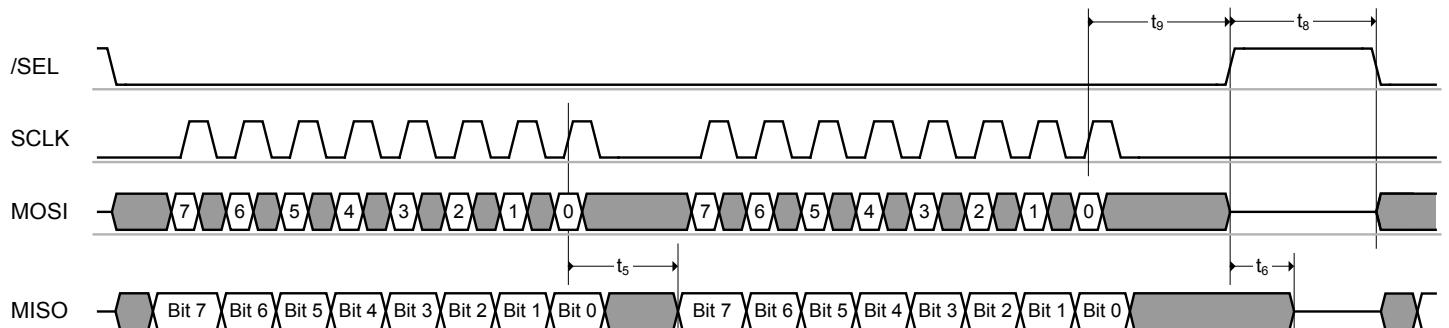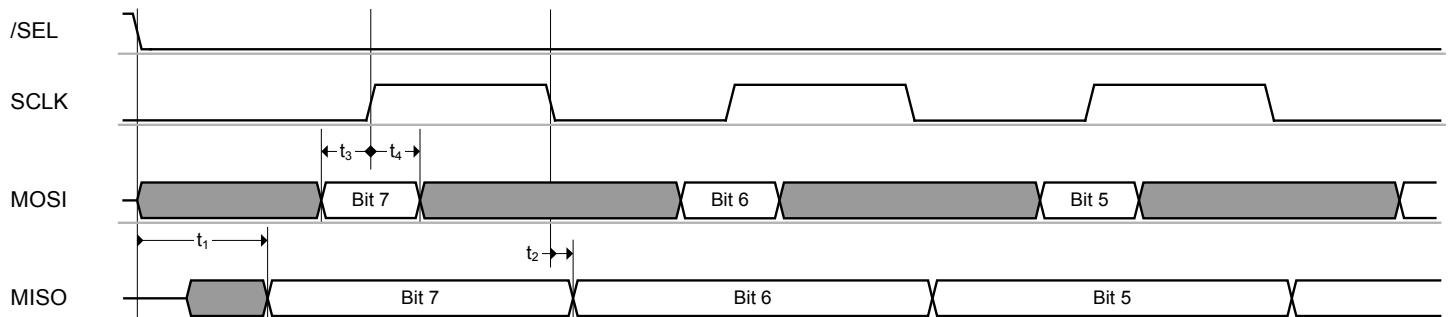
Figure 6-3. SPI Timing, Detailed Drawing of Timing Parameters t_1 to t_4.

The SPI is based on a byte-oriented protocol and is always a bidirectional communication between the master and slave. The SPI master starts the transfer by asserting /SEL = L. Then the master generates eight SPI clock cycles to transfer one byte to the radio transceiver (via MOSI). At the same time, the slave transmits one byte to the master (via MISO). When the master wants to receive one byte of data from the slave, it must also transmit one byte to the slave. All bytes are transferred with the MSB first. An SPI transaction is finished by releasing /SEL = H.

An SPI register access consists of two bytes, a Frame Buffer or SRAM access of at least two or more bytes as described in Section 6.3.

/SEL = L enables the MISO output driver of the Atmel AT86RF233. The MSB of MISO is valid after t_1 (see Section 12.4) and is updated on each SCLK falling edge. If the driver is disabled, there is no internal pull-up transistor connected to it. Driving the appropriate signal level must be ensured by the master device or an external pull-up resistor.

Note: 1.   When both /SEL and /RST are active, the MISO output driver is also enabled.

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Referring to Figure 6-2 and Figure 6-3, Atmel AT86RF233 MOSI is sampled at the rising edge of the SCLK signal and the output is set at the falling edge of SCLK. The signal must be stable before and after the rising edge of SCLK as specified by t_3 and t_4, refer to Section 12.4 parameters.

This SPI operational mode is commonly known as "*SPI mode 0*".

6.3 SPI Protocol

Each SPI sequence starts with transferring a command byte from the SPI master via MOSI (see Table 6-2) with the MSB first. This command byte defines the SPI access mode and additional mode-dependent information.

Table 6-2. SPI Command Byte Definition.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access Mode	Access Type
1	0	Register address [5:0]						Register access	Read access
1	1	Register address [5:0]							Write access
0	0	1	Reserved					Frame Buffer access	Read access
0	1	1	Reserved						Write access
0	0	0	Reserved					SRAM access	Read access
0	1	0	Reserved						Write access

Each SPI transfer returns bytes back to the SPI master on MISO output pin. The content of the first byte (see value "*PHY_STATUS*" in Figure 6-4 to Figure 6-14) is set to zero after reset. To transfer status information of the radio transceiver to the microcontroller, the content of the first byte can be configured with register bits SPI_CMD_MODE (register 0x04, TRX_CTRL_1). For details, refer to Section 6.4.1.

Note: 1.   Return values on MISO stated as XX shall be ignored by the microcontroller.

The different access modes are described within the following sections.
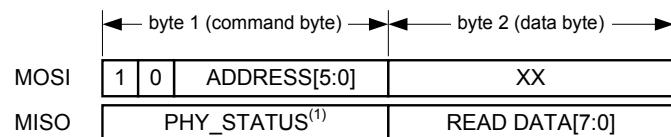
6.3.1 Register Access Mode

Register Access Mode is used to read and write AT86RF233 regsisters (register address from 0x00 up to 0x3F).

A register access mode is a two-byte read/write operation initiated by /SEL = L. The first transferred byte on MOSI is the command byte including an identifier bit (bit[7] = 1), a read/write select bit (bit[6]), and a 6-bit register address.

On read access, the content of the selected register address is returned in the second byte on MISO (see Figure 6-4).
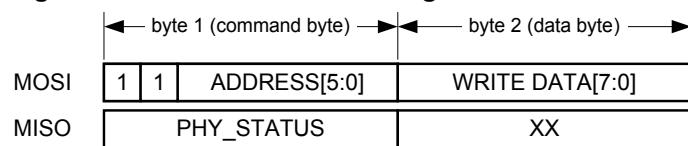
Figure 6-4. Packet Structure - Register Read Access.

Note: 1.   Each SPI access can be configured to return radio controller status information (PHY_STATUS) on MISO, for details refer to Section 6.4.

On write access, the second byte transferred on MOSI contains the write data to the selected address (see Figure 6-5).
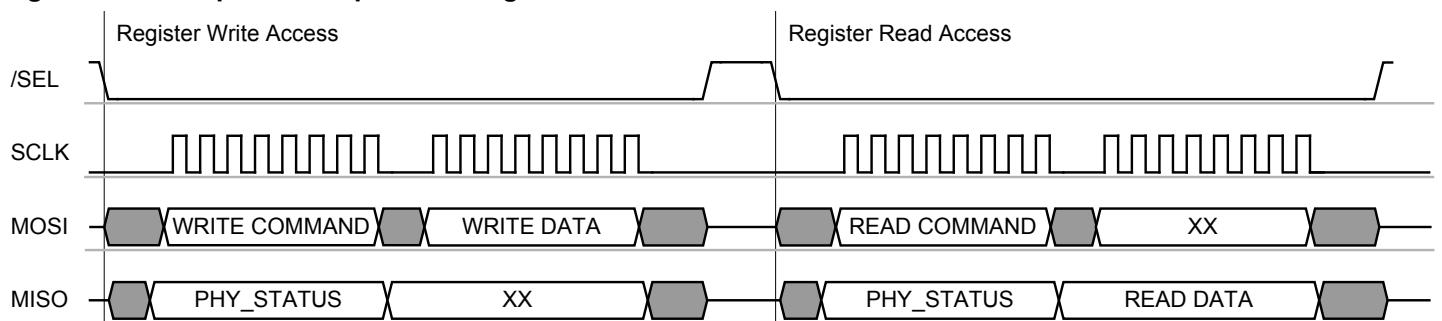
Figure 6-5. Packet Structure - Register Write Access.

	byte 1 (command byte)	byte 2 (data byte)
MOSI	1 1 ADDRESS[5:0]	WRITE DATA[7:0]
MISO	PHY_STATUS	XX

Each register access must be terminated by setting /SEL = H.

Figure 6-6 illustrates a typical SPI sequence for a register access sequence for write and read respectively.

Figure 6-6. Example SPI Sequence – Register Access Mode.

6.3.2 Frame Buffer Access Mode

Frame Buffer Access Mode is used to read and write Atmel AT86RF233 frame buffer. The frame buffer address is always reset to zero and incremented to access PSDU, LQI, ED and RX_STATUS data.
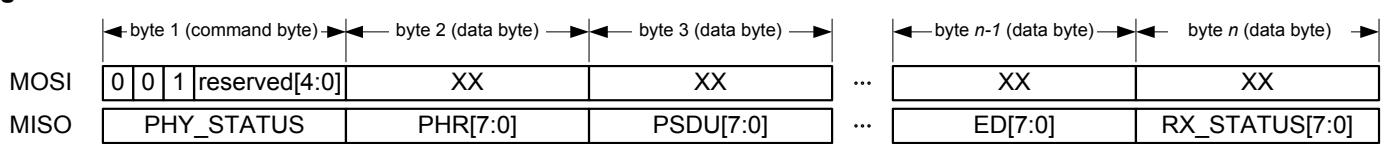
The Frame Buffer can hold up to 128-byte of one PHY service data unit (PSDU) IEEE 802.15.4 data frame. A detailed description of the Frame Buffer can be found in Section 9.3. An introduction to the IEEE 802.15.4 frame format can be found in Section 8.1.

Each access starts with /SEL = L followed by a command byte on MOSI. Each frame read or write access command byte is followed by the PHR data byte, indicating the frame length, followed by the PSDU data, see Figure 6-7 and Figure 6-8.

In Frame Buffer Access Mode during buffer reads, the PHY header (PHR) and the PSDU data are transferred via MISO following PHY_STATUS byte. Once the PSDU data is uploaded, three more bytes are transferred containing the link quality indication (LQI) value, the energy detection (ED) value, and the status information (RX_STATUS) of the received frame, for LQI details refer to Section 8.7. The Figure 6-7 illustrates the packet structure of a Frame Buffer read access.

Note: 1. The frame buffer read access can be terminated immediately at any time by setting pin 23 (/SEL) = H, for example after reading the PHR byte only.

Figure 6-7. Packet Structure - Frame Read Access.

	byte 1 (command byte)	byte 2 (data byte)	byte 3 (data byte)		byte n-1 (data byte)	byte n (data byte)
MOSI	0 0 1 reserved[4:0]	XX	XX	...	XX	XX
MISO	PHY_STATUS	PHR[7:0]	PSDU[7:0]	...	ED[7:0]	RX_STATUS[7:0]

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The structure of RX_STATUS is described in Table 6-3.

Table 6-3. Structure of RX_STATUS.

Bit	7	6	5	4	
	RX_CRC_VALID	TRAC_STATUS			RX_STATUS
Read/Write	R	R	R	R	
Reset value	0	0	0	0	

Bit	3	2	1	0	
	reserved				RX_STATUS
Read/Write	R	R	R	R	
Reset value	0	0	0	0	

Note: 2. More information to RX_CRC_VALID, see Section 8.3.5, and to TRAC_STATUS, see Section 7.2.6.

On frame buffer write access the second byte transferred on MOSI contains the frame length (PHR field) followed by the payload data (PSDU) as shown by Figure 6-8.

Figure 6-8. Packet Structure - Frame Write Access.

The number of bytes *n* for one frame buffer access is calculated as follows:

Read Access: *n* = 5 + *frame_length*

[PHY_STATUS, PHR byte, PSDU data, LQI, ED, and RX_STATUS]

Write Access: *n* = 2 + *frame_length*

[command byte, PHR byte, and PSDU data]

The maximum value of *frame_length* is 127 bytes. That means that *n* ≤ 132 for Frame Buffer read and *n* ≤ 129 for Frame Buffer write accesses.

Each read or write of a data byte automatically increments the address counter of the Frame Buffer until the access is terminated by setting /SEL = H. A Frame Buffer read access can be terminated at any time without any consequences by setting /SEL = H, for example after reading the frame length byte only. A successive Frame Buffer read operation starts again with the PHR field.

The content of the Atmel AT86RF233 Frame Buffer is overwritten by a new received frame or a Frame Buffer write access.

Figure 6-9 and Figure 6-10 illustrate an example SPI sequence of a Frame Buffer access to read a frame with 2-byte PSDU and write a frame with 4-byte PSDU.

**Figure 6-9. Example SPI Sequence - Frame Buffer Read of a Frame with 2-byte PSDU.**
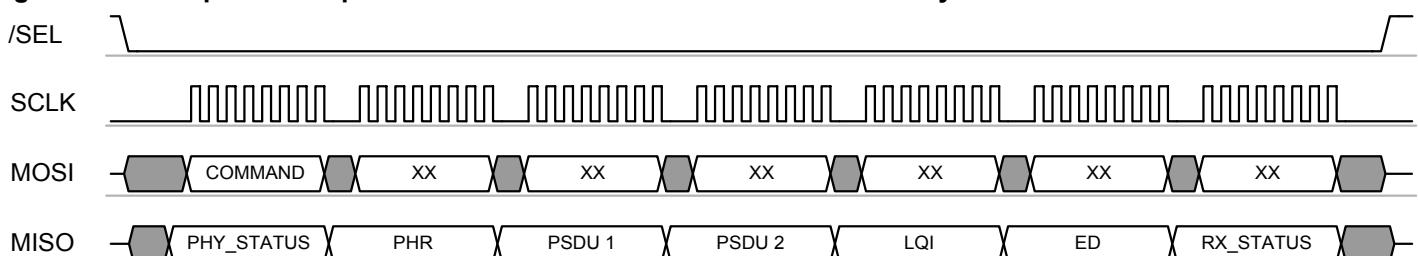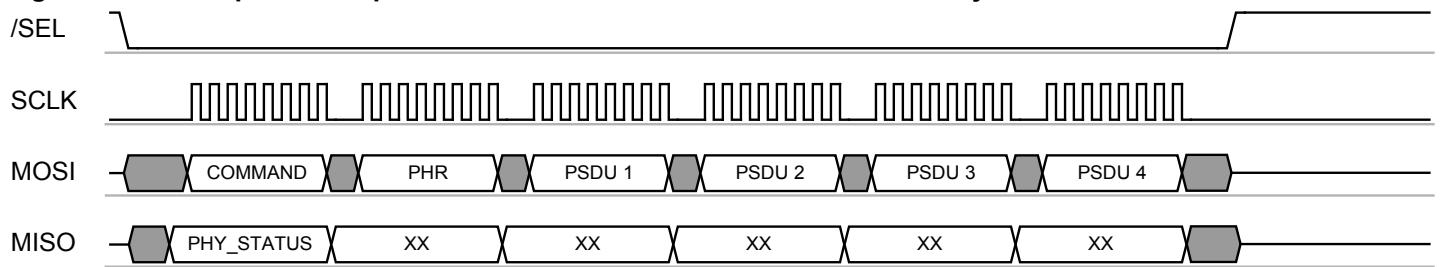
Figure 6-10. Example SPI Sequence - Frame Buffer Write of a Frame with 4-byte PSDU.

Access violations during a Frame Buffer read or write access are indicated by interrupt IRQ_6 (TRX_UR). For further details, refer to Section 9.3.

Notes: 1.   The Frame Buffer is shared between RX and TX operations, the frame data is overwritten by freshly received data frames. If an existing TX payload data frame is to be retransmitted, it must be ensured that no TX data is overwritten by newly received RX data.

2.   To avoid overwriting during receive *Dynamic Frame Buffer Protection* can be enabled, refer to Section 11.8.

3.   For exceptions, receiving acknowledgement frames in Extended Operating Mode (TX_ARET) refer to Section 7.2.4.

6.3.3 SRAM Access Mode

The SRAM access mode is used to read and write Atmel AT86RF233 frame buffer beginning with a specified byte address. It enables to access dedicated buffer data directly from a desired address without a need of incrementing the frame buffer from the top.

The SRAM access mode allows accessing dedicated bytes within the Frame Buffer or AES address space, refer to Section 11.1. This may reduce the SPI traffic.

During frame receive, after occurrence of IRQ_2 (RX_START), an SRAM access can be used to upload the PHR field while preserving Dynamic Frame Buffer Protection, see Section 11.8.
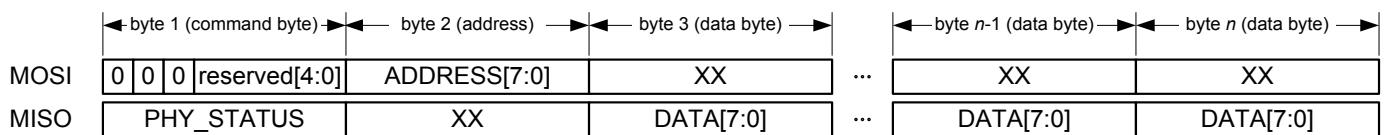
Each SRAM access starts with /SEL = L. The first transferred byte on MOSI shall be the command byte and must indicate an SRAM access mode according to the definition in Table 6-2. The following byte indicates the start address of the write or read access.

SRAM address space:

- Frame Buffer: 0x00 to 0x7F

- AES: 0x82 to 0x94
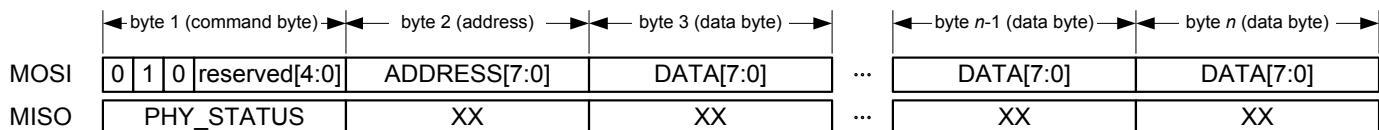
On SRAM read access, one or more bytes of read data are transferred on MISO starting with the third byte of the access sequence; refer to Figure 6-11.

Figure 6-11. Packet Structure – SRAM Read Access.

On SRAM write access, one or more bytes of write data are transferred on MOSI starting with the third byte of the access sequence; refer to Figure 6-12. Do not attempt to read or write bytes beyond the SRAM buffer size.

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Figure 6-12. Packet Structure – SRAM Write Access.

As long as /SEL = L, every subsequent byte read or byte write increments the address counter of the Frame Buffer until the SRAM access is terminated by /SEL = H.

Figure 6-13 and Figure 6-14 illustrate an example SPI sequence of an Atmel AT86RF233 SRAM access to read and write a data package of five byte length, respectively.

Figure 6-13. Example SPI Sequence – SRAM Read Access of a 5-byte Data Package.
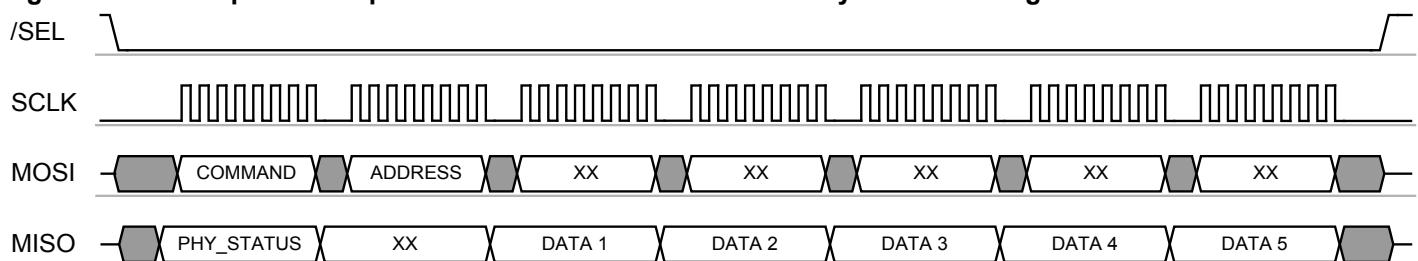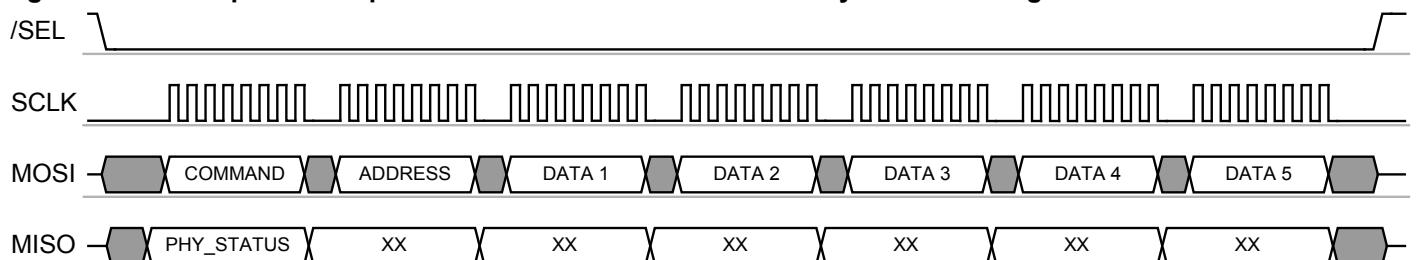

Figure 6-14. Example SPI Sequence – SRAM Write Access of a 5-byte Data Package.

Notes: 1. The SRAM access mode is not intended to be used as an alternative to the Frame Buffer access modes (see Section 6.3.2).

2. Frame Buffer access violations are not indicated by a TRX_UR interrupt when using the SRAM access mode, for further details refer to Section 9.3.3.

6.4 Radio Transceiver Status information

Each Atmel AT86RF233 SPI access can return radio transceiver status information which is a first byte transmitted out of MISO output as the serial data is being shifted into MOSI input. Radio transceiver status information (PHY_STATUS) can be configured using register bits SPI_CMD_MODE (register 0x04, TRX_CTRL_1) to return TRX_STATUS, PHY_RSSI or IRQ_STATUS register as shown in below.

6.4.1 Register Description

Note: 1. Throughout this datasheet, underlined values indicate reset settings.

Register 0x04 (TRX_CTRL_1):

The TRX_CTRL_1 register is a multi-purpose register to control various operating modes and settings of the radio transceiver.