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Features

- **RF Frequency Range of 264–456 MHz**
- **6 dBm RF Output into Matched Antenna**
- **RF Output Power Adjustable over 36 dB with 1 dB Resolution**
- **Phase-locked Loop (PLL) Based Frequency Synthesizer**
- **Supports OOK Modulation**
- **Data Bandwidth of Up to 10 Kbps Manchester**
- **2-volt Operation**
- **8-bit AVR® RISC Microcontroller Core**
- **Minimal External Components**
- **Space-saving 20-lead TSSOP**
- **2 KB (1K x 16) of Flash Program Memory**
- **128 Bytes of EEPROM**
- **128 Bytes of SRAM**
- **In-system Programmable Data and Program Memory**
- **Six I/Os (Serial I/F, LED Drive Outputs, Button Input Interrupts)**
- **Low Battery Detect and Brown-out Protection**
- **Software Fine-tuning of VCO Tank Circuit**

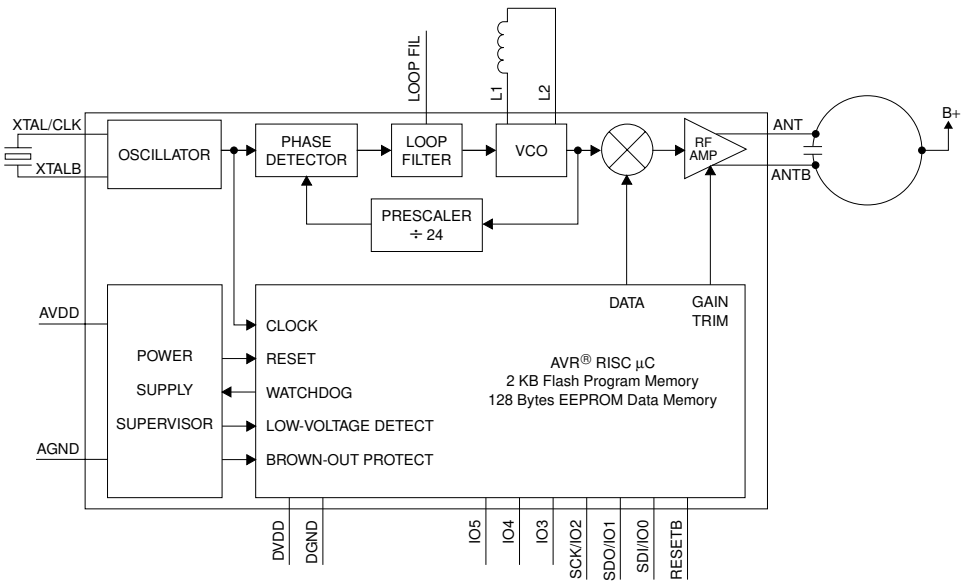
Applications

- **Remote Keyless Entry (RKE) Transmitters**
- **Wireless Security Systems**
- **Home Applicance Control (Lighting Control, Ceiling Fans)**
- **Radio Remote Control (Hobby, Toys)**
- **Garage Door Openers**
- **Wireless PC Peripherals (Keyboard, Mouse)**
- **Telemetry (Tire Pressure, Utility Meter, Asset Tracking)**

Description

The Atmel AT86RF401 Smart RF Microtransmitter is a highly integrated, low-cost RF transmitter, combined with an AVR RISC microcontroller. It requires only a crystal, a single $LiMnO_2$ coin cell (CR2032 or similar), three capacitors, an inductor and a tuned-loop antenna to implement a complete on-off keyed (OOF) wireless RF data transmitter.

Figure 1. Block Diagram



Smart RF Wireless Data Microtransmitter

AT86RF401

1424F–RKE–12/03

In-system programmable, nonvolatile Flash program memory and EEPROM data storage make possible rapid time-to-market and lower inventory costs.

In-system programmable, nonvolatile Flash program memory and EEPROM data storage make possible rapid time-to-market and lower inventory costs.In-system programmable, nonvolatile Flash program memory and EEPROM data storage make possible rapid time-to-market and lower inventory costs.Static current consumption is kept to a minimum with an ultra-low current shutdown mode. Normal operation resumes when a button is pressed. This activates the crystal oscillator circuit that serves as the clock for the AVR microcontroller.

The RF carrier is synthesized utilizing an on-board Voltage Controlled Oscillator (VCO). Optimal tuning of the VCO is maintained over component tolerance through the use of a software-controlled switched capacitor array. Its accuracy is maintained with a PLL detector that compares the crystal oscillator to a frequency-scaled version (divided by 24) of the RF carrier. The resulting error signal adjusts the VCO to produce a very stable RF carrier.

An interrupt-based bit-timer structure, integral to the AVR microcontroller, simplifies the implementation of user-specific, data-bit encoding routines, such as PWM or Manchester, for modulating the RF carrier. Thirty-six dB of RF power output control is available to the user in 1 dB steps and is addressable in software. The RF signal output is placed differentially on a tuned-loop antenna, which may be realized as a counterspread copper trace on a PCB.

The AT86RF401 is fabricated in Atmel's 0.6 µm Mixed Signal CMOS + EEPROM process, enabling true system-level integration (SLI).

Figure 2. 20-lead TSSOP

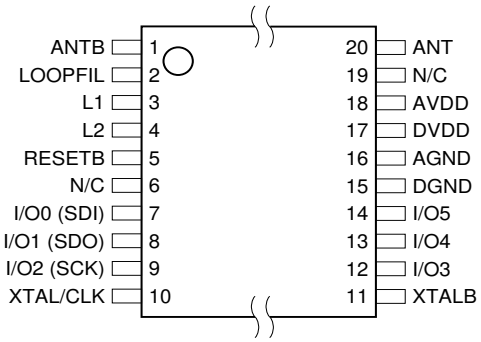


Figure 3. Sample Circuit

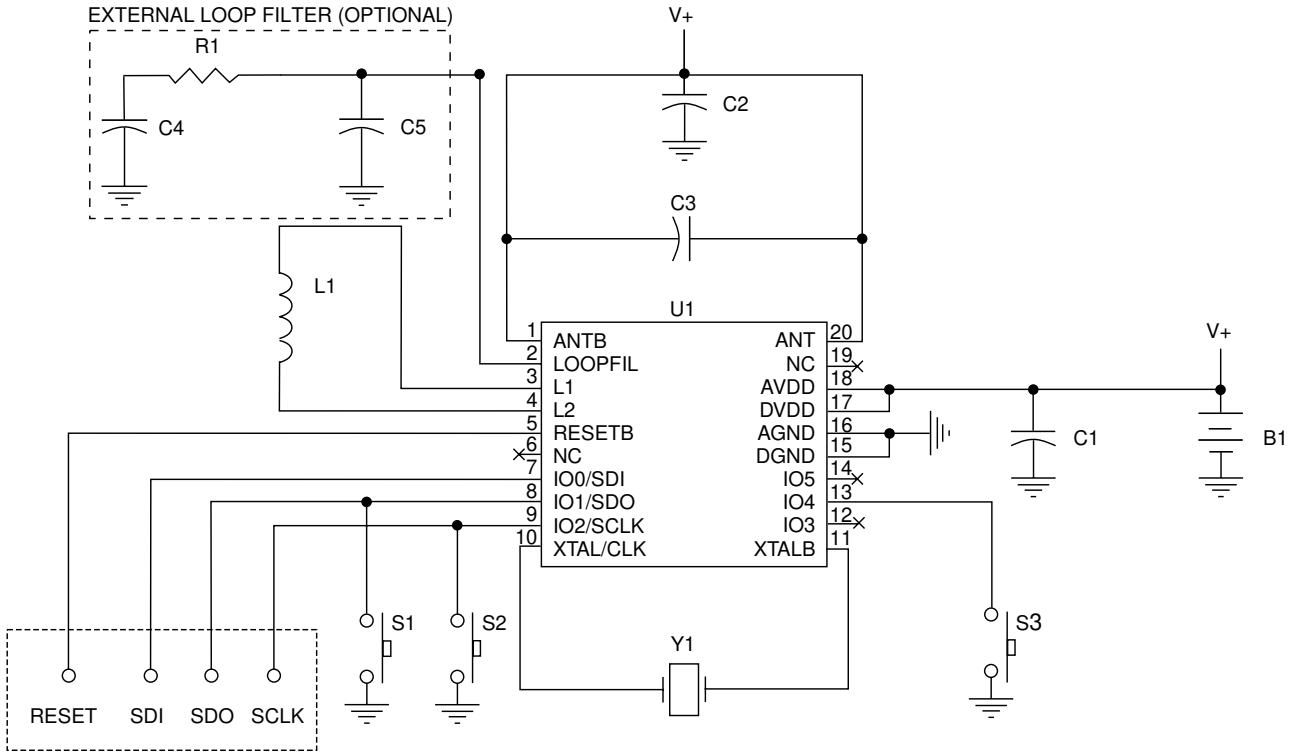


Table 1. Recommended Parts List

Part Number	Value (Common)	Value (315 MHz)	Value (433.92 MHz)	Value (Ext. Loop Filter)	Specification
B1	3.6V				CR2032, Li Battery
C1	0.01 µF				0603, X7R, ± 10%
C2	100 pF				0603, COG, ± 5%
C3		Antenna Dependent	Antenna Dependent	Antenna Dependent	0603, COG, ± 0.1 pF
C4		Not req'd	Not req'd	Frequency Dependent	0603, COG, ± 5%
C5		Not req'd	Not req'd	Frequency Dependent	0603, COG, ± 0.25 pF
L1		82 nH	39 nH	Frequency Dependent	1608, ± 5%
R1		Not req'd	Not req'd	Frequency Dependent	0603, ± 5%
S1	Switch				SPST
S2	Switch				SPST
S3	Switch				SPST
U1	AT86RF401				20-lead TSSOP
Y1		13.125 MHz	18.08 MHz	Frequency Dependent	13.125 MHz: Crystek™ P/N 016757 18.080 MHz: Crystek P/N 016758

Table 2. Pin Descriptions – 20-lead TSSOP

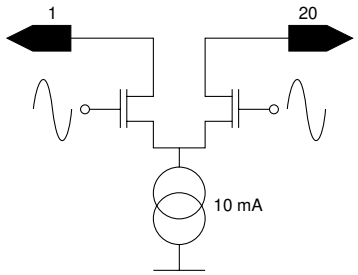
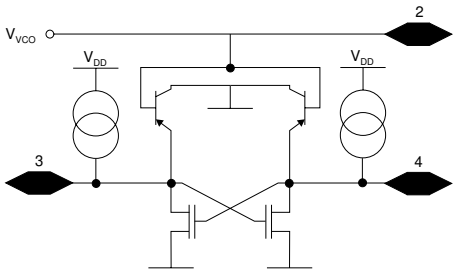
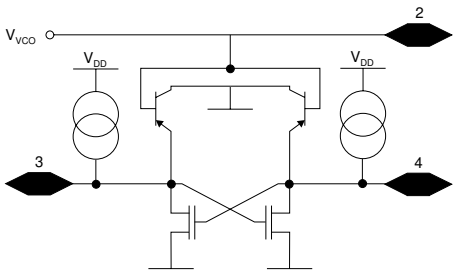
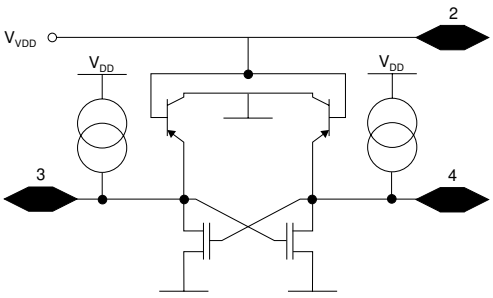
Symbol	Pin		Description
ANTB	1		Differential Antenna Output
LOOPFIL	2		External VCO Loop-filter Connection. V_{VCO} is the VCO control voltage.
L1	3		External VCO Inductor Connection. V_{VCO} is the VCO control voltage.
L2	4		External VCO Inductor Connection. V_{VCO} is the VCO control voltage.

Table 2. Pin Descriptions – 20-lead TSSOP (Continued)

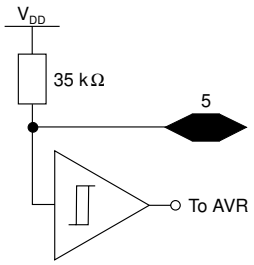
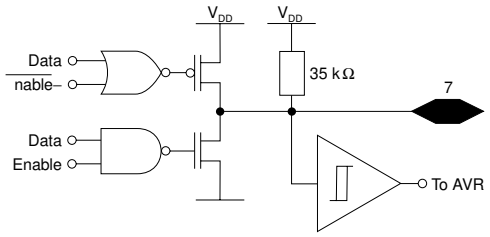
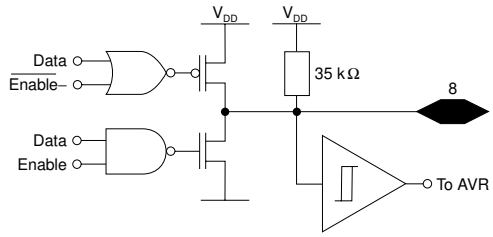
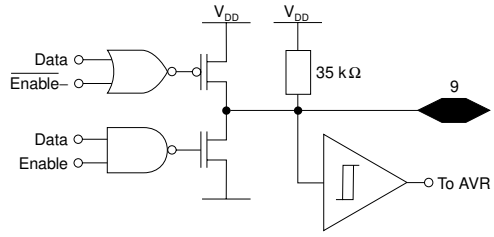
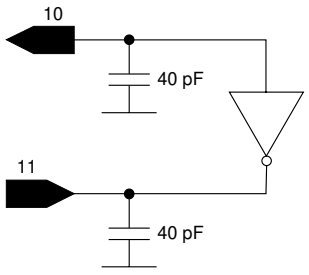
RESETB	5		SPI Reset Input: A “low” on this pin resets the device and puts the part into SPI mode. A logic-high on this pin causes the device to execute its program if the V_{DD} is above the brown-out voltage level.
NC	6		No Connect. Float Pin.
I/O0 (SDI)	7		SPI Data In/Input/Output 0: General-purpose I/O and button input. In SPI mode, this pin serves as SDI (Serial Data Input).
I/O1 (SDO)	8		SPI Data Out/Input/Output 1: General-purpose I/O and button input. In SPI mode, this pin serves as SDO (Serial Data Output).
I/O2 (SCK)	9		SPI Clock/Input/Output 2: General-purpose I/O and button input. In SPI mode, this pin serves as SCK (SPI Clock Input).
XTAL/CLK	10		Crystal/Clock Input: Input to the inverting oscillator amplifier and input to the internal clock operating circuit. This pin may be driven externally for test purposes.

Table 2. Pin Descriptions – 20-lead TSSOP (Continued)

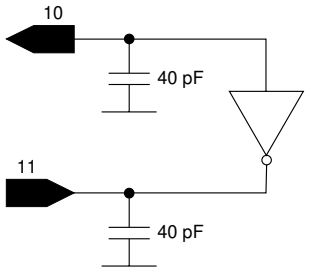
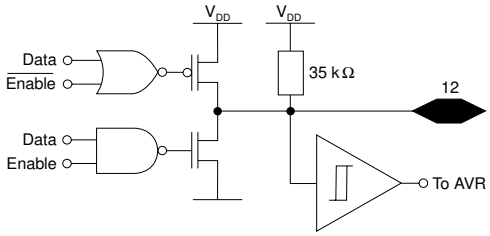
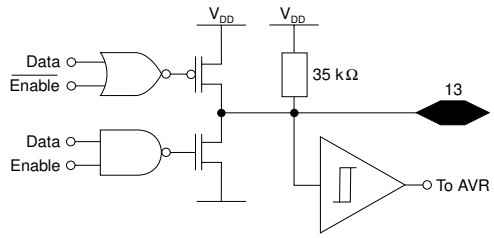
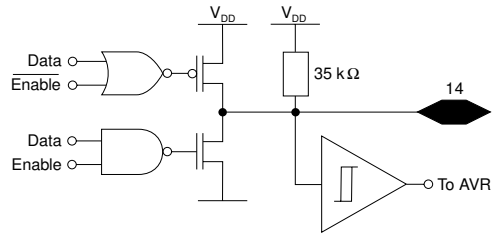
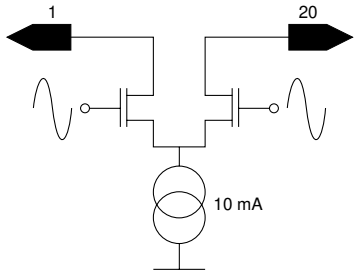
XTALB	11		Crystal Output: Output from the inverting oscillator amplifier
IO3	12		Input/Output 3: General-purpose I/O and button input
IO4	13		Input/Output 4: General-purpose I/O and button input
IO5	14		Input/Output 5: General-purpose I/O and button input
DGND	15		Digital Ground
AGND	16		Analog Ground
DVDD	17		Digital Voltage Supply

Table 2. Pin Descriptions – 20-lead TSSOP (Continued)

AVDD	18		Analog Voltage Supply
N/C	19		No Connect – Float Pin
ANT	20		Differential Antenna Output

Absolute Maximum Ratings*

Antenna Voltage (Pins 1, 20)	–1V to 10V
Operating Temperature	–40°C to +85°C
Storage Temperature (without bias)	–55°C to +125°C
Voltage on V_{DD} with respect to ground	6.0V
Voltage on Pins 2–19 (TSSOP 20)	–0.1 to V_{DD} +0.3V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. DC Characteristics

V_{DD} = 3.3V; f_{XTAL} = 13.125 MHz; $f_{AVR} = f_{XTAL} \div 16$; T_A = 25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
V_{DD}	Supply Voltage		2.0	3.3	5.0	V
I_{DD}	Standby Current (off)	V_{DD} = 3.3V T_A = 25°C	–	0.1	0.5	µA
	AVR Active		–	3.4	–	mA
	Frequency Synthesizer + AVR Active		–	14.3	–	mA
	Transmit (FS, AVR and Power Amp active)	CW modulation	–	23.2	–	mA
Digital Inputs (SDI, SCK, RESETB, IOx)						
V_{IH}	High-level Input Voltage		0.8* V_{DD}	–	V_{DD}	V
V_{IL}	Low-level Input Voltage		0	–	0.2* V_{DD}	V
I_{IH}	High-level Input Current	$V_{IH} = V_{DD}$, V_{DD} = 5.0V	–	–	1	µA
I_{IL}	Low-level Input Current	V_{IL} = 0V, V_{DD} = 5.0V	–140	–	–	µA
Digital Outputs (SDO, IOx)						
V_{OH}	High-level Output Voltage	I_{OH} = –500 µA	V_{DD} –0.4	–	–	V
V_{OL}	Low-level Output Voltage	I_{OL}= 2 mA	–	–	0.4	V
Microcontroller/System						
t_{TX}	Time from Button Wake-up to RF Outputs Active		–	0.5	1.0	ms
f_{AVR}	AVR Clock Frequency		–	–	1.25	MHz
EE_{LIFE}	EEPROM Retention	Initial programming conditions: V_{DD} = 3.3V ± 10% Temp = 25°C ± 10%	–	–	10	years
EE_{CYCLES}	EEPROM Write/Erase Endurance	2.0V ≤ V_{DD} ≤ 5.0V –40°C ≤ Temp ≤ 85°C	–	–	100,000	cycles

Table 4. Analog/RF Specs

V_{DD} = 3.3V; f_{XTAL} = 13.125 MHz; $f_{AVR} = f_{XTAL} \div 16$; T_A = 25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
RF Amplifier						
I_{PA}	Power Amp Output Current	Transmitting (RF "ON"), 0 dB Attenuation	–	8.6	–	mA
$P_{CTLRANGE}$	Power Control Range		–	36	–	dB
P_{CTLRES}	Power Control Resolution		–	1	–	dB
Crystal Oscillator						
f_{OSC}	Oscillation Frequency Range		11	–	19	MHz
Frequency Synthesizer/PLL						
F_{OUT}	Output Frequency Range		264	–	456	MHz
P_{HARM}[1]	Harmonics	I/O Pins Static during RF Transmission Using PCB Trace Antenna	–	–60	–	dBc
f_{MOD}	OOK Modulation Data Rate	Using Manchester Data Bit Encoding	–	–	10	Kbps

Note: 1. Characterized but not guaranteed by test due to dependency on PCB trace antenna

Functional Description

The complete circuit consists of the following functional blocks.

Transmitter

Crystal Oscillator

The crystal oscillator circuit is designed to work with crystals with fundamental frequencies between 11 and 19 MHz. Forty pF of internal capacitance is connected between each of the crystal input pins and (chip) ground. Alternatively, an external clock can be used for these functions.

This circuit provides the master clock for the entire chip. A programmable divider is used to provide the AVR system clock.

Radio Frequency Power Amplifier

The RF power amplifier generates a differential output suitable for driving an off-chip tuned-loop antenna from the PLL output. The PLL output signal is gated using on-off keyed (OOK) modulation before transmission. It is used as the RF carrier frequency for the transmitted data stream. The amplifier can be configured via software to reduce the power output by 36 dB (with 1 dB resolution).

Frequency Synthesizer

The frequency synthesizer utilizes a PLL, which consists of a phase detector, a ÷24 prescaler, an on-chip loop filter and an integrated VCO. The VCO output is buffered prior to the output amplifier. The output frequency is 24 times the crystal frequency. To offset component tolerance, a switched capacitor array is connected between pins 3 and 4 of the VCO. Thirty-two discrete steps of capacitance are available to tune the VCO control voltage. An internal window comparator monitors the magnitude of the tuning voltage and is used by the AVR core to determine the optimal tuning configuration.

Lock Detector

The lock detection block provides an indication of the state of the phase lock loop (PLL). Lock condition is determined by counting the number of cycle slips in a given time

period. A number of registers are available to adjust the performance of the lock detector. These include lock delay and unlock delay timers as well as a cycle slip counter.

Bandgap Reference

The device uses a 1.2V (nominal) bandgap reference generator to provide consistent performance over a wide range of input supply voltages. This reference voltage is used throughout the device.

Brown-out Protection/Low Battery Detection

The brown-out protection and low battery detection functions consist of a voltage reference, a sampling block and an autozero comparator. The circuit's primary operating mode is brown-out protection.

Brown-out Protection

The brown-out protection circuit detects when the level of V_{DD} drops below the minimum voltage that guarantees proper operation. The brown-out voltage for this device is typically 1.8 volts.

If a brown-out occurs, the device enters a reset state. It stays in this state until either of the following occurs:

- The level of V_{DD} increases ~0.1–0.2 volts above the brown-out voltage. This causes the device to enter a warm reboot state.
- The level of V_{DD} drops to ~0 volts, then increases above the POR level. This places the device into the "cold start" mode of operation, identical to battery insertion.

Low Battery Detection

The low battery detection feature allows the programmer to select a voltage threshold (1.5–2.7 volts) for V_{DD} at which a warning flag is issued to the user. For example, this warning may be utilized to activate an I/O port or to change the transmitted message.

Additionally, the programmer has the option of defining the amount of hysteresis on this threshold. More detail can be found in register descriptions for I/O Enable (IO_ENAB, $30, page 39) and Battery Low Configuration (BL_CONFIG, $35, page 42).

Bit Timer

A hardware assist has been included in the AT86RF401 to make transmission of data easier. Keying of the transmitter is timed by this logic, and interrupts are generated when data is needed by the timer or when transmission is complete. The timer also supports code that uses polling instead of interrupts. Using polling instead of interrupts may facilitate higher bit rates. Additionally, this timer may be used to time pulses arriving at the I/O3 pin. This enables the AT86RF401 to be used to decode the signal detected by an external receiver chip. For additional information on how to implement the bit timer, see *AT86RF401 Bit Timer Application Note,* available at *www.atmel.com.*

Bit Timer in Transmit Mode

Bit coding is done by the AVR before data is sent to the bit timer. Bit timing is controlled by the count value in the Bit Timer Count (BTCNT) register and the two most significant bits in the Bit Timer Control Register (BTCR). Generally the time of each bit is:

$$P_{xx} = P \times (countval + 1)$$

where P_{xx} is the period of each time slot and *countval* is the counter value in the BTCNT and BTCR registers. *P* is the AVR clock period that is set in the PWR_CTL register. *countval* = {BTCR[7:6], BTCNT[7:0]}.

There are two interrupts associated with transmit mode:

1. Transmit Buffer Empty Interrupt: This vectors to address 0x04. Flag 0 is set, and, if enabled, this interrupt is generated when the timer removes the value from the DATA bit in the BTCR. This interrupt service routine should load the next transmit bit into the DATA bit in the BTCR.
2. TXDONE Interrupt: This vectors to address 0x02. Flag 2 is set, and, if enabled, an interrupt is generated when the counter has counted down to zero and the buffer is empty. This indicates that the transmission is complete. This interrupt service routine should turn off the transmitter and turn off the bit timer using the mode bits.

Bit Timer in Receive Mode

When put into receive mode, the bit timer times pulses arriving at the I/O3 pin. When enabled, the counter counts up from zero and places that value in the BTCNT register when an edge occurs. If the edge is rising, the DATA bit in the BTCR is set. If the edge is falling, the DATA bit in the BTCR is reset. This mode may be used to decode signals from a receiver chip easily.

Bit Timer in Generic Timer/Counter Mode

The bit timer may be used as a generic timer by not allowing it to key off the transmitter. An interrupt is generated after the amount of time dictated by the count value.

Watchdog Timer

When enabling the watchdog timer, the status of the watchdog time is unknown. The user is advised to execute a WDR instruction before enabling the watchdog. Otherwise, the device might get reset before the first WDR after enabling is reached. To prevent the unintentional disabling of the watchdog, a special turn-off procedure must be followed when the watchdog is disabled. Refer to the description of the Watchdog Timer Control Register on page 38 for details (see Register $22 in I/O Memory). The watchdog timer prescaler determines the number of system clocks that occur before the watchdog reset is asserted. The system clock is determined by Bits[7:5] of the AVR_CONFIG register.

Reset and Interrupt Handling

The AT86RF401 Reset and Interrupt vectors are defined in Table 5. The I-bit in the status register must be set to enable the interrupts.

Table 5. Reset and Interrupt Vectors

Vector Number	Program Address	Source	Interrupt Definition
1	$000	RESETB, Watchdog, Buttons	Hardware Pin or Watchdog or Button Reset
2	$002	Transmission Done (TXDONE)	Bit Timer Flag 2 Interrupt
4	$004	Transmit Buffer Empty	Bit Timer Flag 0 Interrupt

The most typical and general program setup for the Reset and Interrupt Vector Addresses are:

```
Address   Labels    Code                 Comments
$000                jmp      RESET       ; Reset handler
$002                jmp      BT_F2_ISR   ; Bit timer flag 2 interrupt service routine
$004                jmp      BT_F0_ISR   ; Bit timer flag 0 interrupt service routine
$006  MAIN:         <instr>  xxx         ; Main program start
  …          …          …       …
```

Reset Sources

The AT86RF401 has several sources of reset:

- Power-on Reset: The device is reset when the supply voltage is applied between the VDD and GND pins. There are 10^6 cycles of delay between Power-on Reset occurring and the part becoming active. This is to ensure that the power is stable.
- External Reset: The device is reset when a logic low level is present on the RESETB pin. This resets all I/O Registers and puts the part into SPI mode. The I/O Registers may be read and written by the SPI interface after two AVR System Clocks.
- Watchdog Reset: This is similar to power-on reset but is caused by the watchdog timer and does not have a 10^6 cycle delay prior to becoming active.
- Brown-out Reset: This is caused by the battery voltage dropping below the Brown-out Threshold voltage trip point.
- Button Reset (software reset): The part is placed into a special reset state by software. The part is released from reset when a properly configured button is activated, and the part is not in external reset or brown-out reset. In the button reset state, most I/O registers are not reset, and there is no time delay before becoming active.

During power-on reset and watchdog reset, all I/O registers are set to their initial values, and the program starts execution from address $000.

Note: The instruction placed in address $000 must be an RJMP (relative jump) instruction or a JMP (absolute jump) to the reset handling routine. If an RJMP or JMP instruction is not present at address $000, the part is placed into a “no program” reset state. This is to protect the part from fetching instructions when no program is present.

Interrupt Response Time

The interrupt execution response for all the enabled AVR interrupts is a minimum of four clock cycles. After the four clock cycles, the program vector address for the actual interrupt handling routine is executed. During this four clock cycle period, the Program Counter is pushed onto the stack. The vector is a jump to the interrupt routine, and this jump takes two clock cycles. If an interrupt occurs during execution of a multi-cycle instruction, this instruction is completed before the interrupt is served.

A return from an interrupt handling routine takes four clock cycles. During these four clock cycles, the Program Counter is popped back from the stack. When AVR exits from an interrupt, it will always return to the main program and execute one more instruction before any pending interrupt is served.

Note: The Status Register (SREG) is not saved by the AVR hardware. This must be performed by user software when required.

Memory Programming

Program Memory Lock Bits

The AT86RF401 microtransmitter provides two lock bits that can be left unprogrammed (“1”) or can be programmed (“0”) to obtain the additional features listed in Table 6.

Table 6. Lock Bit Protection Modes

Program Lock Bits			
Mode	**LB1**	**LB2**	**Protection Type**
1	1	1	No program lock features
2	0	1	Further serial (SPI) programming of the EEPROM is disabled (both program and data memory).
3	0	0	Same as mode 2, but Verify is also disabled

Note: The lock bits can only be erased with the Chip Erase operation.

In-system Flash and EEPROM

The AT86RF401 offers 2 Kbytes (1K x 16) of in-system reprogrammable Flash program memory and 128 bytes of EEPROM data memory. This memory can be programmed serially via the SPI interface.

SPI Interface

Both the program and data memory arrays can be programmed using the serial SPI bus while RESETB is pulled to GND. The serial interface consists of pins SCK, SDI (input) and SDO (output).

When programming, an auto-erase cycle is built into the self-timed programming operation, and there is no need to first execute the Chip Erase instruction. The Chip Erase operation sets every memory location in the EEPROM array to $FF.

Either an external system clock is supplied at pin XTAL/CLK or a crystal needs to be connected across pins XTAL/CLK and XTALB. The minimum low and high periods for the serial clock (SCK) input are defined as follows:

Low: 4 XTAL Clock Cycles *High:* 16 XTAL Clock Cycles

Serial Programming Algorithm

Refer to Figure 4 (page 15), Figure 5 (page 16) and Figure 6 (page 17). To program and verify the AT86RF401 in the serial programming mode, the following sequence is recommended.

Power-up Sequence:

1. Apply power between VDD and GND while RESETB and SCK are set to “0”. If a crystal is not connected across pins XTAL and XTALB, apply a clock signal to the XTAL pin. If the programmer can not guarantee that SCK is held low during power-up, RESETB must be given a positive pulse after SCK has been set to “0”.
2. Wait for at least 20 ms and enable serial programming by sending the Programming Enable instruction to pin SDI. This must occur prior to any program/erase operations.
3. If a chip erase is performed, wait 4 ms, give RESETB a positive pulse and start over again from Step 2.
4. The array is programmed one byte at a time by supplying the address and data together with the appropriate Write instruction. The memory location is first automatically erased before new data is written. The next byte can be written after 4 ms.
5. Any memory location can be verified by using the Read instruction, which returns the content at the selected address at serial output SDO.
6. At the end of the programming session, RESETB must be set high to commence normal operation.

Signature Bytes

All Atmel microcontrollers have a three-byte signature code that identifies the device. For the AT86RF401, the signature bytes are:

- 0x000: 0x1E (indicates manufactured by Atmel)
- 0x001: 0x91 (indicates 2 Kbytes Flash program memory)
- 0x002: 0x81 (indicates AT86RF401 when 0x001 is 0x91)

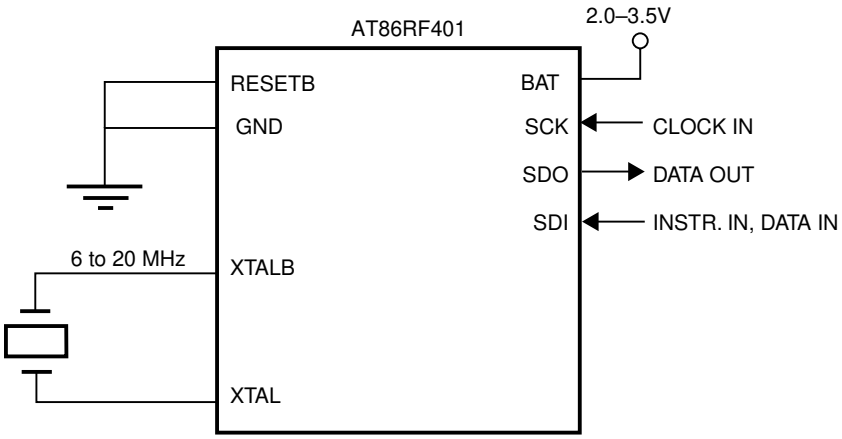
Data EEPROM Access from the AVR

Table 7. AT86RF401 Serial Programming Instruction Set

Instruction	Instruction Format				Operation
	Byte 1	Byte 2	Byte 3	Byte 4	
Programming Enable	1010 1100	0101 0011	xxxx xxxx	xxxx xxxx	Enable Serial Programming after RESETB goes low.
Chip Erase	1010 1100	100x xxxx	xxxx xxxx	xxxx xxxx	Chip erase EEPROM
Read Program Memory	0010 **H**000	0000 00**aa**	bbbb bbbb	oooo oooo	Read **H** (high or low) data **o** from Program memory at word address **a:b**
Write Program Memory	0100 **H**000	0000 00**aa**	bbbb bbbb	iiii iiii	Write **H** (high or low) data **i** to Program memory at word address **a:b**
Read EEPROM Memory	1010 0000	0000 0000	x**bbb bbbb**	oooo oooo	Read data **o** from EEPROM memory at address **b**
Write EEPROM Memory	1100 0000	0000 0000	x**bbb bbbb**	iiii iiii	Write data **i** to EEPROM memory at address **b**
Write Lock Bits	1010 1100	111x x***21***x	xxxx xxxx	xxxx xxxx	Write lock bits. Set bits **21** = “0” to program lock bits.
I/O Read	10110000	0000 0000	00bbbbbb	oooo oooo	Read data 0 from I/O memory address **b**
I/O Write	11010000	0000 0000	00bbbbbb	iiii iiii	Write data i to I/O memory address **b**
Read Signature Byte	0011 0000	000x xxxx	xxxx xxbb	oooo oooo	

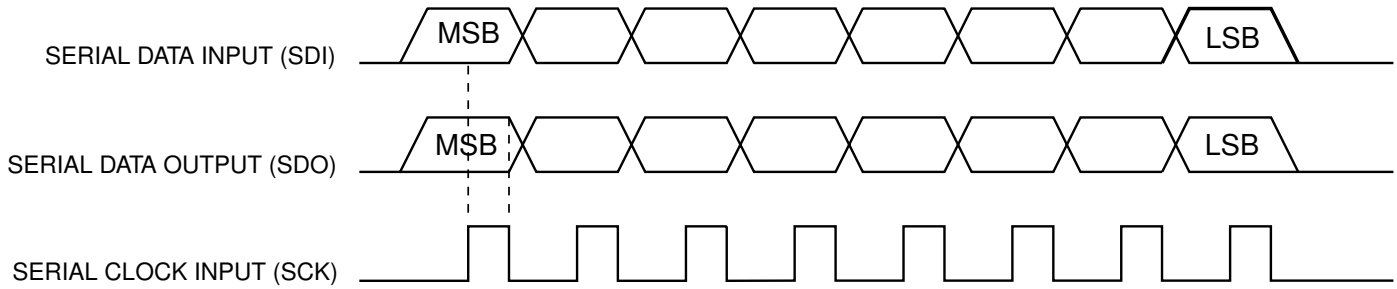
Note: **a** = address high bits
b = address low bits
H = 0: Low byte, 1: High byte
o = data out
i = data in
x = don’t care
1= lock bit 1
2= lock bit 2

Figure 4. Serial Programming and Verify



Notes: 1. When *writing*, data is clocked on the *rising* edge of CLK.
2. When *reading*, data is clocked on the *falling* edge of CLK. See Figure 5 for an explanation.

Figure 5. Serial Programming Waveforms



Note: This device includes an integrated 128-byte EEPROM, which is accessed by three registers located in the I/O memory space. These are the DEECR, DEEDR and DEEAR registers. For more information, refer to I/O Register Description.

AVR Core

Architectural Overview

The fast-access register file concept contains 32 x 8-bit general-purpose working registers with a single clock cycle access time. This means that during one single clock cycle, one Arithmetic Logic Unit (ALU) operation is executed. Two operands are output from the register file, the operation is executed, and the result is stored back in the register file in one clock cycle.

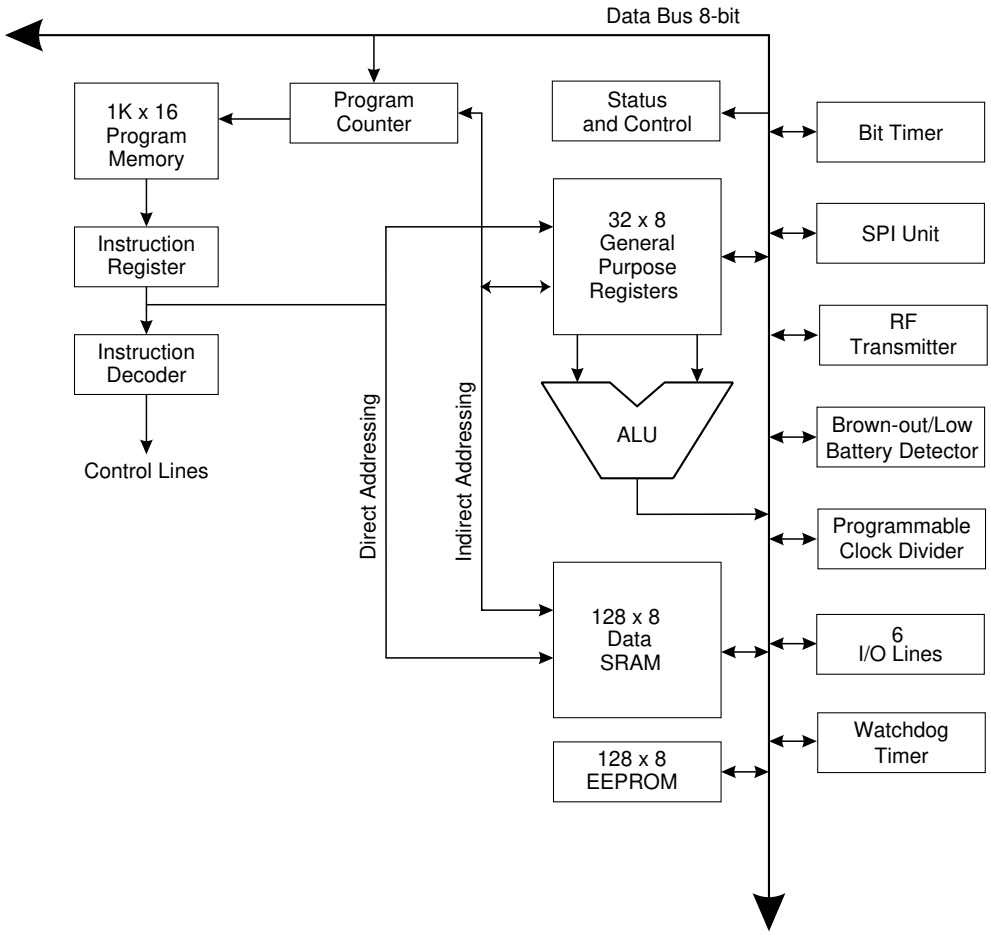
Six of the 32 registers can be used as three 16-bit indirect address register pointers for Data Space addressing, enabling efficient address calculations. One of the three address pointers is also used as the address pointer for look-up tables in Flash program memory. These added function registers are the 16-bit X-register, Y-register and Z-register.

The ALU supports arithmetic and logic operations between registers or between a constant and a register. Single register operations are also executed in the ALU. Figure 6 shows the AT86RF401 AVR architecture.

In addition to the register operation, the conventional memory addressing modes can be used on the register file as well. This is enabled by the fact that the register file is assigned the 32 lowest data space addresses ($00–$1F), allowing them to be accessed as though they were ordinary memory locations.

The I/O memory space contains 64 addresses for CPU peripheral functions as Control Registers, Timer/Counters, A/D converters and other I/O functions. The I/O Memory can be accessed directly or as the Data Space locations following those of the register file, $20–$5F.

Figure 6. AVR Core Architecture



The AVR uses a Harvard architecture concept, with separate memories and buses for program and data. The program memory is executed with a two-stage pipeline. While one instruction is being executed, the next instruction is prefetched from the program memory. This concept enables instructions to be executed in every clock cycle. The program memory is in-system, reprogrammable Flash memory.

With the jump and call instructions, the whole 1K word address space is directly accessed. Most AVR instructions have a single 16-bit word format. Every program memory address contains a 16- or 32-bit instruction.

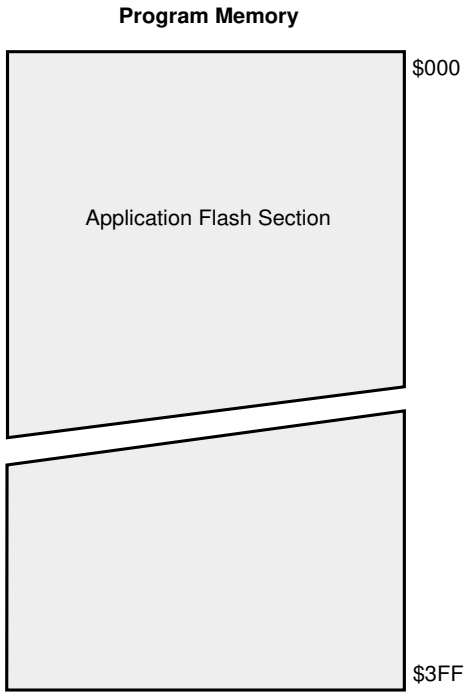
During interrupts and subroutine calls, the return address program counter (PC) is stored on the stack. The stack is effectively allocated in the general data SRAM, and consequently the stack size is only limited by the total SRAM size and the usage of the SRAM. All user programs must initialize the SP in the reset routine (before subroutines or interrupts are executed). The 7-bit stack pointer SP is read/write accessible in the I/O space.

The 128-byte data SRAM can be easily accessed through the five different addressing modes supported in the AVR architecture.

The memory spaces in the AVR architecture are all linear and regular memory maps.

A flexible interrupt module has its control registers in the I/O space with an additional global interrupt enable bit in the status register. All interrupts have a separate interrupt vector in the interrupt vector table at the beginning of the program memory. The interrupts have priority in accordance with their interrupt vector position; the lower the interrupt vector address, the higher the priority.

Figure 7. Memory Maps



General-purpose Register File

Figure 8 shows the structure of the 32 general-purpose working registers in the CPU.

Figure 8. AVR CPU General-purpose Working Registers

7 0	Addr.	
R0	$00	
R1	$01	
R2	$02	
…		
R13	$0D	
R14	$0E	
R15	$0F	
R16	$10	
R17	$11	
…		
R26	$1A	X-register low byte
R27	$1B	X-register high byte
R28	$1C	Y-register low byte
R29	$1D	Y-register high byte
R30	$1E	Z-register low byte
R31	$1F	Z-register high byte

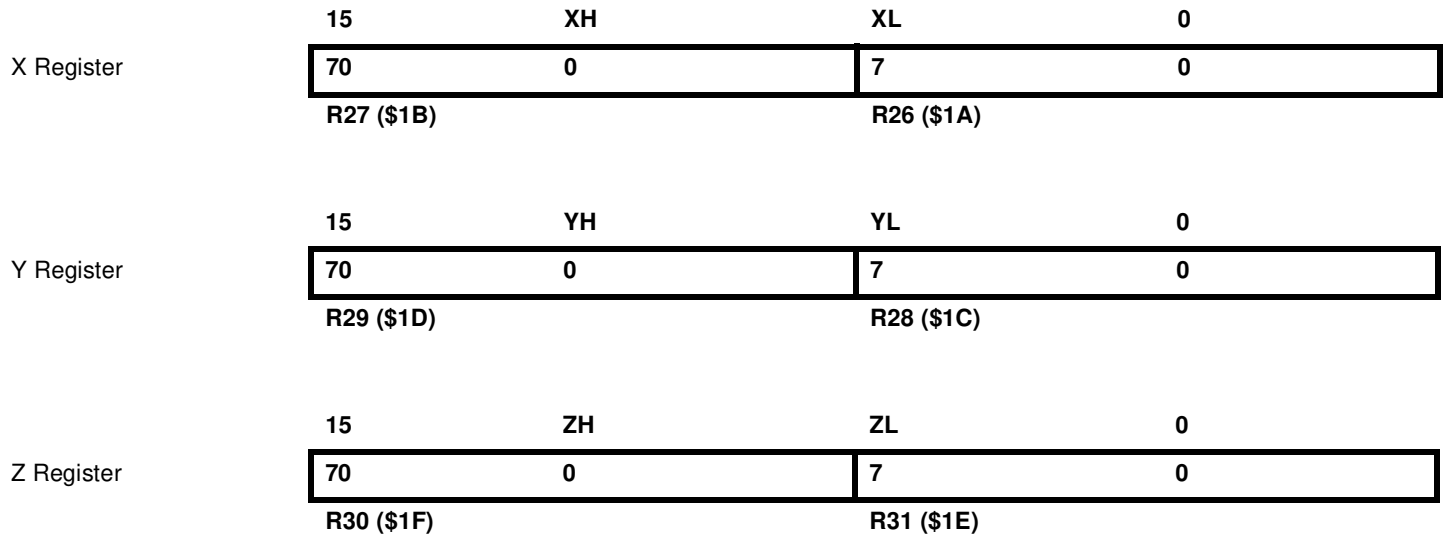
All the register operating instructions in the instruction set have direct and single cycle access to all registers. The only exception is the five constant arithmetic and logic instructions (SBCI, SUBI, CPI, ANDI and ORI) between a constant and a register, and the LDI instruction for load immediate constant data. These instructions apply to the second half of the registers in the register file, R16...R31. The general SBC, SUB, CP, AND and OR and all other operations between two registers or on a single register apply to the entire register file.

As shown in Figure 9, each register is also assigned a data memory address, mapping the registers directly into the first 32 locations of the user data space. Although not being physically implemented as SRAM locations, this memory organization provides great flexibility in access of the registers, as the X, Y and Z registers can be set to index any register in the file.

The X, Y and Z Registers

The registers R26...R31 have some added functions to their general-purpose usage. These registers are address pointers for indirect addressing of the data space. The three indirect address registers X, Y and Z are defined as shown in Figure 9.

Figure 9. The X, Y and Z Registers



In the different addressing modes, these address registers have functions as fixed displacement, automatic increment and decrement (see the descriptions for the different instructions).

Arithmetic Logic Unit (ALU)

The high-performance AVR ALU operates in direct connection with all the 32 general-purpose working registers. Within a single clock cycle, ALU operations between registers in the register file are executed. The ALU operations are divided into three main categories: arithmetic, logical and bit-functions. The multiplier is not present in this version of the core. Therefore, the MUL instruction is not supported.

In-system Self-programmable Flash Program Memory

The AT86RF401 contains 2 Kbytes of on-chip Flash memory for program storage. Since all instructions are 16- or 32-bit words, the Flash is organized as 1K x 16.

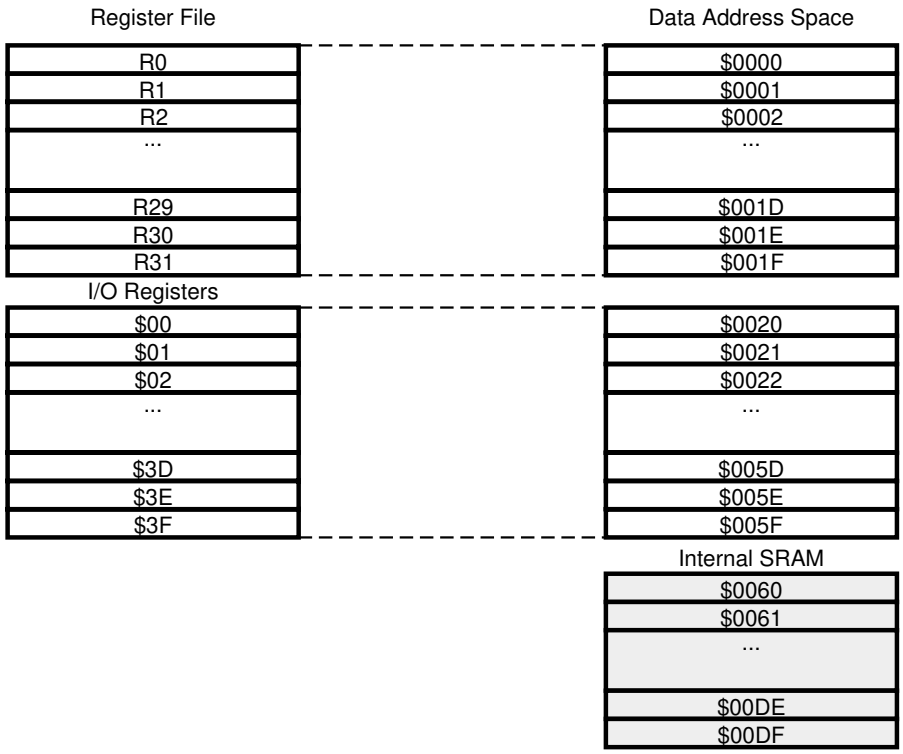
The Flash memory has an endurance of at least 1000 write/erase cycles. The PC is 10 bits wide, thus addressing the 1024 program memory locations. See the Memory Programming section (page 13) for a detailed description on Flash data serial downloading.

Constant tables can be allocated within the entire program memory address space (see Table 22, Instruction Set, page 45).

SRAM Data Memory

Figure 10 shows how the AT86RF401 SRAM memory is organized.

Figure 10. SRAM Organization



The lower 224 Data Memory locations address the Register File, the I/O Memory and the internal data SRAM. The first 96 locations address the Register File + I/O Memory, and the next 128 locations address the internal data SRAM.

The five different addressing modes for the data memory cover: Direct, Indirect with Displacement, Indirect, Indirect with Pre-decrement, and Indirect with Post-increment. In the register file, registers R26 to R31 feature the indirect addressing pointer registers.

The direct addressing reaches the entire data space.

The Indirect with Displacement mode features a 63 address locations reach from the base address given by the Y or Z register.

When using register indirect addressing modes with automatic pre-decrement and post-increment, the address registers X, Y and Z are decremented and incremented.

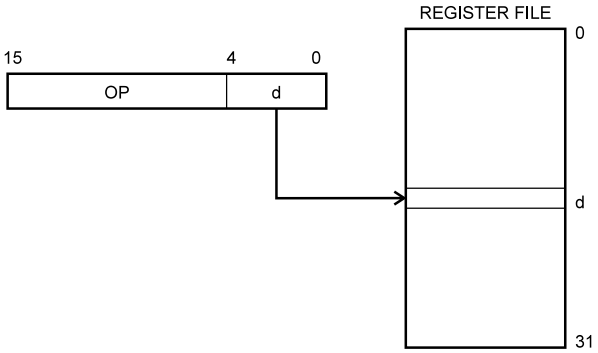
The 32 general-purpose working registers, 64 I/O registers and the 128 bytes of internal data SRAM in the AT86RF401 are all accessible through all these addressing modes.

Program and Data Addressing Modes

The AT86RF401 AVR Enhanced RISC microcontroller supports powerful and efficient addressing modes for access to the program memory (Flash) and data memory (SRAM, Register File and I/O Memory). This section describes the different addressing modes supported by the AVR architecture. In the figures, OP means the operation code part of the instruction word. To simplify, not all figures show the exact location of the addressing bits.

Register Direct, Single Register Rd

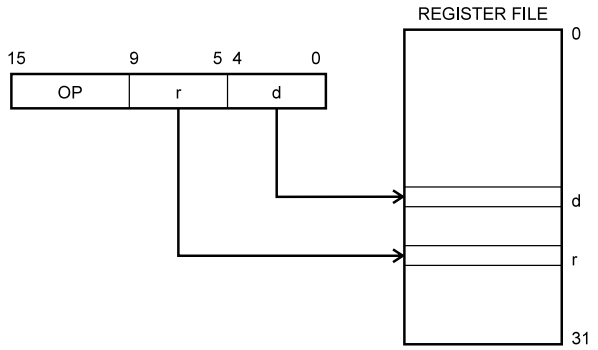
Figure 11. Direct Single Register Addressing



The operand is contained in register d (Rd).

Register Direct, Two Registers Rd and Rr

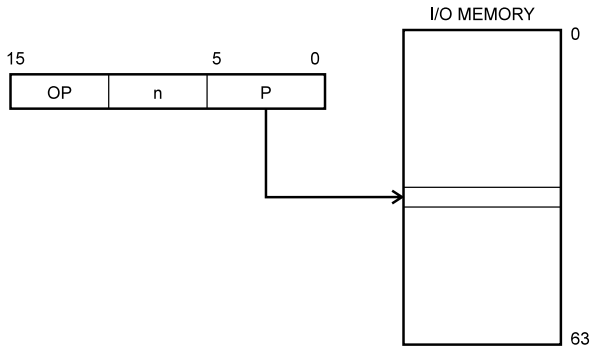
Figure 12. Direct Register Addressing, Two Registers



Operands are contained in register r (Rr) and d (Rd). The result is stored in register d (Rd).

I/O Direct

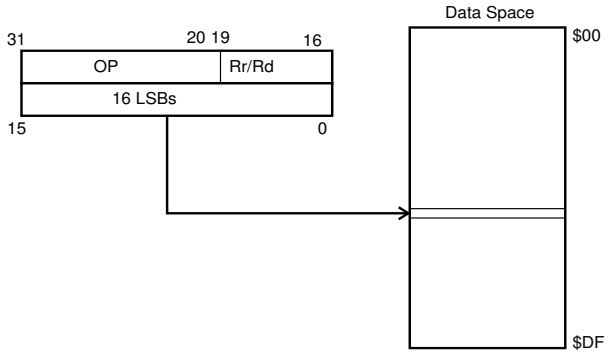
Figure 13. I/O Direct Addressing



Operand address is contained in 6 bits of the instruction word. “n” is the destination or source register address.

Data Direct

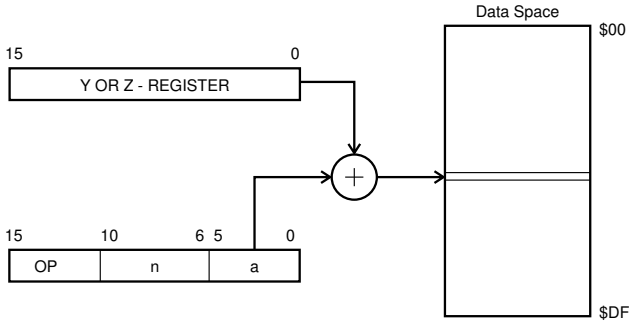
Figure 14. Direct Data Addressing



A 16-bit Data Address is contained in the 16 LSBs of a two-word instruction. Rd/Rr specify the destination or source register.

Data Indirect with Displacement

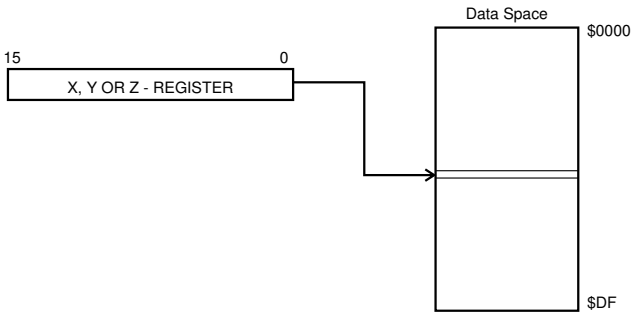
Figure 15. Data Indirect with Displacement



Operand address is the result of the Y or Z register contents added to the address contained in 6 bits of the instruction word.

Data Indirect

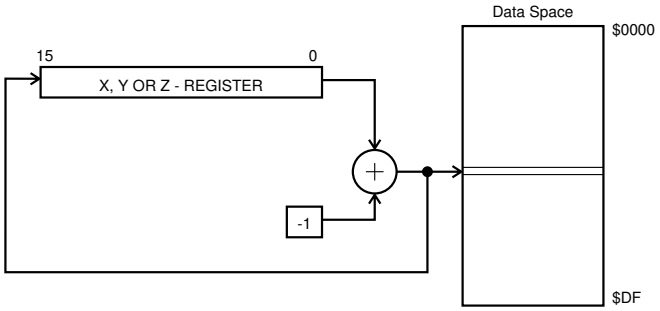
Figure 16. Data Indirect Addressing



Operand address is the contents of the X, Y or Z register.

Data Indirect with Pre-decrement

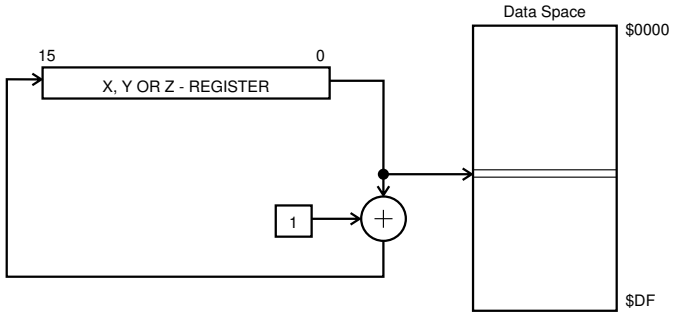
Figure 17. Data Indirect Addressing with Pre-decrement



The X, Y or Z register is decremented before the operation. Operand address is the decremented contents of the X, Y or Z register.

Data Indirect with Post-increment

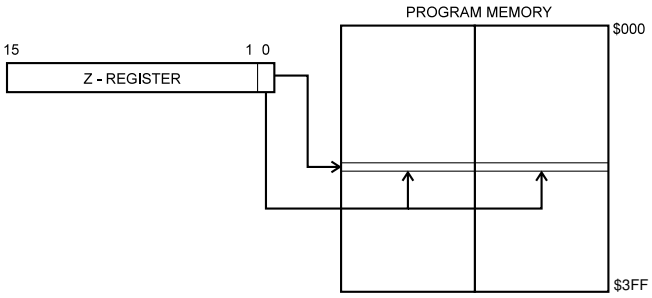
Figure 18. Data Indirect Addressing with Post-increment



The X, Y or Z register is incremented after the operation. Operand address is the content of the X, Y or Z register prior to incrementing.

Constant Addressing Using the LPM Instruction

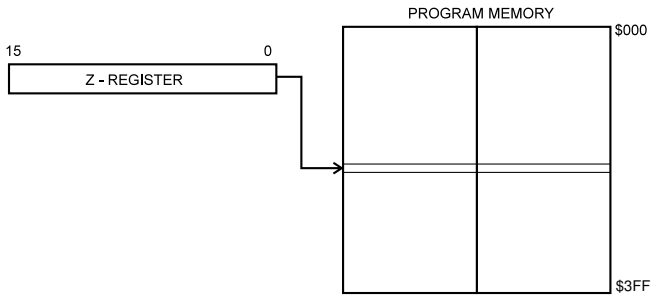
Figure 19. Code Memory Constant Addressing



Constant byte address is specified by the Z register contents. The 10 MSBs select word address (0–1K). For LPM, the LSB selects low byte if cleared (LSB = 0) or high byte if set (LSB = 1).

Indirect Program Addressing, IJMP and ICALL

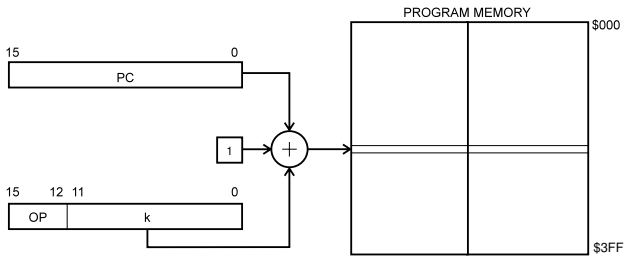
Figure 20. Indirect Program Memory Addressing



Program execution continues at address contained by the Z register (i.e., the PC is loaded with the contents of the Z register).

Relative Program Addressing, RJMP and RCALL

Figure 21. Relative Program Memory Addressing



Program execution continues at address PC + k + 1. The relative address k is from –2048 to 2047.