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Features

- **Compatible with all ISO/IEC 14443 Type B Compliant Cards, Tags, and Transponders**
- **High Performance 13.56 MHz RF Communications Interface**
  - **ISO/IEC 14443-2 Type B Compliant 106 Kbps Signaling**
  - **ISO/IEC 14443-3 Type B Compliant Frame and Data Format Internal Transmitter Drives Antenna with No External Active Circuitry**
  - **Robust Receiver Demodulates and Decodes Type B Signals**
- **Intelligent RF Reader Functions**
  - **ISO/IEC 14443-3 Type B Polling Function**
  - **Type B Frame Formatting and Decoding is Handled Internally**
  - **Internal CRC Generation and Error Detection**
  - **Adjustable Frame Wait Timing**
  - **Internal Data Buffer**
- **Two Serial Communication Interface Options**
  - **Two-Wire Interface (TWI) Slave Device with Clock Speed up to 1 MHz**
  - **SPI Mode 0 Slave Device with Clock Speed up to 2 MHz**
  - **SPI or TWI Mode Selection with Interface Mode Select Pin**
- **Compatible with 3.3 V and 5 V Microcontrollers**
  - **Supply Voltage: 3.0 to 3.6 Volts or 4.5 to 5.5 Volts**
- **Package: 6 by 6 mm QFN, Green compliant (exceeds RoHS)**
- **Industrial Operating Temperature: -40° to +85° C**

Description

The AT88RF1354 is a smart, high performance ISO/IEC 14443 Type B RF Reader IC. The AT88RF1354 communicates with RFID Transponders or Contactless Smartcards using the industry standard ISO/IEC 14443-2 Type B signal modulation scheme and ISO/IEC 14443-3 Type B frame format. Data is exchanged half duplex at a 106k bit per second rate. A two byte CRC_B provides communication error detection capability.

The AT88RF1354 is compatible with 3.3 V and 5 V host microcontrollers with two-wire or SPI serial interfaces. In two-wire interface mode the AT88RF1354 operates as a TWI slave and requires four microcontroller pins for data communication and handshaking. In SPI interface mode the AT88RF1354 operates as a mode 0 SPI slave and requires six microcontroller pins for data communication and handshaking.

To communicate with an RFID transponder the host microcontroller sends a data packet for transmission over the RF communications channel, and receives the response data packet that is received from the transponder over the RF communications channel. AT88RF1354 performs all RF communication packet formatting, decoding, and communication error checking. The host microcontroller is not burdened with RF encoding, timing, or protocol functions since these tasks are all performed by the AT88RF1354.

13.56 MHz Type B RF Reader Specification

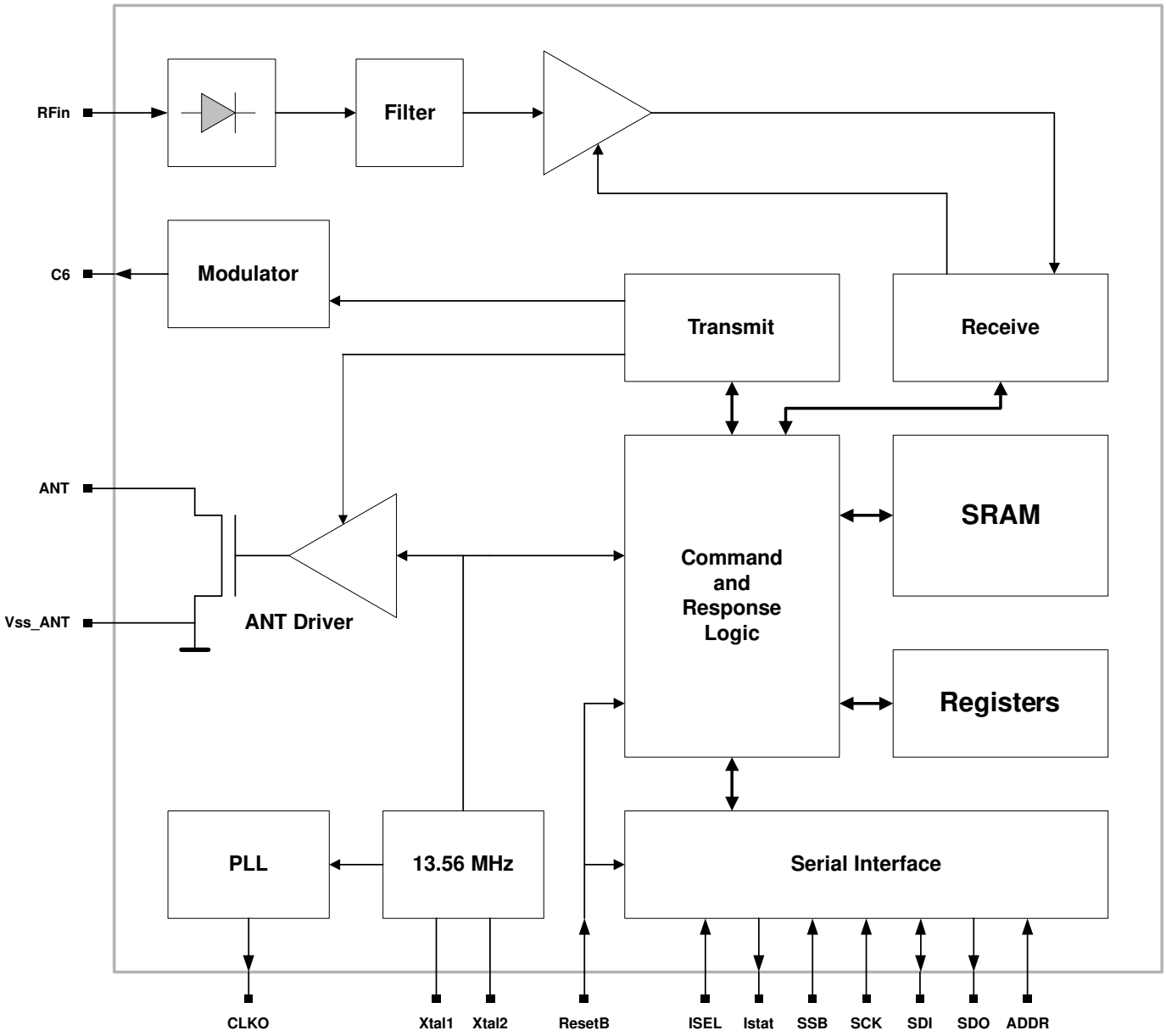
AT88RF1354

8547B–RFID–3/09

1. Introduction

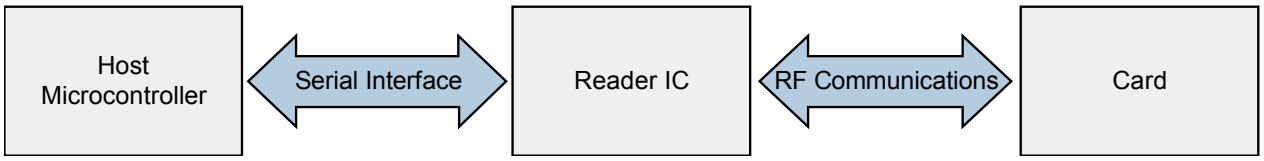
1.1. Block Diagram

Figure 1. Block Diagram



1.2. System Diagram

Figure 2. Communications in an RFID System



1.3. Scope

This AT88RF1354 Specification document contains the electrical and mechanical specifications for the AT88RF1354 RF Reader IC. The AT88RF1354 Command Reference Guide document contains detailed command and register specifications for the AT88RF1354 RF Reader. The AT88RF1354 Command Reference Guide is a reference for software developers and embedded systems programmers using the AT88RF1354 Reader.

Reference Designs and additional technical information is available in AT88RF1354 Application Notes. The reference designs described in the AT88RF1354 Application Notes include schematics, board designs, and a complete bill of materials. Each reference design has been optimized for reliable, robust communications with cards and tags with antenna dimensions within a specified size range. See www.atmel.com

1.4. Conventions

ISO/IEC 14443 nomenclature is used in this document where applicable. The following terms and abbreviations are utilized throughout this document. Additional terms are defined in the section in which they are used, or in 0.

Card: A Contactless Smart Card or RFID Tag in proximity to the reader antenna.

Host: The microcontroller connected to the serial interface of the reader IC.

PCD: Proximity Coupling Device – is the host and reader with antenna.

PICC: Proximity Integrated Circuit Card – is the tag/card containing an IC and antenna.

Reader: The AT88RF1354 IC with loop antenna and associated circuitry

RFU: Reserved for Future Use – is any feature, memory location, or bit that is held as reserved for future use by the ISO standards committee or by Atmel.

$ xx: Hexadecimal Number – denotes a hex number “xx” (Most Significant Bit on left).

xxxx b: Binary Number – denotes a binary number “xxxx” (Most Significant Bit on left).

See Atmel Application Note *Understanding the Requirements of ISO/IEC 14443 for Type B Proximity Contactless Identification Cards* (doc 2056x) at www.atmel.com for detailed information regarding the ISO/IEC 14443 RF communication protocol.

2. Instruction Set

Table 1. Instruction Set Sorted by Command Name

Command Name	Description	Code
Abort	Exit command in progress	$0D
Clear	Exit command in progress, Clear Buffer, Turn RF OFF	$0E
Poll Continuous	Poll Continuously for Type B PICCs	$02
Poll Single	Poll Once for Type B PICCs	$01
Read Buffer	Read Data Buffer	$08
Read Register	Read Configuration Register	$07
RF OFF	Turn off 13.56 MHz RF Field	$0B
RF ON	Turn on 13.56 MHz RF Field	$0A
Sleep	Activate standby mode	$0C
TX Data	Transmit data to PICC and receive the response	$03
Write Buffer	Write data buffer	$09
Write Register	Write configuration register	$06
All other command code values are not supported		

The *AT88RF1354 Command Reference Guide* document contains all of the detailed information required by a software developer or embedded systems programmer to use the AT88RF1354 Instruction Set. See www.atmel.com for the *AT88RF1354 Command Reference Guide* (doc 5150x).

2.1. RF Communication Commands

The RF ON Command and RF OFF Command are used to enable and disable the 13.56 MHz RF Field transmitter. The RF Field is turned on at the beginning of a transaction and off at the end, since ISO/IEC 14443 cards and tags are powered by the RF Field.

The Poll Continuous Command or Poll Single Command is used to search for ISO/IEC 14443 cards in the RF Field using the standard REQB/WUPB and Slot-MARKER commands. These commands automatically perform the time-slot polling function described in ISO/IEC 14443 part 3, and return the response from the first card found to the host microcontroller.

All other RF communication is performed with the TX Data Command. The RF command and data bytes to be transmitted are sent by the host microcontroller with the TX Data Command to AT88RF1354. The bytes received from the host are formatted into a Type B standard frame and transmitted on the RF communications channel, along with the CRC. When a response is received from the card, the response frame is decoded by AT88RF1354 and the resulting bytes are stored in SRAM buffer memory. If a CRC or frame format error is detected in the response, then bits are set in the Error Register (EREG). After the entire frame has been decoded by AT88RF1354, the host microcontroller reads the TX Data Response over the serial interface.

2.2. Reader Configuration Commands

The Read Register Command and Write Register Command are used to read and write the configuration and status registers of the AT88RF1354. Both the Transmitter Register (TXC) and Receiver Register (RXC) must be configured before any RF communication occurs.

The Sleep Command is used to put the AT88RF1354 into Standby Mode. In Standby Mode the internal circuitry is placed in standby, and all internal clocks are stopped.

2.3. Other Commands

The Abort Command can be used to interrupt a Poll Single, Poll Continuous, or TX Data operation that is in progress. If a Poll Continuous Command is sent but there is no card in the field, then an Abort Command is used to interrupt the infinite polling loop. All other commands will timeout if no response is received, so it is usually not necessary to use the Abort Command to interrupt them.

The Clear Command is used to clear the configuration registers and place AT88RF1354 in a known initial state. The Clear Command is usually the first command sent after the reader is powered on and reset.

The Read Buffer Command and Write Buffer Command can be used to read and write the SRAM buffer that is used to store RF commands and RF responses. These commands are never required to be used during normal operation of the AT88RF1354. However, these commands are helpful for testing the integrity of the serial communications channel during system development.

3. Register Summary

The *AT88RF1354 Command Reference Guide* document contains all of the detailed information required by a software developer or embedded systems programmer to use the AT88RF1354 Register Set. See www.atmel.com for the *AT88RF1354 Command Reference Guide* (doc 5150x).

Table 2. Register set sorted by address.

Register Name	Register Address	Description	Register Type
CPR0_L	$00	(Default) Communication Protocol Register 0 - Low Byte	Read-only
CPR0_H	$01	(Default) Communication Protocol Register 0 - High Byte	Read-only
CPR1_L	$02	Communication Protocol Register 1 - Low Byte [RFU]	Read / Write
CPR1_H	$03	Communication Protocol Register 1 - High Byte	Read / Write
CPR2_L	$04	Communication Protocol Register 2 - Low Byte [RFU]	Read / Write
CPR2_H	$05	Communication Protocol Register 2 - High Byte	Read / Write
CPR3_L	$06	Communication Protocol Register 3 - Low Byte [RFU]	Read / Write
CPR3_H	$07	Communication Protocol Register 3 - High Byte	Read / Write
CPR4_L	$08	Communication Protocol Register 4 - Low Byte [RFU]	Read / Write
CPR4_H	$09	Communication Protocol Register 4 - High Byte	Read / Write
SREG	$0A	Status Register	Read-only
EREG	$0B	Error Register	Read-only
IDR	$0C	Hardware ID Register	Read-only
PLL	$0D	PLL Output Configuration Register	Read / Write
TXC	$0E	Transmitter Register	Read / Write
RXC	$0F	Receiver Register	Read / Write
All other register address values are not supported			

The Register Memory Map in Table 3 shows the field names for each register bit. Read-only registers are colored yellow. Read/Write registers are colored green. Any bit identified as RFU or Reserved for Future Use is reserved for future definition by Atmel; these bits must always remain 0 b.

Table 3. Register Memory Map

Register Name	Register Address	Description							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CPR0_L	$00	*Reserved for future use*							
CPR0_H	$01	FWI				*RFU*			
CPR1_L	$02	*Reserved for future use*							
CPR1_H	$03	FWI				*RFU*			
CPR2_L	$04	*Reserved for future use*							
CPR2_H	$05	FWI				*RFU*			
CPR3_L	$06	*Reserved for future use*							
CPR3_H	$07	FWI				*RFU*			
CPR4_L	$08	*Reserved for future use*							
CPR4_H	$09	FWI				*RFU*			
SREG	$0A	RF	POR	CD	*RFU*				
EREG	$0B	CRC	FRAME	BYTE	TIME	COL	SPE	*RFU*	
IDR	$0C	ID							
PLL	$0D	SL!	SL0	ENB	*RFU*			RS1	RS0
TXC	$0E	TXP	ML						
RXC	$0F		G			SS			
All other register address values are not supported									

3.1. Communications Protocol Registers

AT88RF1354 contains five 16 bit Communication Protocol Registers for configuration of the RF communication protocol. Each register contains a high byte (CPRx_H) and a low byte (CPRx_L). The CPRx_H registers are used to configure the Frame Wait Time. The CPRx_L registers are currently unused (Reserved for Future Use) and must remain set to $00.

CPR0 is a read-only register containing the default ISO/IEC 14443 communication protocol settings. The Poll Single and Poll Continuous Commands always use CPR0 to configure the RF channel during polling.

CPR1, CPR2, CPR3, and CPR4 are available for configuration of RF channel for the TX Data Command. Each TX Data Command contains a field that selects the CPR register to be used, so frame wait time is independently configured on each command. If different timeout settings are written to each CPRx register, then the application developer can use an appropriate timeout for each TX Data Command sent, minimizing the time required to recover when no response is received on the RF communication channel.

3.2. Status Registers

AT88RF1354 contains three read-only registers that provide status information. The operational status of the IC is contained in the SREG Register; by reading this register it can be determined if the RF Field is on and if the analog circuits are fully powered up. The RF communication errors flags are stored in EREG; these flags are also returned in the response of RF communication commands.

The IDR Register contains the hardware ID revision of the die; all die manufactured with the same design contain identical IDR Register values. If the die design is changed, then IDR is updated.

3.3. Configuration Registers

Three registers control the configuration of the receiver, transmitter, and CLKO pin. The gain and noise immunity of the receiver is controlled by the RXC Register. The transmit power and modulation index are controlled by the TXC Register. The PLL Register controls the CLKO pin frequency, the CLKO output enable, and standby mode control bits.

4. Pin List

Pin	Name	Description	Type
1	V_{CC}_ANT	Power for Transmitter and Antenna Drive Circuits	Power
2	V_{SS}_ANT	Ground for Transmitter and Antenna Drive Circuits	Ground
3	ANT	Antenna Driver	Output
4	Xtal1	Crystal Pin 1	Xtal Buffer
5	Xtal2	Crystal Pin 2	
6	C5	Bypass Capacitance	Output
7	Test1	V_{SS} by Customer	TEST input
8	CLKO	Programmable Clock Output from PLL	Output
9	ResetB	Reset Bar from Microcontroller	Input
10	ISEL	Select Serial Interface Mode (SPI or TWI)	Input
11	TestD	No Connect by customer	I/O
12	Istat	Serial Interface Status (Handshaking Signal)	Output
13	SSB	SPI Interface "Slave Select"	Input
14	SCK	Serial Data Clock (SPI and TWI)	Input
15	SDI	SPI Serial Data Input or TWI Serial Data Input/Output	I/O
16	Test2	V_{SS} by Customer	TEST input
17	Test3	V_{SS} by Customer	TEST input
18	N.C.	Not Used	
19	SDO	SPI Serial Data Output	Output
20	ADDR	TWI Device Address Select	Input
21	C1	Bypass Capacitance	Output
22	V_{SS}	Ground	Power
23	V_{SS}A	Ground	Power
24	V_{CC}	Power for I/O Buffers, digital and analog circuits	Power
25	C4	Bypass Capacitance	Output
26	C2	Bypass Capacitance	Output
27	C3	Bypass Capacitance	Output
28	N.C.	Not used	
29	C7	Bypass Capacitance	Output
30	N.C.	Not used	
31	TestR	No Connect by customer	Analog Out
32	RFin	Input to RF receiver	Input
33	N.C.	Not used	
34	Rmod	V_{SS} _ANT by customer	Analog TEST
35	C6	Bypass Capacitance	Output
36	N.C.	Not used	

4.1. Power and Ground Pin Descriptions

4.1.1. V_{CC} [24]

Supply Voltage for I/O buffers, digital, and analog circuits. V_{CC} voltage must match the microcontroller I/O voltage since all digital I/O levels are referenced to V_{CC}

Two V_{CC} bypass capacitors must be connected between the V_{CC} pin and V_{SS}. A 15 nF capacitor with SRF of 32 MHz must be placed within 3 mm of the package. A 2.2 uF capacitor should also be placed within 3 cm of the package. Ceramic capacitors with X5R or X7R dielectric and a working voltage of 10 volts minimum should be used.

4.1.2. V_{SS} [22]

Digital ground. Ground for I/O buffers and digital circuits. For maximum performance the digital ground plane must be separated from the analog ground plane (V_{SS}A) and the antenna ground plane (V_{SS}_ANT) by a minimum of 20 mils.

4.1.3. V_{SS}A [23]

Analog ground. Ground for analog circuits. For maximum performance the V_{SS}A ground plane should connect to the V_{SS} ground plane at only a single point within 1 cm of pins 22 and 23. V_{SS}A should not be connected directly to V_{SS}_ANT.

4.1.4. V_{CC}_ANT [1]

Antenna supply voltage. Powers the transmitter and antenna drive circuits.

Two V_{CC}_ANT bypass capacitors must be connected between the V_{CC}_ANT pin and V_{SS}_ANT. A 15 nF capacitor with SRF of 32 MHz must be placed within 3 mm of the package and a 2.2 uF capacitor must be placed within 5 mm of the package. Ceramic capacitors with X5R or X7R dielectric and a working voltage of 10 volts minimum should be used.

4.1.5. V_{SS}_ANT [2]

Antenna ground. High current return path for transmitter and antenna drive circuit current. For maximum performance the V_{SS}_ANT ground plane should connect to V_{SS} at only a single point near the power filters at the edge of the reader circuit block.

4.1.6. QFN Package Thermal Pad [ePad]

Ground for the die substrate. Must be connected directly to the V_{SS} digital ground plane with multiple vias. The package thermal pad must be soldered to a thermal pad on the board as described in Appendix D to dissipate heat generated in the die.

***Warning**: If V_{SS}, V_{SS}A, V_{SS}_ANT, and ePad are tied to a single monolithic ground plane, then transmitter noise will be injected into the receiver circuit. Likewise, if V_{CC} and V_{CC}_ANT are tied to one monolithic power plane, then transmitter noise will be injected into the receiver circuit. These PCB configurations will significantly reduce the communication performance of the reader (reducing the communication distance).*

4.2. Digital Pin Descriptions

4.2.1. ADDR [20]

TWI device address select input pin. Selects between two TWI device addresses as shown in Table 4. In SPI communication mode this pin should be connected to Vss.

Table 4. TWI Device Address

ADDR Pin	TWI Device Address							TWI_R	TWI_W
	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
V_{SS}	0	1	0	1	0	0	0	$51	$50
V_{CC}	1	1	0	1	0	1	0	$D5	$D4
All other values are NOT supported									

4.2.2. CLKO [8]

Clock Out pin. The PLL register selects the frequency of the clock which is output on this pin for use by external circuits. The default CLKO frequency is 1.978 MHz. If the clock is not needed, then the CLKO output should be disabled by programming the ENB bit of the PLL register to one.

Table 5. CLKO Output Frequency Options

Bit 1	Bit 0	CLKo Frequency
0	0	1.978 MHz
0	1	3.955 MHz
1	0	7.910 MHz
1	1	15.82 MHz

4.2.3. ISEL [10]

Interface Select input pin. Selects TWI communications when low. SPI communication mode 0 is selected when high. See Appendix A and Appendix B for more details.

4.2.4. Istat [12]

Interface Status output pin. Istat is the serial interface handshaking signal. A high level on Istat indicates that a byte of data is ready to read from the serial interface port. A low level on Istat indicates that the serial interface buffer is empty.

***Note**: Use of Istat for serial communications control is mandatory, and the AT88RF1354 will not accept commands from the host microcontroller when Istat is high.*

4.2.5. ResetB [9]

Reset Bar input pin. A low on ResetB causes the device to reset. ResetB must be pulled high by the host microcontroller and/or by an external resistor to V_{CC} when the device is in use.

4.2.6. SCK [14]

Serial Clock input pin. In both SPI and TWI serial communication modes this pin is used as the serial interface clock.

4.2.7. SDI [15]

Serial Data In pin. In SPI communication mode this pin functions as the serial data input. In TWI communication mode this pin functions as the serial data I/O.

4.2.8. SDO [19]

Serial Data Out pin. In SPI communication mode this pin functions as the serial data output. In TWI communication mode this pin is not used.

4.2.9. SSB [13]

SPI Slave Select Bar input pin. In SPI communication mode this pin functions as the slave select input. In TWI communication mode this pin is not used and should be connected to V_{SS}.

4.3. RF Pin Descriptions

4.3.1. ANT [3]

Antenna driver. The 13.56 MHz carrier frequency is generated by ANT and is shaped into a sine wave by external passive circuitry.

4.3.2. C6 [35]

C6 Antenna bypass capacitor pin. The C6 pin provides power to the antenna circuits and modulates the power level for communications.

4.3.3. RFin [32]

RF input pin. RFin is the input to the receiver. A resistor/capacitor filter is used to limit the peak to peak voltage on this pin to a safe level. See the AT88RF1354 reference design for appropriate component values.

4.4. Analog Pin Descriptions

4.4.1. C1 [21]

C1 bypass capacitor pin. Bypass capacitance of 0.33 uF for the digital circuits must be connected between the C1 pin and V_{SS}. This capacitor must be placed within 3 mm of the package. Any 0.33 uF ceramic capacitor with X5R or X7R dielectric and a working voltage of 10 volts minimum may be used.

4.4.2. C2 [26]

C2 bypass capacitor pin. Bypass capacitance of 47 nF for the analog circuits must be connected between the C2 pin and $V_{SS}A$. This capacitor must be placed within 3 mm of the package. Any 47 nF ceramic capacitor with X5R or X7R dielectric and a working voltage of 10 volts minimum may be used.

4.4.3. C3 [27]

C3 bypass capacitor pin. Bypass capacitance of 47 nF for the analog circuits must be connected between the C3 pin and $V_{SS}A$. This capacitor must be placed within 3 mm of the package. Any 47 nF ceramic capacitor with X5R or X7R dielectric and a working voltage of 10 volts minimum may be used.

4.4.4. C4 [25]

C4 bypass capacitor pin. Bypass capacitance of 0.33 uF for the analog circuits must be connected between the C4 pin and $V_{SS}A$. This capacitor must be placed within 3 mm of the package. Any 0.33 uF ceramic capacitor with X5R or X7R dielectric and a working voltage of 10 volts minimum may be used.

4.4.5. C5 [6]

C5 bypass capacitor pin. Bypass capacitance of 0.33 uF for the digital circuits must be connected between the C5 pin and V_{SS}. This capacitor must be placed within 3 mm of the package. Any 0.33 uF ceramic capacitor with X5R or X7R dielectric and a working voltage of 10 volts minimum may be used.

4.4.6. C7 [29]

C7 bypass capacitor pin. Bypass capacitance of 47 nF for the analog circuits must be connected between the C7 pin and $V_{SS}A$. This capacitor must be placed within 3 mm of the package. Any 47 nF ceramic capacitor with X5R or X7R dielectric and a working voltage of 10 volts minimum may be used.

4.4.7. Xtal1 [4]

Crystal pin 1. A 13.56 MHz crystal must be connected between Xtal1 and Xtal2.

4.4.8. Xtal2 [5]

Crystal pin 2. A 13.56 MHz crystal must be connected between Xtal1 and Xtal2.

4.5. Test Pin Descriptions

4.5.1. Test1 [7]

Test input pin 1. This pin must be connected to V_{SS} on the board to prevent the IC from entering test mode.

4.5.2. Test2 [16]

Test input pin 2. This pin must be connected to V_{SS} on the board to prevent the IC from entering test mode.

4.5.3. Test3 [17]

Test input pin 3. This pin must be connected to V_{SS} on the board to prevent the IC from entering test mode.

4.5.4. TestD [11]

Test output pin D. This test output must be left open by the user.

4.5.5. TestR [31]

Test output pin R. This test output must be left open by the user.

4.5.6. Rmod [34]

Test pin Rmod. This pin must be connected to V_{SS} _Ant on the board.

4.6. Other Pins

4.6.1. N.C. [18, 28, 30, 33, 36]

No Connect pins. These package pins are not used and can be left open by the user.

5. Typical Application

5.1. Operating Principle

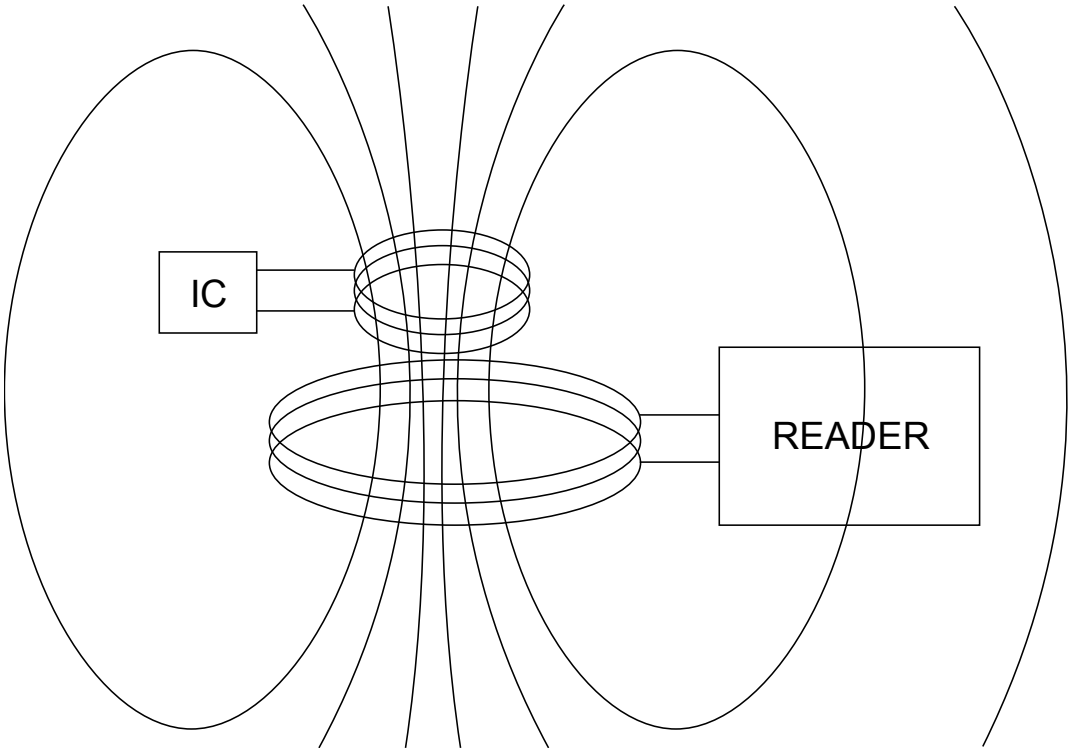
Contactless RF smart cards operating at 13.56 Mhz are powered by and communicate with the reader via inductive coupling of the reader antenna to the card antenna. The two loop antennas effectively form a transformer.

An alternating magnetic field is produced by sinusoidal current flowing thru the reader antenna loop. When the card enters the alternating magnetic field, an alternating current (AC) is induced in the card loop antenna. The PICC integrated circuit contains a rectifier and power regulator to convert the AC to direct current (DC) to power the integrated circuit.

The reader amplitude modulates the RF field to send information to the card. The PICC contains a demodulator to convert the amplitude modulation to digital signals. The data from the reader is clocked in, decoded and processed by the integrated circuit.

The card communicates with the reader by modulating the load on the card antenna, which also modulates the load on the reader antenna. ISO/IEC 14443 PICCs use a 847.5 khz subcarrier for load modulation, which allows the reader to filter the subcarrier frequency off of the reader antenna and decode the data.

Figure 3. The card antenna and reader antenna effectively form a transformer



5.2. Application

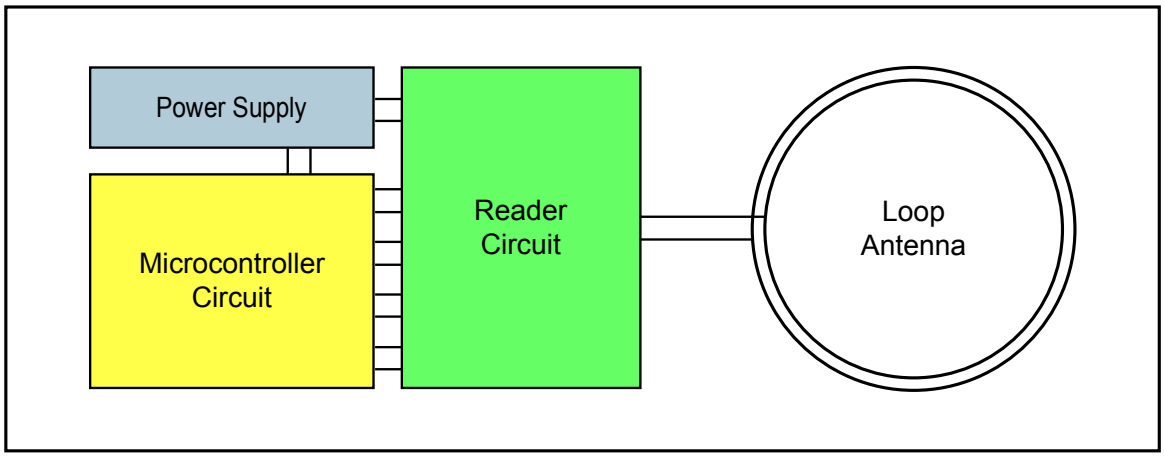
In a typical application the AT88RF1354 reader circuitry and the loop antenna are integrated on a single four layer printed circuit board. The host microcontroller and power supply may reside on the same PCB, or on a separate PCB depending on the application requirements.

The passive components required for the reader IC to function are placed in a small area immediately surrounding the QFN package for optimum RF circuit performance. The PCB loop antenna is placed a minimum of 1 inch away from all other metal, including the reader circuit ground and power planes, to minimize distortion of the magnetic field which reduces RF communication performance. A typical loop antenna is designed for an inductance of 800 to 1600 nanohenries, DC resistance of 0.1 to 0.3 ohms, low parasitic capacitance, and includes a matching electric field shield.

Whether the power supply and microcontroller are integrated in the same board or are on a different board, power filtering is included at the edge of the reader circuit ground and power planes to isolate the reader from in-band system noise and to protect the host microcontroller from reader generated noise. The reader ground and power planes must be isolated from the balance of the system to prevent current loops from forming which will interfere with RF tag performance.

Layout of both the reader circuitry and loop antenna are critical, and are beyond the scope of this document. See the reference designs in the *AT88RF1354 Application Notes* for layout and circuit recommendations.

Figure 4. Typical AT88RF1354 Reader board layout



6. Electrical Characteristics

6.1. Absolute Maximum Ratings*

Operating Temperature (case temp)	−40°C to +85°C
Storage Temperature (case temp)	−65°C to + 150°C
Power Dissipation	2 Watts
Maximum Operating Voltage (V_{CC})	6.0 Volts
Maximum Operating Voltage (V_{CC} _ANT)	6.0 Volts
DC Current: V_{CC} Pin	100 mA
DC Current: V_{CC} _ANT Pin	300 mA
HBM ESD	2000 V minimum

***Notice**: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Warning: This product package includes an integrated (exposed thermal pad) heatsink that must be soldered to the printed circuit board; failure to adequately heatsink this product will affect device reliability.

6.2. DC Characteristics

6.2.1. Operating Voltage

T_C = -40° to +85° C (unless otherwise noted)

Symbol	Parameter	Condition	Min	Nominal	Max	Units
V_{CC}	Supply voltage	5 Volt Digital interface	4.5	5.0	5.5	V
		3.3 Volt Digital Interface	3.0	3.3	3.6	V
V_{CC}_ANT	Supply voltage, antenna driver	High Output Power	4.5	5.0	5.5	V
		Low Output Power	3.0	3.3	3.6	V

***Note**:*

1. *Power is required to be applied to both V_{CC} and V_{CC}_ANT within the specified operating voltage ranges. If power is not applied to both the V_{CC} pin and the V_{CC}_ANT pin the device will be permanently damaged.*
2. *V_{CC} and V_{CC}_ANT are not required to be set to the same voltage.*
3. *V_{SS}, V_{SS}A, V_{SS} _ANT, and the ePad must all be externally connected to ground or the device will be permanently damaged.*
4. *AT88RF1354 does not support hot swapping or hot plugging. Connecting or disconnecting this device to a system while power is energized can cause permanent damage to AT88RF1354.*

6.2.2. Digital I/O Characteristics

T_C = -40° to +85° C (unless otherwise noted)(1)

Symbol	Parameter	Condition	V_{CC} = 3.0 to 3.6 V			V_{CC} = 4.5 to 5.5 V			Units
			Min	Typical	Max	Min	Typical	Max	
V_{IL}	Input Low Voltage		-0.5		$0.3V_{CC}$	-0.5		$0.3V_{CC}$	V
V_{IH}	Input High Voltage		$0.7V_{CC}$		V_{CC} +0.5	$0.7V_{CC}$		V_{CC} +0.5	V
V_{OL1}	Output Low Voltage (SDI pin TWI mode only)	V_{CC} = max I_{OL} = 3 mA	0		0.4	0		0.4	V
R_{SDA}	I/O pin Pull-up Resistor (2) (3)	TWI mode, SCK = 100kHz	1.0		4.0	1.7		8.0	kOhm
		TWI mode, SCK = 1 MHz	1.0		2.0	1.7		3.3	kOhm
R_{RST}	ResetB Pull-up Resistor (3)			10			10		kOhm
R_{PU}	Input Pull-up Resistor (3)	Unused input pin		10			10		kOhm
R_{PD}	Input Pull-down Resistor (3)	Unused input pin	0			0			kOhm

Note: *1. Typical values at 25° C. Maximum values are characterized values and not test limits in production.*
2. Optimum pull-up resistance is dependent on the total capacitance of the TWI serial interface bus.
3. This parameter is not tested. Values are based on characterization and/or simulation data.

6.3. AC Characteristics

6.3.1. System and Reset Timing

T_C = -40° to +85° C (unless otherwise noted)(1)

Symbol	Parameter	Condition	V_{CC} = 3.0 to 3.6 V			V_{CC} = 4.5 to 5.5 V			Units
			Min	Typical	Max	Min	Typical	Max	
f_{SCK}	Serial Interface Clock Frequency	TWI mode			1.0			1.0	MHz
		SPI mode			2.0			2.0	MHz
t_{RST}	Minimum pulse width on ResetB Pin		500			500			uS
t_{OSC}	Crystal Oscillator start-up time (3)	At power-up		1000			1000		uS
t_{RF_ON}	RF Enable time (2) (3)	From end of command to RF 90% power		4.5			1.8		uS
t_{RF_OFF}	RF Disable time (2) (3)	From end of command to RF 10% power		1.7			1.7		uS

Note: *1. Typical values at 25° C. Maximum values are characterized values and not test limits in production.*
2. RF performance is dependent on the reader circuit design, PCB layout, and component specifications. RF timing values in table are measured on an Atmel reference design.
3. This parameter is not tested. Values are based on characterization and/or simulation data.

6.3.2. TWI Mode Timing

T_C = -40° to +85° C V_{CC} = 3.0 to 3.6 V or 4.5 to 5.5 V (unless otherwise noted)[1]

Symbol	Parameter	Condition	100 kHz Operation			1 MHz Operation			Units
			Min	Typical	Max	Min	Typical	Max	
t_{HIGH}	SCK High pulse width		4.0			0.4			uS
t_{LOW}	SCK Low pulse width		4.7			0.5			uS
$t_{SU;DAT}$	Setup time, Data		250			25			nS
$t_{HD;DAT}$	Hold time, Data		300			30			nS
$t_{SU;STA}$	Setup time, Start condition		1000			100			nS
$t_{HD;STA}$	Hold time, Start condition		1000			100			nS
$t_{SU;STO}$	Setup time, Stop Condition		1000			100			nS
t_r	Rise Time of SCK and SDA [4]				1000			100	nS
t_f	Fall time of SCK and SDA [4]				300			30	nS
C_b	Bus Capacitance for each bus line [4]				400			100	pF

Note: 1. *Typical values at 25° C. Maximum values are characterized values and not test limits in production.*
2. *Production test is performed with 50% duty cycle clock at 1 MHz.*
3. *Timing limits for clock frequencies less than 1 MHz are scaled with the clock frequency.*
4. *This parameter is not tested. Values are based on characterization and/or simulation data.*

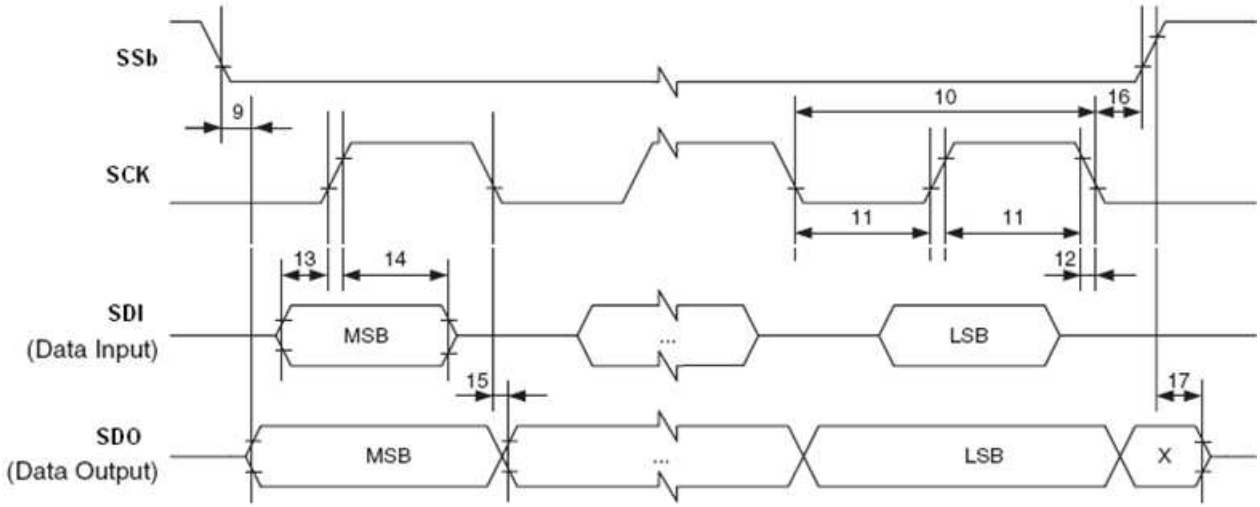
6.3.3. SPI Mode Timing

T_C = -40° to +85° C (unless otherwise noted)[1]

Symbol	Parameter	Condition	V_{CC} = 3.0 to 3.6 V			V_{CC} = 4.5 to 5.5 V			Units
			Min	Typical	Max	Min	Typical	Max	
t_{HIGH}	SCK High pulse width	See 11 in Figure 5.	200			200			nS
t_{LOW}	SCK Low pulse width	See 11 in Figure 5	200			200			nS
t_{SETUP}	MOSI (SDI) Setup to SCK High	See 13 in Figure 5	10			20			nS
t_{HOLD}	MOSI (SDI) Hold after SCK High	See 14 in Figure 5	100			100			nS
t_{VALID}	SCK Low to MISO (SDO) Valid	See 15 in Figure 5		15			15		nS
t_{SSBW}	SCK Low to SSB High [3]	See 16 in Figure 5	20			20			nS
t_{SSBO}	SSB Low to MISO (SDO) Out	See 9 in Figure 5		15			15		nS
t_r	Rise time of all signals [3]	See 12 in Figure 5			1600			1600	nS
t_f	Fall time of all signals [3]	See 12 in Figure 5			1600			1600	nS
t_{TRIO}	SSB High to MISO (SDO) Tristate	See 17 in Figure 5		10			10		nS

Note: 1. *Typical values at 25° C. Maximum values are characterized values and not test limits in production.*
2. *Production test is performed with 50% duty cycle clock at 1 MHz.*
3. *This parameter is not tested. Values are based on characterization and/or simulation data.*

Figure 5. SPI Interface timing requirements



6.3.4. CLKO Output Timing

T_C = -40° to +85° C (unless otherwise noted)[1]

Symbol	Parameter	Condition	V_{CC} = 3.0 to 3.6 V			V_{CC} = 4.5 to 5.5 V			Units
			Min	Typical	Max	Min	Typical	Max	
f_{CLKO}	CLKO Output Frequency [2]	PLL Reg RS1 = 0 b RS2 = 0 b		1.978			1.978		MHz
		PLL Reg RS1 = 0 b RS2 = 1 b		3.955			3.955		MHz
		PLL Reg RS1 = 1 b RS2 = 0 b		7.910			7.910		MHz
		PLL Reg RS1 = 1 b RS2 = 1 b		15.820			15.820		MHz
	CLKO Duty Cycle			50.0			50.0		%

Note: 1. *Typical values at 25° C. Values are based on characterization and are not tested.*
2. *Operating Frequency is dependent on the reader circuit design, PCB layout, and component specifications. An Atmel reference design with 13.560 MHz 50 ppm crystal was used to characterize this parameter.*

7. Typical Characteristics

The performance of AT88RF1354 is dependent on the reader circuit, the loop antenna design, the board layout, the specifications of the passive components, the quality of the supply voltages, the quality of the ground, the electrical noise in the system, and how the reader circuit is connected to the other system components. The specifications that are affected by these factors are included in this section as typical characteristics since they cannot be guaranteed in all situations.

It is recommended that AT88RF1354 be used exactly as described in the reference designs in the *AT88RF1354 Application Notes*. Each reference design has been optimized for reliable, robust communications with cards and tags with antenna dimensions within a specified size range. The reference designs described in the *AT88RF1354 Application Notes* include schematics, board designs, and a complete bill of materials. Gerber files of the PCB layout are available.

Atmel does not provide applications engineering support for customer implementations that deviate from the reference designs; it is strongly recommended that the AT88RF1354 reference designs be implemented exactly as provided. Any modification to the board layout or deviation from the bill of materials will impact both electrical performance and radiated emissions.

7.1. Supply Current

T_C = -40° to +85° C (unless otherwise noted)[1]

Symbol	Parameter	Condition	V_{CC} and V_{CC_ANT} = 3.0 to 3.6 V			V_{CC} and V_{CC_ANT} = 4.5 to 5.5 V			Units
			Min	Typical	Max	Min	Typical	Max	
ICC	Power Supply Current	Idle, No SCK clock, CLKO Disabled		10			15		mA
ICC_ANT	Power Supply Current	Idle, RF Disabled		1			2		mA
		Idle, RF Enabled (TXP = 1 b)		200			250		mA

Note:
1. *Typical values at Tc = 35° C. Values are based on characterization and are not tested.*
2. *The total D.C. supply current is ICC + ICC_ANT*
3. *Supply current is dependent on the reader circuit design, PCB layout, and component specifications. All values in table measured on an Atmel reference design.*
4. *ICC_ANT current increases rapidly when the RF ON Command is sent. The rate of ICC_ANT current change is the slew rate.*

7.2. Standby Current

T_C = -40° to +85° C (unless otherwise noted)[1]

Symbol	Parameter	Condition	V_{CC} and V_{CC_ANT} = 3.0 to 3.6 V			V_{CC} and V_{CC_ANT} = 4.5 to 5.5 V			Units
			Min	Typical	Max	Min	Typical	Max	
ISB	Power Supply Standby Current	Standby, CLKO Disabled, OSC and PLL Enabled		10			15		mA
ISB_ANT	Power Supply Standby Current	Standby, CLKO Enabled, OSC and PLL Enabled		2			3		mA
		Standby, CLKO Disabled, OSC and PLL Enabled		1			2		mA

Note:
1. *Typical values at Tc = 35° C. Values are based on characterization and are not tested.*
2. *Total power supply standby current is ISB + ISB_ANT*
3. *The Sleep Command is sent to enter standby mode. All serial interface signals must remain unchanged to remain in standby mode.*
4. *PLL Register bits control standby mode options: ENB controls CLKO, SL1 controls PLL, SL2 controls OSC (crystal oscillator)*
5. *Supply current is dependent on the reader circuit design, PCB layout, and component specifications. All values in table measured on an Atmel reference design.*

7.3. RF Characteristics

7.3.1. Transmitter Characteristics

Tc = -40° to +85° C (unless otherwise noted)[1]

Symbol	Parameter	Condition	Min	Typical	Max	Units	ISO / IEC Standard
fc	Carrier Frequency [3]	RF Enabled	13.553	13.560	13.567	MHz	14443-2 6.1
M.I.	Field Modulation Index[4]	RF Enabled, Transmitting Data	8	11	14	percent	14443-2 9.1.2
ETU	Elementary Time Unit	RF Enabled, Transmitting Data	9.4346	9.4395	9.4444	uS	14443-2 9.1.1
EGT	Extra Guard Time	RF Enabled, Transmitting Data	0	0	0	uS	14443-3 7.1.2

Note:
1. *Typical values at Tc = 35° C. Values are based on characterization and are not tested.*
2. *Performance is dependent on the reader circuit design, PCB layout, and component specifications. All values in table measured on an Atmel reference design.*
3. *Operating Frequency is dependent on the reader circuit design, PCB layout, and component specifications. An Atmel reference design with 13.560 MHz 50 ppm crystal was used to characterize this parameter.*
4. *Modulation Index is determined by the ML bit setting in the TXC register.*
5. *Unmodulated Magnetic Field strength is different for each reader antenna and reader board design. See AT88RF1354 Application Notes.*

7.3.2. Receiver Characteristics

T_C = -40° to +85° C (unless otherwise noted)[1]

Symbol	Parameter	Condition	Min	Typical	Max	Units	ISO / IEC Standard
ETU	Elementary Time Unit	RF Enabled, Receiving Data	9.4346	9.4395	9.4444	uS	14443-2 9.1.1
EGT	Extra Guard Time	RF Enabled, Receiving Data	0.0		19.0	uS	14443-3 7.1.2
BW	Receiver Bandwidth			1.0		MHz	

Note:
1. *Typical values at Tc = 35° C. Values are based on characterization and are not tested.*
2. *Performance is dependent on the reader circuit design, PCB layout, and component specifications.*

All values in table measured on an Atmel reference design.

8. Mechanical

8.1. Thermal Characteristics

The AT88RF1354 QFN package thermal characteristics were modeled and characterized by Amkor with JEDEC standard methods using a multilayer JEDEC test board with nine thermal vias on the PCB thermal pad. ψ_{JB} is 12.1 °C/W and θ_{JA} is 30.9 °C/W for this package.

Since ψ_{JB} measures the heat transfer between the QFN package and the PC board, it is more relevant than θ_{JA}. θ_{JA} measures heat transfer between the QFN and stagnant air.

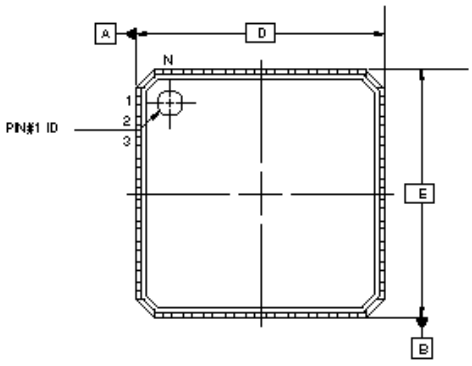
8.2. Moisture Sensitivity

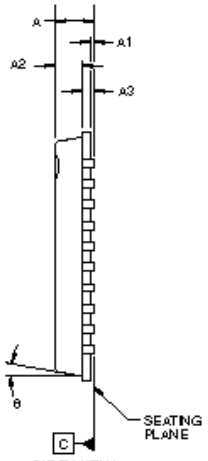
The AT88RF1354 QFN package is qualified to JEDEC MSL3.

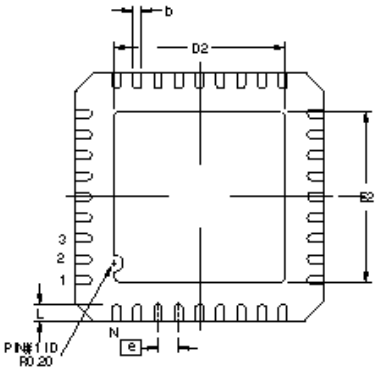
8.3. Composition

The AT88RF1354 QFN package is a lead-free and halogen-free green package.

8.4. Package Drawing







COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
D		6.00 BSC		
E		6.00 BSC		
D2	3.60	3.70	3.80	
E2	3.60	3.70	3.80	
A	-	0.85	0.90	
A1	0.0	0.01	0.05	
A2	-	0.65	0.70	
A3		0.20 REF		
L	0.50	0.60	0.75	
e		0.50 BSC		
b	0.18	0.23	0.30	2

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-220, Variation WJJD-1, for proper dimensions, tolerances, datums, etc.
2. Dimension b applies to metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension should not be measured in that radius area.

8/12/08

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	**36ML1, 36-lead 6.0 x 6.0 mm Body, 0.50 mm** pitch, Molded Quad Flat No Lead Package (QFN) Punched	ZEA	36ML1	A

9. Ordering Information

AT88RF1354 is available in the 6 mm by 6 mm 36 pin QFN package only. Standard delivery format is bulk, in trays. Tape & reel is also available.

Ordering Code	Package	Temperature Range
AT88RF1354-ZU	36 pin QFN thermal package, 6 x 6 mm, Green (exceeds RoHS), in Trays	Industrial (-40° C to 85° C)
AT88RF1354-ZU-T	36 pin QFN thermal package, 6 x 6 mm, Green (exceeds RoHS), Tape & Reel	Industrial (-40° C to 85° C)

9.1. Sample Ordering Information

AT88RF1354 samples are available in the 6 mm by 6 mm 36 pin QFN package.

Ordering Code	Package	Temperature Range
AT88RF1354-ZU	36 pin QFN thermal package, 6 x 6 mm, Green (exceeds RoHS)	Industrial (-40° C to 85° C)

Appendix A. The ISO/IEC 14443 Type B RF Signal Interface

The ISO 14443 specifications refer to cards. In this section, the reader can interchange the terms “card,” “tag,” and “transponder.”

A.1. RF Signal Interface

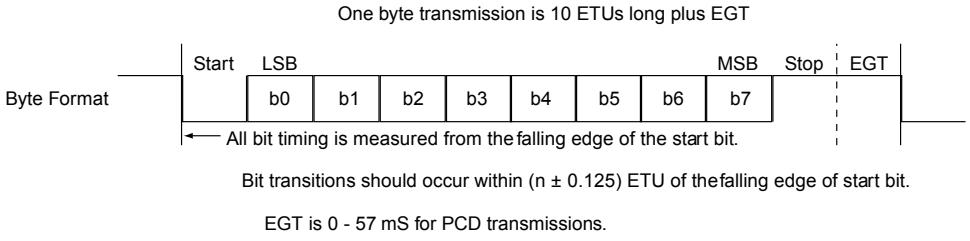
The AT88RF1354 RF communications interface is compliant with the ISO/IEC 14443 part 2 and part 3 Type B signaling requirements when used exactly as described in the AT88RF1354 reference design application notes. Type B signaling utilizes a 10 % amplitude modulation of the RF field for communication from the reader to the card with NRZ encoded data. Communication from card to reader utilizes BPSK load modulation of an 847.5 khz subcarrier with NRZ-L encoded data. The 13.56 MHz RF magnetic field is continuously on for Type B communications.

A.2. Data Format

Data communication between the card and reader is performed using an LSB first data format. Each byte of data is transmitted with a 0b start bit and a 1b stop bit as shown in Figure A-1. The stop bit, start bit, and each data bit are each one elementary time unit (ETU) in length (9.4395 microseconds).

Each byte transmission consists of a start bit, 8 data bits (LSB first), and a stop bit. Each byte may be separated from the next byte by extra guard time (EGT). The EGT may be zero or a fraction of an ETU. EGT cannot exceed 19 microseconds for data transmitted by the PICC. EGT for data transmitted by the AT88RF1354 PCD is zero ETUs. The position of each bit is measured relative to the falling edge of the start bit.

Figure A-1. Byte transmission format requirements for Type B communications.



Despite the fact that data transmissions occur LSB first, all of the commands, data, and CRC bytes in ISO/IEC 14443 and in this specification are listed in the conventional manner, with MSB on the left and LSB on the right.

A.3. Frame Format

Data transmitted by the PCD or PICC is sent as frames. The frame consists of the start of frame (SOF), several bytes of information, and the end of frame (EOF). The SOF and EOF requirements are shown in Figure A-2.