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Features

- 80C52X2 Core (6 Clocks per Instruction)
  - Maximum Core Frequency 48 MHz in X1 Mode, 24 MHz in X2 Mode
  - Dual Data Pointer
  - Full-duplex Enhanced UART (EUART)
  - Three 16-bit Timer/Counters: T0, T1 and T2
  - 256 Bytes of Scratchpad RAM
- 16/32-Kbyte On-chip Flash EEPROM In-System Programming through USB
  - Byte and Page (128 bytes) Erase and Write
  - 100k Write Cycles
- 3-KbyteFlash EEPROM for Bootloader
  - Byte and Page (128 bytes) Erase and Write
  - 100k Write Cycles
- 1-Kbyte EEPROM Data (
  - Byte and Page (128 bytes) Erase and Write
  - 100k Write Cycles
- On-chip Expanded RAM (ERAM): 1024 Bytes
- Integrated Power Monitor (POR/PFD) to Supervise Internal Power Supply
- USB 1.1 and 2.0 Full Speed Compliant Module with Interrupt on Transfer Completion
  - Endpoint 0 for Control Transfers: 32-byte FIFO
  - 6 Programmable Endpoints with In or Out Directions and with Bulk, Interrupt or Isochronous Transfers
    - Endpoint 1, 2, 3: 32-byte FIFO
    - Endpoint 4, 5: 2 x 64-byte FIFO with Double Buffering (Ping-pong Mode)
    - Endpoint 6: 2 x 512-byte FIFO with Double Buffering (Ping-pong Mode)
  - Suspend/Resume Interrupts
  - 48 MHz PLL for Full-speed Bus Operation
  - Bus Disconnection on Microcontroller Request
- 5 Channels Programmable Counter Array (PCA) with 16-bit Counter, High-speed Output, Compare/Capture, PWM and Watchdog Timer Capabilities
- Programmable Hardware Watchdog Timer (One-time Enabled with Reset-out): 100 ms to 3s at 8 MHz
- Keyboard Interrupt Interface on Port P1 (8 Bits)
- TWI (Two Wire Interface) 400Kbit/s
- SPI Interface (Master/Slave Mode)
- 34 I/O Pins
- 4 Direct-drive LED Outputs with Programmable Current Sources: 2-6-10 mA Typical
- 4-level Priority Interrupt System (11 sources)
- Idle and Power-down Modes
- 0 to 24 MHz On-chip Oscillator with Analog PLL for 48 MHz Synthesis
- Industrial Temperature Range
- Extended Range Power Supply: 2.7V to 5.5V (3.3V to 5.5V required for USB)
- Packages: PLCC52, VQFP64, QFN32

8-bit Flash Microcontroller with Full Speed USB Device

AT89C5130A-M
AT89C5131A-M

1. Description

AT89C5130A/31A-M is a high-performance Flash version of the 80C51 single-chip 8-bit microcontrollers with full speed USB functions.

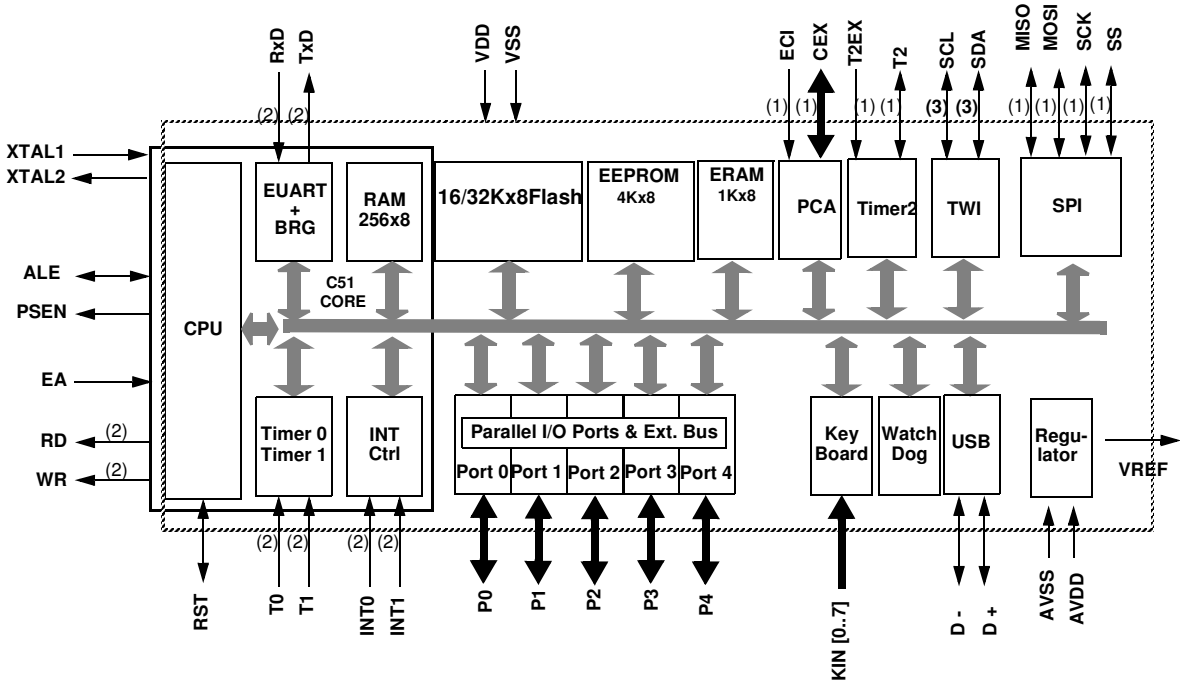
AT89C5130A/31A-M features a full-speed USB module compatible with the USB specifications Version 1.1 and 2.0. This module integrates the USB transceivers with a 3.3V voltage regulator and the Serial Interface Engine (SIE) with Digital Phase Locked Loop and 48 MHz clock recovery. USB Event detection logic (Reset and Suspend/Resume) and FIFO buffers supporting the mandatory control Endpoint (EP0) and up to 6 versatile Endpoints (EP1/EP2/EP3/EP4/EP5/EP6) with minimum software overhead are also part of the USB module.

AT89C5130A/31A-M retains the features of the Atmel 80C52 with extended Flash capacity (16/32-Kbytes), 256 bytes of internal RAM, a 4-level interrupt system, two 16-bit timer/counters (T0/T1), a full duplex enhanced UART (EUART) and an on-chip oscillator.

In addition, AT89C5130A/31A-M has an on-chip expanded RAM of 1024 bytes (ERAM), a dual data pointer, a 16-bit up/down Timer (T2), a Programmable Counter Array (PCA), up to 4 programmable LED current sources, a programmable hardware watchdog and a power-on reset.

AT89C5130A/31A-M has two software-selectable modes of reduced activity for further reduction in power consumption. In the idle mode the CPU is frozen while the timers, the serial ports and the interrupt system are still operating. In the power-down mode the RAM is saved, the peripheral clock is frozen, but the device has full wake-up capability through USB events or external interrupts.

2. Block Diagram



Notes: 1. Alternate function of Port 1
2. Alternate function of Port 3
3. Alternate function of Port 4

3. Pinout Description

3.1 Pinout

Figure 3-1. AT89C5130A/31A-M 52-pin PLCC Pinout

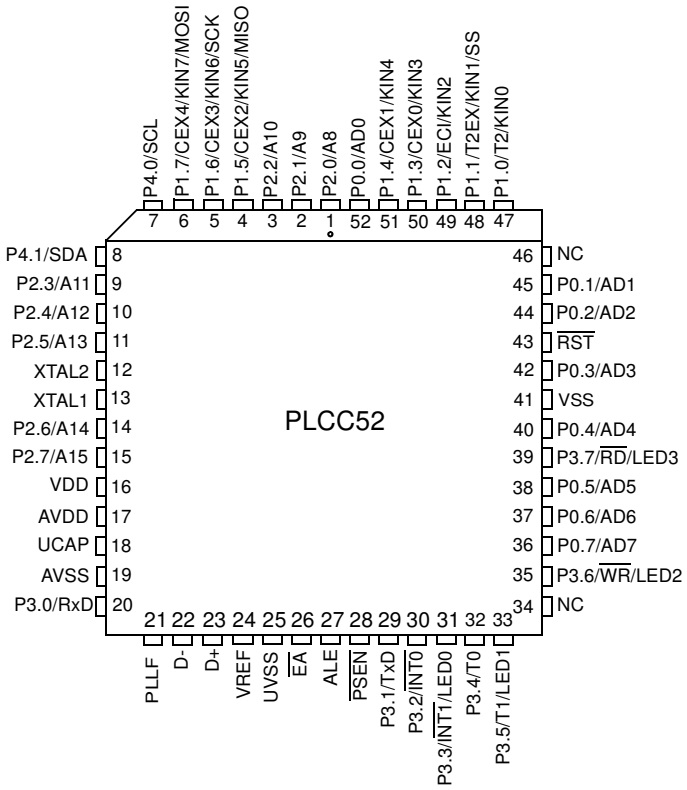


Figure 3-2. AT89C5130A/31A-M 64-pin VQFP Pinout

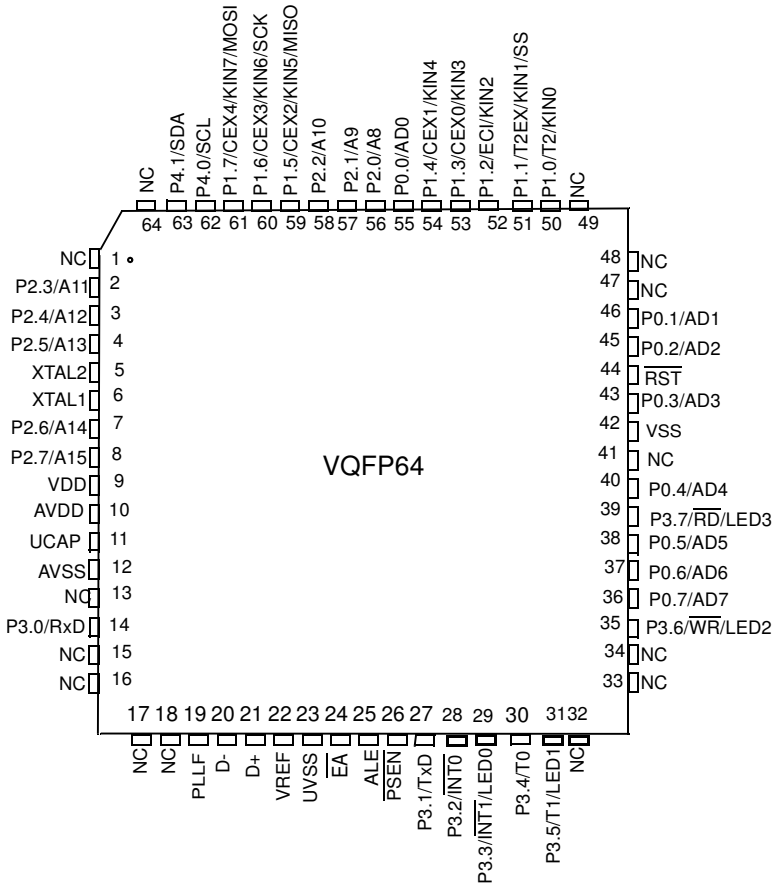
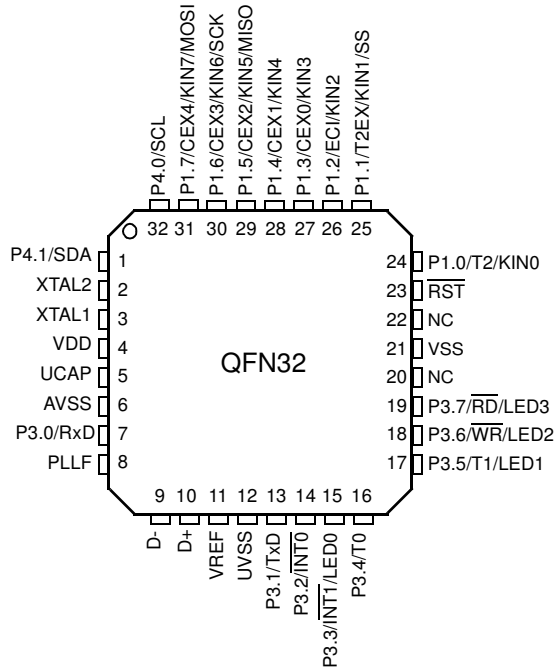


Figure 3-3. AT89C5130A/31A-M 32-pin QFN Pinout



Note : The metal plate can be connected to Vss

3.2 Signals

All the AT89C5130A/31A-M signals are detailed by functionality on Table 3-1 through Table 3-12.

Table 3-1. Keypad Interface Signal Description

Signal Name	Type	Description	Alternate Function
KIN[7:0]	I	**Keypad Input Lines** Holding one of these pins high or low for 24 oscillator periods triggers a keypad interrupt if enabled. Held line is reported in the KBCON register.	P1[7:0]

Table 3-2. Programmable Counter Array Signal Description

Signal Name	Type	Description	Alternate Function
ECI	I	External Clock Input	P1.2

Signal Name	Type	Description	Alternate Function
CEX[4:0]	I/O	Capture External Input Compare External Output	P1.3 P1.4 P1.5 P1.6 P1.7

Table 3-3. Serial I/O Signal Description

Signal Name	Type	Description	Alternate Function
RxD	I	Serial Input Port	P3.0
TxD	O	Serial Output Port	P3.1

Table 3-4. Timer 0, Timer 1 and Timer 2 Signal Description

Signal Name	Type	Description	Alternate Function
INT0	I	**Timer 0 Gate Input** $\overline{INT0}$ serves as external run control for timer 0, when selected by GATE0 bit in TCON register. **External Interrupt 0** $\overline{INT0}$ input set IE0 in the TCON register. If bit IT0 in this register is set, bits IE0 are set by a falling edge on $\overline{INT0}$. If bit IT0 is cleared, bits IE0 is set by a low level on $\overline{INT0}$.	P3.2
INT1	I	**Timer 1 Gate Input** $\overline{INT1}$ serves as external run control for Timer 1, when selected by GATE1 bit in TCON register. **External Interrupt 1** $\overline{INT1}$ input set IE1 in the TCON register. If bit IT1 in this register is set, bits IE1 are set by a falling edge on $\overline{INT1}$. If bit IT1 is cleared, bits IE1 is set by a low level on $\overline{INT1}$.	P3.3
T0	I	**Timer Counter 0 External Clock Input** When Timer 0 operates as a counter, a falling edge on the T0 pin increments the count.	P3.4
T1	I	**Timer/Counter 1 External Clock Input** When Timer 1 operates as a counter, a falling edge on the T1 pin increments the count.	P3.5
T2	I O	Timer/Counter 2 External Clock Input Timer/Counter 2 Clock Output	P1.0
T2EX	I	Timer/Counter 2 Reload/Capture/Direction Control Input	P1.1

Table 3-5. LED Signal Description

Signal Name	Type	Description	Alternate Function
LED[3:0]	O	**Direct Drive LED Output** These pins can be directly connected to the Cathode of standard LEDs without external current limiting resistors. The typical current of each output can be programmed by software to 2, 6 or 10 mA. Several outputs can be connected together to get higher drive capabilities.	P3.3 P3.5 P3.6 P3.7

Table 3-6. TWI Signal Description

Signal Name	Type	Description	Alternate Function
SCL	I/O	**SCL: TWI Serial Clock** SCL output the serial clock to slave peripherals. SCL input the serial clock from master.	P4.0
SDA	I/O	**SDA: TWI Serial Data** SCL is the bidirectional TWI data line.	P4.1

Table 3-7. SPI Signal Description

Signal Name	Type	Description	Alternate Function
SS	I/O	**$\overline{SS}$:** SPI Slave Select	P1.1
MISO	I/O	**MISO:** SPI Master Input Slave Output line When SPI is in master mode, MISO receives data from the slave peripheral. When SPI is in slave mode, MISO outputs data to the master controller.	P1.5
SCK	I/O	**SCK:** SPI Serial Clock SCK outputs clock to the slave peripheral or receive clock from the master	P1.6
MOSI	I/O	**MOSI:** SPI Master Output Slave Input line When SPI is in master mode, MOSI outputs data to the slave peripheral. When SPI is in slave mode, MOSI receives data from the master controller	P1.7

Table 3-8. Ports Signal Description

Signal Name	Type	Description	Alternate Function
P0[7:0]	I/O	**Port 0** P0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high impedance inputs. To avoid any parasitic current consumption, Floating P0 inputs must be pulled to V_{DD} or V_{SS}.	AD[7:0]
P1[7:0]	I/O	**Port 1** P1 is an 8-bit bidirectional I/O port with internal pull-ups.	KIN[7:0] T2 T2EX ECI CEX[4:0]
P2[7:0]	I/O	**Port 2** P2 is an 8-bit bidirectional I/O port with internal pull-ups.	A[15:8]
P3[7:0]	I/O	**Port 3** P3 is an 8-bit bidirectional I/O port with internal pull-ups.	LED[3:0] RxD TxD $\overline{INT0}$ $\overline{INT1}$ T0 T1 $\overline{WR}$ $\overline{RD}$
P4[1:0]	I/O	**Port 4** P4 is an 2-bit open drain port.	SCL SDA

Table 3-9. Clock Signal Description

Signal Name	Type	Description	Alternate Function
XTAL1	I	**Input to the on-chip inverting oscillator amplifier** To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, its output is connected to this pin.	-
XTAL2	O	**Output of the on-chip inverting oscillator amplifier** To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, leave XTAL2 unconnected.	-
PLLF	I	**PLL Low Pass Filter input** Receive the RC network of the PLL low pass filter.	-

Table 3-10. USB Signal Description

Signal Name	Type	Description	Alternate Function
D+	I/O	USB Data + signal Set to high level under reset.	-
D-	I/O	USB Data - signal Set to low level under reset.	-
VREF	O	**USB Reference Voltage** Connect this pin to D+ using a 1.5 kΩ resistor to use the Detach function.	-

Table 3-11. System Signal Description

Signal Name	Type	Description	Alternate Function
AD[7:0]	I/O	Multiplexed Address/Data LSB for external access Data LSB for Slave port access (used for 8-bit and 16-bit modes)	P0[7:0]
A[15:8]	I/O	Address Bus MSB for external access	P2[7:0]
$\overline{RD}$	I/O	**Read Signal** Read signal asserted during external data memory read operation. Control input for slave port read access cycles.	P3.7
$\overline{WR}$	I/O	**Write Signal** Write signal asserted during external data memory write operation. Control input for slave write access cycles.	P3.6
RST	O	**Reset Input** Holding this pin low for 64 oscillator periods while the oscillator is running resets the device. The Port pins are driven to their reset conditions when a voltage lower than V_{IL} is applied, whether or not the oscillator is running. This pin has an internal pull-up resistor which allows the device to be reset by connecting a capacitor between this pin and VSS. Asserting $\overline{RST}$ when the chip is in Idle mode or Power-down mode returns the chip to normal operation. This pin is tied to 0 for at least 12 oscillator periods when an internal reset occurs (hardware watchdog or power monitor).	-
ALE	O	**Address Latch Enable Output** The falling edge of ALE strobes the address into external latch. This signal is active only when reading or writing external memory using MOVX instructions.	-
PSEN	I/O	**Program Strobe Enable / Hardware conditions Input for ISP** Used as input under reset to detect external hardware conditions of ISP mode.	-
$\overline{EA}$	I	External Access Enable This pin must be held low to force the device to fetch code from external program memory starting at address 0000h.	-

Table 3-12. Power Signal Description

Signal Name	Type	Description	Alternate Function
AVSS	GND	**Analog Ground** AVSS is used to supply the on-chip PLL and the USB PAD.	-

Table 3-12. Power Signal Description (Continued)

Signal Name	Type	Description	Alternate Function
AVDD	PWR	**Analog Supply Voltage** AVDD is used to supply the on-chip PLL and the USB PAD.	-
VSS	GND	**Digital Ground** VSS is used to supply the buffer ring and the digital core.	-
UVSS	GND	**USB Digital Ground** UVSS is used to supply the USB pads.	-
UCAP	PWR	**USB Pad Power Capacitor** UCAP must be connect to an external capacitor for USB pad power supply (for typical application see Figure 4-1 on page 12)	-
VDD	PWR	**Digital Supply Voltage** VDD is used to supply the buffer ring on all versions of the device. It is also used to power the on-chip voltage regulator of the Standard versions or the digital core of the Low Power versions.	-
VREF	O	USB pull-up Controlled Output VREF is used to control the USB D+ 1.5 kΩ pull up. The Vref output is in high impedance when the bit DETACH is set in the USBCON register.	-

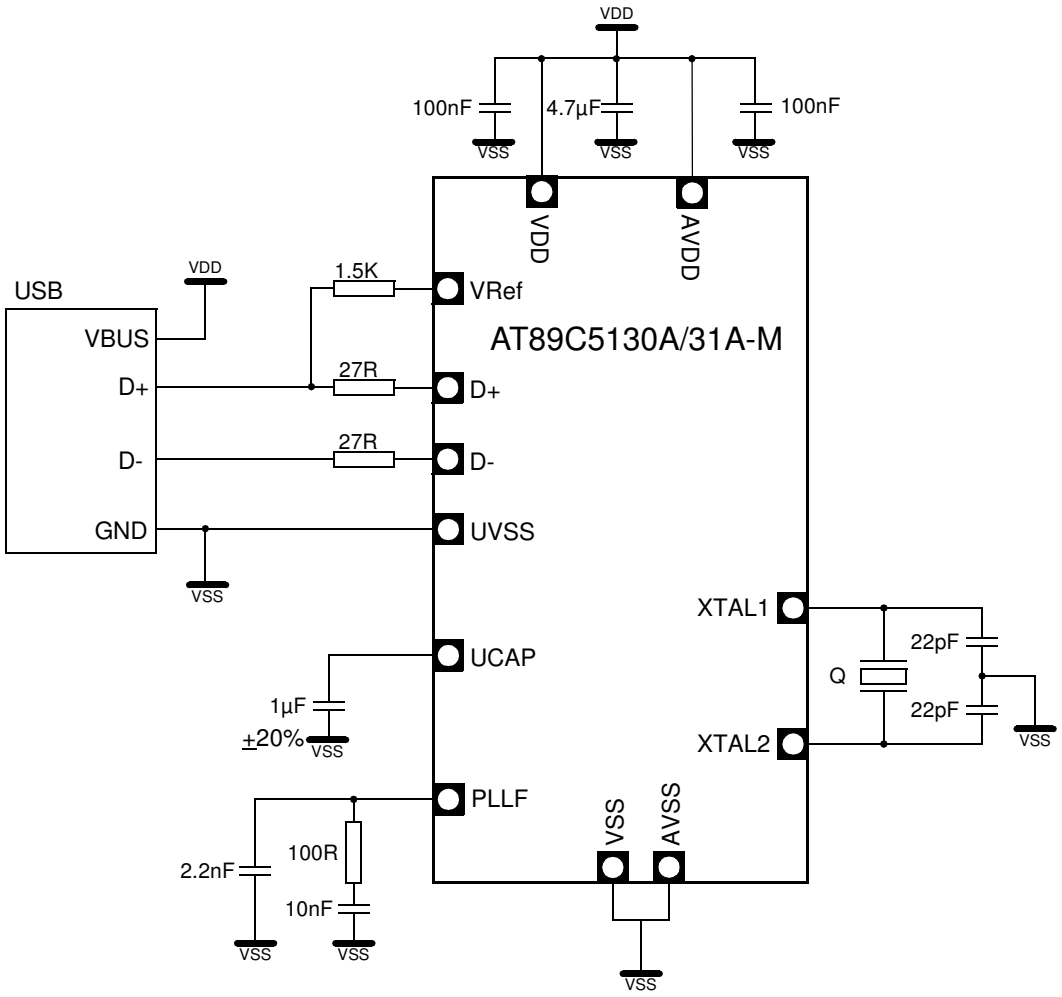
4. Typical Application

4.1 Recommended External components

All the external components described in the figure below must be implemented as close as possible from the microcontroller package.

The following figure represents the typical wiring schematic.

Figure 4-1. Typical Application



4.2 PCB Recommandations

Figure 4-2. USB Pads

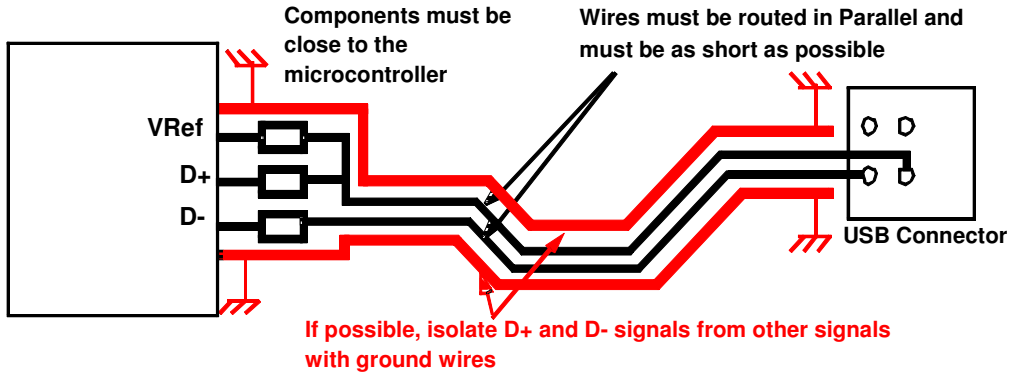
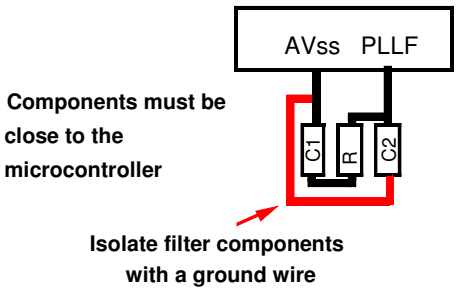


Figure 4-3. USB PLL



5. Clock Controller

5.1 Introduction

The AT89C5130A/31A-M clock controller is based on an on-chip oscillator feeding an on-chip Phase Lock Loop (PLL). All the internal clocks to the peripherals and CPU core are generated by this controller.

The AT89C5130A/31A-M X1 and X2 pins are the input and the output of a single-stage on-chip inverter (see Figure 5-1) that can be configured with off-chip components as a Pierce oscillator (see Figure 5-2). Value of capacitors and crystal characteristics are detailed in the section “DC Characteristics”.

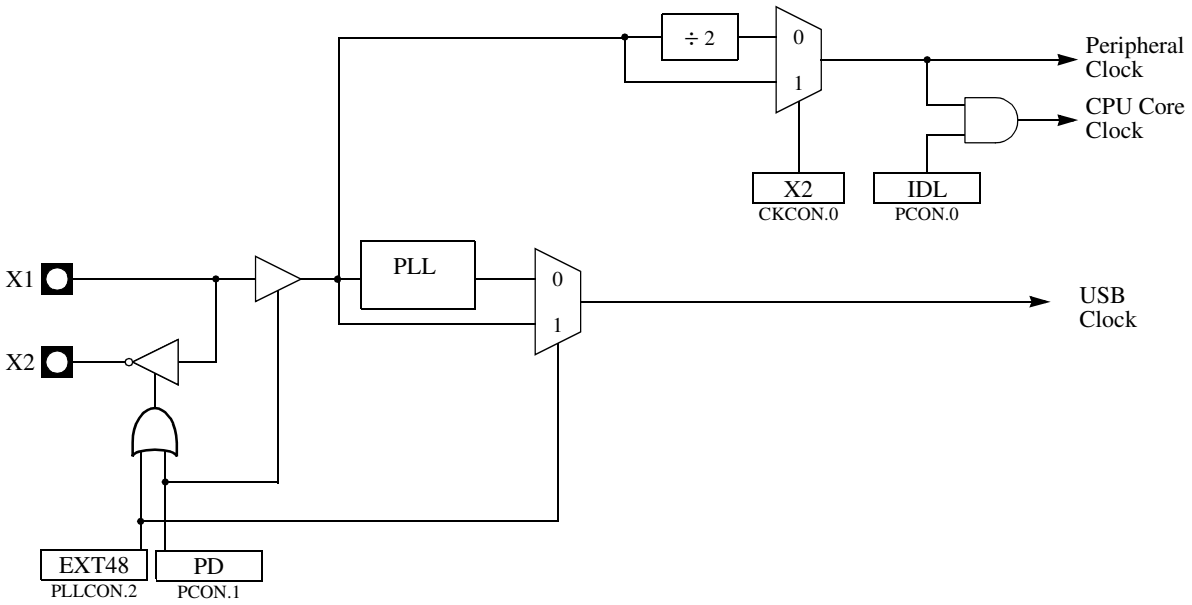
The X1 pin can also be used as input for an external 48 MHz clock.

The clock controller outputs three different clocks as shown in Figure 5-1:

- a clock for the CPU core
- a clock for the peripherals which is used to generate the Timers, PCA, WD, and Port sampling clocks
- a clock for the USB controller

These clocks are enabled or disabled depending on the power reduction mode as detailed in Section “Power Management”, page 155.

Figure 5-1. Oscillator Block Diagram



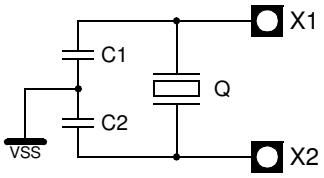
5.2 Oscillator

Two types of clock sources can be used for CPU:

- Crystal oscillator on X1 and X2 pins: Up to 32 MHz (Amplifier Bandwidth)
- External clock on X1 pin: Up to 48MHz

In order to optimize the power consumption, the oscillator inverter is inactive when the PLL output is not selected for the USB device.

Figure 5-2. Crystal Connection



5.3 PLL

5.3.1 PLL Description

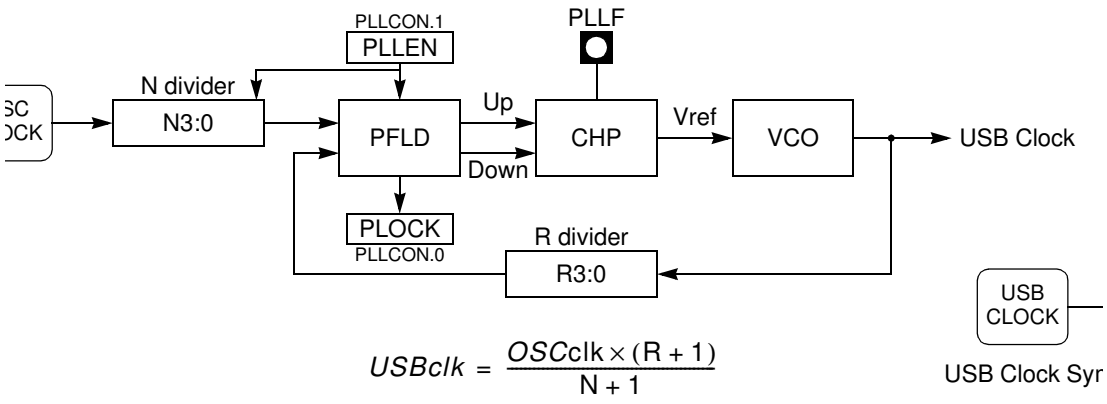
The AT89C5130A/31A-M PLL is used to generate internal high frequency clock (the USB Clock) synchronized with an external low-frequency (the Peripheral Clock). The PLL clock is used to generate the USB interface clock. Figure 5-3 shows the internal structure of the PLL.

The PFLD block is the Phase Frequency Comparator and Lock Detector. This block makes the comparison between the reference clock coming from the N divider and the reverse clock coming from the R divider and generates some pulses on the Up or Down signal depending on the edge position of the reverse clock. The PLLEN bit in PLLCON register is used to enable the clock generation. When the PLL is locked, the bit PLOCK in PLLCON register (see Figure 5-3) is set.

The CHP block is the Charge Pump that generates the voltage reference for the VCO by injecting or extracting charges from the external filter connected on PLLF pin (see Figure 5-4). Value of the filter components are detailed in the Section “DC Characteristics”.

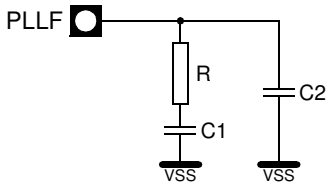
The VCO block is the Voltage Controlled Oscillator controlled by the voltage V_{REF} produced by the charge pump. It generates a square wave signal: the PLL clock.

Figure 5-3. PLL Block Diagram and Symbol



$$USBclk = \frac{OSCclk \times (R + 1)}{N + 1}$$

Figure 5-4. PLL Filter Connection

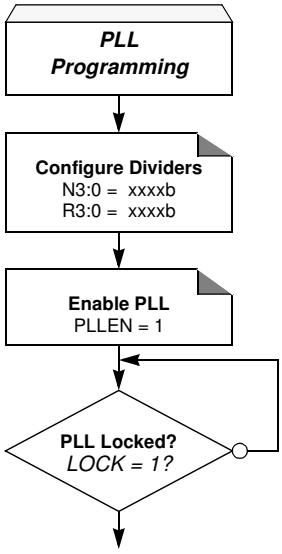


The typical values are: R = 100 Ω, C1 = 10 nf, C2 = 2.2 nF.

5.3.2 PLL Programming

The PLL is programmed using the flow shown in Figure 5-5. As soon as clock generation is enabled user must wait until the lock indicator is set to ensure the clock output is stable.

Figure 5-5. PLL Programming Flow



5.3.3 Divider Values

To generate a 48 MHz clock using the PLL, the divider values have to be configured following the oscillator frequency. The typical divider values are shown in Table 5-1.

Table 5-1. Typical Divider Values

Oscillator Frequency	R+1	N+1	PLLDIV
3 MHz	16	1	F0h
6 MHz	8	1	70h
8 MHz	6	1	50h
12 MHz	4	1	30h
16 MHz	3	1	20h
18 MHz	8	3	72h
20 MHz	12	5	B4h
24 MHz	2	1	10h

Oscillator Frequency	R+1	N+1	PLLDIV
32 MHz	3	2	21h
40 MHz	12	10	B9h

5.4 Registers

Table 5-2. CKCON0 (S:8Fh)
Clock Control Register 0

7	6	5	4	3	2	1	0
TWIX2	WDX2	PCAX2	SIX2	T2X2	T1X2	T0X2	X2

Bit Number	Bit Mnemonic	Description
7	TWIX2	**TWI Clock** **This control bit is validated when the CPU clock X2 is set. When X2 is low, this bit has no effect.** Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
6	WDX2	**Watchdog Clock** **This control bit is validated when the CPU clock X2 is set. When X2 is low, this bit has no effect.** Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
5	PCAX2	**Programmable Counter Array Clock** **This control bit is validated when the CPU clock X2 is set. When X2 is low, this bit has no effect.** Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
4	SIX2	**Enhanced UART Clock (Mode 0 and 2)** **This control bit is validated when the CPU clock X2 is set. When X2 is low, this bit has no effect.** Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
3	T2X2	**Timer2 Clock** **This control bit is validated when the CPU clock X2 is set. When X2 is low, this bit has no effect.** Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
2	T1X2	**Timer1 Clock** **This control bit is validated when the CPU clock X2 is set. When X2 is low, this bit has no effect.** Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
1	T0X2	**Timer0 Clock** **This control bit is validated when the CPU clock X2 is set. When X2 is low, this bit has no effect.** Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
0	X2	**System Clock Control bit** Clear to select 12 clock periods per machine cycle (STD mode, $F_{CPU} = F_{PER} = F_{OSC}/2$). Set to select 6 clock periods per machine cycle (X2 mode, $F_{CPU} = F_{PER} = F_{OSC}$).

Reset Value = 0000 0000b

Table 5-3. CKCON1 (S:AFh)
Clock Control Register 1

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	SPIX2

Bit Number	Bit Mnemonic	Description
7-1	-	**Reserved** The value read from this bit is always 0. Do not set this bit.
0	SPIX2	**SPI Clock** **This control bit is validated when the CPU clock X2 is set. When X2 is low, this bit has no effect.** Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.

Reset Value = 0000 0000b

Table 5-4. PLLCON (S:A3h)
PLL Control Register

7	6	5	4	3	2	1	0
-	-	-	-	-	EXT48	PLLEN	PLOCK

Bit Number	Bit Mnemonic	Description
7-3	-	**Reserved** The value read from this bit is always 0. Do not set this bit.
2	EXT48	**External 48 MHz Enable Bit** Set this bit to bypass the PLL and disable the crystal oscillator. Clear this bit to select the PLL output as USB clock and to enable the crystal oscillator.
1	PLLEN	**PLL Enable Bit** Set to enable the PLL. Clear to disable the PLL.
0	PLOCK	**PLL Lock Indicator** Set by hardware when PLL is locked. Clear by hardware when PLL is unlocked.

Reset Value = 0000 0000b

Table 5-5. PLLDIV (S:A4h)
PLL Divider Register

7	6	5	4	3	2	1	0
R3	R2	R1	R0	N3	N2	N1	N0

Bit Number	Bit Mnemonic	Description
7-4	R3:0	**PLL R Divider Bits**
3-0	N3:0	**PLL N Divider Bits**

Reset Value = 0000 0000

6. SFR Mapping

The Special Function Registers (SFRs) of the AT89C5130A/31A-M fall into the following categories:

- C51 core registers: ACC, B, DPH, DPL, PSW, SP
- I/O port registers: P0, P1, P2, P3, P4
- Timer registers: T2CON, T2MOD, TCON, TH0, TH1, TH2, TMOD, TL0, TL1, TL2, RCAP2L, RCAP2H
- Serial I/O port registers: SADDR, SADEN, SBUF, SCON
- PCA (Programmable Counter Array) registers: CCON, CMOD, CCAPMx, CL, CH, CCAPxH, CCAPxL (x: 0 to 4)
- Power and clock control registers: PCON
- Hardware Watchdog Timer registers: WDTRST, WDTPRG
- Interrupt system registers: IEN0, IPL0, IPH0, IEN1, IPL1, IPH1
- Keyboard Interface registers: KBE, KBF, KBLS
- LED register: LEDCON
- Two Wire Interface (TWI) registers: SSCON, SSCS, SSDAT, SSADR
- Serial Port Interface (SPI) registers: SPCON, SPSTA, SPDAT
- USB registers: Uxxx (17 registers)
- PLL registers: PLLCON, PLLDIV
- BRG (Baud Rate Generator) registers: BRL, BDRCON
- Flash register: FCON (FCON access is reserved for the Flash API and ISP software)
- EEPROM register: EECON
- Others: AUXR, AUXR1, CKCON0, CKCON1

The table below shows all SFRs with their address and their reset value.

Table 6-1. SFR Descriptions

	Bit Addressable	**Non-Bit Addressable**							
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
F8h	UEPINT 0000 0000	CH 0000 0000	CCAP0H XXXX XXXX	CCAP1H XXXX XXXX	CCAP2H XXXX XXXX	CCAP3H XXXX XXXX	CCAP4H XXXX XXXX		FFh
F0h	B 0000 0000	LEDCON 0000 0000							F7h
E8h		CL 0000 0000	CCAP0L XXXX XXXX	CCAP1L XXXX XXXX	CCAP2L XXXX XXXX	CCAP3L XXXX XXXX	CCAP4L XXXX XXXX		EFh
E0h	ACC 0000 0000		UBYCTLX 0000 0000	UBYCTHX 0000 0000					E7h
D8h	CCON 00X0 0000	CMOD 00XX X000	CCAPM0 X000 0000	CCAPM1 X000 0000	CCAPM2 X000 0000	CCAPM3 X000 0000	CCAPM4 X000 0000		DFh
D0h	PSW 0000 0000	FCON (1) XXXX 0000	EECON XXXX XX00		UEPCONX 1000 0000	UEPRST 0000 0000			D7h
C8h	T2CON 0000 0000	T2MOD XXXX XX00	RCAP2L 0000 0000	RCAP2H 0000 0000	TL2 0000 0000	TH2 0000 0000	UEPSTAX 0000 0000	UEPDATX 0000 0000	CFh
C0h	P4 XXXX 1111		UEPIEN 0000 0000	SPCON 0001 0100	SPSTA 0000 0000	SPDAT XXXX XXXX	USBADDR 1000 0000	UEPNUM 0000 0000	C7h
B8h	IPL0 X000 000	SADEN 0000 0000	UFNUML 0000 0000	UFNUMH 0000 0000	USBCON 0000 0000	USBINT 0000 0000	USBIEN 0000 0000		BFh
B0h	P3 1111 1111	IEN1 X0XX X000	IPL1 X0XX X000	IPH1 X0XX X000				IPH0 X000 0000	B7h
A8h	IEN0 0000 0000	SADDR 0000 0000						CKCON1 0000 0000	AFh
A0h	P2 1111 1111		AUXR1 XXXX X0X0	PLLCON XXXX XX00	PLLDIV 0000 0000		WDTRST XXXX XXXX	WDTPRG XXXX X000	A7h
98h	SCON 0000 0000	SBUF XXXX XXXX	BRL 0000 0000	BDRCON XXX0 0000	KBLS 0000 0000	KBE 0000 0000	KBF 0000 0000		9Fh
90h	P1 1111 1111			SSCON 0000 0000	SSCS 1111 1000	SSDAT 1111 1111	SSADR 1111 1110		97h
88h	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	AUXR XX0X 0000	CKCON0 0000 0000	8Fh
80h	P0 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000				PCON 00X1 0000	87h
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

Note: 1. FCON access is reserved for the Flash API and ISP software.

Reserved

The Special Function Registers (SFRs) of the AT89C5131 fall into the following categories:

Table 6-2. C51 Core SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
ACC	E0h	Accumulator								
B	F0h	B Register								
PSW	D0h	Program Status Word								
SP	81h	Stack Pointer LSB of SPX								
DPL	82h	Data Pointer Low byte LSB of DPTR								
DPH	83h	Data Pointer High byte MSB of DPTR								

Table 6-3. I/O Port SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
P0	80h	Port 0								
P1	90h	Port 1								
P2	A0h	Port 2								
P3	B0h	Port 3								
P4	C0h	Port 4 (2bits)								

Table 6-4. Timer SFR's

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
TH0	8Ch	Timer/Counter 0 High byte								
TL0	8Ah	Timer/Counter 0 Low byte								
TH1	8Dh	Timer/Counter 1 High byte								
TL1	8Bh	Timer/Counter 1 Low byte								
TH2	CDh	Timer/Counter 2 High byte								
TL2	CCh	Timer/Counter 2 Low byte								
TCON	88h	Timer/Counter 0 and 1 control	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
TMOD	89h	Timer/Counter 0 and 1 Modes	GATE1	C/T1#	M11	M01	GATE0	C/T0#	M10	M00
T2CON	C8h	Timer/Counter 2 control	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2#	CP/RL2#
T2MOD	C9h	Timer/Counter 2 Mode							T2OE	DCEN

Table 6-4. Timer SFR's (Continued)

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
RCAP2H	CBh	Timer/Counter 2 Reload/Capture High byte								
RCAP2L	CAh	Timer/Counter 2 Reload/Capture Low byte								
WDTRST	A6h	WatchDog Timer Reset								
WDTPRG	A7h	WatchDog Timer Program						S2	S1	S0

Table 6-5. Serial I/O Port SFR's

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
SCON	98h	Serial Control	FE/SM0	SM1	SM2	REN	TB8	RB8	TI	RI
SBUF	99h	Serial Data Buffer								
SADEN	B9h	Slave Address Mask								
SADDR	A9h	Slave Address								

Table 6-6. Baud Rate Generator SFR's

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
BRL	9Ah	Baud Rate Reload								
BDRCON	9Bh	Baud Rate Control				BRR	TBCK	RBCK	SPD	SRC

Table 6-7. PCA SFR's

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
CCON	D8h	PCA Timer/Counter Control	CF	CR		CCF4	CCF3	CCF2	CCF1	CCF0
CMOD	D9h	PCA Timer/Counter Mode	CIDL	WDTE				CPS1	CPS0	ECF
CL	E9h	PCA Timer/Counter Low byte								
CH	F9h	PCA Timer/Counter High byte								
CCAPM0	DAh	PCA Timer/Counter Mode 0		ECOM0	CAPP0	CAPN0	MAT0	TOG0	PWM0	ECCF0
CCAPM1	DBh	PCA Timer/Counter Mode 1		ECOM1	CAPP1	CAPN1	MAT1	TOG1	PWM1	ECCF1
CCAPM2	DCh	PCA Timer/Counter Mode 2		ECOM2	CAPP2	CAPN2	MAT2	TOG2	PWM2	ECCF2
CCAPM3	DDh	PCA Timer/Counter Mode 3		ECOM3	CAPP3	CAPN3	MAT3	TOG3	PWM3	ECCF3
CCAPM4	DEh	PCA Timer/Counter Mode 4		ECOM4	CAPP4	CAPN4	MAT4	TOG4	PWM4	ECCF4

Table 6-7. PCA SFR's

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
CCAP0H		PCA Compare Capture Module 0 H								
CCAP1H	FAh	PCA Compare Capture Module 1 H	CCAP0H7	CCAP0H6	CCAP0H5	CCAP0H4	CCAP0H3	CCAP0H2	CCAP0H1	CCAP0H0
CCAP2H	FBh	PCA Compare Capture Module 2 H	CCAP1H7	CCAP1H6	CCAP1H5	CCAP1H4	CCAP1H3	CCAP1H2	CCAP1H1	CCAP1H0
CCAP3H	FCh	PCA Compare Capture Module 3 H	CCAP2H7	CCAP2H6	CCAP2H5	CCAP2H4	CCAP2H3	CCAP2H2	CCAP2H1	CCAP2H0
CCAP4H	FDh	PCA Compare Capture Module 4 H	CCAP3H7	CCAP3H6	CCAP3H5	CCAP3H4	CCAP3H3	CCAP3H2	CCAP3H1	CCAP3H0
	FEh		CCAP4H7	CCAP4H6	CCAP4H5	CCAP4H4	CCAP4H3	CCAP4H2	CCAP4H1	CCAP4H0
CCAP0L		PCA Compare Capture Module 0 L								
CCAP1L	EAh	PCA Compare Capture Module 1 L	CCAP0L7	CCAP0L6	CCAP0L5	CCAP0L4	CCAP0L3	CCAP0L2	CCAP0L1	CCAP0L0
CCAP2L	EBh	PCA Compare Capture Module 2 L	CCAP1L7	CCAP1L6	CCAP1L5	CCAP1L4	CCAP1L3	CCAP1L2	CCAP1L1	CCAP1L0
CCAP3L	ECh	PCA Compare Capture Module 3 L	CCAP2L7	CCAP2L6	CCAP2L5	CCAP2L4	CCAP2L3	CCAP2L2	CCAP2L1	CCAP2L0
CCAP4L	EDh	PCA Compare Capture Module 4 L	CCAP3L7	CCAP3L6	CCAP3L5	CCAP3L4	CCAP3L3	CCAP3L2	CCAP3L1	CCAP3L0
	EEh		CCAP4L7	CCAP4L6	CCAP4L5	CCAP4L4	CCAP4L3	CCAP4L2	CCAP4L1	CCAP4L0

Table 6-8. Interrupt SFR's

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
IEN0	A8h	Interrupt Enable Control 0	EA	EC	ET2	ES	ET1	EX1	ET0	EX0
IEN1	B1h	Interrupt Enable Control 1		EUSB				ESPI	ETWI	EKB
IPL0	B8h	Interrupt Priority Control Low 0		PPCL	PT2L	PSL	PT1L	PX1L	PT0L	PX0L
IPH0	B7h	Interrupt Priority Control High 0		PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H
IPL1	B2h	Interrupt Priority Control Low 1		PUSBL				PSPIL	PTWIL	PKBL
IPH1	B3h	Interrupt Priority Control High 1		PUSBH				PSPIH	PTWIH	PKBH

Table 6-9. PLL SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
PLLCON	A3h	PLL Control						EXT48	PLLEN	PLOCK
PLLDIV	A4h	PLL Divider	R3	R2	R1	R0	N3	N2	N1	N0

Table 6-10. Keyboard SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
KBF	9Eh	Keyboard Flag Register	KBF7	KBF6	KBF5	KBF4	KBF3	KBF2	KBF1	KBF0
KBE	9Dh	Keyboard Input Enable Register	KBE7	KBE6	KBE5	KBE4	KBE3	KBE2	KBE1	KBE0

Table 6-10. Keyboard SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
KBLS	9Ch	Keyboard Level Selector Register	KBLS7	KBLS6	KBLS5	KBLS4	KBLS3	KBLS2	KBLS1	KBLS0

Table 6-11. TWI SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
SSCON	93h	Synchronous Serial Control	CR2	SSIE	STA	STO	SI	AA	CR1	CR0
SSCS	94h	Synchronous Serial Control-Status	SC4	SC3	SC2	SC1	SC0	-	-	-
SSDAT	95h	Synchronous Serial Data	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
SSADR	96h	Synchronous Serial Address	A7	A6	A5	A4	A3	A2	A1	A0

Table 6-12. SPI SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
SPCON	C3h	Serial Peripheral Control	SPR2	SPEN	SSDIS	MSTR	CPOL	CPHA	SPR1	SPR0
SPSTA	C4h	Serial Peripheral Status-Control	SPIF	WCOL	SSERR	MODF	-	-	-	-
SPDAT	C5h	Serial Peripheral Data	R7	R6	R5	R4	R3	R2	R1	R0

Table 6-13. USB SFR's

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
USBCON	BCh	USB Global Control	USBE	SUSPCLK	SDRMWUP	DETACH	UPRSM	RMWUPE	CONFG	FADDEN
USBADDR	C6h	USB Address	FEN	UADD6	UADD5	UADD4	UADD3	UADD2	UADD1	UADD0
USBINT	BDh	USB Global Interrupt	-	-	WUPCPU	EORINT	SOFINT	-	-	SPINT
USBIEN	BEh	USB Global Interrupt Enable	-	-	EWUPCPU	EEORINT	ESOFINT	-	-	ESPINT
UEPNUM	C7h	USB Endpoint Number	-	-	-	-	EPNUM3	EPNUM2	EPNUM1	EPNUM0
UEPCONX	D4h	USB Endpoint X Control	EPEN	-	-	-	DTGL	EPDIR	EPTYPE1	EPTYPE0
UEPSTAX	CEh	USB Endpoint X Status	DIR	RXOUTB1	STALLRQ	TXRDY	STLCRC	RXSETUP	RXOUTB0	TXCMP
UEPRST	D5h	USB Endpoint Reset	-	EP6RST	EP5RST	EP4RST	EP3RST	EP2RST	EP1RST	EP0RST
UEPINT	F8h	USB Endpoint Interrupt	-	EP6INT	EP5INT	EP4INT	EP3INT	EP2INT	EP1INT	EP0INT
UEPIEN	C2h	USB Endpoint Interrupt Enable	-	EP6INTE	EP5INTE	EP4INTE	EP3INTE	EP2INTE	EP1INTE	EP0INTE
UEPDATX	CFh	USB Endpoint X FIFO Data	FDAT7	FDAT6	FDAT5	FDAT4	FDAT3	FDAT2	FDAT1	FDAT0