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Features

- 80C52 Compatible
  - 8051 Instruction Compatible
  - Six 8-bit I/O Ports (64 pins or 68 Pins Versions)
  - Four 8-bit I/O Ports (44 Pins Version)
  - Three 16-bit Timer/Counters
  - 256 bytes Scratch Pad RAM
  - 10 Interrupt Sources With 4 Priority Levels
- ISP (In-System Programming) Using Standard V_{CC} Power Supply
- Integrated Power Monitor (POR/PFD) to Supervise Internal Power Supply
- Boot ROM Contains Low Level Flash Programming Routines and a Default Serial Loader
- High-speed Architecture
  - In Standard Mode:
    - 40 MHz (Vcc 2.7V to 5.5V, Both Internal and External Code Execution)
    - 60 MHz (Vcc 4.5V to 5.5V and Internal Code Execution Only)
  - In X2 Mode (6 Clocks/Machine Cycle)
    - 20 MHz (Vcc 2.7V to 5.5V, Both Internal and External Code Execution)
    - 30 MHz (Vcc 4.5V to 5.5V and Internal Code Execution Only)
- 64K bytes On-chip Flash Program/Data Memory
  - Byte and Page (128 bytes) Erase and Write
  - 100k Write Cycles
- On-chip 1792 bytes Expanded RAM (XRAM)
  - Software Selectable Size (0, 256, 512, 768, 1024, 1792 bytes)
  - 768 bytes Selected at Reset for T89C51RD2 Compatibility
- On-chip 2048 bytes EEPROM block for Data Storage
  - 100k Write Cycles
- Dual Data Pointer
- 32 KHz Crystal Oscillator
- Variable Length MOVX for Slow RAM/Peripherals
- Improved X2 Mode with Independant Selection for CPU and Each Peripheral
- Keyboard Interrupt Interface on Port 1
- SPI Interface (Master/Slave Mode)
- 8-bit Clock Prescaler
- Two Wire Interface 400K bit/s
- Programmable Counter Array with:
  - High Speed Output
  - Compare/Capture
  - Pulse Width Modulator
  - Watchdog Timer Capabilities
- Asynchronous Port Reset
- Full Duplex Enhanced UART with Dedicated Internal Baud Rate Generator
- Low EMI (inhibit ALE)
- Hardware Watchdog Timer (One-time Enabled with Reset-Out), Power-Off Flag
- Power Control Modes: Idle Mode, Power-down Mode
- Power Supply: 2.7V to 5.5V
- Temperature Ranges: Industrial (-40 to +85°C)
- Packages: PLCC44, VQFP44

Description

AT89C51ID2 is a high performance CMOS Flash version of the 80C51 CMOS single chip 8-bit microcontroller. It contains a 64 Kbytes Flash memory block for program and for data.

The 64 Kbytes Flash memory can be programmed either in parallel mode or in serial mode with the ISP capability or with software. The programming voltage is internally generated from the standard V_{CC} pin.

8-bit Flash Microcontroller

AT89C51ID2

4289C–8051–11/05

The AT89C51ID2 retains all features of the Atmel 80C52 with 256 bytes of internal RAM, a 10-source 4-level interrupt controller and three timer/counters.

In addition, the AT89C51ID2 has a Programmable Counter Array, an XRAM of 1792 bytes, a Hardware Watchdog Timer, SPI and Keyboard, a more versatile serial channel that facilitates multiprocessor communication (EUART) and a speed improvement mechanism (X2 mode).

The fully static design of the AT89C51ID2 allows to reduce system power consumption by bringing the clock frequency down to any value, even DC, without loss of data.

The AT89C51ID2 has 2 software-selectable modes of reduced activity and 8-bit clock prescaler for further reduction in power consumption. In the Idle mode the CPU is frozen while the peripherals and the interrupt system are still operating. In the power-down mode the RAM is saved and all other functions are inoperative.

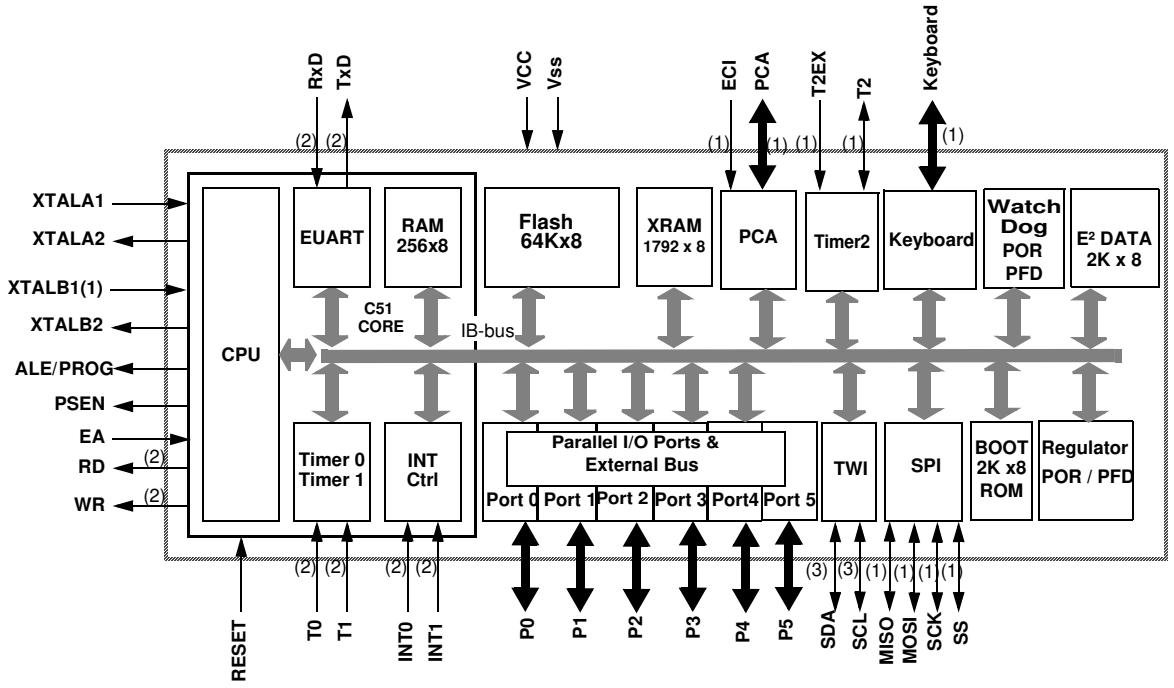
The added features of the AT89C51ID2 make it more powerful for applications that need pulse width modulation, high speed I/O and counting capabilities such as alarms, motor control, corded phones, smart card readers.

Table 1. Memory Size and I/O pins

AT89C51ID2	Flash (bytes)	XRAM (bytes)	TOTAL RAM (bytes)	I/O
PLCC44/VQFP44	64K	1792	2048	34

Block Diagram

Figure 1. Block Diagram



(1): Alternate function of Port 1

(2): Alternate function of Port 3

(3): Alternate function of Port I2

SFR Mapping

The Special Function Registers (SFRs) of the AT89C51ID2 fall into the following categories:

- C51 core registers: ACC, B, DPH, DPL, PSW, SP
- I/O port registers: P0, P1, P2, P3, PI2
- Timer registers: T2CON, T2MOD, TCON, TH0, TH1, TH2, TMOD, TL0, TL1, TL2, RCAP2L, RCAP2H
- Serial I/O port registers: SADDR, SADEN, SBUF, SCON
- PCA (Programmable Counter Array) registers: CCON, CCAPMx, CL, CH, CCAPxH, CCAPxL (x: 0 to 4)
- Power and clock control registers: PCON
- Hardware Watchdog Timer registers: WDTRST, WDTPRG
- Interrupt system registers: IE0, IPL0, IPH0, IE1, IPL1, IPH1
- Keyboard Interface registers: KBE, KBF, KBLS
- SPI registers: SPCON, SPSTR, SPDAT
- 2-wire Interface registers: SSCON, SSCS, SSDAT, SSADR
- BRG (Baud Rate Generator) registers: BRL, BDRCON
- Flash register: FCON
- Clock Prescaler register: CKRL
- 32 kHz Sub Clock Oscillator registers: CKSEL, OSSCON
- Others: AUXR, AUXR1, CKCON0, CKCON1

Table 2. C51 Core SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
ACC	E0h	Accumulator								
B	F0h	B Register								
PSW	D0h	Program Status Word	CY	AC	F0	RS1	RS0	OV	F1	P
SP	81h	Stack Pointer								
DPL	82h	Data Pointer Low byte								
DPH	83h	Data Pointer High byte								

Table 3. System Management SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
PCON	87h	Power Control	SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL
AUXR	8Eh	Auxiliary Register 0	-	-	M0		XRS1	XRS0	EXTRAM	AO
AUXR1	A2h	Auxiliary Register 1	-	-	ENBOOT	-	GF3	0	-	DPS
CKRL	97h	Clock Reload Register	-	-	-	-	-	-	-	-
CKSEL	85h	Clock Selection Register	-	-	-	-	-	-	-	CKS
OSCON	86h	Oscillator Control Register	-	-	-	-	-	SCLKT0	OscBEn	OscAEn
CKCKON0	8Fh	Clock Control Register 0	TWIX2	WDTX2	PCAX2	SIX2	T2X2	T1X2	T0X2	X2
CKCKON1	AFh	Clock Control Register 1	-	-	-	-	-	-	-	SPIX2

Table 4. Interrupt SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
IEN0	A8h	Interrupt Enable Control 0	EA	EC	ET2	ES	ET1	EX1	ET0	EX0
IEN1	B1h	Interrupt Enable Control 1	-	-	-	-	-	ESPI	ETWI	EKBD
IPH0	B7h	Interrupt Priority Control High 0	-	PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H
IPL0	B8h	Interrupt Priority Control Low 0	-	PPCL	PT2L	PSL	PT1L	PX1L	PT0L	PX0L
IPH1	B3h	Interrupt Priority Control High 1	-	-	-	-	-	SPIH	IE2CH	KBDH
IPL1	B2h	Interrupt Priority Control Low 1	-	-	-	-	-	SPIL	IE2CL	KBDL

Table 5. Port SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
P0	80h	8-bit Port 0								
P1	90h	8-bit Port 1								
P2	A0h	8-bit Port 2								
P3	B0h	8-bit Port 3								
P4	C0h	8-bit Port 4								
P5	E8h	8-bit Port 5	-	-	-	-				
P5	C7h	8-bit Port 5 (byte addressable)								

Table 6. Flash and EEPROM Data Memory SFR

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
FCON	D1h	Flash Control	FPL3	FPL2	FPL1	FPL0	FPS	FMOD1	FMOD0	FBUSY
EECON		EEPROM data Control								

Table 7. Timer SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
TCON	88h	Timer/Counter 0 and 1 Control	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
TMOD	89h	Timer/Counter 0 and 1 Modes	GATE1	C/T1#	M11	M01	GATE0	C/T0#	M10	M00
TL0	8Ah	Timer/Counter 0 Low Byte								
TH0	8Ch	Timer/Counter 0 High Byte								
TL1	8Bh	Timer/Counter 1 Low Byte								
TH1	8Dh	Timer/Counter 1 High Byte								
WDTRST	A6h	WatchDog Timer Reset								
WDTPRG	A7h	WatchDog Timer Program	-	-	-	-	-	WTO2	WTO1	WTO0
T2CON	C8h	Timer/Counter 2 control	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2#	CP/RL2#
T2MOD	C9h	Timer/Counter 2 Mode	-	-	-	-	-	-	T2OE	DCEN
RCAP2H	CBh	Timer/Counter 2 Reload/Capture High byte								
RCAP2L	CAh	Timer/Counter 2 Reload/Capture Low byte								
TH2	CDh	Timer/Counter 2 High Byte								
TL2	CCh	Timer/Counter 2 Low Byte								

Table 8. PCA SFRs

Mnemo-nic	Add	Name	7	6	5	4	3	2	1	0
CCON	D8h	PCA Timer/Counter Control	CF	CR	-	CCF4	CCF3	CCF2	CCF1	CCF0
CMOD	D9h	PCA Timer/Counter Mode	CIDL	WDTE	-	-	-	CPS1	CPS0	ECF
CL	E9h	PCA Timer/Counter Low byte								
CH	F9h	PCA Timer/Counter High byte								
CCAPM0	DAh	PCA Timer/Counter Mode 0		ECOM0	CAPP0	CAPN0	MAT0	TOG0	PWM0	ECCF0
CCAPM1	DBh	PCA Timer/Counter Mode 1		ECOM1	CAPP1	CAPN1	MAT1	TOG1	PWM1	ECCF1
CCAPM2	DCh	PCA Timer/Counter Mode 2	-	ECOM2	CAPP2	CAPN2	MAT2	TOG2	PWM2	ECCF2
CCAPM3	DDh	PCA Timer/Counter Mode 3		ECOM3	CAPP3	CAPN3	MAT3	TOG3	PWM3	ECCF3
CCAPM4	DEh	PCA Timer/Counter Mode 4		ECOM4	CAPP4	CAPN4	MAT4	TOG4	PWM4	ECCF4
CCAP0H	FAh	PCA Compare Capture Module 0 H	CCAP0H7	CCAP0H6	CCAP0H5	CCAP0H4	CCAP0H3	CCAP0H2	CCAP0H1	CCAP0H0
CCAP1H	FBh	PCA Compare Capture Module 1 H	CCAP1H7	CCAP1H6	CCAP1H5	CCAP1H4	CCAP1H3	CCAP1H2	CCAP1H1	CCAP1H0
CCAP2H	FCh	PCA Compare Capture Module 2 H	CCAP2H7	CCAP2H6	CCAP2H5	CCAP2H4	CCAP2H3	CCAP2H2	CCAP2H1	CCAP2H0
CCAP3H	FDh	PCA Compare Capture Module 3 H	CCAP3H7	CCAP3H6	CCAP3H5	CCAP3H4	CCAP3H3	CCAP3H2	CCAP3H1	CCAP3H0
CCAP4H	FEh	PCA Compare Capture Module 4 H	CCAP4H7	CCAP4H6	CCAP4H5	CCAP4H4	CCAP4H3	CCAP4H2	CCAP4H1	CCAP4H0
CCAP0L	EAh	PCA Compare Capture Module 0 L	CCAP0L7	CCAP0L6	CCAP0L5	CCAP0L4	CCAP0L3	CCAP0L2	CCAP0L1	CCAP0L0
CCAP1L	EBh	PCA Compare Capture Module 1 L	CCAP1L7	CCAP1L6	CCAP1L5	CCAP1L4	CCAP1L3	CCAP1L2	CCAP1L1	CCAP1L0
CCAP2L	ECh	PCA Compare Capture Module 2 L	CCAP2L7	CCAP2L6	CCAP2L5	CCAP2L4	CCAP2L3	CCAP2L2	CCAP2L1	CCAP2L0
CCAP3L	EDh	PCA Compare Capture Module 3 L	CCAP3L7	CCAP3L6	CCAP3L5	CCAP3L4	CCAP3L3	CCAP3L2	CCAP3L1	CCAP3L0
CCAP4L	EEh	PCA Compare Capture Module 4 L	CCAP4L7	CCAP4L6	CCAP4L5	CCAP4L4	CCAP4L3	CCAP4L2	CCAP4L1	CCAP4L0

Table 9. Serial I/O Port SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
SCON	98h	Serial Control	FE/SM0	SM1	SM2	REN	TB8	RB8	TI	RI
SBUF	99h	Serial Data Buffer								
SADEN	B9h	Slave Address Mask								
SADDR	A9h	Slave Address								
BDRCON	9Bh	Baud Rate Control				BRR	TBCK	RBCK	SPD	SRC
BRL	9Ah	Baud Rate Reload								

Table 10. SPI Controller SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
SPCON	C3h	SPI Control	SPR2	SPEN	SSDIS	MSTR	CPOL	CPHA	SPR1	SPR0
SPSTA	C4h	SPI Status	SPIF	WCOL	SSERR	MODF	-	-	-	-
SPDAT	C5h	SPI Data	SPD7	SPD6	SPD5	SPD4	SPD3	SPD2	SPD1	SPD0

Table 11. Two-Wire Interface Controller SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
SSCON	93h	Synchronous Serial control	SSCR2	SSPE	SSSTA	SSSTO	SSI	SSAA	SSCR1	SSCR0
SSCS	94h	Synchronous Serial Status	SSC4	SSC3	SSC2	SSC1	SSC0	0	0	0
SSDAT	95h	Synchronous Serial Data	SSD7	SSD6	SSD5	SSD4	SSD3	SSD2	SSD1	SSD0
SSADR	96h	Synchronous Serial Address	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSGC

Table 12. Keyboard Interface SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
KBLS	9Ch	Keyboard Level Selector	KBLS7	KBLS6	KBLS5	KBLS4	KBLS3	KBLS2	KBLS1	KBLS0
KBE	9Dh	Keyboard Input Enable	KBE7	KBE6	KBE5	KBE4	KBE3	KBE2	KBE1	KBE0
KBF	9Eh	Keyboard Flag Register	KBF7	KBF6	KBF5	KBF4	KBF3	KBF2	KBF1	KBF0

Table 13. EEPROM data Memory SFR

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
EECON	D2h	EEPROM Data Control							EEE	EEBUSY

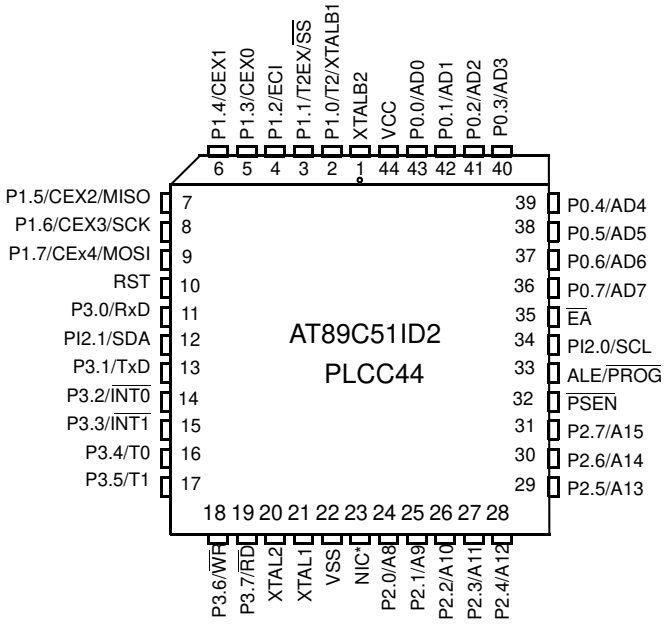
Table below shows all SFRs with their address and their reset value.

Table 14. SFR Mapping

	Bit addressable	**Non Bit addressable**							
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
F8h	PI2 XXXX XX11	CH 0000 0000	CCAP0H XXXX XXXX	CCAP1H XXXX XXXX	CCAP2H XXXX XXXX	CCAP3H XXXX XXXX	CCAP4H XXXX XXXX		FFh
F0h	B 0000 0000								F7h
E8h	P5 bit addressable 1111 1111	CL 0000 0000	CCAP0L XXXX XXXX	CCAP1L XXXX XXXX	CCAP2L XXXX XXXX	CCAP3L XXXX XXXX	CCAP4L XXXX XXXX		EFh
E0h	ACC 0000 0000								E7h
D8h	CCON 00X0 0000	CMOD 00XX X000	CCAPM0 X000 0000	CCAPM1 X000 0000	CCAPM2 X000 0000	CCAPM3 X000 0000	CCAPM4 X000 0000		DFh
D0h	PSW 0000 0000	FCON (1) XXXX 0000	EECON xxxx xx00						D7h
C8h	T2CON 0000 0000	T2MOD XXXX XX00	RCAP2L 0000 0000	RCAP2H 0000 0000	TL2 0000 0000	TH2 0000 0000			CFh
C0h	P4 1111 1111			SPCON 0001 0100	SPSTA 0000 0000	SPDAT XXXX XXXX		P5 byte Addressable 1111 1111	C7h
B8h	IPL0 X000 000	SADEN 0000 0000							BFh
B0h	P3 1111 1111	IEN1 XXXX X000	IPL1 XXXX X000	IPH1 XXXX X111				IPH0 X000 0000	B7h
A8h	IEN0 0000 0000	SADDR 0000 0000						CKCON1 XXXX XXX0	AFh
A0h	P2 1111 1111		AUXR1 XXXX X0X0				WDTRST XXXX XXXX	WDTPRG XXXX X000	A7h
98h	SCON 0000 0000	SBUF XXXX XXXX	BRL 0000 0000	BDRCON XXX0 0000	KBLS 0000 0000	KBE 0000 0000	KBF 0000 0000		9Fh
90h	P1 1111 1111			SSCON 0000 0000	SSCS 1111 1000	SSDAT 1111 1111	SSADR 1111 1110	CKRL 1111 1111	97h
88h	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	AUXR XX00 1000	CKCON0 0000 0000	8Fh
80h	P0 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000		CKSEL XXXX XXX0	OSSCON XXXX X001	PCON 00X1 0000	87h
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

Reserved

Pin Configurations



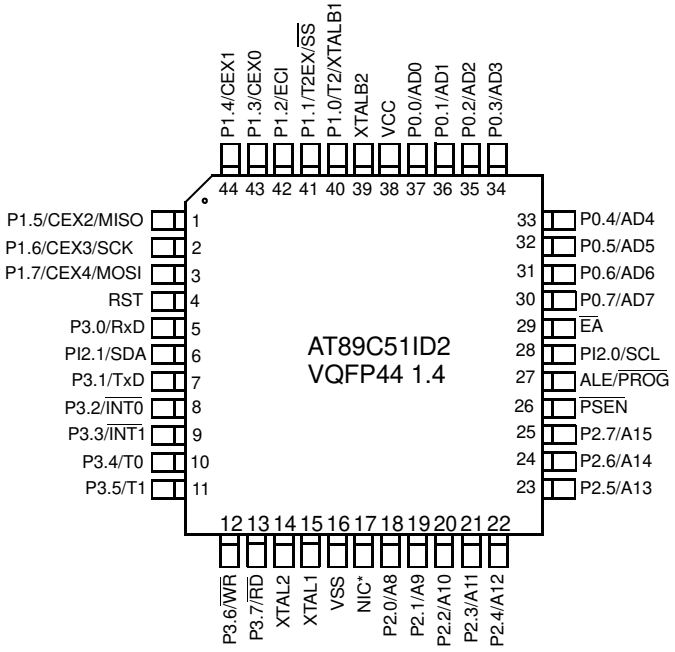


Table 15. Pin Description

Mnemonic	Pin Number PLCC44	Pin Number VQFP44	Type	Name and Function
V_{SS}	22	16	I	**Ground:** 0V reference
V_{CC}	44	38	I	**Power Supply:** This is the power supply voltage for normal, idle and power-down operation
P0.0 - P0.7	43 - 36	37 - 30	I/O	**Port 0**: Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high impedance inputs. Port 0 must be polarized to V_{CC} or V_{SS} in order to prevent any parasitic current consumption. Port 0 is also the multiplexed low-order address and data bus during access to external program and data memory. In this application, it uses strong internal pull-up when emitting 1s. Port 0 also inputs the code bytes during EPROM programming. External pull-ups are required during program verification during which P0 outputs the code bytes.
P1.0 - P1.7	2 - 9	40 - 44 1 - 3	I/O	**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current because of the internal pull-ups. Port 1 also receives the low-order address byte during memory programming and verification. Alternate functions for AT89C51ID2 Port 1 include:
	2	40	I/O	**P1.0**: Input/Output
			I/O	**T2 (P1.0):** Timer/Counter 2 external count input/Clockout
			I	**XTALB1 (P1.0):** Sub Clock input to the inverting oscillator amplifier
	3	41	I/O	**P1.1:** Input/Output
			I	**T2EX:** Timer/Counter 2 Reload/Capture/Direction Control
			I	$\overline{\textbf{SS}}$**:** SPI Slave Select
	4	42	I/O	**P1.2:** Input/Output
			I	**ECI:** External Clock for the PCA
	5	43	I/O	**P1.3:** Input/Output
			I/O	**CEX0:** Capture/Compare External I/O for PCA module 0
	6	44	I/O	**P1.4:** Input/Output
			I/O	**CEX1:** Capture/Compare External I/O for PCA module 1
	7	1	I/O	**P1.5:** Input/Output
			I/O	**CEX2:** Capture/Compare External I/O for PCA module 2
			I/O	**MISO:** SPI Master Input Slave Output line When SPI is in master mode, MISO receives data from the slave peripheral. When SPI is in slave mode, MISO outputs data to the master controller.
	8	2	I/O	**P1.6:** Input/Output
			I/O	**CEX3:** Capture/Compare External I/O for PCA module 3
			I/O	**SCK:** SPI Serial Clock
	9	3	I/O	**P1.7:** Input/Output:
			I/O	**CEX4:** Capture/Compare External I/O for PCA module 4

Table 15. Pin Description (Continued)

Mnemonic	Pin Number		Type	Name and Function
	PLCC44	VQFP44		
			I/O	**MOSI:** SPI Master Output Slave Input line When SPI is in master mode, MOSI outputs data to the slave peripheral. When SPI is in slave mode, MOSI receives data from the master controller.
XTALA1	21	15	I	**Crystal A 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTALA2	20	14	O	**Crystal A 2:** Output from the inverting oscillator amplifier
XTALB1	2	40	I	**Crystal B 1: (**Sub Clock) Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTALB2	1	39	O	**Crystal B 2:** (Sub Clock) Output from the inverting oscillator amplifier
P2.0 - P2.7	24 - 31	18 - 25	I/O	**Port 2**: Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR).In this application, it uses strong internal pull-ups emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 emits the contents of the P2 SFR.
P3.0 - P3.7	11, 13 - 19	5, 7 - 13	I/O	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current because of the internal pull-ups. Port 3 also serves the special features of the 80C51 family, as listed below.
	11	5	I	**RXD (P3.0):** Serial input port
	13	7	O	**TXD (P3.1):** Serial output port
	14	8	I	**$\overline{\text{INT0}}$ (P3.2):** External interrupt 0
	15	9	I	**$\overline{\text{INT1}}$ (P3.3):** External interrupt 1
	16	10	I	**T0 (P3.4):** Timer 0 external input
	17	11	I	**T1 (P3.5):** Timer 1 external input
	18	12	O	**$\overline{\text{WR}}$ (P3.6):** External data memory write strobe
	19	13	O	**$\overline{\text{RD}}$ (P3.7):** External data memory read strobe
P4.0 - P4.7	-	-	I/O	**Port 4:** Port 4 is an 8-bit bidirectional I/O port with internal pull-ups. Port 5 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 4 pins that are externally pulled low will source current because of the internal pull-ups.
P5.0 - P5.7	-	-	I/O	**Port 5:** Port 5 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 5 pins that are externally pulled low will source current because of the internal pull-ups.
PI2.0 - PI2.1	34, 12	28, 6		**Port I2:** Port I2 is an open drain. It can be used as inputs (must be polarized to Vcc with external resistor to prevent any parasitic current consumption).
	34	28	I/O	**SCL (PI2.0): 2-wire Serial Clock** SCL output the serial clock to slave peripherals SCL input the serial clock from master

Table 15. Pin Description (Continued)

Mnemonic	Pin Number		Type	Name and Function
	PLCC44	VQFP44		
	12	6	I/O	**SDA (PI2.1): 2-wire Serial Data** SDA is the bidirectional 2-wire data line
RST	10	4	I	**Reset:** A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V_{SS} permits a power-on reset using only an external capacitor to V_{CC}. This pin is an output when the hardware watchdog forces a system reset.
ALE/$\overline{PROG}$	33	27	O (I)	**Address Latch Enable/Program Pulse:** Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 (1/3 in X2 mode) the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming. ALE can be disabled by setting SFR's AUXR.0 bit. With this bit set, ALE will be inactive during internal fetches.
PSEN	32	26	O	**Program Strobe ENable:** The read strobe to external program memory. When executing code from the external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory. $\overline{PSEN}$ is not activated during fetches from internal program memory.
EA	35	29	I	**External Access Enable:** $\overline{EA}$ must be externally held low to enable the device to fetch code from external program memory locations 0000H to FFFFH. If security level 1 is programmed, $\overline{EA}$ will be internally latched on Reset.

Oscillators

Overview

Two oscillators are available (for AT8xC51IxD2 devices only, the others part number provide only the main high frequency oscillator):

- OSCA used for high frequency: Up to 40 MHz
- OSCB used for low frequency: 32.768 kHz

Several operating modes are available and programmable by software:

- to switch OSCA to OSCB and vice-versa
- to stop OSCA or OSCB to reduce consumption

In order to optimize the power consumption and the execution time needed for a specific task, an internal prescaler feature has been implemented between the selected oscillator and the CPU.

Registers

Table 16. CKSEL Register (for AT8xC51Ix2 only)

CKSEL - Clock Selection Register (85h)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	CKS

Bit Number	Bit Mnemonic	Description
7	-	**Reserved**
6	-	**Reserved**
5	-	**Reserved**
4	-	**Reserved**
3	-	**Reserved**
2	-	**Reserved**
1	-	**Reserved**
0	CKS	**CPU Oscillator Select Bit: (CKS)** Cleared, CPU and peripherals connected to OSCB Set, CPU and peripherals connected to OSCA Programmed by hardware after a Power-up regarding Hardware Security Byte (HSB).HSB.OSC (Default setting, OSCA selected)

Reset Value = 0000 000'HSB.OSC'b (see Hardware Security Byte (HSB))
Not bit addressable

Table 17. OSCCON Register (for AT8xC51Ix2 only)

OSCCON- Oscillator Control Register (86h)

7	6	5	4	3	2	1	0
-	-	-	-	-	SCLKT0	OscBEn	OscAEn

Bit Number	Bit Mnemonic	Description
7	-	**Reserved**
6	-	**Reserved**
5	-	**Reserved**
4	-	**Reserved**
3	-	**Reserved**
2	SCLKT0	**Sub Clock Timer0** Cleared by software to select T0 pin Set by software to select T0 Sub Clock Cleared by hardware after a Power Up
1	OscBEn	**OscB enable bit** Set by software to run OscB Cleared by software to stop OscB Programmed by hardware after a Power-up regarding HSB.OSC (Default cleared, OSCB stopped)
0	OscAEn	**OscA enable bit** Set by software to run OscA Cleared by software to stop OscA Programmed by hardware after a Power-up regarding HSB.OSC(Default Set, OSCA runs)

Reset Value = XXXX X0'$\overline{\text{HSB.OSC}}$''HSB.OSC'b (see Hardware Security Byte (HSB))
Not bit addressable

Table 18. CKRL Register

CKRL - Clock Reload Register

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-

Bit Number	Mnemonic	Description
7:0	CKRL	**Clock Reload Register:** Prescaler value

Reset Value = 1111 1111b
Not bit addressable

Table 19. PCON Register

PCON - Power Control Register (87h)

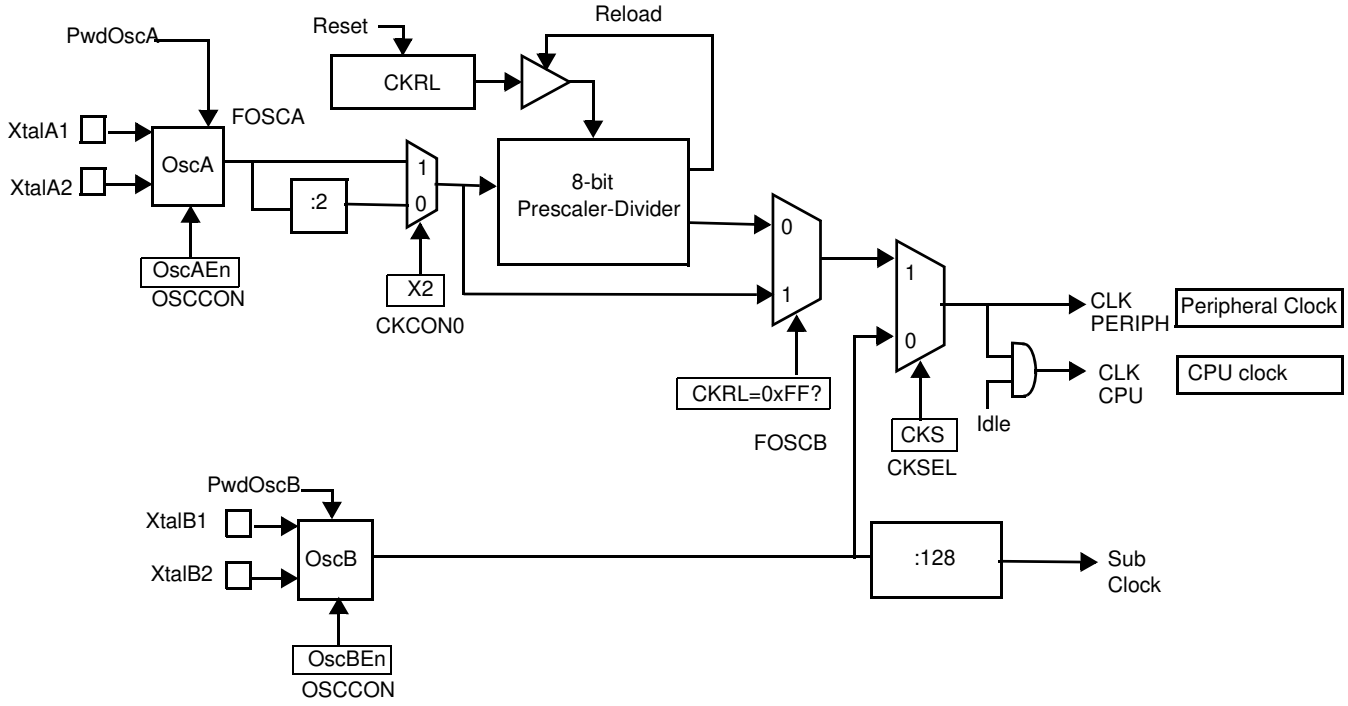
7	6	5	4	3	2	1	0
SMOD1	**SMOD0**	**-**	**POF**	**GF1**	**GF0**	**PD**	**IDL**

Bit Number	Bit Mnemonic	Description
7	SMOD1	**Serial port Mode bit 1** Set to select double baud rate in mode 1, 2 or 3.
6	SMOD0	**Serial port Mode bit 0** Cleared to select SM0 bit in SCON register. Set to select FE bit in SCON register.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	POF	**Power-Off Flag** Cleared to recognize next reset type. Set by hardware when VCC rises from 0 to its nominal voltage. Can also be set by software.
3	GF1	**General purpose Flag** Cleared by software for general purpose usage. Set by software for general purpose usage.
2	GF0	**General purpose Flag** Cleared by software for general purpose usage. Set by software for general purpose usage.
1	PD	**Power-Down mode bit** Cleared by hardware when reset occurs. Set to enter power-down mode.
0	IDL	**Idle mode bit** Cleared by hardware when interrupt or reset occurs. Set to enter idle mode.

Reset Value = 00X1 0000b
Not bit addressable

Functional Block Diagram

Figure 2. Functional Oscillator Block Diagram



Operating Modes

Reset

A hardware RESET puts the Clock generator in the following state:

The selected oscillator depends on OSC bit in Hardware Security Byte (HSB).

HSB.OSC = 1 (Oscillator A selected)

- OscAEn = 1 & OscBEn = 0: OscA is running, OscB is stopped.
- CKS = 1: OscA is selected for CPU.

HSB.OSC = 0 (Oscillator B selected)

- OscAEn = 0 & OscBEn = 1: OscB is running, OscA is stopped.
- CKS = 0: OscB is selected for CPU.

Functional Modes

Normal Modes

- CPU and Peripherals clock depend on the software selection using CKCON0, CKCON1 and CKRL registers
- CKS bit in CKSEL register selects either OscA or OscB
- CKRL register determines the frequency of the OscA clock.
- It is always possible to switch dynamically by software from OscA to OscB, and vice versa by changing CKS bit.

Idle Modes

- IDLE modes are achieved by using any instruction that writes into PCON.0 bit (IDL)
- IDLE modes A and B depend on previous software sequence, prior to writing into PCON.0 bit:
- IDLE MODE A: OscA is running (OscAEn = 1) and selected (CKS = 1)
- IDLE MODE B: OscB is running (OscBEn = 1) and selected (CKS = 0)
- The unused oscillator OscA or OscB can be stopped by software by clearing OscAEn or OscBEn respectively.
- IDLE mode can be canceled either by Reset, or by activation of any enabled interruption
- In both cases, PCON.0 bit (IDL) is cleared by hardware
- Exit from IDLE modes will leave Oscillators control bits (OscEnA, OscEnB, CKS) unchanged.

Power Down Modes

- POWER DOWN modes are achieved by using any instruction that writes into PCON.1 bit (PD)
- POWER DOWN modes A and B depend on previous software sequence, prior to writing into PCON.1 bit:
- Both OscA and OscB will be stopped.
- POWER DOWN mode can be cancelled either by a hardware Reset, an external interruption, or the keyboard interrupt.
- By Reset signal: The CPU will restart according to OSC bit in Hardware Security Bit (HSB) register.
- By INT0 or INT1 interruption, if enabled: (standard behavioral), request on Pads must be driven low enough to ensure correct restart of the oscillator which was selected when entering in Power down.
- By keyboard Interrupt if enabled: a hardware clear of the PCON.1 flag ensure the restart of the oscillator which was selected when entering in Power down.

Table 20. Overview

PCON.1	PCON.0	OscBEn	OscAEn	CKS	Selected Mode	Comment
0	0	0	1	1	NORMAL MODE A, OscB stopped	Default mode after power-up or Warm Reset
0	0	1	1	1	NORMAL MODE A, OscB running	Default mode after power-up or Warm Reset + OscB running
0	0	1	0	0	NORMAL MODE B, OscA stopped	OscB running and selected
0	0	1	1	0	NORMAL MODE B, OscA running	OscB running and selected + OscA running
X	X	0	0	X	INVALID	OscA & OscB cannot be stopped at the same time
X	X	X	0	1	INVALID	OscA must not be stopped, as used for CPU and peripherals
X	X	0	X	0	INVALID	OscB must not be stopped as used for CPU and peripherals
0	1	X	1	1	IDLE MODE A	The CPU is off, OscA supplies the peripherals, OscB can be disabled (OscBEn = 0)

Table 20. Overview (Continued)

PCON.1	PCON.0	OscBEn	OscAEn	CKS	Selected Mode	Comment
0	1	1	X	0	IDLE MODE B	The CPU is off, OscB supplies the peripherals, OscA can be disabled (OscAEn = 0)
1	X	X	1	X	POWER DOWN MODE	The CPU and peripherals are off, OscA and OscB are stopped

Design Considerations

Oscillators Control

- PwdOscA and PwdOscB signals are generated in the Clock generator and used to control the hard blocks of oscillators A and B.
- PwdOscA ='1' stops OscA
- PwdOscB ='1' stops OscB
- The following tables summarize the Operating modes:

PCON.1	OscAEn	PwdOscA	Comments
0	1	0	OscA running
1	X	1	OscA stopped by Power-down mode
0	0	1	OscA stopped by clearing OscAEn

PCON.1	OscBEn	PwdOscB	Comments
0	1	0	OscB running
1	X	1	OscB stopped by Power-down mode
0	0	1	OscB stopped by clearing OscBEn

Prescaler Divider

- A hardware RESET puts the prescaler divider in the following state:
  - CKRL = FFh: $F_{CLK\ CPU} = F_{CLK\ PERIPH} = F_{OSCA}/2$ (Standard C51 feature)
- CKS signal selects OSCA or OSCB: $F_{CLK\ OUT} = F_{OSCA}$ or F_{OSCB}
- Any value between FFh down to 00h can be written by software into CKRL register in order to divide frequency of the selected oscillator:
  - CKRL = 00h: minimum frequency
    $F_{CLK\ CPU} = F_{CLK\ PERIPH} = F_{OSCA}/1020$ (Standard Mode)
    $F_{CLK\ CPU} = F_{CLK\ PERIPH} = F_{OSCA}/510$ (X2 Mode)
  - CKRL = FFh: maximum frequency
    $F_{CLK\ CPU} = F_{CLK\ PERIPH} = F_{OSCA}/2$ (Standard Mode)
    $F_{CLK\ CPU} = F_{CLK\ PERIPH} = F_{OSCA}$ (X2 Mode)

– $F_{CLK\ CPU}$ and $F_{CLK\ PERIPH}$, for CKRL≠0xFF
In X2 Mode:

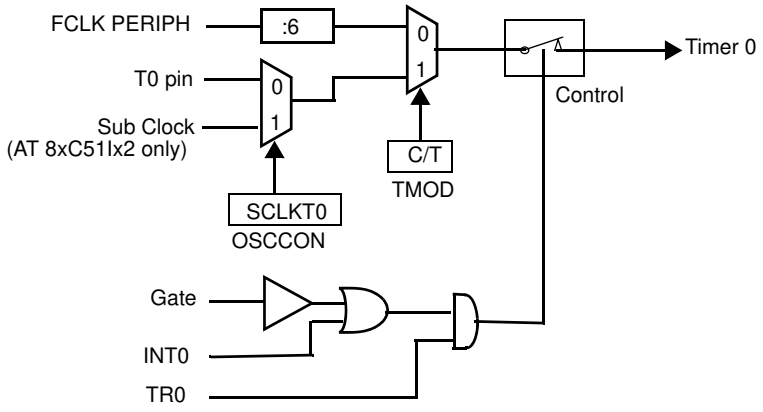
$$F_{CPU} = F_{CLKPERIPH} = \frac{F_{OSCA}}{2 \times (255 - CKRL)}$$

In X1 Mode:

$$F_{CPU} = F_{CLKPERIPH} = \frac{F_{OSCA}}{4 \times (255 - CKRL)}$$

Timer 0: Clock Inputs

Figure 1. Timer 0: Clock Inputs



Note: The SCLKT0 bit in OSCCON register allows to select Timer 0 Subsidiary clock.

SCLKT0 = 0: Timer 0 uses the standard T0 pin as clock input (Standard mode)

SCLKT0 = 1: Timer 0 uses the special Sub Clock as clock input, this feature can be use as periodic interrupt for time clock.

Enhanced Features

In comparison to the original 80C52, the AT89C51ID2 implements some new features, which are:

- X2 option
- Dual Data Pointer
- Extended RAM
- Programmable Counter Array (PCA)
- Hardware Watchdog
- SPI interface
- 4-level interrupt priority system
- power-off flag
- ONCE mode
- ALE disabling
- Enhanced features on the UART and the timer 2

X2 Feature

The AT89C51ID2 core needs only 6 clock periods per machine cycle. This feature called 'X2' provides the following advantages:

- Divide frequency crystals by 2 (cheaper crystals) while keeping same CPU power.
- Save power consumption while keeping same CPU power (oscillator power saving).
- Save power consumption by dividing dynamically the operating frequency by 2 in operating and idle modes.
- Increase CPU power by 2 while keeping same crystal frequency.

In order to keep the original C51 compatibility, a divider by 2 is inserted between the XTAL1 signal and the main clock input of the core (phase generator). This divider may be disabled by software.

Description

The clock for the whole circuit and peripherals is first divided by two before being used by the CPU core and the peripherals.

This allows any cyclic ratio to be accepted on XTAL1 input. In X2 mode, as this divider is bypassed, the signals on XTAL1 must have a cyclic ratio between 40 to 60%.

Figure 3 shows the clock generation block diagram. X2 bit is validated on the rising edge of the XTAL1÷2 to avoid glitches when switching from X2 to STD mode. Figure 4 shows the switching mode waveforms.

Figure 3. Clock Generation Diagram

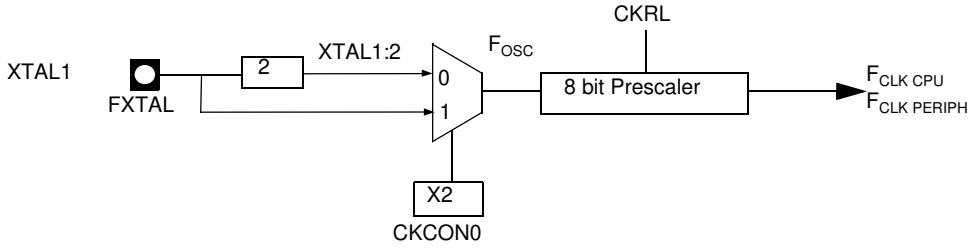
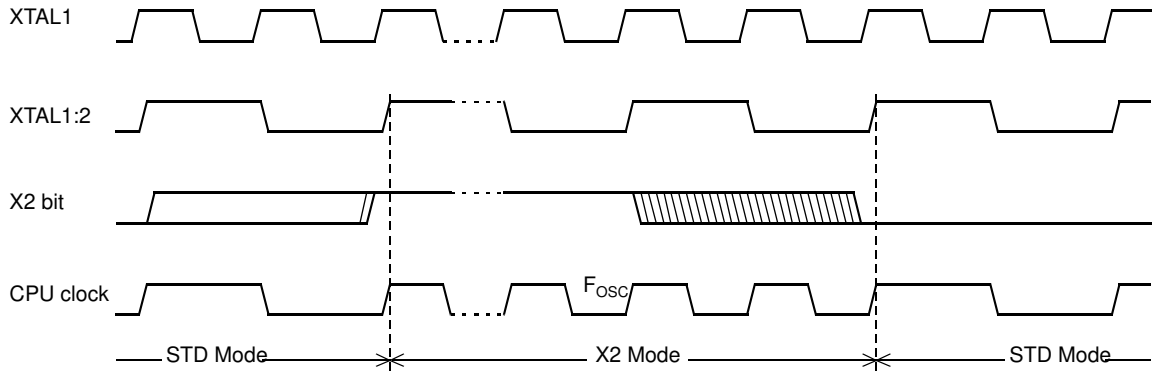


Figure 4. Mode Switching Waveforms



The X2 bit in the CKCON0 register (see Table 21) allows a switch from 12 clock periods per instruction to 6 clock periods and vice versa. At reset, the speed is set according to X2 bit of Hardware Security Byte (HSB). By default, Standard mode is active. Setting the X2 bit activates the X2 feature (X2 mode).

The T0X2, T1X2, T2X2, UartX2, PcaX2, and WdX2 bits in the CKCON0 register (See Table 21.) and SPIX2 bit in the CKCON1 register (see Table 22) allows a switch from standard peripheral speed (12 clock periods per peripheral clock cycle) to fast peripheral speed (6 clock periods per peripheral clock cycle). These bits are active only in X2 mode.

Table 21. CKCON0 Register

CKCON0 - Clock Control Register (8Fh)

7	6	5	4	3	2	1	0
TWIX2	WDX2	PCAX2	SIX2	T2X2	T1X2	T0X2	X2

Bit Number	Bit Mnemonic	Description
7	TWIX2	**2-wire clock** (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect) Cleared to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
6	WDX2	**Watchdog Clock** (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect). Cleared to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
5	PCAX2	**Programmable Counter Array Clock** (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect). Cleared to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
4	SIX2	**Enhanced UART Clock (Mode 0 and 2)** (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect). Cleared to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
3	T2X2	**Timer2 Clock** (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect). Cleared to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
2	T1X2	**Timer1 Clock** (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect). Cleared to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
1	T0X2	**Timer0 Clock** (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect). Cleared to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
0	X2	**CPU Clock** Cleared to select 12 clock periods per machine cycle (STD mode) for CPU and all the peripherals. Set to select 6clock periods per machine cycle (X2 mode) and to enable the individual peripherals'X2' bits. Programmed by hardware after Power-up regarding Hardware Security Byte (HSB), Default setting, X2 is cleared.

Reset Value = 0000 000'HSB. X2'b (See "Hardware Security Byte")
Not bit addressable

Table 22. CKCON1 Register

CKCON1 - Clock Control Register (AFh)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	SPIX2

Bit Number	Bit Mnemonic	Description
7	-	**Reserved**
6	-	**Reserved**
5	-	**Reserved**
4	-	**Reserved**
3	-	**Reserved**
2	-	**Reserved**
1	-	**Reserved**
0	SPIX2	**SPI** (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect). Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.

Reset Value = XXXX XXX0b
Not bit addressable

Dual Data Pointer Register DPTR

The additional data pointer can be used to speed up code execution and reduce code size.

The dual DPTR structure is a way by which the chip will specify the address of an external data memory location. There are two 16-bit DPTR registers that address the external memory, and a single bit called DPS = AUXR1.0 (see Table 23) that allows the program code to switch between them (Refer to Figure 5).

Figure 5. Use of Dual Pointer