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Features

- Compatible with MCS®51 Products
- 20 MIPS Throughput at 20 MHz Clock Frequency and 2.4V, 85°C Operating Conditions
- Single Clock Cycle per Byte Fetch
- 2/4K Bytes of In-System Programmable (ISP) Flash Memory
  - Serial Interface for Program Downloading
  - 32-byte Fast Page Programming Mode
  - 32-byte User Signature Array
- 2.4V to 5.5V V_{CC} Operating Range
- Fully Static Operation: 0 Hz to 20 MHz
- 2-level Program Memory Lock
- 256 x 8 Internal RAM
- Hardware Multiplier
- 15 Programmable I/O Lines
- Configurable I/O with Quasi-bidirectional, Input, Push-pull Output, and Open-drain Modes
- Enhanced UART with Automatic Address Recognition and Framing Error Detection
- Enhanced SPI with Double-buffered Send/Receive
- Programmable Watchdog Timer with Software Reset
- 4-level Interrupt Priority
- Analog Comparator with Selectable Interrupt and Debouncing
- Two 16-bit Enhanced Timer/Counters with 8-bit PWM
- Brown-out Detector and Power-off Flag
- Internal Power-on Reset
- Low Power Idle and Power-down Modes
- Interrupt Recovery from Power-down Mode

8-bit Microcontroller with 2/4-Kbyte Flash

AT89LP2052
AT89LP4052

1. Description

The AT89LP2052/LP4052 is a low-power, high-performance CMOS 8-bit microcontroller with 2/4K bytes of In-System Programmable Flash memory. The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry-standard MCS-51 instruction set. The AT89LP2052/LP4052 is built around an enhanced CPU core that can fetch a single byte from memory every clock cycle. In the classic 8051 architecture, each fetch required 6 clock cycles, forcing instructions to execute in 12, 24 or 48 clock cycles. In the AT89LP2052/LP4052 CPU, instructions need only 1 to 4 clock cycles providing 6 to 12 times more throughput than the standard 8051. Seventy percent of instructions need only as many clock cycles as they have bytes to execute, and most of the remaining instructions require only one additional clock. The enhanced CPU core is capable of 20 MIPS throughput whereas the classic 8051 CPU can deliver only 4 MIPS at the same current consumption. Conversely, at the same throughput as the classic 8051, the new CPU core runs at a much lower speed and thereby greatly reduces power consumption.

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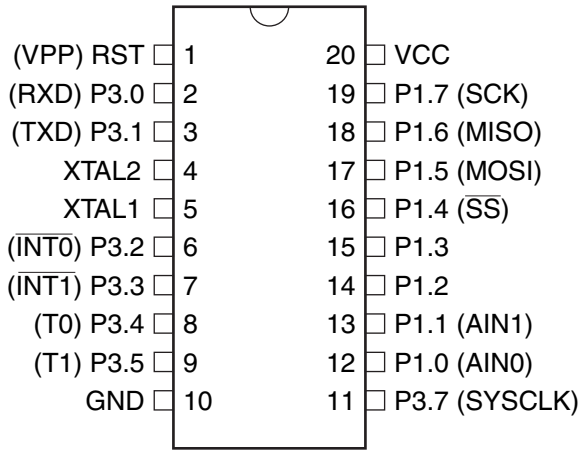
The two timer/counters in the AT89LP2052/LP4052 are enhanced with two new modes. Mode 0 can be configured as a variable 9- to 16-bit timer/counter and Mode 1 can be configured as a 16-bit auto-reload timer/counter. In addition both timer/counters may be configured as 8-bit Pulse Width Modulators with 8-bit prescalers.

The I/O ports of the AT89LP2052/LP4052 can be independently configured in one of four operating modes. In quasi-bidirectional mode, the ports operate as in the classic 8051. In input mode, the ports are tri-stated. Push-pull output mode provides full CMOS drivers and open-drain mode provides just a pull-down.

2. Pin Configuration

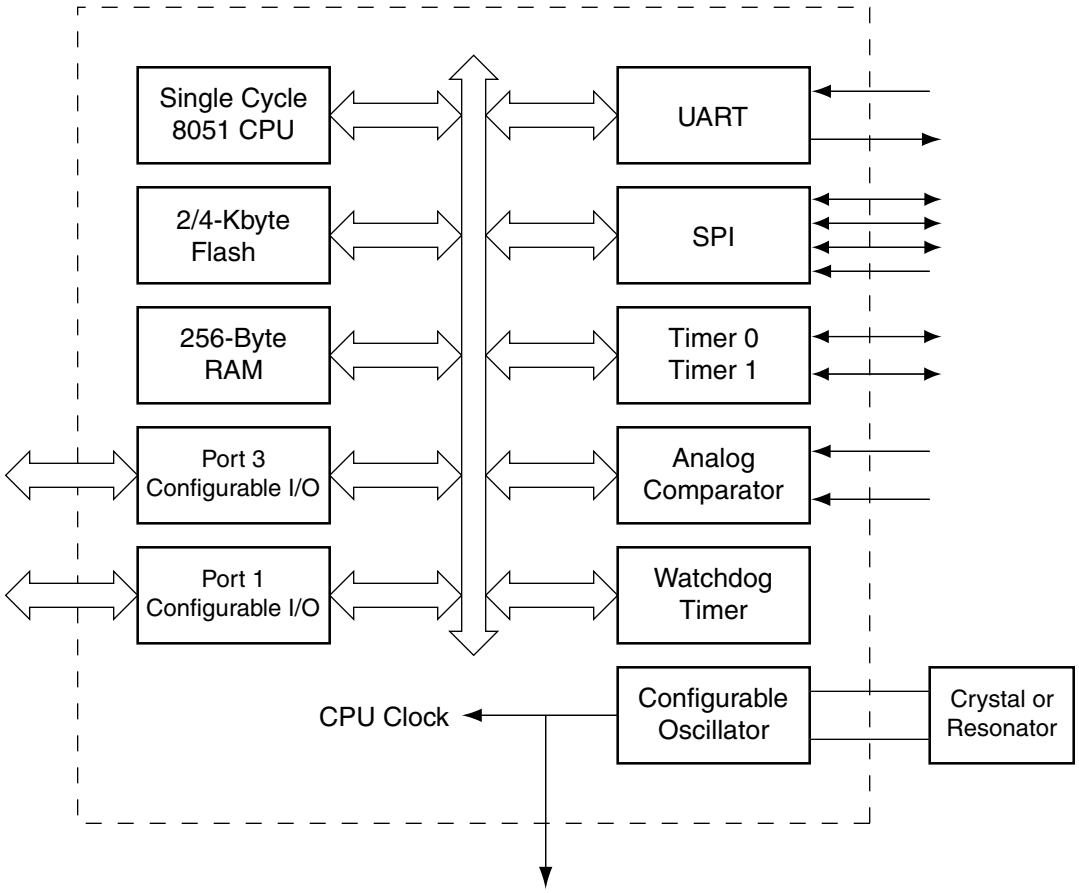
2.1 20-lead PDIP/SOIC/TSSOP



3. Pin Description

Pin	Symbol	Type	Description
1	RST	I I	**RST**: External **Active-High** Reset input. **VPP**: Parallel Programming Voltage. Raise to 12V to enable programming.
2	P3.0	I/O I	**P3.0**: User-configurable I/O Port 3 bit 0. **RXD**: Serial Port Receiver input.
3	P3.1	I/O O	**P3.1**: User-configurable I/O Port 3 bit 1. **TXD**: Serial Port Transmitter output.
4	XTAL2	O	**XTAL2**: Output from inverting oscillator amplifier.
5	XTAL1	I	**XTAL1**: Input to the inverting oscillator amplifier and internal clock generation circuits.
6	P3.2	I/O I	**P3.2**: User-configurable I/O Port 3 bit 2. **INT0**: External Interrupt 0 input.
7	P3.3	I/O I	**P3.3**: User-configurable I/O Port 3 bit 3. **INT1**: External Interrupt 1input.
8	P3.4	I/O I/O	**P3.4**: User-configurable I/O Port 3 bit 4. **T0**: Timer 0 Counter input or PWM output
9	P3.5	I/O I/O	**P3.5**: User-configurable I/O Port 3 bit 5. **T1**: Timer 1 Counter input or PWM output
10	GND	I	Ground
11	P3.7	I/O O	**P3.7**: User-configurable I/O Port 3 bit 7. **SYSCLK**: System Clock Output when System Clock Fuse is enabled.
12	P1.0	I/O I	**P1.0**: User-configurable I/O Port 1 bit 0. **AIN0**: Analog Comparator Positive input.
13	P1.1	I/O I	**P1.1**: User-configurable I/O Port 1 bit 1. **AIN1**: Analog Comparator Negative input.
14	P1.2	I/O	**P1.2**: User-configurable I/O Port 1 bit 2.
15	P1.3	I/O	**P1.3**: User-configurable I/O Port 1 bit 3
16	P1.4	I/O I	**P1.4**: User-configurable I/O Port 1 bit 4. $\overline{\textbf{SS}}$: SPI slave select.
17	P1.5	I/O I/O	**P1.5**: User-configurable I/O Port 1 bit 5. **MOSI**: SPI master-out/slave-in. When configured as master, this pin is an output. When configured as slave, this pin is an input.
18	P1.6	I/O I/O	**P1.6**: User-configurable I/O Port 1 bit 6. **MISO**: SPI master-in/slave-out. When configured as master, this pin is an input. When configured as slave, this pin is an output.
19	P1.7	I/O I/O	**P1.7**: User-configurable I/O Port 1 bit 7. **SCK**: SPI Clock. When configured as master, this pin is an output. When configured as slave, this pin is an input.
20	VCC	I	Supply Voltage

4. Block Diagram



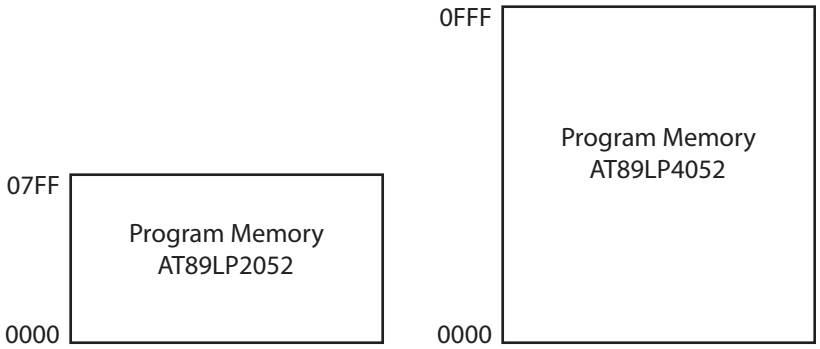
5. Memory Organization

The AT89LP2052/LP4052 uses a Harvard Architecture with separate address spaces for program and data memory. The program memory has a regular linear address space with support for up to 64K bytes of directly addressable application code. The data memory has 256 bytes of internal RAM which is divided into regions that may be accessed by different instruction classes. The AT89LP2052/LP4052 does not support external RAM.

5.1 Program Memory

The AT89LP2052/LP4052 contains 2/4K bytes of on-chip In-System Programmable Flash memory for program storage. The Flash memory has an endurance of at least 10,000 write/erase cycles. Section 23. “Programming the Flash Memory” on page 57 contains a detailed description on Flash Programming in ISP or Parallel Programming mode. The reset and interrupt vectors are located within the first 59 bytes of program memory (see Section 14. “Interrupts” on page 16). Constant tables can be allocated within the entire 2/4-Kbyte program memory address space for access by the MOVC instruction.

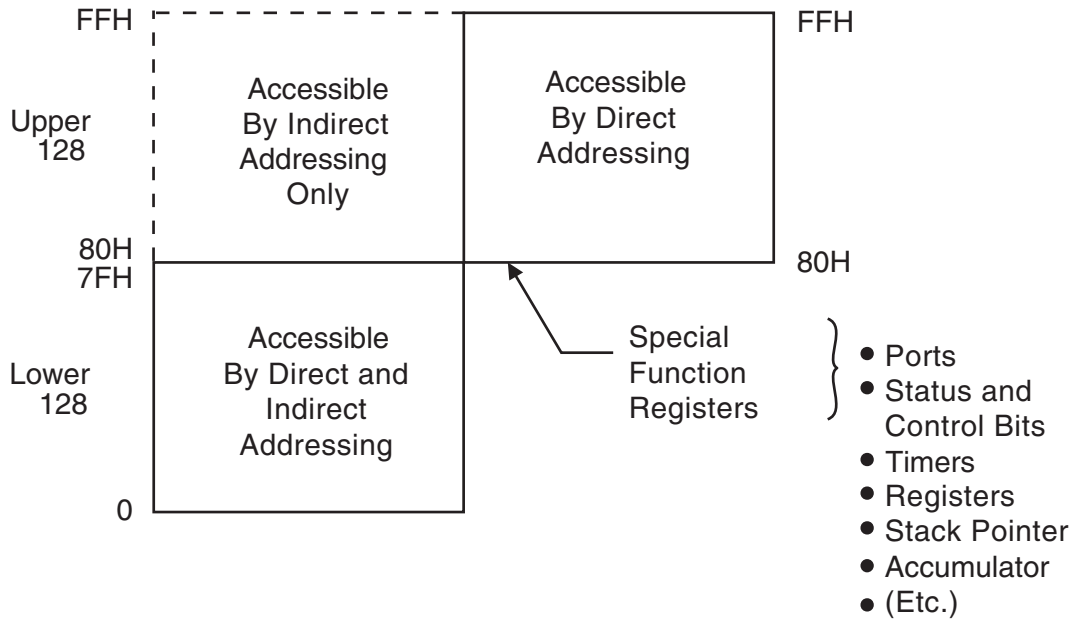
Figure 5-1. Program Memory Map



5.2 Data Memory

The AT89LP2052/LP4052 contains 256 bytes of general SRAM data memory plus 128 bytes of I/O memory. The lower 128 bytes of data memory may be accessed through both direct and indirect addressing. The upper 128 bytes of data memory and the 128 bytes of I/O memory share the same address space (see Figure 5-2). The upper 128 bytes of data memory may only be accessed using indirect addressing. The I/O memory can only be accessed through direct addressing and contains the Special Function Registers (SFRs). The lowest 32 bytes of data memory are grouped into 4 banks of 8 registers each. The RS0 and RS1 bits (PSW.3 and PSW.4) select which register bank is in use. Instructions using register addressing will only access the currently specified bank. The AT89LP2052/LP4052 does not support external data memory.

Figure 5-2. Data Memory Map



6. Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 6-1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect. User software should not write to these unlisted locations, since they may be used in future products to invoke new features.

Table 6-1. AT89LP2052/LP4052 SFR Map and Reset Values

0F8H									0FFH
0F0H	B* 0000 0000								0F7H
0E8H									0EFH
0E0H	ACC* 0000 0000								0E7H
0D8H									0DFH
0D0H	PSW* 0000 0000					SPCR 0000 0000			0D7H
0C8H									0CFH
0C0H			P1M0 1111 1111	P1M1 0000 0000			P3M0 1111 1111	P3M1 0000 0000	0C7H
0B8H	IP* x0x0 0000	SADEN 0000 0000							0BFH
0B0H	P3* 1111 1111							IPH x0x0 0000	0B7H
0A8H	IE* 00x0 0000	SADDR 0000 0000	SPSR 000x xx00						0AFH
0A0H							WDTRST (write-only)	WDTCON 0000 x000	0A7H
98H	SCON* 0000 0000	SBUF xxxx xxxx							9FH
90H	P1* 1111 1111	TCONB 0010 0100	RL0 0000 0000	RL1 0000 0000	RH0 0000 0000	RH1 0000 0000		ACSR xx00 0000	97H
88H	TCON* 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000			8FH
80H		SP 0000 0111	DPL 0000 0000	DPH 0000 0000			SPDR xxxx xxxx	PCON 000x 0000	87H

Note: *These SFRs are bit-addressable.

7. Comparison to Standard 8051

The AT89LP2052/LP4052 is part of a family of devices with enhanced features that are fully binary compatible with the MCS-51 instruction set. In addition, most SFR addresses, bit assignments, and pin alternate functions are identical to Atmel's existing standard 8051 products. However, due to the high performance nature of the device, some system behaviors are different from those of Atmel's standard 8051 products such as AT89S52 or AT89S2051. The differences from the standard 8051 are outlined in the following paragraphs.

7.1 System Clock

The CPU clock frequency equals the external XTAL1 frequency. The oscillator is no longer divided by 2 to provide the internal clock, and x2 mode is not supported.

7.2 Instruction Execution with Single-cycle Fetch

The CPU fetches one code byte from memory every clock cycle instead of every six clock cycles. This greatly increases the throughput of the CPU. As a consequence, the CPU no longer executes instructions in 12 to 48 clock cycles. Each instruction executes in only 1 to 4 clock cycles. See Section 22. “Instruction Set Summary” on page 52 for more details.

7.3 Interrupt Handling

The interrupt controller polls the interrupt flags during the last clock cycle of any instruction. In order for an interrupt to be serviced at the end of an instruction, its flag needs to have been latched as active during the next to last clock cycle of the instruction, or in the last clock cycle of the previous instruction if the current instruction executes in only a single clock cycle.

7.4 Timer/Counters

The Timer/Counters increment at a rate of once per clock cycle. This compares to once every 12 clocks in the standard 8051.

7.5 Serial Port

The baud rate of the UART in Mode 0 is 1/2 the clock frequency, compared to 1/12 the clock frequency in the standard 8051. In should also be noted that when using Timer 1 to generate the baud rate in Mode 1 or Mode 3, the timer counts at the clock frequency and not at 1/12 the clock frequency. To maintain the same baud rate in the AT89LP2052/LP4052 while running at the same frequency as a standard 8051, the time-out period must be 12 times longer. Mode 1 of Timer 1 supports 16-bit auto-reload to facilitate longer time-out periods for generating low baud rates.

7.6 Watchdog Timer

The Watchdog Timer in AT89LP2052/LP4052 counts at a rate of once per clock cycle. This compares to once every 12 clocks in the standard 8051.

7.7 I/O Ports

The I/O ports of the AT89LP2052/LP4052 may be configured in four different modes. On the AT89LP2052/LP4052, all the I/O ports revert to input-only (tri-stated) mode at power-up or reset. In the standard 8051, all ports are weakly pulled high during power-up or reset. To enable 8051-like ports, the ports must be put into quasi-bidirectional mode by clearing the P1M0 and P3M0 SFRs.

7.8 Reset

The RST pin in the AT89LP2052/LP4052 has different pulse width requirements than the standard 8051. The RST pin is sampled every clock cycle and must be held **high** for a minimum of two clock cycles, instead of 24 clock cycles, to be recognized as a valid reset pulse

8. Enhanced CPU

The AT89LP2052/LP4052 uses an enhanced 8051 CPU that runs at 6 to 12 times the speed of standard 8051 devices (or 3 to 6 times the speed of X2-mode 8051 devices). The increase in performance is due to two factors. First, the CPU fetches one instruction byte from the code memory every clock cycle. Second, the CPU uses a simple two-stage pipeline to fetch and execute instructions in parallel. This basic pipelining concept allows the CPU to obtain up to 1 MIPS per MHz. A simple example is shown in Figure 8-1.

The MCS-51 instruction set allows for instructions of variable length from 1 to 3 bytes. In a single-clock-per-byte-fetch system this means each instruction takes at least as many clocks as it has bytes to execute. A majority of the instructions in the AT89LP2052/LP4052 follow this rule: the instruction execution time in clock cycles equals the number of bytes per instruction with a few exceptions. Branches and Calls require an additional cycle to compute the target address and some other complex instructions require multiple cycles. See Section 22. “Instruction Set Summary” on page 52 for more detailed information on individual instructions. Figures 8-2 and 8-3 show examples of one- and two-byte instructions.

Figure 8-1. Parallel Instruction Fetches and Executions

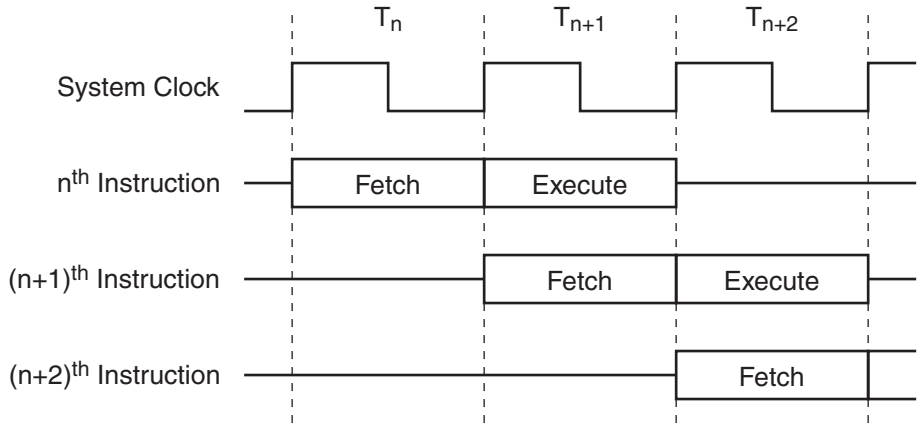


Figure 8-2. Single-cycle ALU Operation (Example: INC R0)

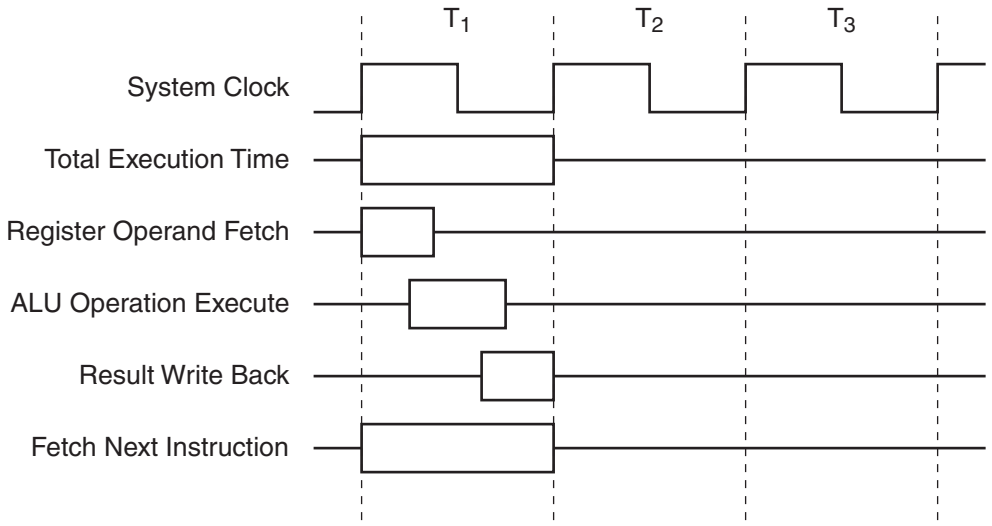
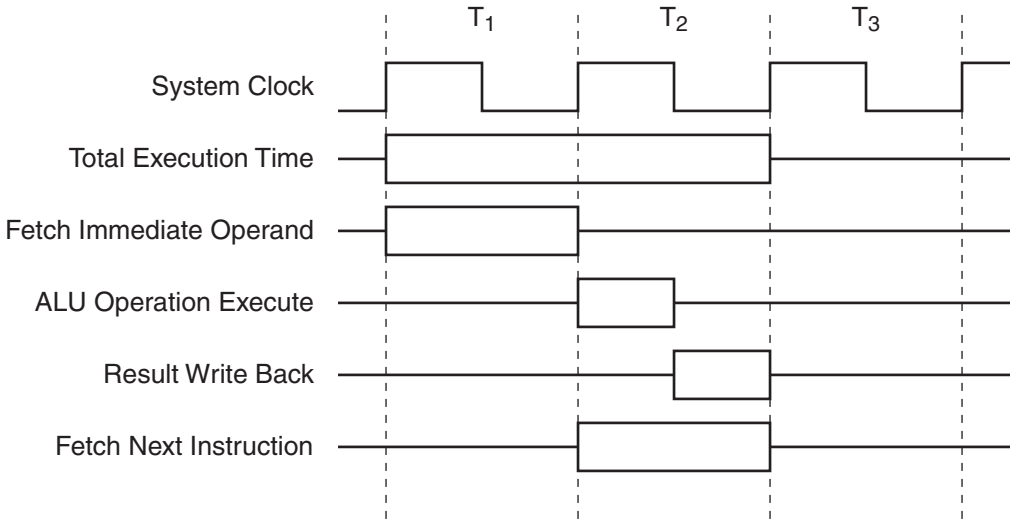


Figure 8-3. Two-Cycle ALU Operation (Example: ADD A, #data)



9. Restrictions on Certain Instructions

The AT89LP2052/LP4052 is an economical and cost-effective member of Atmel's growing family of microcontrollers. It contains 2/4K bytes of Flash program memory. It is fully compatible with the MCS-51 architecture, and can be programmed using the MCS-51 instruction set. However, there are a few considerations one must keep in mind when utilizing certain instructions to program this device. All the instructions related to jumping or branching should be restricted such that the destination address falls within the physical program memory space of the device, which is 2K bytes for the AT89LP2052 and 4K bytes for the AT89LP4052. This should be the responsibility of the software programmer. For example, LJMP 7E0H would be a valid instruction for the AT89LP2052 (with 2K bytes of memory), whereas LJMP 900H would not.

9.1 Branching Instructions

The LCALL, LJMP, ACALL, AJMP, SJMP, and JMP @A+DPTR unconditional branching instructions will execute correctly as long as the programmer keeps in mind that the destination branching address must fall within the physical boundaries of the program memory size (locations 000H to 7FFH for the AT89LP2052, 000H to FFFH for the AT89LP4052). Violating the physical space limits may cause unknown program behavior. With the CJNE [...], DJNZ [...], JB, JNB, JC, JNC, JBC, JZ, and JNZ conditional branching instructions, the same previous rule applies. Again, violating the memory boundaries may cause erratic execution. For applications involving interrupts, the normal interrupt service routine address locations of the 8051 family architecture have been preserved.

9.2 MOVX-related Instructions, Data Memory

External DATA memory access is not supported in this device, nor is external PROGRAM memory execution. Therefore, no MOVX [...] instructions should be included in the program. A typical 8051 assembler will still assemble instructions, even if they are written in violation of the restrictions mentioned above. It is the responsibility of the user to know the physical features and limitations of the device being used and to adjust the instructions used accordingly.

10. System Clock

The system clock is generated directly from one of two selectable clock sources. The two sources are the on-chip crystal oscillator and external clock source. No internal clock division is used to generate the CPU clock from the system clock.

10.1 Crystal Oscillator

When enabled, the internal inverting oscillator amplifier is connected between XTAL1 and XTAL2 for connection to an external quartz crystal or ceramic resonator. When using the crystal oscillator, XTAL2 should not be used to drive a board-level clock.

10.2 External Clock Source

The external clock option is selected by setting the Oscillator Bypass fuse. This disables the amplifier and allows XTAL1 to be driven directly by the clock source. XTAL2 may be left unconnected.

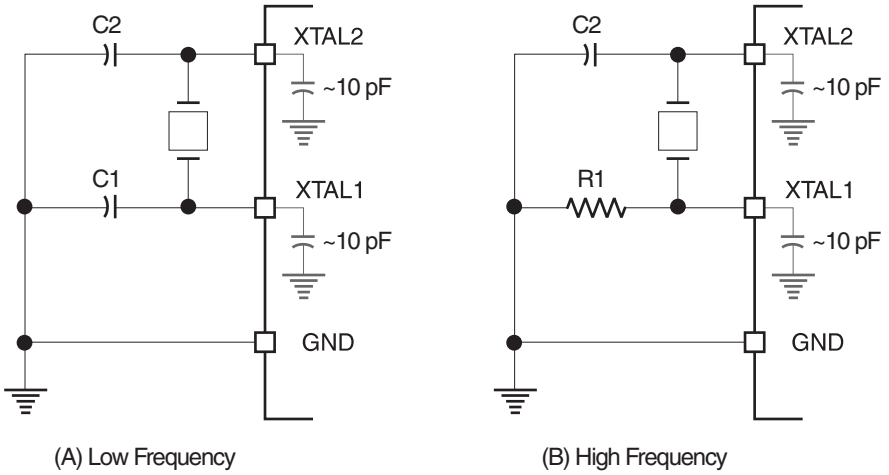
10.3 System Clock Out

When the System Clock Out fuse is enabled, P3.7 will output the system clock with no division using the push-pull output mode. During Power-down the system clock will output as “1”.

11. Oscillator Characteristics

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 11-1. Either a quartz crystal or ceramic resonator may be used. For frequencies above 16MHz it is recommended that C1 be replaced with R1 for improved startup performance. Note that the internal structure of the devices adds about 10 pF of capacitance to both XTAL1 and XTAL2. The total capacitance on XTAL1 or XTAL2, including the external load capacitor (C1/C2) plus internal device load, board trace and crystal loadings, should not exceed 20 pF. Figure 11-2, 11-3, 11-4 and 11-5 illustrate the relationship between clock loading and the respective resulting clock amplitudes.

Figure 11-1. Oscillator Connections



Note: C1, C2 = 0–10 pF for Crystals
= 0–10 pF for Ceramic Resonators
R1 = 4–5 MΩ

Figure 11-2. Quartz Crystal Clock Source (A)

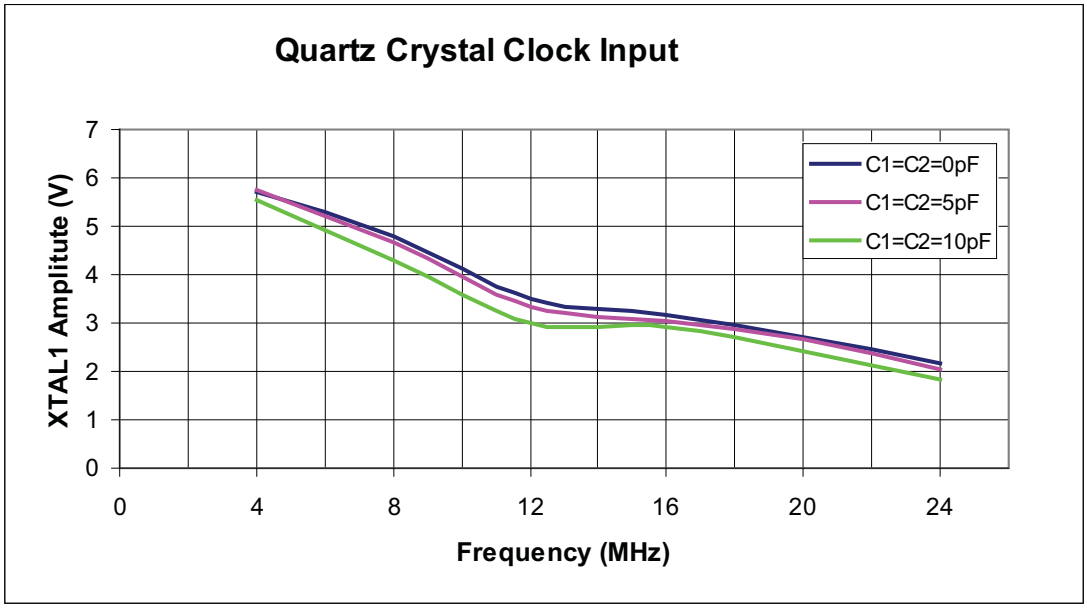


Figure 11-3. Quartz Crystal Clock Source (B)

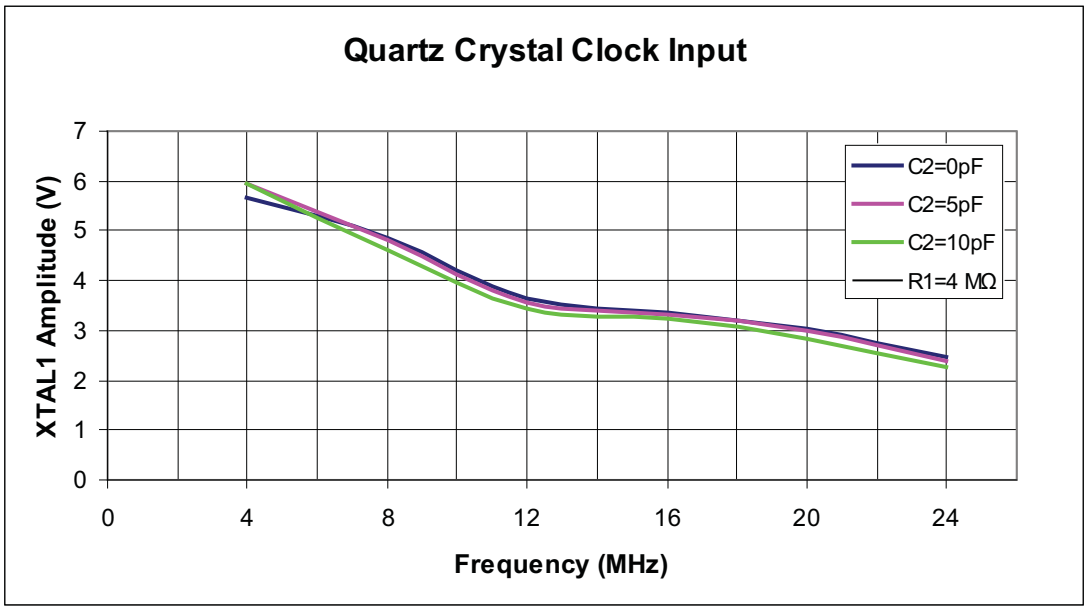


Figure 11-4. Ceramic Resonator Clock Source (A)

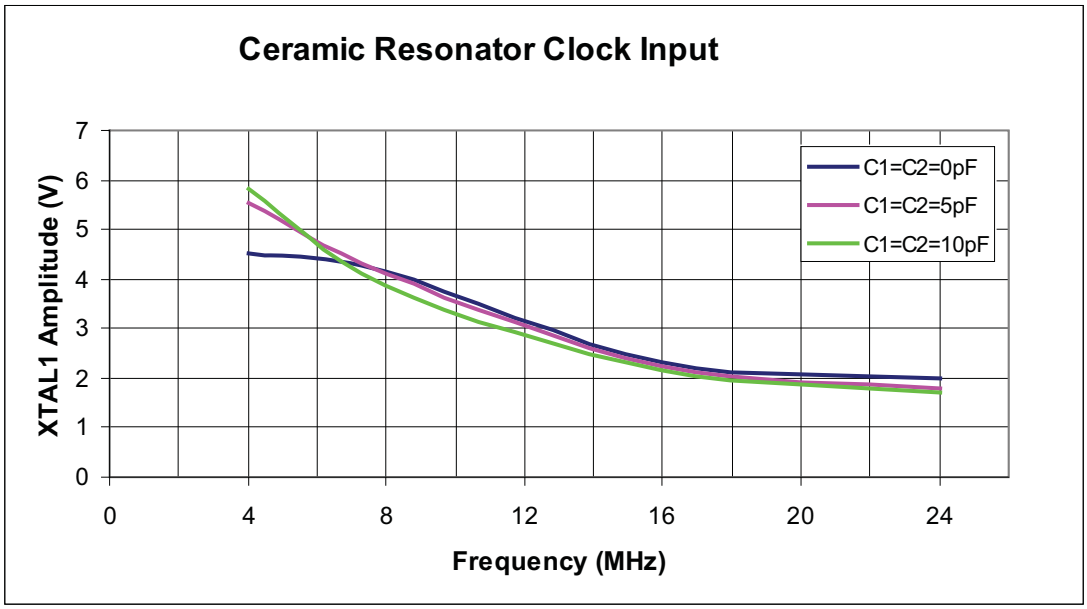
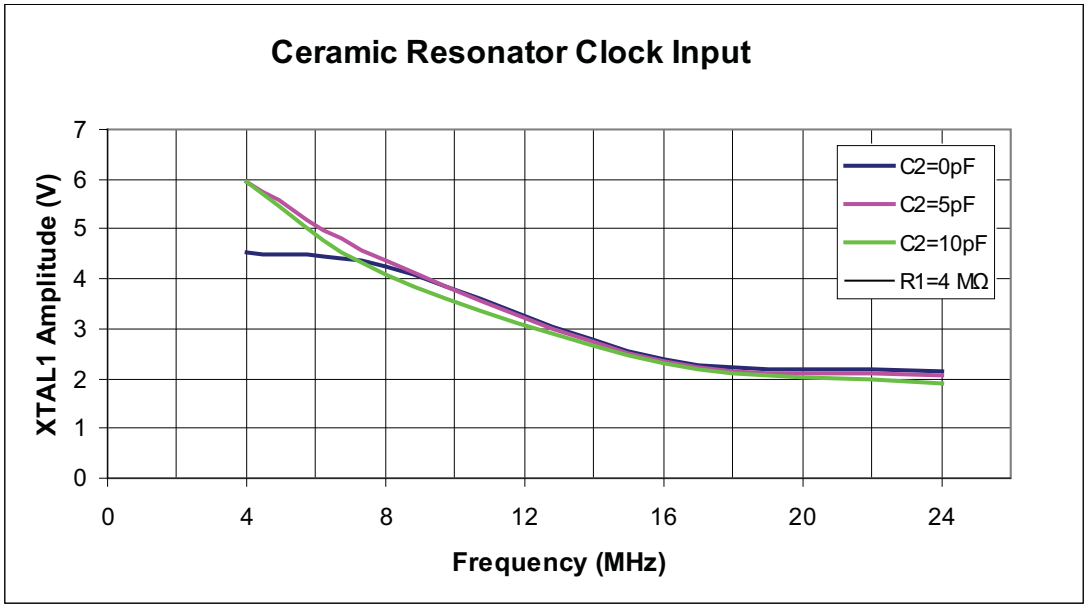
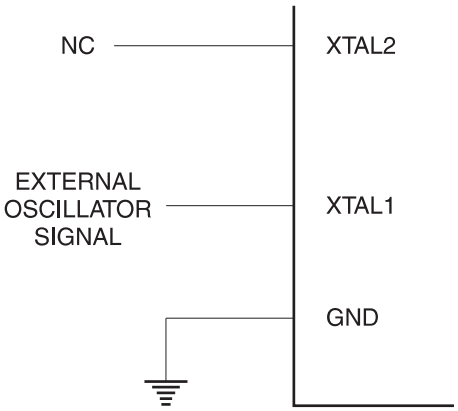


Figure 11-5. Ceramic Resonator Clock Source (B)



To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 11-6.

Figure 11-6. External Clock Drive Configuration



12. Reset

During reset, all I/O Registers are set to their initial values, the port pins are tri-stated, and the program starts execution from the Reset Vector, 0000H. The AT89LP2052/LP4052 has four sources of reset: power-on reset, brown-out reset, external reset, and watchdog reset.

12.1 Power-on Reset

A Power-on Reset (POR) is generated by an on-chip detection circuit. The detection level is nominally 1.4V. The POR is activated whenever V_{CC} is below the detection level. The POR circuit can be used to trigger the start-up reset or to detect a supply voltage failure in devices without a brown-out detector. The POR circuit ensures that the device is reset from power-on. When V_{CC} reaches the Power-on Reset threshold voltage, the POR delay counter determines how long the device is kept in POR after V_{CC} rise. The POR signal is activated again, without any delay, when V_{CC} falls below the POR threshold level. A Power-on Reset (i.e. a cold reset) will set the POF flag in PCON.

12.2 Brown-out Reset

The AT89LP2052/LP4052 has an on-chip Brown-out Detection (BOD) circuit for monitoring the V_{CC} level during operation by comparing it to a fixed trigger level. The trigger level for the BOD is nominally 2.2V. The purpose of the BOD is to ensure that if V_{CC} fails or dips while executing at speed, the system will gracefully enter reset without the possibility of errors induced by incorrect execution. When V_{CC} decreases to a value below the trigger level, the Brown-out Reset is immediately activated. When V_{CC} increases above the trigger level, the BOD delay counter starts the MCU after the time-out period has expired.

12.3 External Reset

The RST pin functions as an active-high reset input. The pin must be held high for at least two clock cycles to trigger the internal reset. RST also serves as the In-System Programming (ISP) enable. ISP is enabled when the external reset pin is held high and the ISP Enable fuse is enabled.

12.4 Watchdog Reset

When the Watchdog times out, it will generate an internal reset pulse lasting 16 clock cycles. Watchdog reset will also set the WDTOVF flag in WDTCON. To prevent a Watchdog reset, the watchdog reset sequence 1EH/E1H must be written to WDTRST before the Watchdog times out. A Watchdog reset will occur only if the Watchdog has been enabled. The Watchdog is disabled by default after any reset and must always be re-enabled if needed.

13. Power Saving Modes

The AT89LP2052/LP4052 supports two different power-reducing modes: Idle and Power-down. These modes are accessed through the PCON register.

13.1 Idle Mode

Setting the IDL bit in PCON enters Idle mode. Idle mode halts the internal CPU clock. The CPU state is preserved in its entirety, including the RAM, stack pointer, program counter, program status word, and accumulator. The Port pins hold the logic states they had at the time that Idle was activated. Idle mode leaves the peripherals running in order to allow them to wake up the CPU when an interrupt is generated. The Timer, UART and SPI blocks continue to function during Idle. The comparator and watchdog may be selectively enabled or disabled during Idle. Any enabled interrupt source or reset may terminate Idle mode. When exiting Idle mode with an interrupt, the interrupt will immediately be serviced, and following RETI the next instruction to be executed will be the one following the instruction that put the device into Idle.

13.2 Power-down Mode

Setting the Power-down (PD) bit in PCON enters Power-down mode. Power-down mode stops the oscillator and powers down the Flash memory in order to minimize power consumption. Only the power-on circuitry will continue to draw power during Power-down. During Power-down, the power supply voltage may be reduced to the RAM keep-alive voltage. The RAM contents will be retained, but the SFR contents are not guaranteed once V_{CC} has been reduced. Power-down may be exited by external reset, power-on reset, or certain interrupts.

The user should not attempt to enter (or re-enter) the power-down mode for a minimum of 4 µs until after one of the following conditions has occurred: Start of code execution (after any type of reset), or Exit from power-down mode.

13.2.1 Interrupt Recovery from Power-down

Two external interrupts may be configured to terminate Power-down mode. Pins P3.2 and P3.3 may be used to exit Power-down through external interrupts $\overline{INT0}$ and $\overline{INT1}$. To wake up by external interrupts $\overline{INT0}$ or $\overline{INT1}$, that interrupt must be enabled and configured for level-sensitive operation. If configured as inputs, $\overline{INT0}$ and $\overline{INT1}$ should not be left floating during Power-down even if interrupt recovery is not used.

When terminating Power-down by an interrupt, two different wake-up modes are available. When PWDEX in PCON is zero, the wake-up period is internally timed. At the falling edge on the interrupt pin, Power-down is exited, the oscillator is restarted, and an internal timer begins counting. The internal clock will not be allowed to propagate to the CPU until after the timer has counted for nominally 2 ms. After the time-out period the interrupt service routine will begin. The interrupt pin may be held low until the device has timed out and begun executing, or it may return high before the end of the time-out period. If the pin remains low, the service routine should disable the interrupt before returning to avoid re-triggering the interrupt.

When PWDEX = “1”, the wake-up period is controlled externally by the interrupt. Again, at the falling edge on the interrupt pin, Power-down is exited and the oscillator is restarted. However, the internal clock will not propagate until the rising edge of the interrupt pin. The interrupt should be held low long enough for the selected clock source to stabilize.

13.2.2 Reset Exit from Power-down

The wake-up from Power-down through an external reset is similar to the interrupt with PWDEX = “0”. At the rising edge of RST, Power-down is exited, the oscillator is restarted, and an internal timer begins counting. The internal clock will not be allowed to propagate to the CPU until after the timer has counted for nominally 2 ms. The RST pin must be held high for longer than the time-out period to ensure that the device is reset properly. The device will begin executing once RST is brought back low.

Table 13-1. PCON – Power Control Register

PCON = 87H — Reset Value = 000X 0000B

Not Bit Addressable

	SMOD1	SMOD0	PWDEX	POF	GF1	GF0	PD	IDL
Bit	7	6	5	4	3	2	1	0

Symbol	Function
SMOD1	Double Baud Rate bit. Doubles the baud rate of the UART in Modes 1, 2, or 3.
SMOD0	Frame Error Select. When SMOD0 = 1, SCON.7 is SM0. When SMOD0 = 1, SCON.7 is FE. Note that FE will be set after a frame error regardless of the state of SMOD0.
PWDEX	Power-down Exit Mode. When PWDEX = 1, wake up from Power-down is externally controlled. When PWDEX = 0, wake up from Power-down is internally timed.
POF	Power Off Flag. POF is set to “1” during power up (i.e. cold reset). It can be set or reset under software control and is not affected by RST or BOD (i.e. warm resets).
GF1, GF0	General-purpose Flags
PD	Power-down bit. Setting this bit activates power-down operation.
IDL	Idle Mode bit. Setting this bit activates Idle mode operation

14. Interrupts

The AT89LP2052/LP4052 provides 6 interrupt sources: two external interrupts, two timer interrupts, a serial port interrupt, and an analog comparator interrupt. These interrupts and the system reset each have a separate program vector at the start of the program memory space. Each interrupt source can be individually enabled or disabled by setting or clearing a bit in the interrupt enable register IE. The IE register also contains a global disable bit, EA, which disables all interrupts.

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the interrupt priority registers IP and IPH. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt cannot be interrupted by any other interrupt source. If two requests of different priority levels are pending at the end of an instruction, the request of higher priority level is serviced. If requests of the same priority level are pending at the end of an instruction, an internal polling sequence determines which request is serviced. The polling sequence is based on the vector address; an interrupt with a lower vector address has higher priority than an interrupt with a higher vector address. Note that the polling sequence is only used to resolve pending requests of the same priority level.

The External Interrupts $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ can each be either level-activated or edge-activated, depending on bits IT0 and IT1 in Register TCON. The flags that actually generate these interrupts are the IE0 and IE1 bits in TCON. When the service routine is vectored to, hardware clears the flag that generated an external interrupt only if the interrupt was edge-activated. If the interrupt was level activated, then the external requesting source (rather than the on-chip hardware) controls the request flag.

The Timer 0 and Timer 1 Interrupts are generated by TF0 and TF1, which are set by a rollover in their respective Timer/Counter registers (except for Timer 0 in Mode 3). When a timer interrupt is generated, the on-chip hardware clears the flag that generated it when the service routine is vectored to.

The Serial Port Interrupt is generated by the logic OR of RI and TI in SCON plus SPIF in SPSR. None of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine normally must determine whether RI, TI, or SPIF generated the interrupt, and the bit must be cleared by software.

The CF bit in ACSR generates the Comparator Interrupt. The flag is not cleared by hardware when the service routine is vectored to and must be cleared by software.

Most of the bits that generate interrupts can be set or cleared by software, with the same result as though they had been set or cleared by hardware. That is, interrupts can be generated and pending interrupts can be canceled in software. The exception is the SPI interrupt flag SPIF. This flag is only set by hardware and may only be cleared by software.

Table 14-1. Interrupt Vector Addresses

Interrupt	Source	Vector Address
System Reset	RST or POR or BOD	0000H
External Interrupt 0	IE0	0003H
Timer 0 Overflow	TF0	000BH
External Interrupt 1	IE1	0013H
Timer 1 Overflow	TF1	001BH
Serial Port	RI or TI or SPIF	0023H
Reserved	–	002BH
Analog Comparator	CF	0033H

14.1 Interrupt Response Time

The interrupt flags may be set by their hardware in any clock cycle. The interrupt controller polls the flags in the last clock cycle of the instruction in progress. If one of the flags was set in the preceding cycle, the polling cycle will find it and the interrupt system will generate an LCALL to the appropriate service routine as the next instruction, provided that the interrupt is not blocked by any of the following conditions: an interrupt of equal or higher priority level is already in progress; the instruction in progress is RETI or any write to the IE, IP, or IPH registers. Either of these conditions will block the generation of the LCALL to the interrupt service routine. The second condition ensures that if the instruction in progress is RETI or any access to IE, IP or IPH, then at least one more instruction will be executed before any interrupt is vectored to. The polling cycle is repeated at the last cycle of each instruction, and the values polled are the values that were present at the previous clock cycle. If an active interrupt flag is not being serviced because of one of the above conditions and is no longer active when the blocking condition is removed, the denied interrupt will not be serviced. In other words, the fact that the interrupt flag was once active but not serviced is not remembered. Every polling cycle is new.

If a request is active and conditions are met for it to be acknowledged, a hardware subroutine call to the requested service routine will be the next instruction executed. The call itself takes four cycles. Thus, a minimum of five complete clock cycles elapsed between activation of an interrupt request and the beginning of execution of the first instruction of the service routine. A longer response time results if the request is blocked by one of the previously listed conditions. If an interrupt of equal or higher priority level is already in progress, the additional wait time depends on the nature of the other interrupt's service routine. If the instruction in progress is not in its final clock cycle, the additional wait time cannot be more than 3 cycles, since the longest are only 4 cycles long. If the instruction in progress is RETI or an access to IE or IP, the additional wait time cannot be more than 7 cycles (a maximum of three more cycles to complete the instruction in progress, plus a maximum of 4 cycles to complete the next instruction). Thus, in a single-interrupt system, the response time is always more than 5 clock cycles and less than 13 clock cycles. See Figures 14-1 and 14-2.

Figure 14-1. Minimum Interrupt Response Time

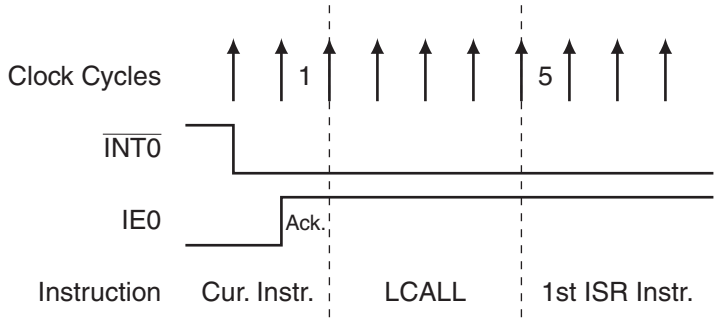


Figure 14-2. Maximum Interrupt Response Time

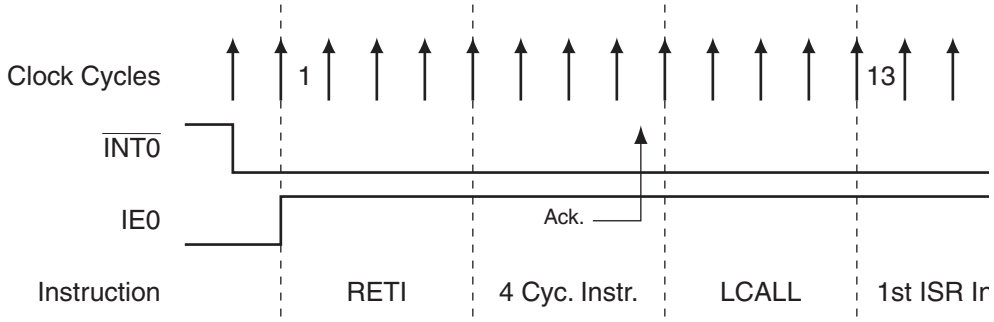


Table 14-2. IE – Interrupt Enable Register

IE = A8H — Reset Value = 00X0 0000B

Bit Addressable

	EA	EC	–	ES	ET1	EX1	ET0	EX0
Bit	7	6	5	4	3	2	1	0

Symbol	Function
EA	Global enable/disable. All interrupts are disabled when EA = 0. When EA = 1, each interrupt source is enabled/disabled by setting /clearing its own enable bit.
EC	Comparator Interrupt Enable
ES	Serial Port Interrupt Enable
ET1	Timer 1 Interrupt Enable
EX1	External Interrupt 1 Enable
ET0	Timer 0 Interrupt Enable
EX0	External Interrupt 0 Enable

Table 14-3. IP – Interrupt Priority Register

IP = B8H — Reset Value = X0X0 0000B

Bit Addressable

	–	PC	–	PS	PT1	PX1	PT0	PX0
Bit	7	6	5	4	3	2	1	0

Symbol	Function
PC	Comparator Interrupt Priority Low
PS	Serial Port Interrupt Priority Low
PT1	Timer 1 Interrupt Priority Low
PX1	External Interrupt 1 Priority Low
PT0	Timer 0 Interrupt Priority Low
PX0	External Interrupt 0 Priority Low

Table 14-4. IPH – Interrupt Priority High Register

IPH = B7H — Reset Value = X0X0 0000B

Not Bit Addressable

	–	PCH	–	PSH	PT1H	PX1H	PT0H	PX0H
Bit	7	6	5	4	3	2	1	0

Symbol	Function
PCH	Comparator Interrupt Priority High
PSH	Serial Port Interrupt Priority High
PT1H	Timer 1 Interrupt Priority High
PX1H	External Interrupt 1 Priority High
PT0H	Timer 0 Interrupt Priority High
PX0H	External Interrupt 0 Priority High

15. I/O Ports

All 15 port pins on the AT89LP2052/LP4052 may be configured to one of four modes: quasi-bidirectional (standard 8051 port outputs), push-pull output, open-drain output, or input-only. Port modes may be assigned in software on a pin-by-pin basis as shown in Table 15-1. All port pins default to input-only mode after reset. Each port pin also has a Schmitt-triggered input for improved input noise rejection. During Power-down all the Schmitt-triggered inputs are disabled with the exception of P3.2 and P3.3, which may be used to wake-up the device. Therefore P3.2 and P3.3 should not be left floating during Power-down.

Table 15-1. Configuration Modes for Port x, Bit y

PxM0.y	PxM1.y	Port Mode
0	0	Quasi-bidirectional
0	1	Push-pull Output
1	0	Input Only (High Impedance)
1	1	Open-Drain Output

15.1 Quasi-bidirectional Output

Port pins in quasi-bidirectional output mode function similar to standard 8051 port pins. A Quasi-bidirectional port can be used both as an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic high, it is weakly driven, allowing an external device to pull the pin low. When the pin is driven low, it is driven strongly and able to sink a large current. There are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

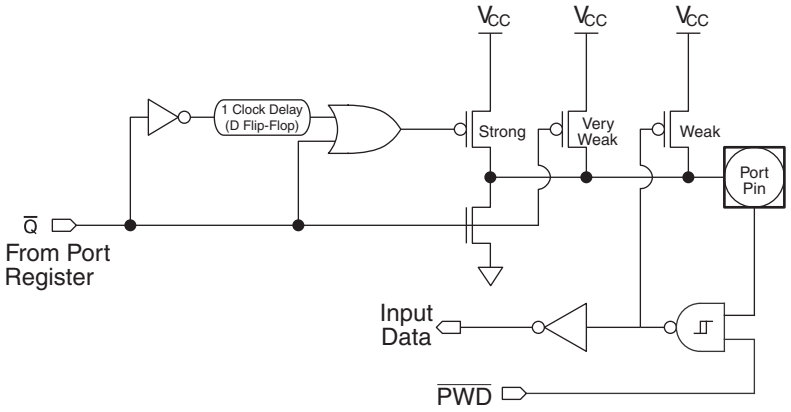
One of these pull-ups, called the “very weak” pull-up, is turned on whenever the port register for the pin contains a logic “1”. This very weak pull-up sources a very small current that will pull the pin high if it is left floating.

A second pull-up, called the “weak” pull-up, is turned on when the port register for the pin contains a logic “1” and the pin itself is also at a logic “1” level. This pull-up provides the primary source current for a quasi-bidirectional pin that is outputting a 1. If this pin is pulled low by an external device, this weak pull-up turns off, and only the very weak pull-up remains on. In order to pull the pin low under these conditions, the external device has to sink enough current to overpower the weak pull-up and pull the port pin below its input threshold voltage.

The third pull-up is referred to as the “strong” pull-up. This pull-up is used to speed up low-to-high transitions on a quasi-bidirectional port pin when the port register changes from a logic “0” to a logic “1”. When this occurs, the strong pull-up turns on for one CPU clock, quickly pulling the port pin high.

When in quasi-bidirectional mode the port pin will always output a “0” when corresponding bit in the port register is also “0”. When the port register is “1” the pin may be used either as an input or an output of “1”. The quasi-bidirectional port configuration is shown in Figure 15-1. The input circuitry of P3.2 and P3.3 is not disabled during Power-down (see Figure 15-3).

Figure 15-1. Quasi-bidirectional Output



15.2 Input-only Mode

The input port configuration is shown in Figure 15-2. It is a Schmitt-triggered input for improved input noise rejection.

Figure 15-2. Input Only

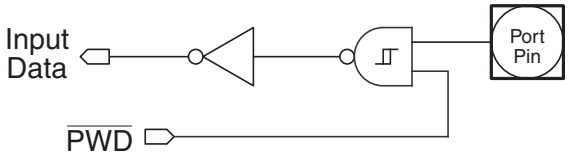
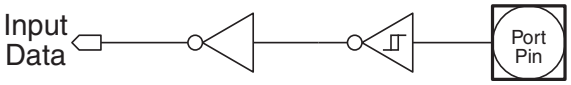


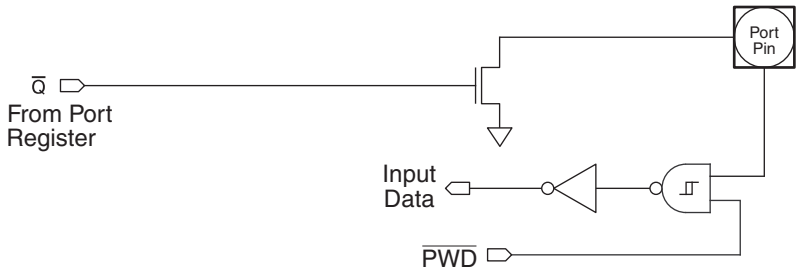
Figure 15-3. Input Only for P3.2 and P3.3



15.3 Open-drain Output

The open-drain output configuration turns off all pull-ups and only drives the pull-down transistor of the port pin when the port register contains a logic “0”. To be used as a logic output, a port configured in this manner must have an external pull-up, typically a resistor tied to V_{CC}. The pull-down for this mode is the same as for the quasi-bidirectional mode. The open-drain port configuration is shown in Figure 15-4. The input circuitry of P3.2 and P3.3 is not disabled during Power-down (see Figure 15-3).

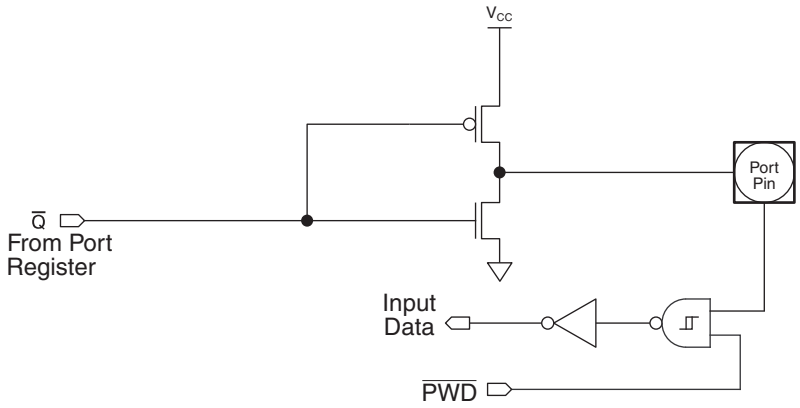
Figure 15-4. Open-Drain Output



15.4 Push-pull Output

The push-pull output configuration has the same pull-down structure as both the open-drain and the quasi-bidirectional output modes, but provides a continuous strong pull-up when the port register contains a logic “1”. The push-pull mode may be used when more source current is needed from a port output. The push-pull port configuration is shown in Figure 15-5. The input circuitry of P3.2 and P3.3 is not disabled during Power-down (see Figure 15-3).

Figure 15-5. Push-pull Output



15.5 Port 1 Analog Functions

The AT89LP2052/LP4052 incorporates an analog comparator. In order to give the best analog performance and minimize power consumption, pins that are being used for analog functions must have both the digital outputs and digital inputs disabled. Digital outputs are disabled by putting the port pins into the input-only mode as described in Section 15. “I/O Ports” on page 20.

Digital inputs on P1.0 and P1.1 are disabled whenever the Analog Comparator is enabled by setting the CEN bit in ACSR. CEN forces the $\overline{PWD}$ input on P1.0 and P1.1 low, thereby disabling the Schmitt trigger circuitry.

15.6 Port Read-Modify-Write

A read from a port will read either the state of the pins or the state of the port register depending on which instruction is used. Simple read instructions will always access the port pins directly. Read-modify-write instructions, which read a value, possibly modify it, and then write it back, will always access the port register. This includes bit write instructions such as CLR or SETB as they actually read the entire port, modify a single bit, then write the data back to the entire port. See Table 15-2 for a complete list of Read-Modify-Write instruction which may access the ports.

Table 15-2. Port Read-Modify-Write Instructions

Mnemonic	Instruction	Example
ANL	Logical AND	ANL P1, A
ORL	Logical OR	ORL P1, A
XRL	Logical EX-OR	XRL P1, A
JBC	Jump if bit set and clear bit	JBC P3.0, LABEL
CPL	Complement bit	CPL P3.1
INC	Increment	INC P1
DEC	Decrement	DEC P3
DJNZ	Decrement and jump if not zero	DJNZ P3, LABEL
MOV PX.Y, C	Move carry to bit Y of Port X	MOV P1.0, C
CLR PX.Y	Clear bit Y of Port X	CLR P1.1
SETB PX.Y	Set bit Y of Port X	SETB P3.2

15.7 Port Alternate Functions

Most general-purpose digital I/O pins of the AT89LP2052/LP4052 share functionality with the various I/Os needed for the peripheral units. Table 15-4 lists the alternate functions of the port pins. Alternate functions are connected to the pins in a logic AND fashion. In order to enable the alternate function on a port pin, that pin must have a “1” in its corresponding port register bit, otherwise, the input/output will always be “0”. Furthermore, each pin must be configured for the correct input/output mode as required by its peripheral before it may be used as such. Table 15-3 shows how to configure a generic pin for use with an alternate function.

Table 15-3. Alternate Function Configurations for Pin y of Port x

PxM0.y	PxM1.y	Px.y	I/O Mode
0	0	1	Bidirectional (internal pull-up)
0	1	1	Output
1	0	X	Input
1	1	1	Bidirectional (external pull-up)

Table 15-4. Port Pin Alternate Functions

Port Pin	Configuration Bits		Alternate Function	Notes
	PxM0.y	PxM1.y		
P1.0	P1M0.0	P1M1.0	AIN0	Input-only
P1.1	P1M0.1	P1M1.1	AIN1	Input-only
P1.4	P1M0.4	P1M1.4	$\overline{SS}$	Refer to Section 19.4 “SPI Pin Configuration” on page 48
P1.5	P1M0.5	P1M1.5	MOSI	
P1.6	P1M0.6	P1M1.6	MISO	
P1.7	P1M0.7	P1M1.7	SCK	
P3.0	P3M0.0	P3M1.0	RXD	
P3.1	P3M0.1	P3M1.1	TXD	
P3.2	P3M0.2	P3M1.2	INT0	
P3.3	P3M0.3	P3M1.3	INT1	
P3.4	P3M0.4	P3M1.4	T0	Refer to Section 16.6 “Timer/Counter Pin Configuration” on page 30
P3.5	P3M0.5	P3M1.5	T1	
P3.6	Not configurable		CMPOUT	Pin is tied to comparator output

16. Enhanced Timer/Counters

The AT89LP2052/LP4052 has two 16-bit Timer/Counter registers: Timer 0 and Timer 1. As a Timer, the register is incremented every clock cycle. Thus, the register counts clock cycles. Since a clock cycle consists of one oscillator period, the count rate is equal to the oscillator frequency.

As a Counter, the register is incremented in response to a 1-to-0 transition at its corresponding input pin, T0 or T1. The external input is sampled every clock cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during the cycle following the one in which the transition was detected. Since 2 clock cycles are required to recognize a 1-to-0 transition, the maximum count rate is 1/2 of the oscillator frequency. There are no restrictions on the duty cycle of the input signal, but it should be held for at least one full clock cycle to ensure that a given level is sampled at least once before it changes.

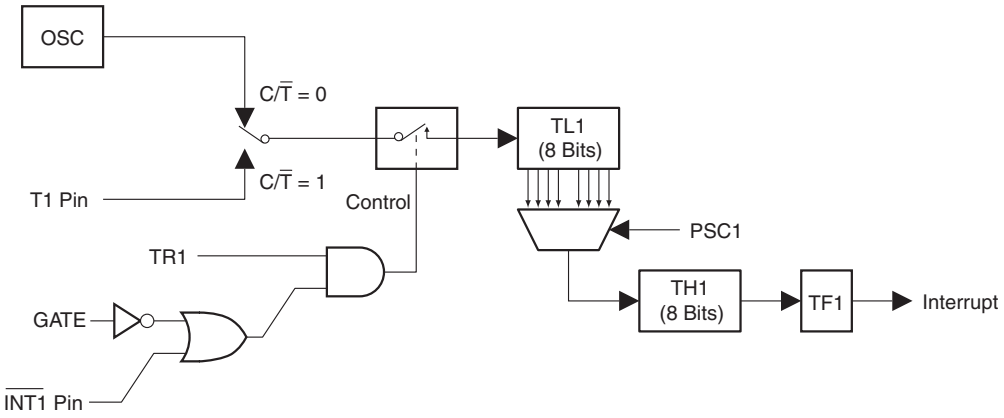
Furthermore, the Timer or Counter functions for Timer 0 and Timer 1 have four operating modes: variable width timer/counter, 16 bit auto-reload timer/counter, 8 bit auto-reload timer/counter, and split timer/counter. The control bits C/$\overline{T}$ in the Special Function Register TMOD select the Timer or Counter function. The bit pairs (M1, M0) in TMOD select the operating modes.

16.1 Mode 0

Both Timers in Mode 0 are 8-bit Counters with a variable prescaler. The prescaler may vary from 1 to 8 bits depending on the PSC bits in TCONB, giving the timer a range of 9 to 16 bits. By default the timer is configured as a 13-bit timer compatible to Mode 0 in the standard 8051. Figure 16-1 shows the Mode 0 operation as it applies to Timer 1 in 13-bit mode. As the count rolls over from all “1”s to all “0”s, it sets the Timer interrupt flag TF1. The counted input is enabled to the Timer when TR1 = 1 and either GATE = 0 or $\overline{INT1}$ = 1. Setting GATE = 1 allows the Timer to be controlled by external input $\overline{INT1}$, to facilitate pulse width measurements. TR1 is

a control bit in the Special Function Register TCON. GATE is in TMOD. The 13-bit register consists of all 8 bits of TH1 and the lower 5 bits of TL1. The upper 3 bits of TL1 are indeterminate and should be ignored. Setting the run flag (TR1) does not clear the registers. See Figure 16-1.

Figure 16-1. Timer/Counter 1 Mode 0: Variable Width Counter



Mode 0 operation is the same for Timer 0 as for Timer 1, except that TR0, TF0 and $\overline{INT0}$ replace the corresponding Timer 1 signals in Figure 16-1. There are two different GATE bits, one for Timer 1 (TMOD.7) and one for Timer 0 (TMOD.3).

16.2 Mode 1

In Mode 1 the Timers are configured for 16-bit auto-reload. The Timer register is run with all 16 bits. The 16-bit reload value is stored in the high and low reload registers (RH1/RL1). The clock is applied to the combined high and low timer registers (TH1/TL1). As clock pulses are received, the timer counts up: 0000H, 0001H, 0002H, etc. An overflow occurs on the FFFFH-to-0000H transition, upon which the timer register is reloaded with the value from RH1/RL1 and the overflow flag bit in TCON is set. See Figure 16-2. The reload registers default to 0000H, which gives the full 16-bit timer period compatible with the standard 8051. Mode 1 operation is the same for Timer/Counter 0.

Figure 16-2. Timer/Counter 1 Mode 1: 16-bit Auto-Reload