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Features

- High-performance and Low-power AVR® 8-bit RISC Architecture
  - 118 Powerful Instructions – Most Single Cycle Execution
  - 32 x 8 General Purpose Working Registers
  - Up to 8 MIPS Throughput at 8 MHz
- Data and Non-volatile Program Memory
  - 4K Bytes of In-System Programmable Flash
    Endurance 1,000 Write/Erase Cycles
  - 128 Bytes of SRAM
  - 256 Bytes of In-System Programmable EEPROM
    Endurance: 100,000 Write/Erase Cycles
  - Programming Lock for Flash Program and EEPROM Data Security
- Peripheral Features
  - One 8-bit Timer/Counter with Separate Prescaler
  - Expanded 16-bit Timer/Counter with Separate Prescaler, Compare, Capture Modes and 8-, 9-, or 10-bit PWM
  - On-chip Analog Comparator
  - Programmable Watchdog Timer with Separate On-chip Oscillator
  - Programmable UART
  - 6-channel, 10-bit ADC
  - Master/Slave SPI Serial Interface
- Special Microcontroller Features
  - Brown-out Reset Circuit
  - Enhanced Power-on Reset Circuit
  - Low-power Idle and Power-down Modes
- Power Consumption at 4 MHz, 3V, 25°C
  - Active: 3.4 mA
  - Idle Mode: 1.4 mA
  - Power-down Mode: <1 µA
- I/O and Packages
  - 20 Programmable I/O Lines
  - 28-lead PDIP and 32-lead TQFP
- Operating Voltage
  - 2.7V - 6.0V for the AT90LS4433
  - 4.0V - 6.0V for the AT90S4433
- Speed Grades
  - 0 - 4 MHz for the AT90LS4433
  - 0 - 8 MHz for the AT90S4433

8-bit AVR® Microcontroller with 4K Bytes of In-System Programmable Flash

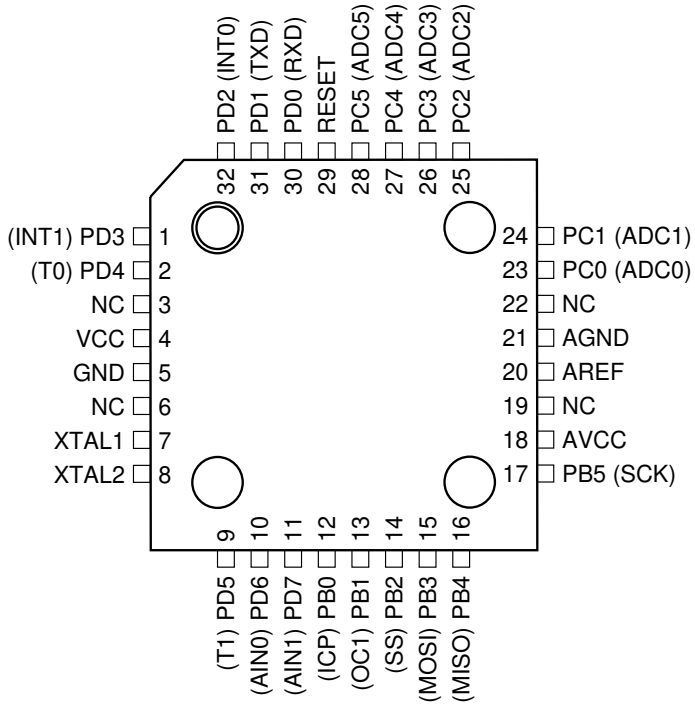
AT90S4433
AT90LS4433

Not Recommend for New Designs. Use ATmega8.

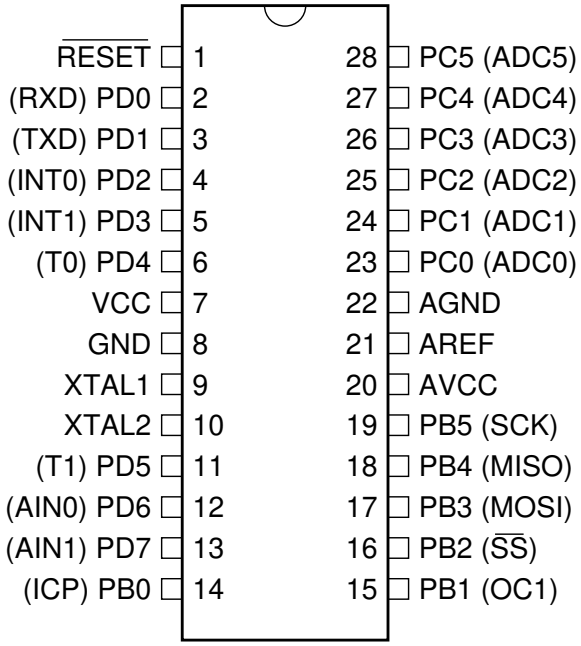
Rev. 1042H–AVR–04/03

Pin Configurations

TQFP Top View



PDIP



Description

The AT90S4433 is a low-power CMOS 8-bit microcontroller based on the AVR RISC architecture. By executing powerful instructions in a single clock cycle, the AT90S4433 achieves throughputs approaching 1 MIPS per MHz, allowing the system designer to optimize power consumption versus processing speed.

The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction, executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The AT90S4433 provides the following features: 4K bytes of In-System Programmable Flash, 256 bytes of EEPROM, 128 bytes of SRAM, 20 general purpose I/O lines, 32 general purpose working registers, two flexible Timer/Counters with compare modes, internal and external interrupts, a programmable serial UART, 6-channel, 10-bit ADC, programmable Watchdog Timer with internal Oscillator, an SPI serial port and two software-selectable Power-saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, SPI port and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or Hardware Reset.

The device is manufactured using Atmel's high-density non-volatile memory technology. The On-chip Flash Program memory can be re-programmed In-System through an SPI serial interface or by a conventional non-volatile memory programmer. By combining a RISC 8-bit CPU with In-System Programmable Flash on a monolithic chip, the Atmel AT90S4433 is a powerful microcontroller that provides a highly flexible and cost-effective solution to many embedded control applications.

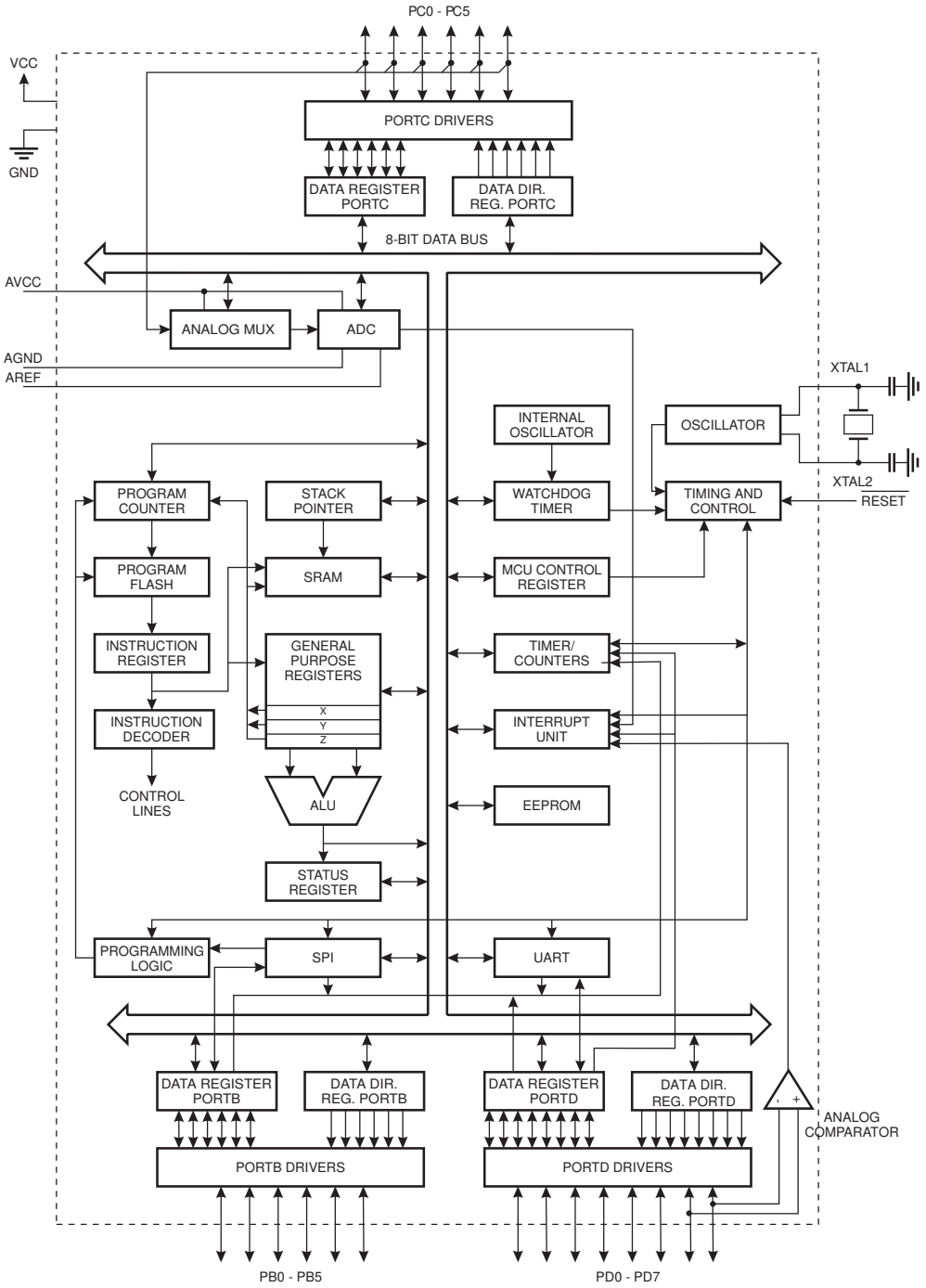
The AT90S4433 AVR is supported with a full suite of program and system development tools including: C Compilers, macro assemblers, program debugger/simulators, In-Circuit Emulators and evaluation kits.

Table 1. Comparison Table

Device	Flash	EEPROM	SRAM	Voltage Range	Frequency
AT90S4433	4K	256B	128B	4.0V - 6.0V	0 - 8 MHz
AT90LS4433	4K	256B	128B	2.7V - 6.0V	0 - 4 MHz

Block Diagram

Figure 1. The AT90S4433 Block Diagram



Pin Descriptions

VCC — Supply voltage.

GND — Ground.

Port B (PB5..PB0) — Port B is a 6-bit bi-directional I/O port with internal pull-up resistors. The Port B output buffers can sink 20 mA. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated.

Port B also serves the functions of various special features of the AT90S4433 as listed on page 73.

The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port C (PC5..PC0) — Port C is a 6-bit bi-directional I/O port with internal pull-up resistors. The Port C output buffers can sink 20 mA. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. Port C also serves as the analog inputs to the A/D Converter.

The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port D (PD7..PD0) — Port D is an 8-bit bi-directional I/O port with internal pull-up resistors. The Port D output buffers can sink 20 mA. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated.

Port D also serves the functions of various special features of the AT90S4433 as listed on page 81.

The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

$\overline{\text{RESET}}$ — Reset input. An External Reset is generated by a low level on the $\overline{\text{RESET}}$ pin. Reset pulses longer than 50 ns will generate a reset, even if the clock is not running. Shorter pulses are not guaranteed to generate a reset.

XTAL1 — Input to the inverting oscillator amplifier and input to the internal clock operating circuit

XTAL2 — Output from the inverting oscillator amplifier

AVCC — AVCC is the supply voltage for Port A and the A/D Converter. If the ADC is not used, this pin must be connected to V_{CC}. If the ADC is used, this pin should be connected to V_{CC} via a low-pass filter. See page 64 for details on operation of the ADC.

AREF — AREF is the analog reference input for the A/D Converter. For ADC operations, a voltage in the range 2.0V to AVCC must be applied to this pin.

AGND — If the board has a separate analog ground plane, this pin should be connected to this ground plane. Otherwise, connect to GND.

Clock Options

Crystal Oscillator

XTAL1 and XTAL2 are input and output, respectively, of an inverting amplifier, which can be configured for use as an On-chip Oscillator, as shown in Figure 2 and Figure 3. Either a quartz crystal or a ceramic resonator may be used.

External Clock

If the Oscillator is to be used as a clock for an external device, the clock signal from XTAL2 may be routed to one HC buffer while reducing the load capacitor by 5 pF, as shown in Figure 3. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 4.

Figure 2. Oscillator Connections

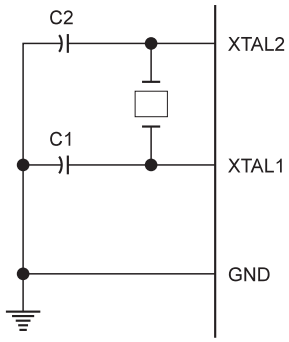


Figure 3. Using MCU Oscillator as a Clock for an External Device

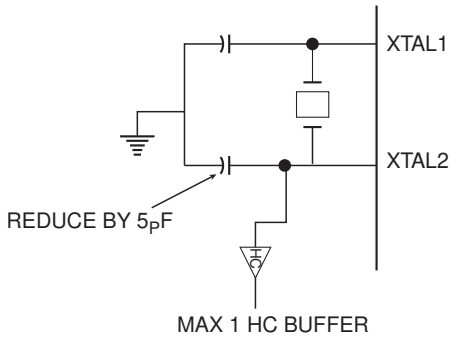
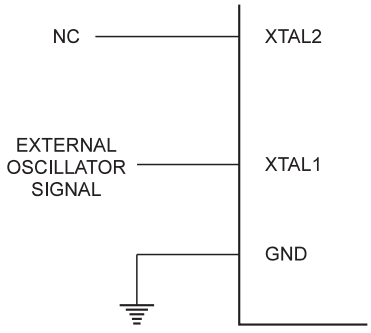


Figure 4. External Clock Drive Configuration



Architectural Overview

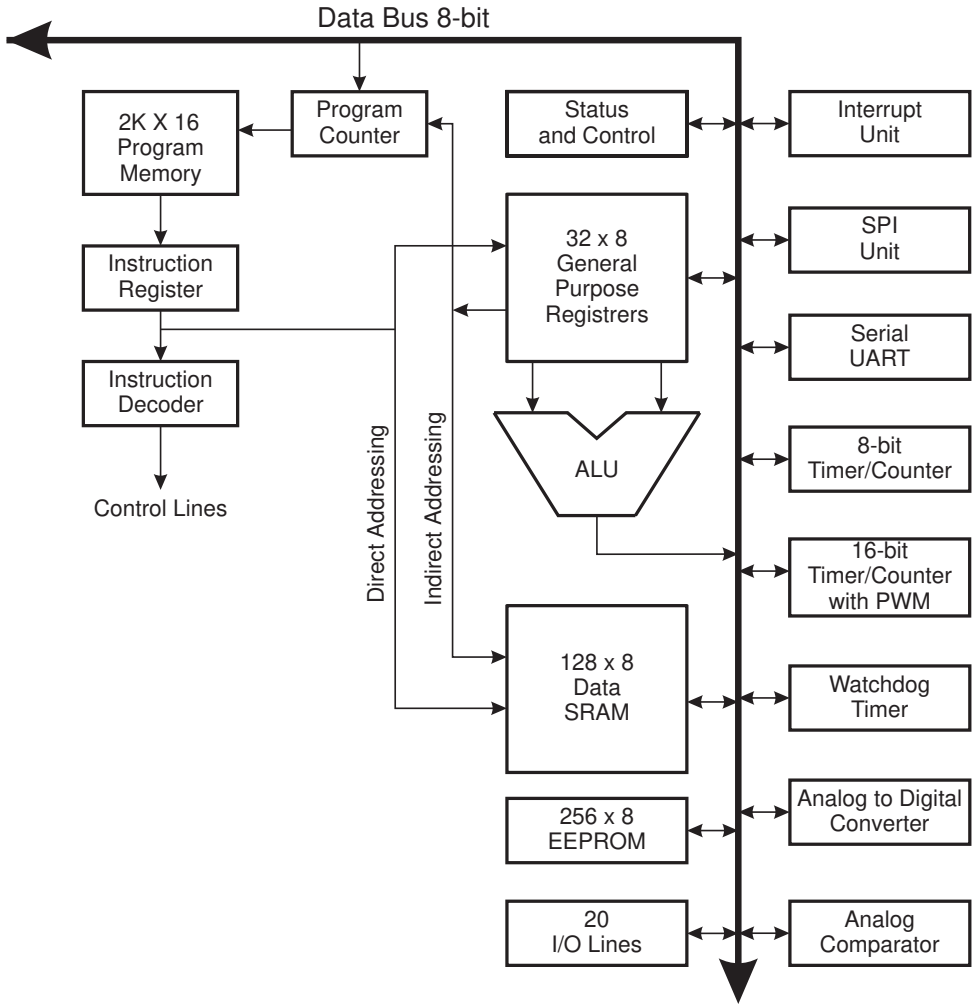
The fast-access Register File concept contains 32 x 8-bit general purpose working registers with a single clock cycle access time. This means that during one single clock cycle, one Arithmetic Logic Unit (ALU) operation is executed. Two operands are output from the Register File, the operation is executed, and the result is stored back in the Register File – in one clock cycle.

Six of the 32 registers can be used as three 16-bit indirect address register pointers for Data Space addressing, enabling efficient address calculations. One of the three address pointers is also used as the address pointer for the constant table look-up function. These added function registers are the 16-bit X-, Y-, and Z-register.

The ALU supports arithmetic and logic functions between registers or between a constant and a register. Single register operations are also executed in the ALU. Figure 5 shows the AT90S4433 AVR RISC microcontroller architecture.

In addition to the register operation, the conventional Memory Addressing modes can be used on the Register File as well. This is enabled by the fact that the Register File is assigned the 32 lowermost Data Space addresses ($00 - $1F), allowing them to be accessed as though they were ordinary memory locations.

Figure 5. The AT90S4433 AVR RISC Architecture



The I/O memory space contains 64 addresses for CPU peripheral functions such as Control Registers, Timer/Counters, A/D Converters and other I/O functions. The I/O memory can be accessed directly, or as the Data Space locations following those of the Register File, $20 - $5F.

The AVR uses a Harvard architecture concept – with separate memories and buses for program and data. The Program memory is executed with a two-stage pipeline. While one instruction is being executed, the next instruction is pre-fetched from the Program memory. This concept enables instructions to be executed in every clock cycle.

The Program memory is In-System Programmable Flash memory.

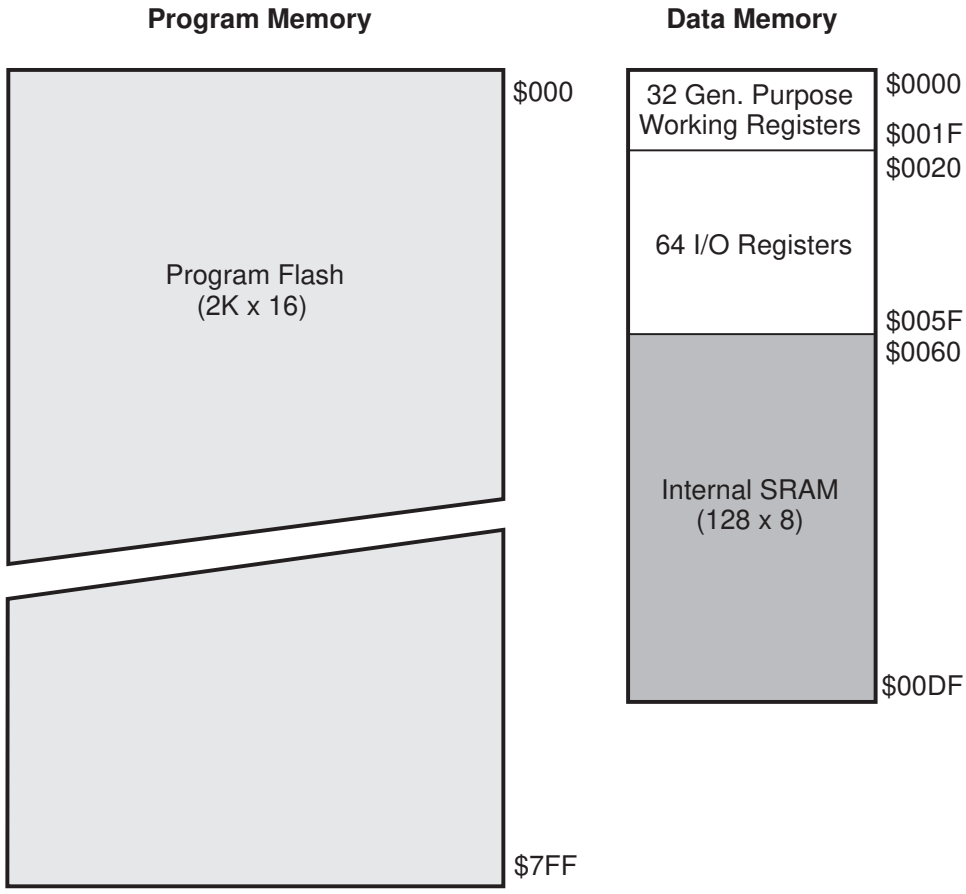
With the relative jump and call instructions, the whole 2K word address space is directly accessed. Most AVR instructions have a single 16-bit word format. Every program memory address contains a 16- or 32-bit instruction.

During interrupts and subroutine calls, the return address Program Counter (PC) is stored on the Stack. The Stack is effectively allocated in the general data SRAM and, consequently, the Stack size is only limited by the total SRAM size and the usage of the SRAM. All user programs must initialize the SP in the reset routine (before subroutines or interrupts are executed). The 8-bit Stack Pointer (SP) is read/write accessible in the I/O space.

The 128 bytes of data SRAM can be easily accessed through the five different addressing modes supported in the AVR architecture.

The memory spaces in the AVR architecture are all linear and regular memory maps.

Figure 6. AT90S4433 Memory Maps

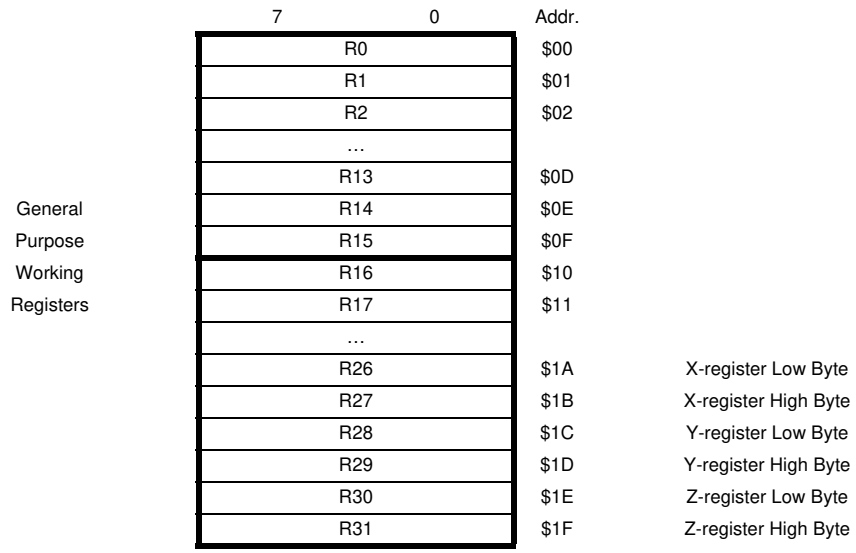


A flexible interrupt module has its control registers in the I/O space with an additional Global Interrupt Enable bit in the Status Register. All the different interrupts have a separate Interrupt Vector in the Interrupt Vector table at the beginning of the Program memory. The different interrupts have priority in accordance with their Interrupt Vector position. The lower the Interrupt Vector address, the higher the priority.

General Purpose Register File

Figure 7 shows the structure of the 32 general purpose working registers in the CPU.

Figure 7. AVR CPU General Purpose Working Registers



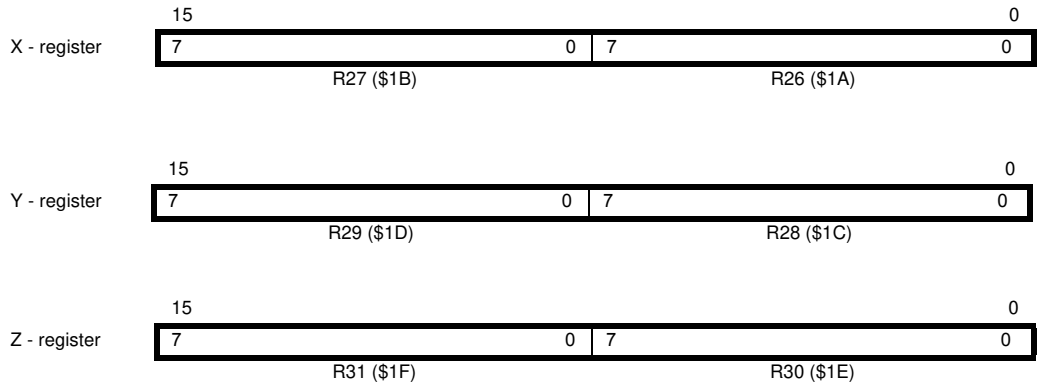
All the register operating instructions in the instruction set have direct and single cycle access to all registers. The only exceptions are the five constant arithmetic and logic instructions SBCI, SUBI, CPI, ANDI, and ORI between a constant and a register, and the LDI instruction for load immediate constant data. These instructions apply to the second half of the registers in the Register File (R16..R31). The general SBC, SUB, CP, AND, and OR, and all other operations between two registers or on a single register apply to the entire Register File.

As shown in Figure 7, each register is also assigned a data memory address, mapping them directly into the first 32 locations of the user Data Space. Although not being physically implemented as SRAM locations, this memory organization provides great flexibility in access of the registers, as the X-, Y- ,and Z-registers can be set to index any register in the file.

X-register, Y-register and Z-register

The registers R26..R31 have some added functions to their general purpose usage. These registers are address pointers for indirect addressing of the Data Space. The three indirect address registers X, Y, and Z are defined as:

Figure 8. X-, Y-, and Z-registers



In the different addressing modes, these address registers have functions as fixed displacement, automatic increment and decrement (see the descriptions for the different instructions).

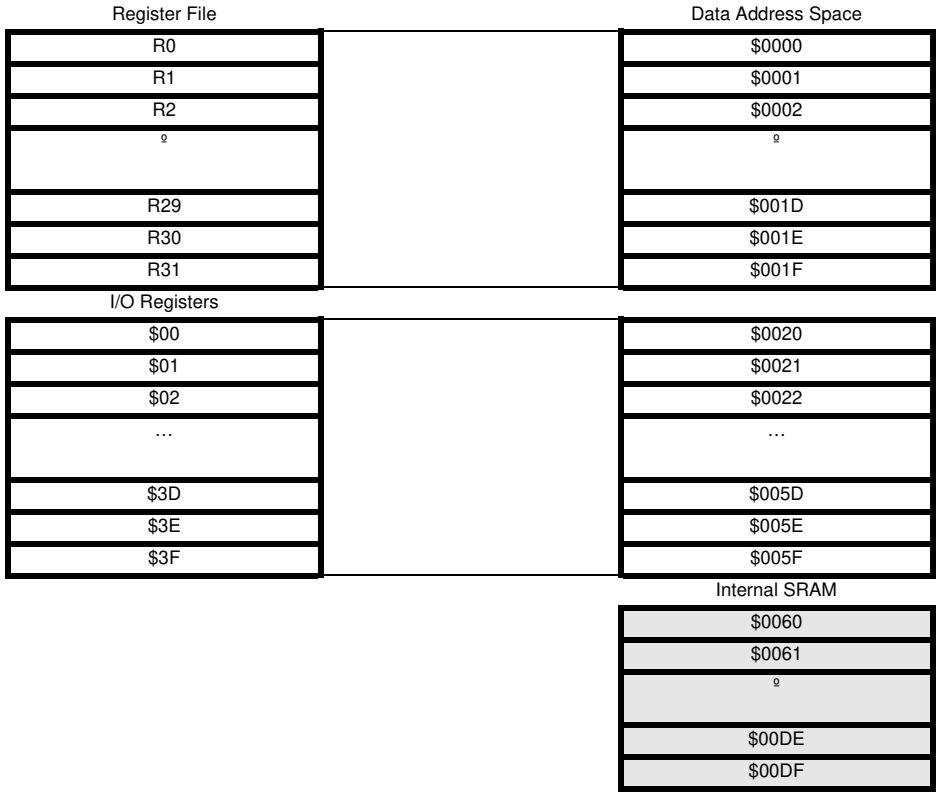
ALU – Arithmetic Logic Unit

The high-performance AVR ALU operates in direct connection with all the 32 general purpose working registers. Within a single clock cycle, ALU operations between registers in the Register File are executed. The ALU operations are divided into three main categories: arithmetic, logical, and bit functions.

In-System Programmable Flash Program Memory

The AT90S4433 contains 4K bytes of On-chip, In-System Programmable Flash memory for program storage. Since all instructions are 16- or 32-bit words, the Flash is organized as 2K x 16. The Flash memory has an endurance of at least 1,000 write/erase cycles. The AT90S4433 Program Counter (PC) is 11 bits wide, thus addressing the 2,048 program memory addresses. See page 93 for a detailed description of Flash data downloading. See page 12 for the different program memory addressing modes.

Figure 9. SRAM Organization



SRAM Data Memory

Figure 9 shows how the AT90S4433 SRAM memory is organized.

The lower 224 data memory locations address the Register File, the I/O memory and the internal data SRAM. The first 96 locations address the Register File and I/O memory, and the next 128 locations address the internal data SRAM.

The five different addressing modes for the data memory cover: Direct, Indirect with Displacement, Indirect, Indirect with Pre-decrement, and Indirect with Post-increment. In the Register File, registers R26 to R31 feature the indirect addressing pointer registers.

The direct addressing reaches the entire data space. The Indirect with Displacement mode features 63 address locations reached from the base address given by the Y- or Z-register.

When using register indirect addressing modes with automatic pre-decrement and post-increment, the address registers X, Y, and Z are decremented and incremented.

The 32 general purpose working registers, 64 I/O Registers and the 128 bytes of internal data SRAM in the AT90S4433 are all accessible through all these addressing modes.

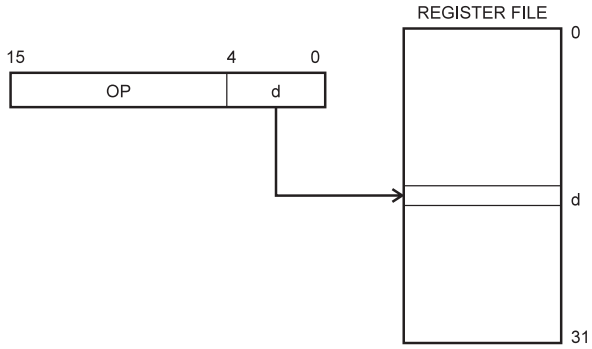
See the next section for a detailed description of the different addressing modes.

Program and Data Addressing Modes

The AT90S4433 AVR RISC microcontroller supports powerful and efficient addressing modes for access to the Flash Program memory, SRAM, Register File, and I/O data memory. This section describes the different addressing modes supported by the AVR architecture. In the figures, OP means the operation code part of the instruction word. To simplify, not all figures show the exact location of the addressing bits.

Register Direct, Single Register Rd

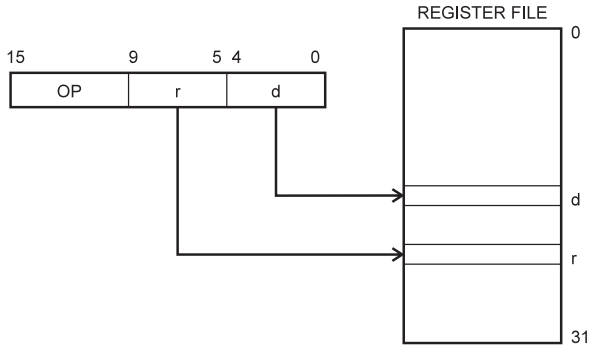
Figure 10. Direct Single Register Addressing



The operand is contained in register d (Rd).

Register Direct, Two Registers Rd and Rr

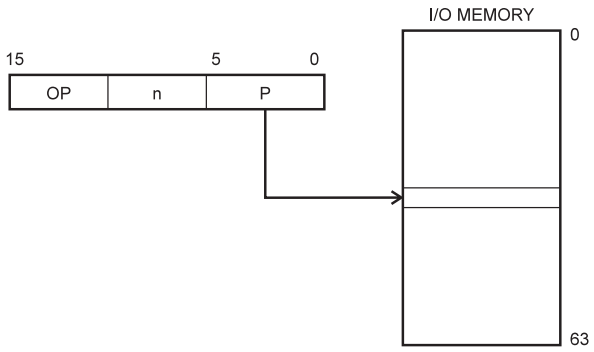
Figure 11. Direct Register Addressing, Two Registers



Operands are contained in registers r (Rr) and d (Rd). The result is stored in register d (Rd).

I/O Direct

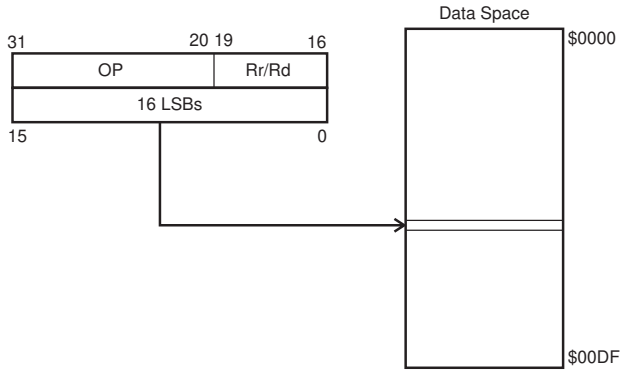
Figure 12. I/O Direct Addressing



Operand address is contained in six bits of the instruction word. n is the destination or source register address.

Data Direct

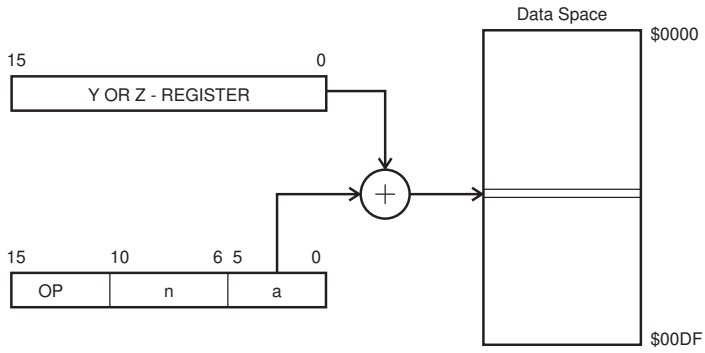
Figure 13. Direct Data Addressing



A 16-bit data address is contained in the 16 LSBs of a two-word instruction. Rd/Rr specify the destination or source register.

Data Indirect with Displacement

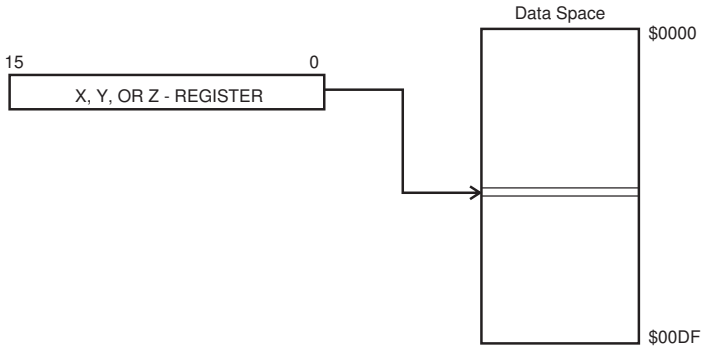
Figure 14. Data Indirect with Displacement



Operand address is the result of the Y- or Z-register contents added to the address contained in six bits of the instruction word.

Data Indirect

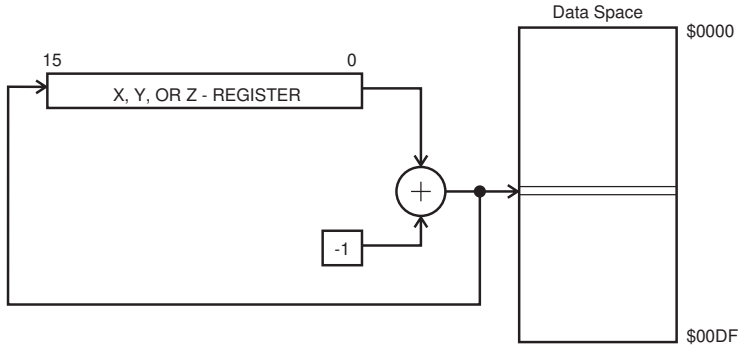
Figure 15. Data Indirect Addressing



Operand address is the contents of the X-, Y-, or the Z-register.

Data Indirect with Pre-decrement

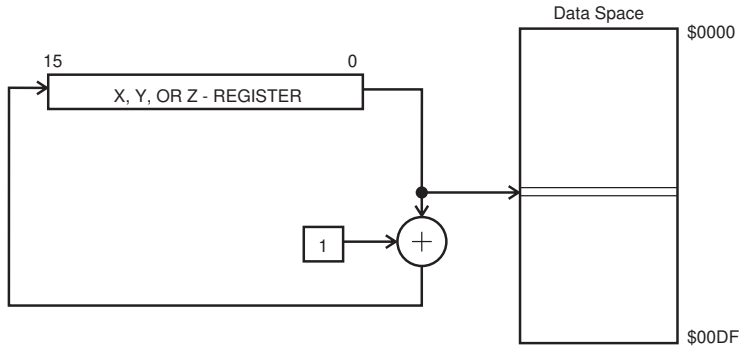
Figure 16. Data Indirect Addressing with Pre-decrement



The X-, Y-, or the Z-register is decremented before the operation. Operand address is the decremented contents of the X-, Y-, or the Z-register.

Data Indirect with Post-increment

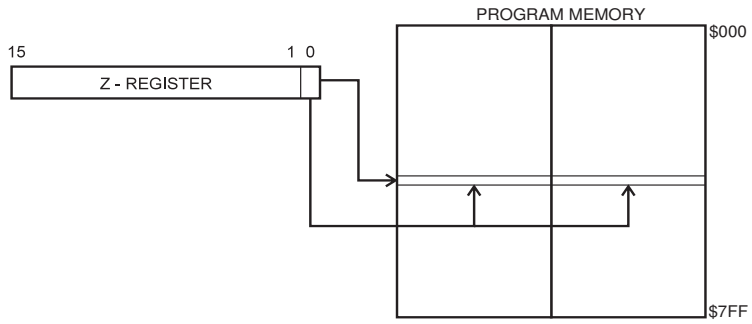
Figure 17. Data Indirect Addressing with Post-increment



The X-, Y-, or the Z-register is incremented after the operation. Operand address is the content of the X-, Y-, or the Z-register prior to incrementing.

Constant Addressing Using the LPM Instruction

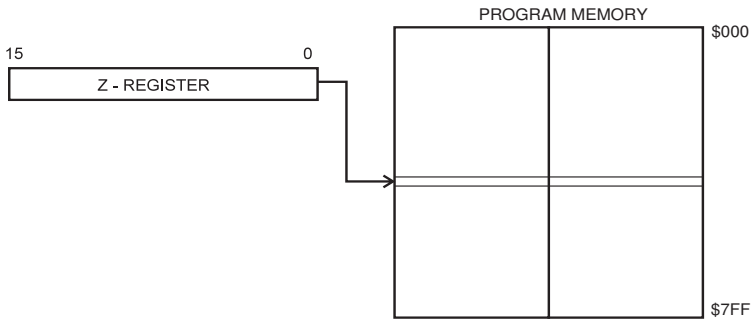
Figure 18. Code Memory Constant Addressing



Constant byte address is specified by the Z-register contents. The 15 MSBs select word address (0 - 2K), the LSB selects Low Byte if cleared (LSB = 0) or High Byte if set (LSB = 1).

Indirect Program Addressing, IJMP and ICALL

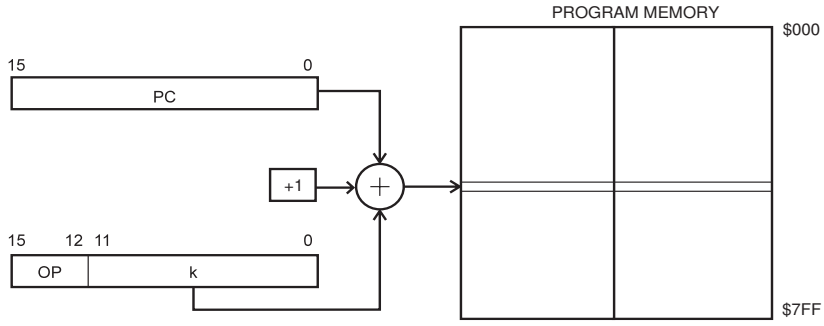
Figure 19. Indirect Program Memory Addressing



Program execution continues at address contained by the Z-register (i.e., the PC is loaded with the contents of the Z-register).

Relative Program Addressing, RJMP and RCALL

Figure 20. Relative Program Memory Addressing



Program execution continues at address PC + k + 1. The relative address k is from -2048 to 2047.

EEPROM Data Memory

The AT90S4433 contains 256 bytes of data EEPROM memory. It is organized as a separate data space, in which single bytes can be read and written. The EEPROM has an endurance of at least 100,000 write/erase cycles per location. The access between the EEPROM and the CPU is described on page 53, specifying the EEPROM Address Registers, the EEPROM Data Register and the EEPROM Control Register.

For the SPI Data downloading, see page 93 for a detailed description. The EEPROM Data memory is In-System Programmable through the SPI port. Please refer to the "EEPROM Read/Write Access" section on page 45 for a thorough description of EEPROM access.

Memory Access Times and Instruction Execution Timing

This section describes the general access timing concepts for instruction execution and internal memory access.

The AVR CPU is driven by the System Clock Ø, directly generated from the external clock crystal for the chip. No internal clock division is used.

Figure 21 shows the parallel instruction fetches and instruction executions enabled by the Harvard architecture and the fast-access Register File concept. This is the basic pipelining concept to obtain up to 1 MIPS per MHz with the corresponding unique results for functions per cost, functions per clocks and functions per power unit.

Figure 21. The Parallel Instruction Fetches and Instruction Executions

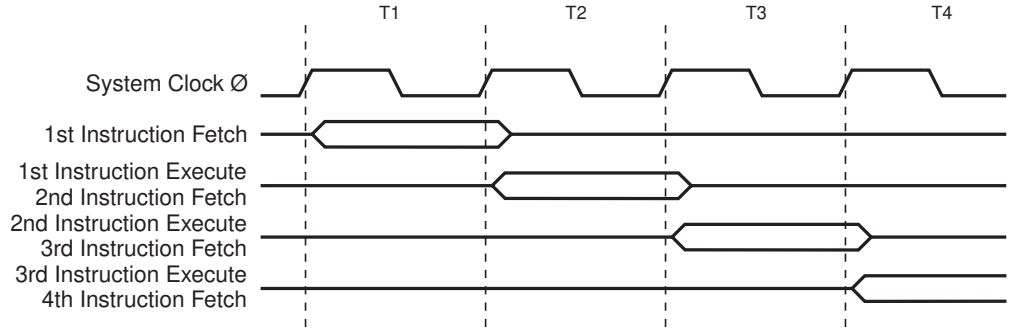
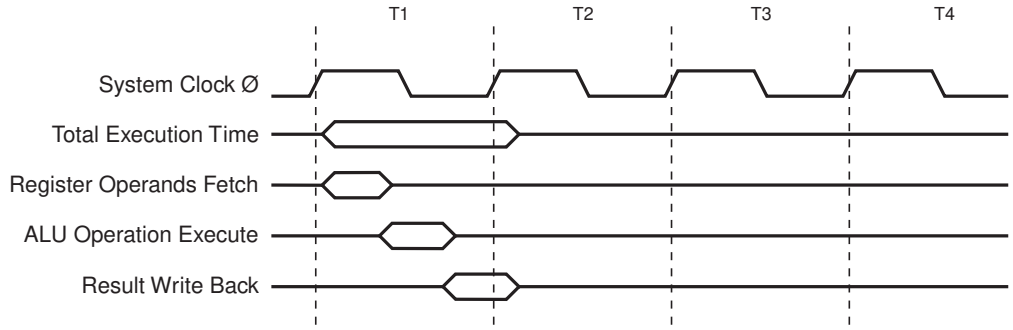


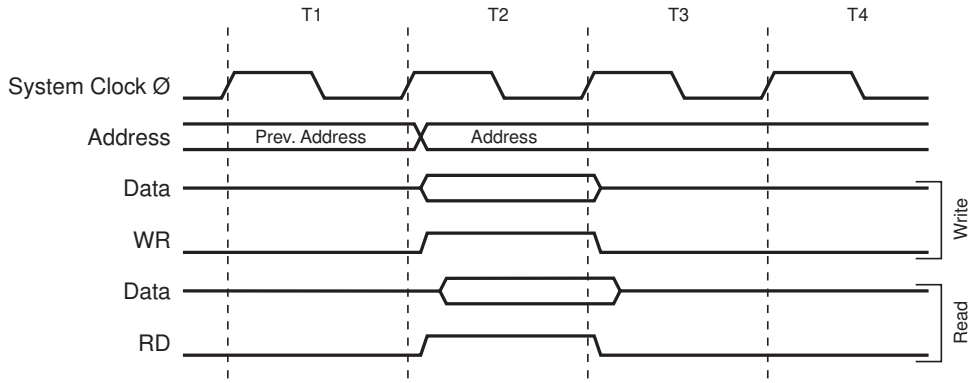
Figure 22 shows the internal timing concept for the Register File. In a single clock cycle an ALU operation using two register operands is executed and the result is stored back to the destination register.

Figure 22. Single Cycle ALU Operation



The internal data SRAM access is performed in two System Clock cycles as described in Figure 23.

Figure 23. On-chip Data SRAM Access Cycles



I/O Memory

The I/O space definition of the AT90S4433 is shown in Table 2.

Table 2. AT90S4433 I/O Space[1]

I/O Address (SRAM Address)	Name	Function
$3F ($5F)	SREG	Status Register
$3D ($5D)	SP	Stack Pointer
$3B ($5B)	GIMSK	General Interrupt MaSK Register
$3A ($5A)	GIFR	General Interrupt Flag Register
$39 ($59)	TIMSK	Timer/Counter Interrupt MaSK Register
$38 ($58)	TIFR	Timer/Counter Interrupt Flag Register
$35 ($55)	MCUCR	MCU general Control Register
$34 ($54)	MCUSR	MCU general Status Register
$33 ($53)	TCCR0	Timer/Counter0 Control Register
$32 ($52)	TCNT0	Timer/Counter0 (8-bit)
$2F ($4F)	TCCR1A	Timer/Counter1 Control Register A
$2E ($4E)	TCCR1B	Timer/Counter1 Control Register B
$2D ($4D)	TCNT1H	Timer/Counter1 High Byte
$2C ($4C)	TCNT1L	Timer/Counter1 Low Byte
$2B ($4B)	OCR1H	Timer/Counter1 Output Compare Register High Byte
$2A ($4A)	OCR1L	Timer/Counter1 Output Compare Register Low Byte
$27 ($47)	ICR1H	Timer/Counter1 Input Capture Register High Byte
$26 ($46)	ICR1L	Timer/Counter 1 Input Capture Register Low Byte
$21 ($41)	WDTCR	Watchdog Timer Control Register
$1E ($3E)	EEAR	EEPROM Address Register
$1D ($3D)	EEDR	EEPROM Data Register
$1C ($3C)	EECR	EEPROM Control Register
$18 ($38)	PORTB	Data Register, Port B

Table 2. AT90S4433 I/O Space[1] (Continued)

I/O Address (SRAM Address)	Name	Function
$17 ($37)	DDRB	Data Direction Register, Port B
$16 ($36)	PINB	Input Pins, Port B
$15 ($35)	PORTC	Data Register, Port C
$14 ($34)	DDRC	Data Direction Register, Port C
$13 ($33)	PINC	Input Pins, Port C
$12 ($32)	PORTD	Data Register, Port D
$11 ($31)	DDRD	Data Direction Register, Port D
$10 ($30)	PIND	Input Pins, Port D
$0F ($2F)	SPDR	SPI I/O Data Register
$0E ($2E)	SPSR	SPI Status Register
$0D ($2D)	SPCR	SPI Control Register
$0C ($2C)	UDR	UART I/O Data Register
$0B ($2B)	UCSRA	UART Control and Status Register A
$0A ($2A)	UCSRB	UART Control and Status Register B
$09 ($29)	UBRR	UART Baud Rate Register
$08 ($28)	ACSR	Analog Comparator Control and Status Register
$07 ($27)	ADMUX	ADC Multiplexer Select Register
$06 ($26)	ADCSR	ADC Control and Status Register
$05 ($25)	ADCH	ADC Data Register High
$04 ($24)	ADCL	ADC Data Register Low
$03 ($23)	UBRRHI	UART Baud Rate Register High

Note: 1. Reserved and unused locations are not shown in the table.

All AT90S4433 I/Os and peripherals are placed in the I/O space. The I/O locations are accessed by the IN and OUT instructions transferring data between the 32 general purpose working registers and the I/O space. I/O Registers within the address range $00 - $1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions. Refer to the instruction set section for more details. When using the I/O specific commands IN and OUT, the I/O addresses $00 - $3F must be used. When addressing I/O Registers as SRAM, $20 must be added to this address. All I/O Register addresses throughout this document are shown with the SRAM address in parentheses.

For compatibility with future devices, reserved bits should be written to zero when accessed. Reserved I/O memory addresses should never be written.

Some of the Status Flags are cleared by writing a logical “1” to them. Note that the CBI and SBI instructions will operate on all bits in the I/O Register, writing a one back into any flag read as set, thus clearing the flag. The CBI and SBI instructions work with registers $00 to $1F only.

The I/O and Peripherals Control Registers are explained in the following sections.

Status Register – SREG

The AVR Status Register (SREG) at I/O space location $3F ($5F) is defined as:

Bit	7	6	5	4	3	2	1	0	
$3F ($5F)	I	T	H	S	V	N	Z	C	SREG
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – I: Global Interrupt Enable**

The Global Interrupt Enable bit must be set (one) for the interrupts to be enabled. The individual interrupt enable control is then performed in separate control registers. If the Global Interrupt Enable Register is cleared (zero), none of the interrupts are enabled independent of the individual interrupt enable settings. The I-bit is cleared by hardware after an interrupt has occurred and is set by the RETI instruction to enable subsequent interrupts.

- **Bit 6 – T: Bit Copy Storage**

The Bit Copy Instructions BLD (Bit LoaD) and BST (Bit STore) use the T-bit as source and destination for the operated bit. A bit from a register in the Register File can be copied into T by the BST instruction, and a bit in T can be copied into a bit in a register in the Register File by the BLD instruction.

- **Bit 5 – H: Half Carry Flag**

The Half Carry Flag H indicates a Half Carry in some arithmetical operations. See the Instruction Set description for detailed information.

- **Bit 4 – S: Sign Bit, S = N $\oplus$ V**

The S-bit is always an exclusive or between the Negative Flag N and the Two's Complement Overflow Flag V. See the Instruction Set description for detailed information.

- **Bit 3 – V: Two's Complement Overflow Flag**

The Two's Complement Overflow Flag V supports two's complement arithmetics. See the Instruction Set description for detailed information.

- **Bit 2 – N: Negative Flag**

The Negative Flag N indicates a negative result from an arithmetical or logical operation. See the Instruction Set description for detailed information.

- **Bit 1 – Z: Zero Flag**

The Zero Flag Z indicates a zero result from an arithmetical or logical operation. See the Instruction Set description for detailed information.

- **Bit 0 – C: Carry Flag**

The Carry Flag C indicates a carry in an arithmetical or logical operation. See the Instruction Set description for detailed information.

Note that the Status Register is not automatically stored when entering an interrupt routine and restored when returning from an interrupt routine. This must be handled by software.

Stack Pointer – SP

The AT90S4433 Stack Pointer is implemented as an 8-bit register in the I/O space location $3D ($5D). As the AT90S4433 data memory has $0DF locations, eight bits are used.

	7	6	5	4	3	2	1	0	
$3D ($5D)	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	SP
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

The Stack Pointer points to the data SRAM stack area where the Subroutine and Interrupt stacks are located. This stack space in the data SRAM must be defined by the program before any subroutine calls are executed or interrupts are enabled. The Stack Pointer must be set to point above $60. The Stack Pointer is decremented by one when data is pushed onto the stack with the PUSH instruction, and it is decremented by two when an address is pushed onto the Stack with subroutine calls and interrupts. The Stack Pointer is incremented by one when data is popped from the stack with the POP instruction, and it is incremented by two when an address is popped from the Stack with return from subroutine RET or return from interrupt RETI.

Reset and Interrupt Handling

The AT90S4433 provides 13 different interrupt sources. These interrupts and the separate reset vector each have a separate Program Vector in the Program memory space. All interrupts are assigned individual enable bits, which must be set (one) together with the I-bit in the Status Register in order to enable the interrupt.

The lowest addresses in the Program memory space are automatically defined as the Reset and Interrupt Vectors. The complete list of Vectors is shown in Table 3. The list also determines the priority levels of the different interrupts. The lower the address, the higher the priority level. RESET has the highest priority, and next is INT0 (the External Interrupt Request 0), etc.

Table 3. Reset and Interrupt Vectors

Vector No.	Program Address	Source	Interrupt Definition
1	$000	RESET	External Pin, Power-on Reset, Brown-out Reset and Watchdog Reset
2	$001	INT0	External Interrupt Request 0
3	$002	INT1	External Interrupt Request 1
4	$003	TIMER1 CAPT	Timer/Counter1 Capture Event
5	$004	TIMER1 COMP	Timer/Counter1 Compare Match
6	$005	TIMER1 OVF	Timer/Counter1 Overflow
7	$006	TIMER0 OVF	Timer/Counter0 Overflow
8	$007	SPI, STC	Serial Transfer Complete
9	$008	UART, RX	UART, Rx Complete
10	$009	UART, UDRE	UART Data Register Empty
11	$00A	UART, TX	UART, Tx Complete
12	$00B	ADC	ADC Conversion Complete
13	$00C	EE_RDY	EEPROM Ready
14	$00D	ANA_COMP	Analog Comparator

The most typical program setup for the Reset and Interrupt Vector addresses are:

```
Address   Labels  Code              Comments
$000              rjmp    RESET      ; Reset Handler
$001              rjmp    EXT_INT0   ; IRQ0 Handler
$002              rjmp    EXT_INT1   ; IRQ1 Handler
$003              rjmp    TIM1_CAPT  ; Timer1 Capture Handler
$004              rjmp    TIM1_COMP  ; Timer1 compare Handler
$005              rjmp    TIM1_OVF   ; Timer1 Overflow Handler
$006              rjmp    TIM0_OVF   ; Timer0 Overflow Handler
$007              rjmp    SPI_STC;   ; SPI Transfer Complete Handler
$008              rjmp    UART_RXC   ; UART RX Complete Handler
$009              rjmp    UART_DRE   ; UDR Empty Handler
$00a              rjmp    UART_TXC   ; UART TX Complete Handler
$00b              rjmp    ADC      ; ADC Conversion Complete Interrupt Handler
$00c              rjmp    EE_RDY     ; EEPROM Ready Handler
$00d              rjmp    ANA_COMP   ; Analog Comparator Handler
;
$00e      MAIN:   ldi     r16,low(RAMEND); Main program start
$00f              out     SP,r16;
$010              <instr>  xxx       ;
  …       …       …      …
```

Reset Sources

The AT90S4433 has four sources of reset:

- Power-on Reset. The MCU is reset when the supply voltage is below the Power-on Reset threshold (V_{POT}).
- External Reset. The MCU is reset when a low level is present on the $\overline{\text{RESET}}$ pin for more than 50 ns.
- Watchdog Reset. The MCU is reset when the Watchdog Timer period expires and the Watchdog is enabled.
- Brown-out Reset. The MCU is reset when the supply voltage (V_{CC}) falls below a certain voltage.

During Reset, all I/O Registers are then set to their Initial Values, and the program starts execution from address $000. The instruction placed in address $000 must be an RJMP (relative jump) instruction to the reset handling routine. If the program never enables an interrupt source, the Interrupt Vectors are not used, and regular program code can be placed at these locations. The circuit diagram in Figure 24 shows the Reset Logic. Table 4 and Table 5 define the timing and electrical parameters of the reset circuitry.

Figure 24. Reset Logic

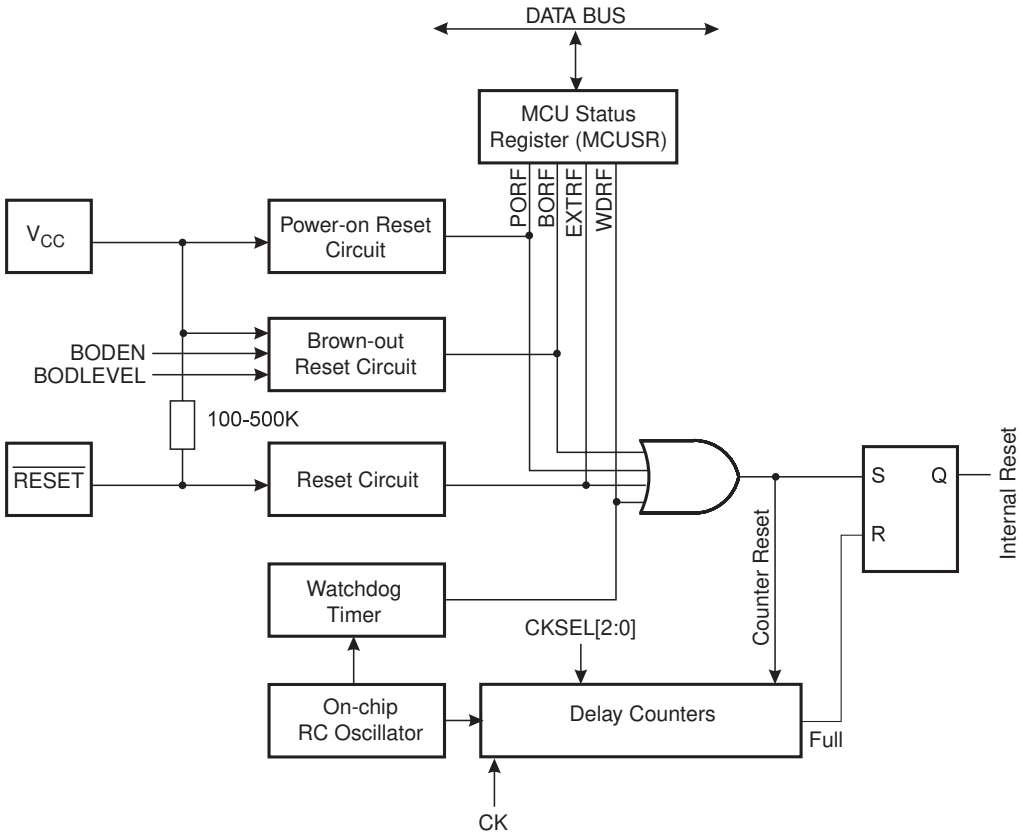


Table 4. Reset Characteristics (V_{CC} = 5.0V)

Symbol	Parameter	Min	Typ	Max	Units
V_{POT}[1]	Power-on Reset Threshold Voltage, rising	1.0	1.4	1.8	V
	Power-on Reset Threshold Voltage, falling	0.4	0.6	0.8	V
V_{RST}	$\overline{\text{RESET}}$ Pin Threshold Voltage		0.6 V_{CC}		V
V_{BOT}	Brown-out Reset Threshold Voltage	2.2 (BODLEVEL=1)	2.7 (BODLEVEL=1)	3.0 (BODLEVEL=1)	V
		3.5 (BODLEVEL=0)	4.0 (BODLEVEL=0)	4.5 (BODLEVEL=0)	

Note: 1. The Power-on Reset will not work unless the supply voltage has been below V_{POT} (falling).

Table 5. Reset Delay Selections

CKSEL [2:0]	Start-up Time, t_{TOUT} at V_{CC} = 2.7V	Start-up Time, t_{TOUT} at V_{CC} = 5.0V	Recommended Usage
000	16 ms + 6 CK	4 ms + 6 CK	External Clock, slowly rising power
001	6 CK	6 CK	External Clock, BOD enabled(1)
010	256 ms + 16K CK	64 ms + 16K CK	Crystal Oscillator
011	16 ms + 16K CK	4 ms + 16K CK	Crystal Oscillator, fast rising power
100	16K CK	16K CK	Crystal Oscillator, BOD enabled(1)
101	256 ms + 1K CK	64 ms + 1K CK	Ceramic Resonator
110	16 ms + 1K CK	4 ms + 1K CK	Ceramic Resonator, fast rising power
111	1K CK	1K CK	Ceramic Resonator, BOD enabled(1)

Note: 1. Or external Power-on Reset.

This table shows the Start-up times from Reset. From sleep, only the clock counting part of the Start-up time is used. The Watchdog Oscillator is used for timing the Real Time part of the Start-up time. The number WDT Oscillator cycles used for each time-out is shown in Table 6.

Table 6. Number of Watchdog Oscillator Cycles

Time-out	Number of Cycles
4.0 ms (at V_{CC} = 5.0V)	4K
64 ms (at V_{CC} = 5.0V)	64K

The frequency of the Watchdog Oscillator is voltage dependent, as shown in the Electrical Characteristics section.

Power-on Reset

A Power-on Reset (POR) pulse is generated by an On-chip Detection circuit. The detection level is nominally 2.2V. The POR is activated whenever V_{CC} is below the detection level. The POR circuit can be used to trigger the Start-up Reset, as well as detect a failure in supply voltage.

The Power-on Reset (POR) circuit ensures that the device is Reset from Power-on. Reaching the Power-on Reset threshold voltage invokes a delay counter, which determines the delay, for which the device is kept in RESET after V_{CC} rise. The Time-out period of the delay counter is a combination of Internal RC Oscillator cycles and External Oscillator cycles, and it can be defined by the user through the CKSEL Fuses. The eight different selections for the delay period are presented in Table 5. The RESET signal is activated again, without any delay, when the V_{CC} decreases to below detection level.

Figure 25. MCU Start-up, $\overline{\text{RESET}}$ Tied to V_{CC}

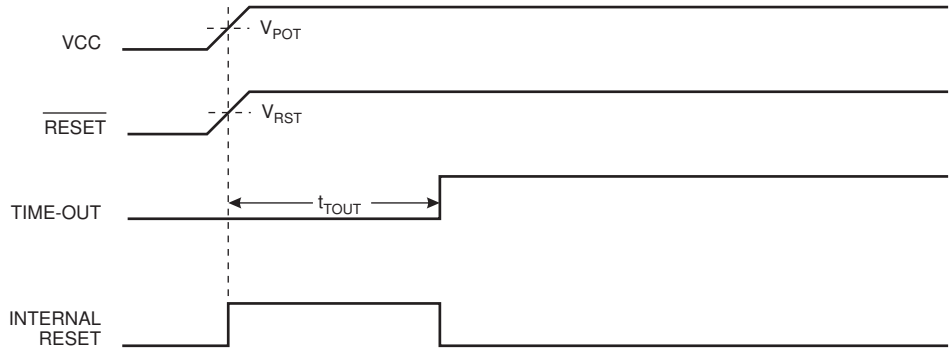
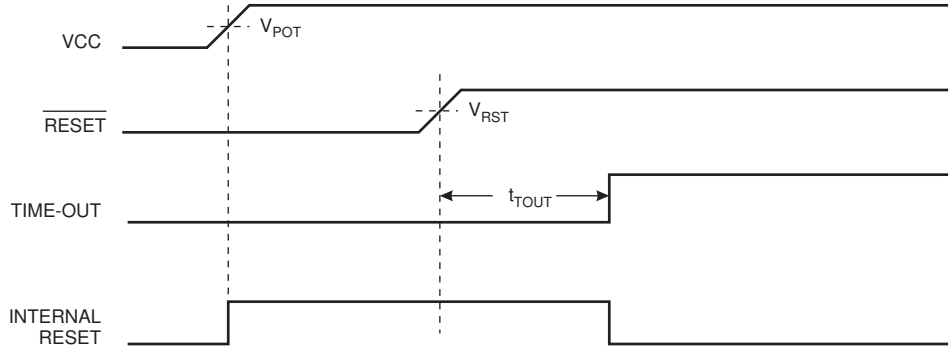


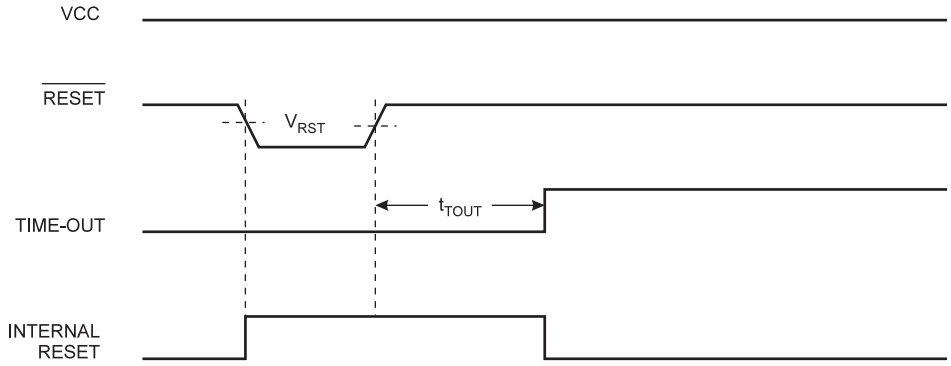
Figure 26. MCU Start-up, $\overline{\text{RESET}}$ Controlled Externally



External Reset

An External Reset is generated by a low level on the $\overline{\text{RESET}}$ pin. Reset pulses longer than 50 ns will generate a Reset, even if the clock is not running. Shorter pulses are not guaranteed to generate a Reset. When the applied signal reaches the Reset Threshold Voltage (V_{RST}) on its positive edge, the delay timer starts the MCU after the Time-out period (t_{TOUT}) has expired.

Figure 27. External Reset during Operation

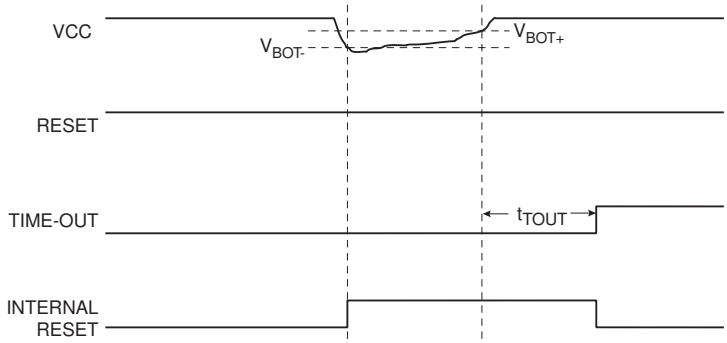


Brown-out Detection

AT90S4433 has an On-chip Brown-out Detection (BOD) circuit for monitoring the V_{CC} level during the operation. The power supply must be decoupled with a 47 nF to 100 nF capacitor if the BOD function is used. The BOD circuit can be enabled/disabled by the fuse BODEN. When BODEN is enabled (BODEN programmed), and V_{CC} decreases to a value below the trigger level, the Brown-out Reset is immediately activated. When V_{CC} increases above the trigger level, the Brown-out Reset is deactivated after a delay. The delay is defined by the user in the same way as the delay of POR signal (see Table 5). The trigger level for the BOD can be selected by the fuse BODLEVEL to be 2.7V (BODLEVEL unprogrammed), or 4.0V (BODLEVEL programmed). The trigger level has a hysteresis of 50 mV to ensure spike-free Brown-out Detection.

The BOD circuit will only detect a drop in V_{CC} if the voltage stays below the trigger level for longer than 3 µs for trigger level 4.0V, 7 µs for trigger level 2.7V (typical values).

Figure 28. Brown-out Reset during Operation



Watchdog Reset

When the Watchdog times out, it will generate a short reset pulse of one XTAL cycle duration. On the falling edge of this pulse, the delay timer starts counting the Time-out period (t_{TOUT}). See page 43 for details on operation of the Watchdog.

Figure 29. Watchdog Reset during Operation