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# AT91CAP9A-DK Development Kit

# User Guide

6321B–CAP–02-Jul-07

## Table of Contents

# Section 1

# AT91CAP9A-DK Development Board and AT91CAP-DKM Motherboard Overview

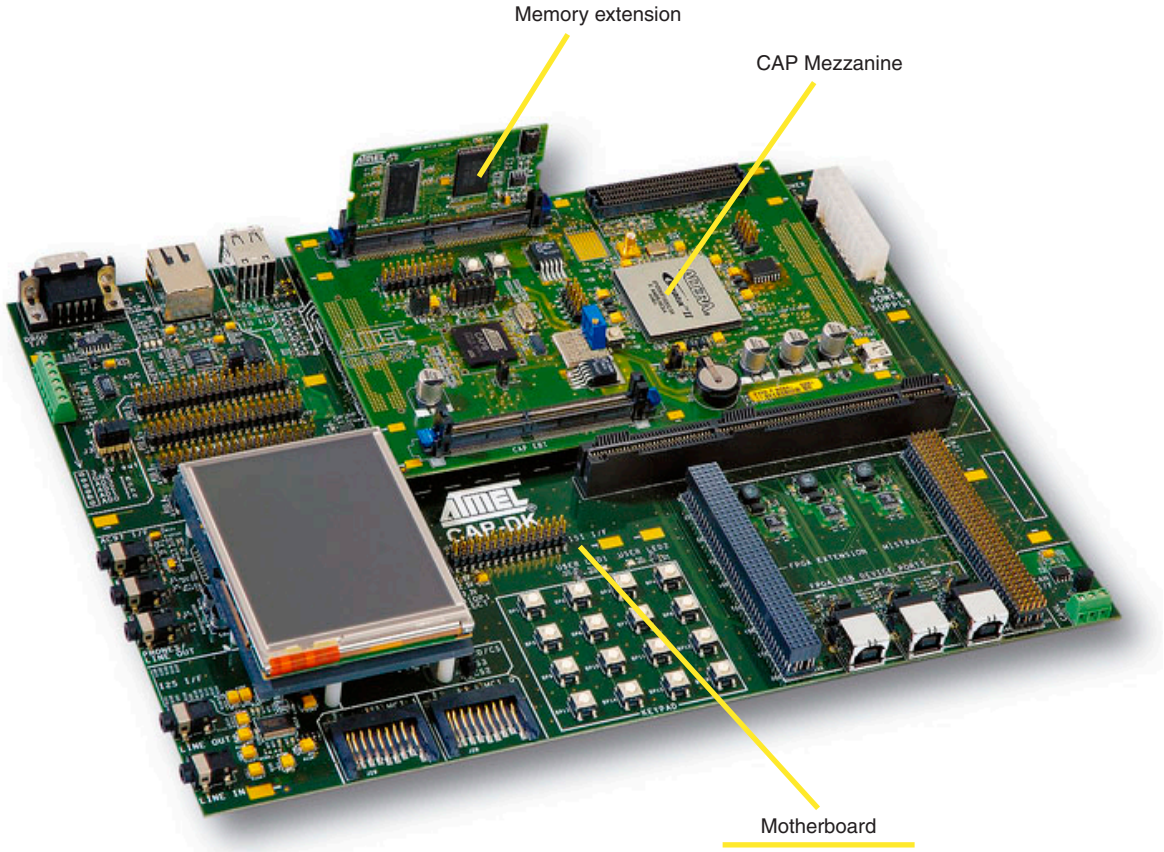
## 1.1 Scope

The AT91CAP9/Altera® development board (AT91CAP9A-DK) or “kit” is composed of three associated boards, namely **Motherboard, Mezzanine** and **Memory Extension** to be used jointly in order to develop AT91CAP9 processor applications.

The AT91CAP9A-DK development board implements the fixed portion of the AT91CAP9 device as a microcontroller standard product, tightly coupled to a high-density FPGA that emulates the MP Block. The boards also include a range of memories and physical interfaces/connectors representing external system components. This configuration enables parallel hardware/software testing of the application under development at close to operational speed, with no penalty for hardware modifications. This enables software development to proceed in parallel with hardware development, and significantly reduces the design cycle time, increasing confidence in a right-first-time system solution.

**Section 1** through **Section 4** provide essential usage documentation for the AT91CAP-DKM **Motherboard**.

***Figure 1-1.*** Overview of AT91CAP9A-DK Development Kit/AT91CAP-DKM Motherboard




## 1.2 Purpose

The AT91CAP-DKM Motherboard provides all the service items of an AT91CAP9A-DK development system. That is:

- Power supply input, conversion and distribution,
- Standard user interfaces,
- Prototyping interface and extension means.

# Section 2

# Setting Up the AT91CAP-DKM Motherboard

## 2.1 Electrostatic Warning

Upon delivery, the AT91CAP-DKM motherboard is wrapped in a protective anti-static bag. The board must not be exposed to electrostatic discharges. A grounding strap or similar protective device should be worn when handling the board. Avoid touching the component pins or any other on-board metallic element.

## 2.2 Requirements

In order to set up an AT91CAP9A-DK development system, the following items are needed:

- AT91CAP-DKM motherboard
- PC/ATX standard power supply unit
- AT91CAP9A-DKZ mezzanine board (see Sections 5 through 8), with a memory extension (see sections 9 through 14)

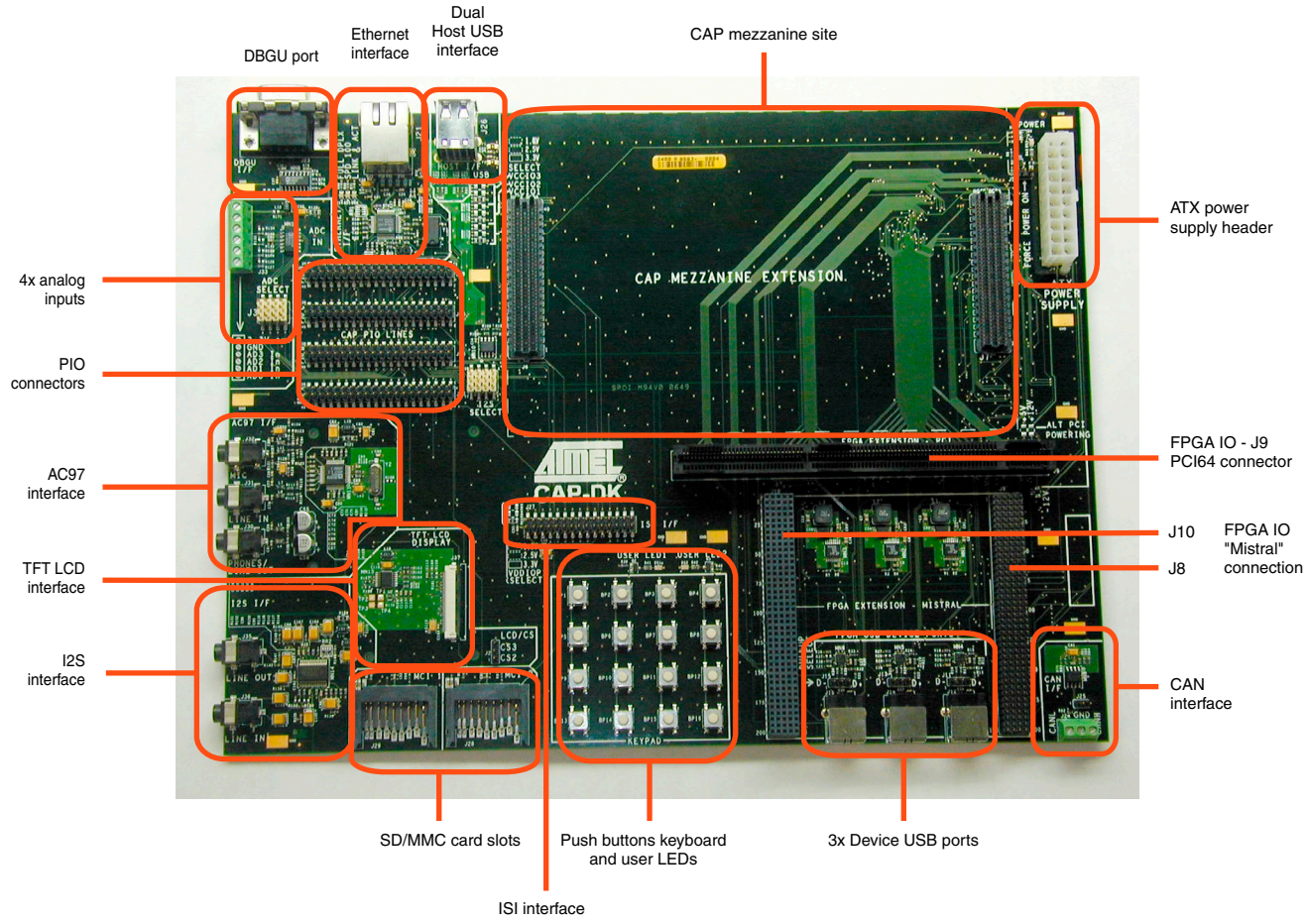
## 2.3 Layout

The AT91CAP-DKM motherboard features the following on-board interfaces:

- ATX power supply connector
- 2x Full-speed Host USB interfaces
- 100-base TX Ethernet PHY with three status LEDs
- DBGU serial communication port
- 4x analog inputs
- AC97 interface with three 3.5 mm audio jack connectors (MIC IN, LINE IN, LINE OUT)
- I2S audio codec with two 3.5 mm audio jack connectors (LINE IN, LINE OUT)
- 2x SD/MMC card slots
- Atmel TWI serial EEPROM
- 1/4 inch TFT LCD VGA interface
- Touch Screen Controller
- Image Sensor expansion connector
- 16 push buttons arranged in a keypad form
- CAN bus interface
- Software controlled Power LED
- 2x general-purpose LEDs

- PIO expansion connectors (PIOA, PIOB, PIOC, PIOD)
- CAP Mezzanine extension connectors (2x 320 pins)
- PCI64 form FPGA I/O extension connector
- Custom mezzanine-style FPGA I/O extension connector
- 3x USB device PHY interfaces with USB B connectors (FPGA controlled)

***Figure 2-1.*** AT91CAP-DKM Motherboard Layout - Top View




## 2.4 Powering Up the Board

A complete AT91CAP9A-DK system is powered through the AT91CAP-DKM motherboard via a standard ATX PC power supply.

The power control signal is connected to the SHDN signal, generated by the AT91CAP9 chip from the AT91CAP9A-DKZ mezzanine board.

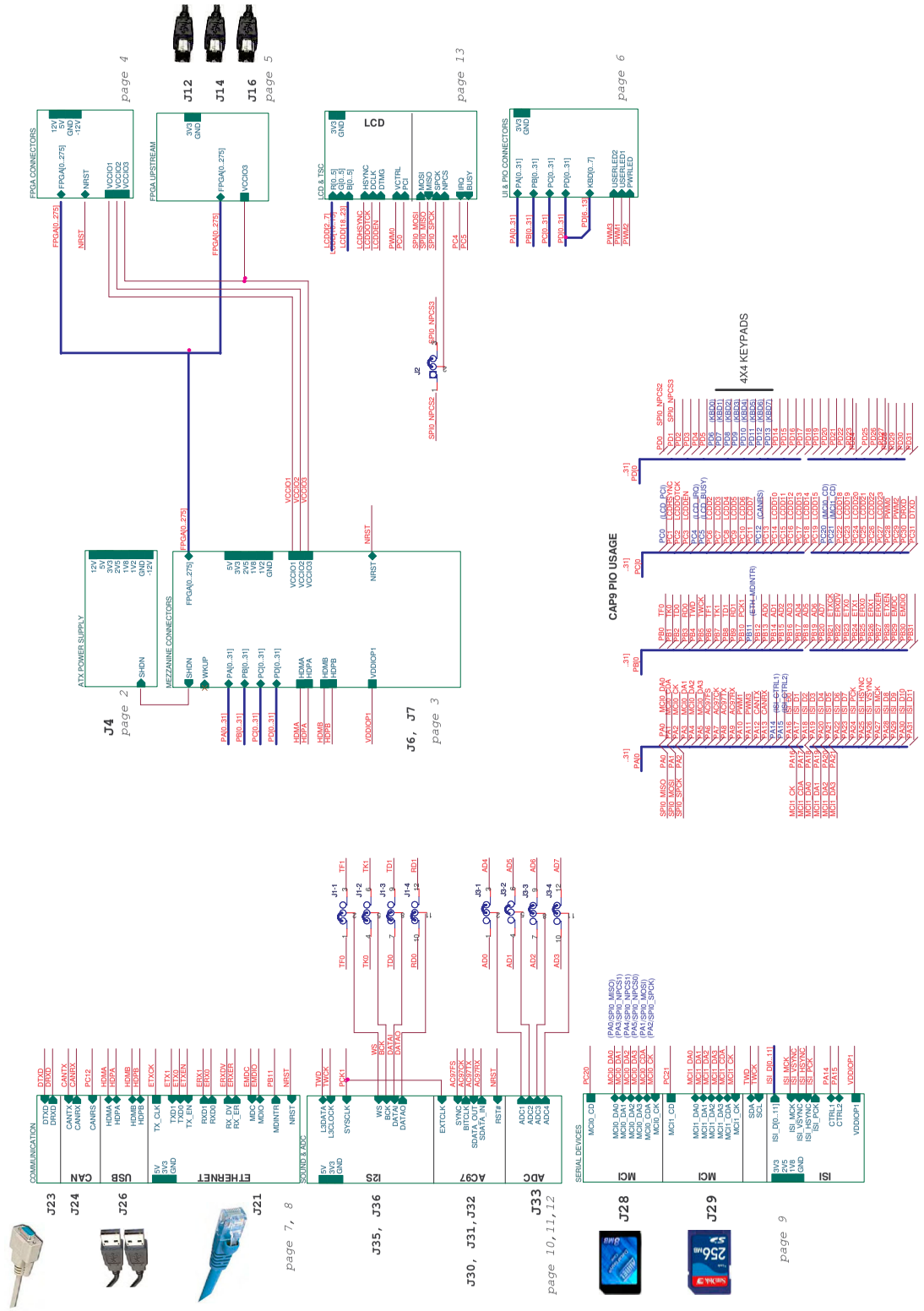
In case the AT91CAP-DKM motherboard has to be powered without a mezzanine or an AT91CAP9 chip in place, the “Force Power ON” jumper J5 must be installed.

# Section 3

# AT91CAP-DKM Motherboard

## 3.1 Block Diagram

***Figure 3-1.*** AT91CAP-DKM Motherboard (see the complete schematic in Section 15, “AT91CAP-DKM Schematics”



## 3.2 Clock Circuity

There are two on-board clock sources:

- 24.576 MHz standard crystal for the AC97 audio interface
- 50.000 MHz oscillator for the RMII Ethernet interface

## 3.3 Reset Circuity

The AT91CAP9A-DKZ mezzanine board generates the NRST signal for the whole system.

## 3.4 Shutdown Controller

The SHDN signal issued by the Reset Controller of the AT91CAP9 chip is provided by the AT91CAP9A-DKZ mezzanine board and routed to the ATW connector, in order to control the power supply unit.

As explained in Section 2.4 “Powering Up the Board” on page 2-2, the remote controlling of the power supply can be bypassed with jumper J5.

## 3.5 Power Supply Circuity

The AT91CAP-DKM motherboard derives the necessary system voltages from the ATX supply.

On-board switching regulators provide the following voltage sources:

- 1.2V
- 1.8V
- 2.5V

## 3.6 Memory

The only memory resource available on the AT91CAP-DKM motherboard is an Atmel serial EEPROM (TWI bus connection).

System memory resources are to be connected directly to the AT91CAP9A-DKZ mezzanine via the AT91CAP9-MEMxx extension boards.

## 3.7 Remote Communication

### 3.7.1 CAN Interface

The AT91CAP-DKM board features one serial CAN 2.0B communication port which is physically connected to a J24 3-way screw-style connector.

An on-board standard 120-Ohm terminator is available. Simply install jumper J25 to enable termination.

### 3.7.2 Host USB Interface

A dual host connection (J26 = dual Type A socket) is available on the AT91CAP-DKM motherboard.

These two ports are routed directly from/to the AT91CAP9 chip installed on the mezzanine. In function of the AT91CAP9 chip connected in the system, these two ports can be non operating. For further information, please refer to the documentation specific to the mezzanine you intend to use.

### 3.7.3 Device USB Interface

Please refer to Section 3.14 “FPGA Extension” on page 3-5.

### 3.7.4 Ethernet Interface

On-board RMII 100-base TX PHY: DM9161 MN7 connected to a standard RJ45 socket J21. Three status LEDs (DS4, 5, 6) provide network activity feedback.

## 3.8 Audio Stereo Interface

### 3.8.1 AC97

One AC97 2.3 compliant Codec (MN11 = AD1981B, 20-bit PCM DAC) with the following connectors:

- 32-ohm stereo headset line-out
- stereo line input
- stereo electret microphone input

This interface has some configuration elements. Please refer to Section 4 “AT91CAP-DKM Configuration” and/or “AT91CAP-DKM Schematics” for in-depth details.

### 3.8.2 I2S

One I2S audio codec MN14 = UDA1342TS with the following connectors:

- line-out
- line-in

## 3.9 Analog Interface

Four analog inputs (range up to 3.3V). These are available through the J33 connector and are buffered by a quadruple gain-1 amplifier, MN12 = AD8040ARZ.

These four buffered signals can be connected to the eight AT91CAP9 analog input channels via the four configuration jumpers J3-1 to J3-4. Refer to Table 4-1 for more details.

## 3.10 User Interface

The various items interfaced with the AT91CAP-DKM motherboard are all driven by the PIO busses of the AT91CAP9 chip. (Refer to “AT91CAP-DKM Schematics” for detailed assignation)

- 4x4 keypad: uses 8 PIO lines in a matrix scheme, each button shunts two of them
- Two green LEDs
- One yellow power LED (note that it is software controlled)
- One 3.5 inch VGA display LCD with Touch Panel and white LED backlight

- One ISI connector (camera interface)

## 3.11 Debug Interface

The AT91CAP standard serial debug interface (DBGU) is carried through the DB9 male socket, J23. It is routed to the DBGU port of the AT91CAP9 chip installed on the mezzanine.

## 3.12 Memory Expansion Slots

Two memory card dedicated connectors:

- J28 for DataFlash, SD/SDIO/MMC card slot
- J29 for SD/SDIO/MMC card slot

Note that both adopt the same connector but that J28 is also DataFlash® compatible due to its signal muxing (refer to "PIO Usage" on page 3-24, (PIO A muxing table) and "AT91CAP-DKM Schematics").

## 3.13 PIO Connectors

All PIOs of the AT91CAP9 are routed to peripheral extension connectors (J17 to J20). This allows the developer to add external hardware components or boards.

***Note:*** Most of the PIO lines already have an assignment on board. Therefore be aware of the schematic routing prior to customizing these lines in any way. Do not cause electrical contention as this may potentially damage the boards and the AT91CAP9 chip.

## 3.14 FPGA Extension

### 3.14.1 Overview

The AT91CAP-DKM motherboard routes most of the FPGA IOs coming from the mezzanine to on-board prototyping ports (free for custom user board implementation). These are grouped on sheet 4/13 of Section 15 "AT91CAP-DKM Schematics":

- J9 = PCI64 female connector for FPGA I/O expansion
- J8/J10 = two 200-pin connectors for "Mistral" extension board

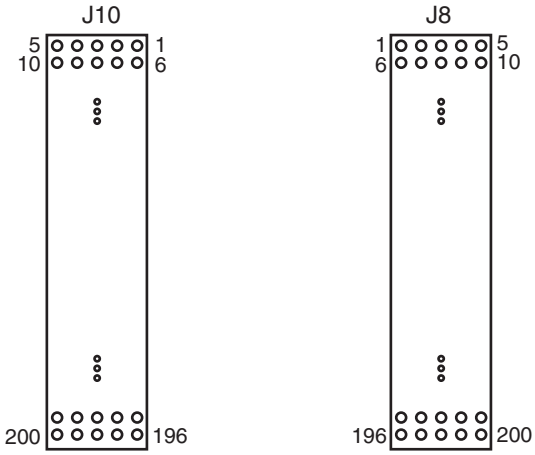
**Warning:** FPGA IOs are distributed among J8, J9 and J10 connectors and also the three USB device ports, some having dual connections as follows:

*Table 3-1.* FPGA IO Overlapping Table

| Net Name Range | J8 | J10 | J9 | USB |
|---|---|---|---|---|
| FPGA000<br>FPGA001<br>FPGA004..FPGA 093<br>FPGA098..FPGA117 | X | | | |
| FPGA250..FPGA 252<br>FPGA260..FPGA 262 | X | | X | |
| FPGA118..FPGA174 | | X | | |
| FPGA175..FPGA 189<br>FPGA191..FPGA 228<br>FPGA270 | | X | X | |
| FPGA229..FPGA245 | | | X | |
| FPGA190<br>FPGA246..FPGA 249<br>FPGA253..FPGA 259<br>FPGA263..FPGA 269<br>FPGA271..FPGA 275 | | | X | X |
| FPGA002<br>FPGA003<br>FPGA094..FPGA 097 | | | | X |

### 3.14.2 AT91CAP-DKM Extension Connectors

*Figure 3-2.* J8 and J10 (Top View)




J8 and J10 as seen on AT91CAP9-DKM from above

### 3.14.3 “Mistral” Extension Connectors

Pins not listed in Table 3-2 below are not connected.

*Table 3-2.* J-8 (male) Pin Assignment Table

| J8 Pin | FPGA Bank | FPGA Pin Function | Other FPGA Pin Information | FPGA Ball | Board Net |
|---|---|---|---|---|---|
| 1 | B1 | IO | CLK2p/DIFFIO_RX_C1p | U32 | FPGA0 |
| 2 | | | | | GND |
| 3 | B1 | IO | CLK2n/DIFFIO_RX_C1n | U31 | FPGA1 |
| 4 | | | | | GND |
| 5 | B3 | IO | DQ15T | E26 | FPGA250 |
| 6 | B3 | IO | | F21 | FPGA251 |
| 7 | | | | | GND |
| 8 | B1 | IO | DIFFIO_RX28p | V31 | FPGA4 |
| 9 | | | | | GND |
| 10 | B1 | IO | DIFFIO_RX28n | V30 | FPGA5 |
| 11 | B1 | IO | DIFFIO_TX28p | U23 | FPGA6 |
| 12 | | | | | GND |
| 13 | B1 | IO | DIFFIO_TX28n | U22 | FPGA7 |
| 14 | | | | | GND |
| 15 | B1 | IO | DIFFIO_RX27p | W32 | FPGA8 |
| 16 | B1 | IO | DIFFIO_RX27n | W31 | FPGA9 |
| 17 | | | | | GND |
| 18 | B1 | IO | DIFFIO_TX27p | U28 | FPGA10 |
| 19 | | | | | GND |
| 20 | B1 | IO | DIFFIO_TX27n | U27 | FPGA11 |
| 21 | B1 | IO | DIFFIO_RX26p | AA32 | FPGA12 |
| 22 | | | | | GND |
| 23 | B1 | IO | DIFFIO_RX26n | AA31 | FPGA13 |
| 24 | | | | | GND |
| 25 | B1 | IO | DIFFIO_TX26p | V29 | FPGA14 |
| 26 | B1 | IO | DIFFIO_TX26n | V28 | FPGA15 |
| 27 | | | | | GND |
| 28 | B1 | IO | DIFFIO_RX25p | Y31 | FPGA16 |
| 29 | | | | | GND |
| 30 | B1 | IO | DIFFIO_RX25n | Y30 | FPGA17 |
| 31 | B1 | IO | DIFFIO_TX25p | V24 | FPGA18 |
| 32 | | | | | GND |
| 33 | B1 | IO | DIFFIO_TX25n | V23 | FPGA19 |
| 34 | | | | | GND |
| 35 | B1 | IO | DIFFIO_RX24p | AB32 | FPGA20 |
| 36 | B1 | IO | DIFFIO_RX24n | AB31 | FPGA21 |

*Table 3-2.* J-8 (male) Pin Assignment Table (Continued)

| J8 Pin | FPGA Bank | FPGA Pin Function | Other FPGA Pin Information | FPGA Ball | Board Net |
|---|---|---|---|---|---|
| 37 | | | | | GND |
| 38 | B1 | IO | DIFFIO_TX24p | W29 | FPGA22 |
| 39 | | | | | GND |
| 40 | B1 | IO | DIFFIO_TX24n | W28 | FPGA23 |
| 41 | B1 | IO | DIFFIO_RX23p | AA30 | FPGA24 |
| 42 | | | | | GND |
| 43 | B1 | IO | DIFFIO_RX23n | AA29 | FPGA25 |
| 44 | | | | | GND |
| 45 | B1 | IO | DIFFIO_TX23p | W27 | FPGA26 |
| 46 | B1 | IO | DIFFIO_TX23n | W26 | FPGA27 |
| 47 | | | | | GND |
| 48 | B1 | IO | DIFFIO_RX22p | Y29 | FPGA28 |
| 49 | | | | | GND |
| 50 | B1 | IO | DIFFIO_RX22n | Y28 | FPGA29 |
| 51 | B1 | IO | DIFFIO_TX22p | W25 | FPGA30 |
| 52 | | | | | GND |
| 53 | B1 | IO | DIFFIO_TX22n | W24 | FPGA31 |
| 54 | | | | | GND |
| 55 | B1 | IO | DIFFIO_RX21p | AB30 | FPGA32 |
| 56 | B1 | IO | DIFFIO_RX21n | AB29 | FPGA33 |
| 57 | | | | | GND |
| 58 | B1 | IO | DIFFIO_TX21p | Y27 | FPGA34 |
| 59 | | | | | GND |
| 60 | B1 | IO | DIFFIO_TX21n | Y26 | FPGA35 |
| 61 | B1 | IO | DIFFIO_RX20p | AC32 | FPGA36 |
| 62 | | | | | GND |
| 63 | B1 | IO | DIFFIO_RX20n | AC31 | FPGA37 |
| 64 | | | | | GND |
| 65 | B1 | IO | DIFFIO_TX20p | AA27 | FPGA38 |
| 66 | B1 | IO | DIFFIO_TX20n | AA26 | FPGA39 |
| 67 | | | | | GND |
| 68 | B1 | IO | DIFFIO_RX19p | AB28 | FPGA40 |
| 69 | | | | | GND |
| 70 | B1 | IO | DIFFIO_RX19n | AB27 | FPGA41 |
| 71 | B1 | IO | DIFFIO_TX19p | Y25 | FPGA42 |
| 72 | | | | | GND |

*Table 3-2.* J-8 (male) Pin Assignment Table (Continued)

| J8 Pin | FPGA Bank | FPGA Pin Function | Other FPGA Pin Information | FPGA Ball | Board Net |
|---|---|---|---|---|---|
| 73 | B1 | IO | DIFFIO_TX19n | Y24 | FPGA43 |
| 74 | | | | | GND |
| 75 | B1 | IO | DIFFIO_RX18p | AD32 | FPGA44 |
| 76 | B1 | IO | DIFFIO_RX18n | AD31 | FPGA45 |
| 77 | | | | | GND |
| 78 | B1 | IO | DIFFIO_TX18p | W23 | FPGA46 |
| 79 | | | | | GND |
| 80 | B1 | IO | DIFFIO_TX18n | W22 | FPGA47 |
| 81 | B1 | IO | DIFFIO_RX17p | AE32 | FPGA48 |
| 82 | | | | | GND |
| 83 | B1 | IO | DIFFIO_RX17n | AE31 | FPGA49 |
| 84 | | | | | GND |
| 85 | B1 | IO | DIFFIO_TX17p | AD27 | FPGA50 |
| 86 | B1 | IO | DIFFIO_TX17n | AD26 | FPGA51 |
| 87 | | | | | GND |
| 88 | B1 | IO | DIFFIO_RX16p | AF32 | FPGA52 |
| 89 | | | | | GND |
| 90 | B1 | IO | DIFFIO_RX16n | AF31 | FPGA53 |
| 91 | B1 | IO | DIFFIO_TX16p | AC27 | FPGA54 |
| 92 | | | | | GND |
| 93 | B1 | IO | DIFFIO_TX16n | AC26 | FPGA55 |
| 94 | | | | | GND |
| 95 | B1 | IO | DIFFIO_RX15p | AG32 | FPGA56 |
| 96 | | | | | NRST |
| 97 | | | | | GND |
| 98 | B1 | IO | DIFFIO_RX15n | AG31 | FPGA57 |
| 99 | | | | | GND |
| 100 | B1 | IO | DIFFIO_TX15p | Y23 | FPGA58 |
| 101 | B1 | IO | DIFFIO_TX15n | Y22 | FPGA59 |
| 102 | | | | | GND |
| 103 | B1 | IO | DIFFIO_RX14p | AC30 | FPGA60 |
| 104 | | | | | GND |
| 105 | B1 | IO | DIFFIO_RX14n | AC29 | FPGA61 |
| 106 | B1 | IO | DIFFIO_TX14p | AA25 | FPGA62 |
| 107 | | | | | GND |
| 108 | B1 | IO | DIFFIO_TX14n | AA24 | FPGA63 |

*Table 3-2.* J-8 (male) Pin Assignment Table (Continued)

| J8 Pin | FPGA Bank | FPGA Pin Function | Other FPGA Pin Information | FPGA Ball | Board Net |
|---|---|---|---|---|---|
| 109 | | | | | GND |
| 110 | B1 | IO | DIFFIO_RX13p | AD30 | FPGA64 |
| 111 | B1 | IO | DIFFIO_RX13n | AD29 | FPGA65 |
| 112 | | | | | GND |
| 113 | B1 | IO | DIFFIO_TX13p | AB26 | FPGA66 |
| 114 | | | | | GND |
| 115 | B1 | IO | DIFFIO_TX13n | AB25 | FPGA67 |
| 116 | B1 | IO | DIFFIO_RX12p | AH32 | FPGA68 |
| 117 | | | | | GND |
| 118 | B1 | IO | DIFFIO_RX12n | AH31 | FPGA69 |
| 119 | | | | | GND |
| 120 | B1 | IO | DIFFIO_TX12p | AA23 | FPGA70 |
| 121 | B1 | IO | DIFFIO_TX12n | AA22 | FPGA71 |
| 122 | | | | | GND |
| 123 | B1 | IO | DIFFIO_RX11p | AE30 | FPGA72 |
| 124 | | | | | GND |
| 125 | B1 | IO | DIFFIO_RX11n | AE29 | FPGA73 |
| 126 | B1 | IO | DIFFIO_TX11p | AB24 | FPGA74 |
| 127 | | | | | GND |
| 128 | B1 | IO | DIFFIO_TX11n | AB23 | FPGA75 |
| 129 | | | | | GND |
| 130 | B1 | IO | DIFFIO_RX10p | AJ32 | FPGA76 |
| 131 | B1 | IO | DIFFIO_RX10n | AJ31 | FPGA77 |
| 132 | | | | | GND |
| 133 | B1 | IO | DIFFIO_TX10p | AC25 | FPGA78 |
| 134 | | | | | GND |
| 135 | B1 | IO | DIFFIO_TX10n | AC24 | FPGA79 |
| 136 | B1 | IO | DIFFIO_RX9p | AF30 | FPGA80 |
| 137 | | | | | GND |
| 138 | B1 | IO | DIFFIO_RX9n | AF29 | FPGA81 |
| 139 | | | | | GND |
| 140 | B1 | IO | DIFFIO_TX9p | AD25 | FPGA82 |
| 141 | B1 | IO | DIFFIO_TX9n | AD24 | FPGA83 |
| 142 | | | | | GND |
| 143 | B1 | IO | DIFFIO_RX8p | AG30 | FPGA84 |
| 144 | | | | | GND |

*Table 3-2.* J-8 (male) Pin Assignment Table (Continued)

| J8 Pin | FPGA Bank | FPGA Pin Function | Other FPGA Pin Information | FPGA Ball | Board Net |
|---|---|---|---|---|---|
| 145 | B1 | IO | DIFFIO_RX8n | AG29 | FPGA85 |
| 146 | B1 | IO | DIFFIO_TX8p | AE26 | FPGA86 |
| 147 | | | | | GND |
| 148 | B1 | IO | DIFFIO_TX8n | AE25 | FPGA87 |
| 149 | | | | | GND |
| 150 | B1 | IO | DIFFIO_RX7p | AH30 | FPGA88 |
| 151 | B1 | IO | DIFFIO_RX7n | AH29 | FPGA89 |
| 152 | | | | | GND |
| 153 | B1 | IO | DIFFIO_TX7p | AE28 | FPGA90 |
| 154 | | | | | GND |
| 155 | B1 | IO | DIFFIO_TX7n | AE27 | FPGA91 |
| 156 | B1 | IO | DIFFIO_RX6p | AF28 | FPGA92 |
| 157 | | | | | GND |
| 158 | B1 | IO | DIFFIO_RX6n | AF27 | FPGA93 |
| 159 | | | | | GND |
| 160 | B3 | IO | DQS16T | B27 | FPGA252 |
| 161 | B3 | IO | DQS17T | C28 | FPGA260 |
| 162 | | | | | GND |
| 163 | B3 | IO | DQ17T | B29 | FPGA261 |
| 164 | | | | | GND |
| 165 | B3 | IO | DQ17T | A29 | FPGA262 |
| 166 | B2 | IO | DIFFIO_TX51p | K25 | FPGA98 |
| 167 | | | | | GND |
| 168 | B2 | IO | DIFFIO_TX51n | K24 | FPGA99 |
| 169 | | | | | GND |
| 170 | B2 | IO | DIFFIO_RX50p | G28 | FPGA100 |
| 171 | B2 | IO | DIFFIO_RX50n | G27 | FPGA101 |
| 172 | | | | | GND |
| 173 | B2 | IO | DIFFIO_TX50p | H28 | FPGA102 |
| 174 | | | | | GND |
| 175 | B2 | IO | DIFFIO_TX50n | H27 | FPGA103 |
| 176 | B2 | IO | DIFFIO_RX49p | E30 | FPGA104 |
| 177 | | | | | GND |
| 178 | B2 | IO | DIFFIO_RX49n | E29 | FPGA105 |
| 179 | | | | | GND |
| 180 | B2 | IO | DIFFIO_TX49p | K27 | FPGA106 |

*Table 3-2.* J-8 (male) Pin Assignment Table (Continued)

| J8 Pin | FPGA Bank | FPGA Pin Function | Other FPGA Pin Information | FPGA Ball | Board Net |
|---|---|---|---|---|---|
| 181 | B2 | IO | DIFFIO_TX49n | K26 | FPGA107 |
| 182 | | | | | GND |
| 183 | B2 | IO | DIFFIO_RX48p | D32 | FPGA108 |
| 184 | | | | | GND |
| 185 | B2 | IO | DIFFIO_RX48n | D31 | FPGA109 |
| 186 | B2 | IO | DIFFIO_TX48p | J27 | FPGA110 |
| 187 | | | | | GND |
| 188 | B2 | IO | DIFFIO_TX48n | J26 | FPGA111 |
| 189 | | | | | GND |
| 190 | B2 | IO | DIFFIO_RX47p | F30 | FPGA112 |
| 191 | B2 | IO | DIFFIO_RX47n | F29 | FPGA113 |
| 192 | | | | | GND |
| 193 | B2 | IO | DIFFIO_TX47p | L28 | FPGA114 |
| 194 | | | | | GND |
| 195 | B2 | IO | DIFFIO_TX47n | L27 | FPGA115 |
| 196 | B2 | IO | DIFFIO_RX46p | G30 | FPGA116 |
| 197 | | | | | GND |
| 198 | B2 | IO | DIFFIO_RX46n | G29 | FPGA117 |
| 199 | | | | | GND |

Pins not listed in Table 3-3 below are not connected.

*Table 3-3.* J10 (female) Pin Assignment Table

| J10 Pin | FPGA Bank | FPGA Pin Function | Other FPGA Pin Information | FPGA Ball | Board Net |
|---|---|---|---|---|---|
| 1 | B2 | IO | DIFFIO_TX46p | L26 | FPGA118 |
| 2 | | | | | GND |
| 3 | B2 | IO | DIFFIO_TX46n | L25 | FPGA119 |
| 4 | | | | | GND |
| 5 | B2 | IO | DIFFIO_RX45p | H30 | FPGA120 |
| 6 | B2 | IO | DIFFIO_RX45n | H29 | FPGA121 |
| 7 | | | | | GND |
| 8 | B2 | IO | DIFFIO_TX45p | L24 | FPGA122 |
| 9 | | | | | GND |
| 10 | B2 | IO | DIFFIO_TX45n | L23 | FPGA123 |
| 11 | B2 | IO | DIFFIO_RX44p | J30 | FPGA124 |
| 12 | | | | | GND |

*Table 3-3.* J10 (female) Pin Assignment Table (Continued)

| J10 Pin | FPGA Bank | FPGA Pin Function | Other FPGA Pin Information | FPGA Ball | Board Net |
|---|---|---|---|---|---|
| 13 | B2 | IO | DIFFIO_RX44n | J29 | FPGA125 |
| 14 | | | | | GND |
| 15 | B2 | IO | DIFFIO_TX44p | M25 | FPGA126 |
| 16 | B2 | IO | DIFFIO_TX44n | M24 | FPGA127 |
| 17 | | | | | GND |
| 18 | B2 | IO | DIFFIO_RX43p | E32 | FPGA128 |
| 19 | | | | | GND |
| 20 | B2 | IO | DIFFIO_RX43n | E31 | FPGA129 |
| 21 | B2 | IO | DIFFIO_TX43p | M23 | FPGA130 |
| 22 | | | | | GND |
| 23 | B2 | IO | DIFFIO_TX43n | M22 | FPGA131 |
| 24 | | | | | GND |
| 25 | B2 | IO | DIFFIO_RX42p | F32 | FPGA132 |
| 26 | B2 | IO | DIFFIO_RX42n | F31 | FPGA133 |
| 27 | | | | | GND |
| 28 | B2 | IO | DIFFIO_TX42p | M27 | FPGA134 |
| 29 | | | | | GND |
| 30 | B2 | IO | DIFFIO_TX42n | M26 | FPGA135 |
| 31 | B2 | IO | DIFFIO_RX41p | G32 | FPGA136 |
| 32 | | | | | GND |
| 33 | B2 | IO | DIFFIO_RX41n | G31 | FPGA137 |
| 34 | | | | | GND |
| 35 | B2 | IO | DIFFIO_TX41p | N25 | FPGA138 |
| 36 | B2 | IO | DIFFIO_TX41n | N24 | FPGA139 |
| 37 | | | | | GND |
| 38 | B2 | IO | DIFFIO_RX40p | H32 | FPGA140 |
| 39 | | | | | GND |
| 40 | B2 | IO | DIFFIO_RX40n | H31 | FPGA141 |
| 41 | B2 | IO | DIFFIO_TX40p | N23 | FPGA142 |
| 42 | | | | | GND |
| 43 | B2 | IO | DIFFIO_TX40n | N22 | FPGA143 |
| 44 | | | | | GND |
| 45 | B2 | IO | DIFFIO_RX39p | J32 | FPGA144 |
| 46 | B2 | IO | DIFFIO_RX39n | J31 | FPGA145 |
| 47 | | | | | GND |
| 48 | B2 | IO | DIFFIO_TX39p | P23 | FPGA146 |

*Table 3-3.* J10 (female) Pin Assignment Table (Continued)

| J10 Pin | FPGA Bank | FPGA Pin Function | Other FPGA Pin Information | FPGA Ball | Board Net |
|---|---|---|---|---|---|
| 49 | | | | | GND |
| 50 | B2 | IO | DIFFIO_TX39n | P22 | FPGA147 |
| 51 | B2 | IO | DIFFIO_RX38p | K30 | FPGA148 |
| 52 | | | | | GND |
| 53 | B2 | IO | DIFFIO_RX38n | K29 | FPGA149 |
| 54 | | | | | GND |
| 55 | B2 | IO | DIFFIO_TX38p | N27 | FPGA150 |
| 56 | B2 | IO | DIFFIO_TX38n | N26 | FPGA151 |
| 57 | | | | | GND |
| 58 | B2 | IO | DIFFIO_RX37p | K32 | FPGA152 |
| 59 | | | | | GND |
| 60 | B2 | IO | DIFFIO_RX37n | K31 | FPGA153 |
| 61 | B2 | IO | DIFFIO_TX37p | P29 | FPGA154 |
| 62 | | | | | GND |
| 63 | B2 | IO | DIFFIO_TX37n | P28 | FPGA155 |
| 64 | | | | | GND |
| 65 | B2 | IO | DIFFIO_RX36p | L30 | FPGA156 |
| 66 | B2 | IO | DIFFIO_RX36n | L29 | FPGA157 |
| 67 | | | | | GND |
| 68 | B2 | IO | DIFFIO_TX36p | P27 | FPGA158 |
| 69 | | | | | GND |
| 70 | B2 | IO | DIFFIO_TX36n | P26 | FPGA159 |
| 71 | B2 | IO | DIFFIO_RX35p | N29 | FPGA160 |
| 72 | | | | | GND |
| 73 | B2 | IO | DIFFIO_RX35n | N28 | FPGA161 |
| 74 | | | | | GND |
| 75 | B2 | IO | DIFFIO_TX35p | P25 | FPGA162 |
| 76 | B2 | IO | DIFFIO_TX35n | P24 | FPGA163 |
| 77 | | | | | GND |
| 78 | B2 | IO | DIFFIO_RX34p | M30 | FPGA164 |
| 79 | | | | | GND |
| 80 | B2 | IO | DIFFIO_RX34n | M29 | FPGA165 |
| 81 | B2 | IO | DIFFIO_TX34p | R27 | FPGA166 |
| 82 | | | | | GND |
| 83 | B2 | IO | DIFFIO_TX34n | R26 | FPGA167 |
| 84 | | | | | GND |

*Table 3-3.* J10 (female) Pin Assignment Table (Continued)

| J10 Pin | FPGA Bank | FPGA Pin Function | Other FPGA Pin Information | FPGA Ball | Board Net |
|---|---|---|---|---|---|
| 85 | B2 | IO | DIFFIO_RX33p | L32 | FPGA168 |
| 86 | B2 | IO | DIFFIO_RX33n | L31 | FPGA169 |
| 87 | | | | | GND |
| 88 | B2 | IO | DIFFIO_TX33p | R23 | FPGA170 |
| 89 | | | | | GND |
| 90 | B2 | IO | DIFFIO_TX33n | R22 | FPGA171 |
| 91 | B2 | IO | DIFFIO_RX32p | N31 | FPGA172 |
| 92 | | | | | GND |
| 93 | B2 | IO | DIFFIO_RX32n | N30 | FPGA173 |
| 94 | | | | | GND |
| 95 | B2 | IO | DIFFIO_TX32p | R25 | FPGA174 |
| 96 | B2 | CLK1p | INPUT | T30 | FPGA175 |
| 97 | | | | | GND |
| 98 | B2 | IO | DIFFIO_RX31p | M32 | FPGA176 |
| 99 | | | | | GND |
| 100 | B2 | IO | DIFFIO_RX31n | M31 | FPGA177 |
| 101 | B2 | IO | DIFFIO_TX31p | R29 | FPGA178 |
| 102 | | | | | GND |
| 103 | B2 | IO | DIFFIO_TX31n | R28 | FPGA179 |
| 104 | | | | | GND |
| 105 | B2 | IO | DIFFIO_RX30p | P32 | FPGA180 |
| 106 | B2 | IO | DIFFIO_RX30n | P31 | FPGA181 |
| 107 | | | | | GND |
| 108 | B2 | IO | DIFFIO_TX30p | T28 | FPGA182 |
| 109 | | | | | GND |
| 110 | B2 | IO | DIFFIO_TX30n | T27 | FPGA183 |
| 111 | B2 | IO | DIFFIO_RX29p | R31 | FPGA184 |
| 112 | | | | | GND |
| 113 | B2 | IO | DIFFIO_RX29n | R30 | FPGA185 |
| 114 | | | | | GND |
| 115 | B2 | IO | DIFFIO_TX29p | T23 | FPGA186 |
| 116 | B2 | IO | DIFFIO_TX29n | T22 | FPGA187 |
| 117 | | | | | GND |
| 118 | B2 | IO | CLK0n/DIFFIO_RX_C0n | T31 | FPGA188 |
| 119 | | | | | GND |
| 120 | B2 | IO | CLK0p/DIFFIO_RX_C0p | T32 | FPGA189 |