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AT91CAP9-STK Starter Kit

User Guide

6351B–CAP–27-Jun-08

Table of Contents

Section 1

Introduction

1.1 Purpose

This document is a presentation of the hardware associated with the AT91CAP9-STK® Starter Kit.

This product is derived from the Atmel AT91CAP9-MZ and AT91CAP9-MB demonstration boards.

1.2 CAP™ Starter Kit Board

The AT91CAP9-STK Starter Kit is built on a single PCB, including:

- AT91CAP9S ARM926EJ-S™ -based microcontroller system-on-chip
- 64M Bytes of SDRAM application memory
- 512M Bytes of NAND Flash
- DataFlash® with up to 8M Bytes
- External interfaces for:
  - 10/100 Base-T Ethernet
  - USB Host and Full Speed/High Speed Device
  - ¼ VGA LCD Panel with Touch Screen
  - SD Card
  - 4 analog inputs
  - audio headphones
- Altera® Stratix®2 EP2S15F484 FPGA and its associated EPCS16 serial configuration memory. The FPGA provides 15600 four-input Lookup Table (LUT) equivalents, corresponding to approximately 124800 gates in the CAP MP Block.
- 64 general-purpose I/O connections from the AT91CAP9S, and 2 banks of 64 I/Os from the FPGA, for application-specific external interfaces
- CE-JTAG interface for CAP9 JTAG programming, and a USB-Blaster-JTAG interface for Stratix2 JTAG programming. These facilitate system debug.
- Atmel's AT73C224 and AT73C239 ICs for power supply and battery management.
- Atmel's AT73C213 for audio DAC
- Atmel's AT73C205 for battery charger

1.3 CAP Starter Kit Development Tools

The CAP Starter Kit is supplied with an essential set of development tools in order to get started immediately. These include:

- KickStart version of IAR™ Embedded Workbench® for ARM®
- Microsoft® Windows CE ® Board Support Package and demonstration from Adeneo
- Instructions for downloading Altera's free Quartus® 2 Web Edition tools for FPGA programming

1.4 Related Documents

1.4.1 Standards

JTAG IEEE® 1149.1 Standard.

1.4.2 Reference Documents

Table 1-1. Reference Documents

Description	Reference
Evaluation motherboard ORCAD schematics	20061027_11H20_AT91CAP9.dsn
Evaluation motherboard BOM	20061212_BOMASSY_ID2400_MOTHERBOARD.xls
Evaluation mezzanine board ORCAD schematics	20061122_09H00_AT91CAP9_MEZ.dsn
Evaluation mezzanine board BOM	20061207_ID2399_BOMASSY_MEZZANINE.xls
Atmel Specification	New Specification CAP9 Starter Kit
CAP9-STK hardware description.doc	ref. 4658D03
CAP9-STK ORCAD schematics	ref. ADEC101389001
CAP9-STK BOM	ref. ADEC101389003
CAP9-STK equipment plan	ref. ADEC101389EQ2

1.5 Glossary

BOM	Bill Of Materials
ICE	In-Circuit Emulator
JTAG	Joint Test Action Group
CAP	Customizable Microcontroller-based SoC Platform
CAP9-STK	CAP9 Starter Kit
FPGA	Field Programmable Gate Array
I/O	Input/Output
MCI	Multimedia Card Interface
MPB	Metal Programmable Block
MPIO	Metal Programmable I/O
NC	Not Connected
OHCI	Open Host Controller Interface
PLL	Phase Locked Loop
PMC	Power Management Circuit

Section 2

Requirements

2.1 General Description

The CAP9-STK's objective is to provide a rapid evaluation of the AT91CAP9 product and its derivatives. It does not allow a full emulation of a customized version of the CAP9, but is intended to familiarize the user with the customization concept and architecture of the CAP9.

It also demonstrates the operations of the analog companions provided by Atmel's AT73C family of products and the availability of the operating systems and software layers.

2.2 Interface and Function General Overview

AT91CAP9-STK interfaces and functions are as follows:

(Refer also to Figure 2-1 on page 2-3.)

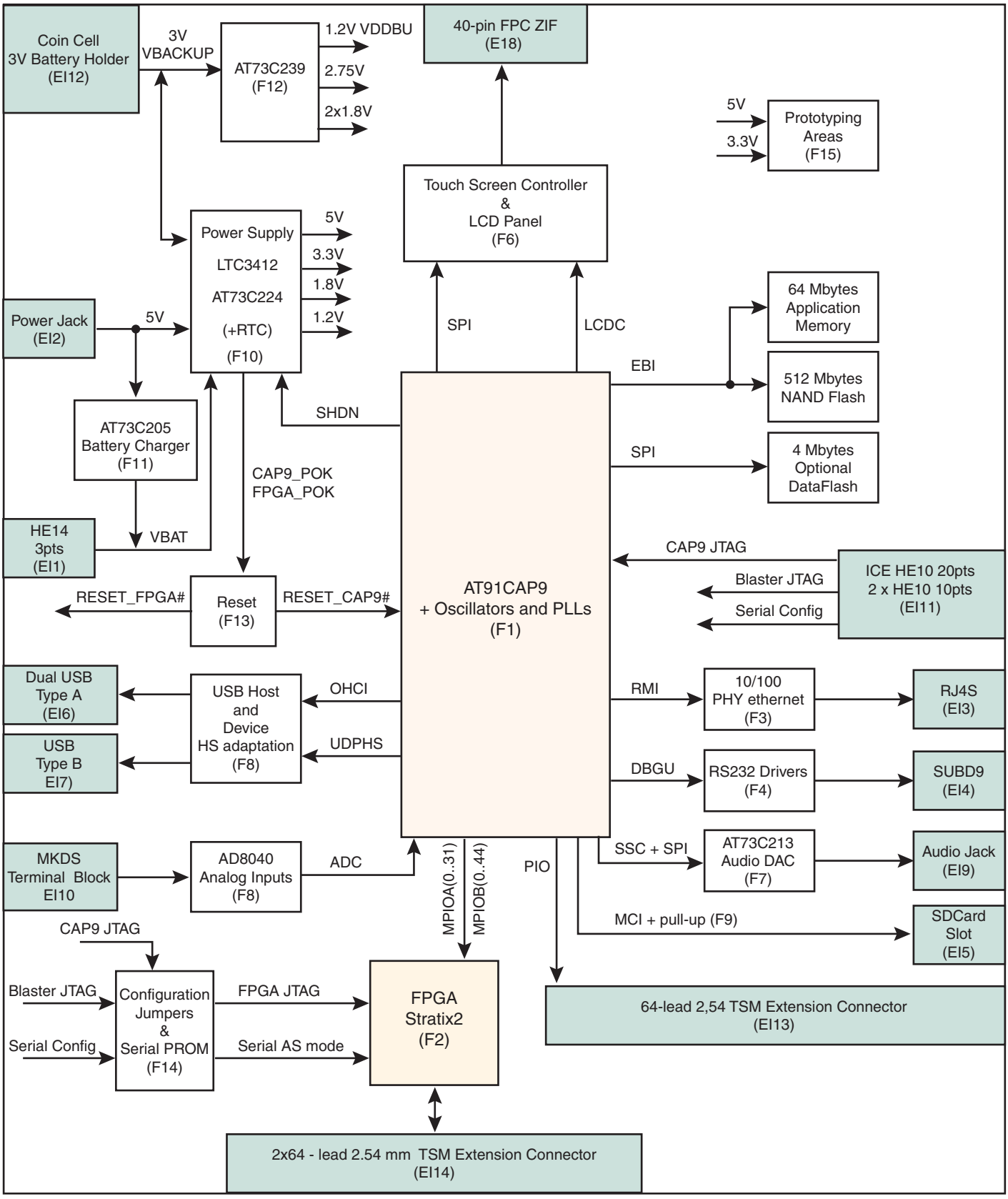
Interface

- EI1: 1 external Lithium-Ion battery
- EI2: 5V AC/DC sector adapter
- EI3: 1 RMII 10/100 Base-T Ethernet
- EI4: 1 Serial port, connected to the Debug Unit
- EI5: 1 SD Card slot
- EI6: 2 USB HOST interface
- EI7: 1 USB High Speed Device interface
- EI8: ¼ VGA LCD panel with Touch Screen
- EI9: 1 Audio stereo headset
- EI10: 4 Analog inputs
- EI11: 2 JTAG and 1 serial configuration interfaces
- EI12: 1 Manganese-Lithium coin battery
- EI13: 64-lead extension connector for the CAP9 I/O lines
- EI14: Two 64-lead extension connectors for the FPGA I/O lines

Function

- F1: AT91CAP9 microcontroller
- F2: FPGA and MPIO bus
- F3: RMII 10/100 Base-T Fast-Ethernet PHY Auto-MDIX.
- F4: RS232 driver
- F5: USB Host and Device
- F6: Touch screen controller and LCD panel
- F7: Audio DAC
- F8: Analog Inputs adaptation
- F9: SD Card
- F10: Power supplies and low power mode
- F11: Battery charger
- F12: RTC and Backup
- F13: Reset configuration
- F14: Programming and configuration
- F15: Prototyping Area

Figure 2-1. AT91CAP9-STK Interface and Function Overview



2.3 External Interfaces

2.3.1 EI1: External Lithium-ion Battery

The AT91CAP9-STK board implements one external Li-Ion battery 3-pin HE14 type connector..

Table 2-1. HE 14-3 Pinout

Pin	Signal Name	Description	Type	Level
1	VBAT	Battery power	I/O	4,5V
2	GND	Electrical ground	O	-
3	BAT_TS	Thermistor temperature sense	I	4,5V

2.3.2 EI2: 5VAC/DC Sector Adapter

CAP9-STK board implements one RAPC722 Switchcraft right angle miniature power jack with the following electrical characteristics:

- Contact resistance: 30 mΩ max
- Current carrying capability: 5A

2.3.3 EI3: RMII 10/100 Base-T Ethernet

An RJ45 8-pin Integrated Magnetics Connector is implement for the 10/100 Base-T Ethernet interface.

The connector integrates a 1 nF capacitor for HF shielding of the signal with chassis ground. (External connection between chassis and electrical ground is possible too.)

Table 2-2. RJ45-8 Pinout

Pin	Signal Name	Description	Type
1	TX+	Positive differential emission	O
2	TX-	Negative differential emission	O
3	RX+	Positive differential reception	I
6	RX-	Negative differential reception	I
4, 5, 7, 8	NC	-	-

2.3.4 EI4: Serial Port, Connected to the Debug Unit

A Debug right angle SUBD-9 connector is available in order to communicate with the AT91CAP9 microcontroller debug unit. This port is an electrical RS232 type connection. The connector integrates 2 additional pins (10, 11) for signal shielding.

Table 2-3. SUBD-P Pinout

Pin	Signal Name	Description	Type	Level
2	RXD	RS232 receive	I	±30V
3	TXD	RS232 transmit	O	±5V to ±5.2V
5, 10, 11	GND	Electrical ground	-	-
1, 4, 6, 7, 8, 9	NC	-	-	-

2.3.5 EI5: SD Card Slot

The AT91CAP9-STK board implements a 12-pin short type SDCARD slot on the bottom side.

Table 2-4. SD CARD Pinout

Pin	Signal Name	Description	Type	Level
1	MCI_DA3	Data 3	I/O	3.3V
2	MCI_CDA	Command/response	I/O open-drain	3.3V
3	GND	Electrical ground	-	-
4	3V3	3.3V power supply	O	3.3V
5	MCI_CK	Clock	O	3.3V
6	GND	Electrical ground	-	-
7	MCI_DA0	DATA 0	I/O	3.3V
8	MCI_DA1	DATA 1	I/O	3.3V
9	MCI_DA2	DATA 2	I/O	3.3V
10	MCI_CD	Card Detect	I	3.3V
11	GND	Electrical ground	-	-
12	NC	-	-	-

2.3.6 EI6: Two USB Host Interfaces

Two USB HOST connectors are available on a sign dual-port Type A connector.

Table 2-5. Dual-port Type A Connector Pinout

Pin	Signal Name	Description	Type
A1	5V	5V power supply (fuse 500mA)	O
A2	HDMA	Negative differential port A	I/O
A3	HDPA	Positive differential port A	I/O
A4	GND	Electrical ground	-
B1	5V	5V power supply (fuse 500mA)	O
B2	HDMB	Negative differential port B	I/O
B3	HDPB	Positive differential port B	I/O
B4	GND	Electrical ground	-
1 to 4	GND	Electrical ground	-

2.3.7 EI7: USB High Speed Device Interface

One USB Device High/Full Speed connector is available on a Type B connector.

Table 2-6. Type B Connector Pinout

Pin	Signal Name	Description	Type	Level
1	VBUS	5V supply	I	1
2	HSDM / FSDM	Negative differential port A	I/O	2
3	HSDP / FSDP	Positive differential port A	I/O	3
4, 5, 6	GND	Electrical	-	4, 5, 6

2.3.8 EI8: 1/4 VGA LCD Panel with Touch Screen

The AT91CAP9-STK board implements a 0.5 FPC, 40-pin ZIF LCD Panel connector, with contact on the bottom side. The connector integrates two additional pins (MC1, MC2) for signal shielding.

Table 2-7. 40-pin ZIF Connector Pinout

Pin	Signal Name	Description	Type	Level
1	3V3	3.3V power supply	O	3.3V
2	3V3	3.3V power supply	O	3.3V
3	3V3	3.3V power supply	O	3.3V
4	LCDDOTCK	Dot clock	O	3.3V
5	GND	Electrical ground	-	-
6	LCDHSYNC	Horizontal synchronization pulse	O	3.3V
7	GND	Electrical ground	-	-
8	LCDDEN	Timing signal for data	O	3.3V
9	GND	Electrical ground	-	-
10	NC	-	-	-
11	GND	Electrical ground	-	-
12	LCDD7	RED data 5	O	3.3V
13	LCDD6	RED data 4	O	3.3V
14	LCDD5	RED data 3	O	3.3V
15	GND	Electrical ground	-	-
16	LCDD4	RED data 2	O	3.3V
17	LCDD3	RED data 1	O	3.3V
18	LCDD2	RED data 0	O	3.3V
19	GND	Electrical ground	-	-
20	LCDD15	GREEN data 5	O	3.3V
21	LCDD14	GREEN data 4	O	3.3V
22	LCDD13	GREEN data 3	O	3.3V
23	GND	Electrical ground	-	-
24	LCDD12	GREEN data 2	O	3.3V
25	LCDD11	GREEN data 1	O	3.3V
26	LCDD10	GREEN data 0	O	3.3V
27	GND	Electrical ground	-	-
28	LCDD23	BLUE data 5	O	3.3V
29	LCDD22	BLUE data 4	O	3.3V
30	LCDD21	BLUE data 3	O	3.3V
31	GND	Electrical ground	-	-
32	LCDD20	BLUE data 2	O	3.3V
33	LCDD19	BLUE data 1	O	3.3V
34	LCDD18	BLUE data 0	O	3.3V
35	PCI	Power control	O	3.3V

Table 2-7. 40-pin ZIF Connector Pinout (Continued)

Pin	Signal Name	Description	Type	Level
36	VCTRL	LED current control	O	3.3V
37	Y_UP	Touch panel upper side	O	3.3V
38	X_LEFT	Touch panel left side	O	3.3V
39	Y_LOW	Touch panel low side	O	3.3V
40	X_RIGHT	Touch panel right side	O	3.3V

2.3.9 EI9: Audio Stereo Headset

A headset audio interface connector is available for a 3.5 phone jack stereo plug.

SMT 1503-03 Lumberg is used.

2.3.10 EI10: Analog Inputs

The AT91CAP9-STK board implements a 3.81mm-pitch Phoenix MKDS 6-pin terminal block. This connector receives four analog inputs.

Table 2-8. MKDS 6-pin Terminal Block Pinout

Pin	Signal Name	Description	Type	Level
1	ANALOG_I1	Analog input 1	I	3.3V
2	ANALOG_I2	Analog input 2	I	3.3V
3	ANALOG_I3	Analog input 3	I	3.3V
4	ANALOG_I4	Analog input 4	I	3.3V
5	GND	Electrical ground	-	-
6	NC (3V3)	- (It can be connected to 3.3V by 0Ω strap)	- (O)	- (3.3V)

2.3.11 EI11: JTAG and Serial Configuration Interfaces

Two programming JTAG interfaces and one serial configuration device interface are available on the board.

2.3.11.1 ICE-JTAG Interface

One ICE-JTAG interface is a right angle male, HE10 2x10-pin connector, to receive CAP9 ICE debugger probe for CAP9 JTAG programming.

Table 2-9. HE10 2x10-pin Connector Pinout

Pin	Signal Name	Description	Type	Level
1	3V3	3.3V power supply	O	3.3V
3	NTRST	Test Reset	I	3.3V (active low)
5	TDI	Test Data In	I	3.3V
7	TMS	Test Mode Select	I	3.3V
9	TCK	Test Clock	I	3.3V
11	RTCK	Returned Test Clock	O	3.3V
13	TDO	Test Data Out	O	3.3V

Table 2-9. HE10 2x10-pin Connector Pinout (Continued)

Pin	Signal Name	Description	Type	Level
15	NRST	Microcontroller Reset	I/O	3.3V (active low)
17, 19	NC	-	-	-
4, 6, 8, 10, 12, 14, 16, 18, 20	GND	Electrical ground	-	-

2.3.11.2 USB-Blaster-JTAG Interface

One USB-Blaster-JTAG interface is a straight male, HE10 2x5-pin connector, to receive the Altera FPGA USB Blaster probe for Stratix2 JTAG programming.

Table 2-10. HE10 2x5-pin Connector Pinout

Pin	Signal Name	Description	Type	Level
1	TCK	Test Clock	I	3.3V
3	TDO	Test Data Out	O	3.3V
5	TMS	Test Mode Select	I	3.3V
9	TDI	Test Data In	I	3.3V
4, 6	3V3	3.3V power supply	O	3.3V
7, 8	NC	-	-	-
2, 10	GND	Electrical ground	-	-

2.3.11.3 Serial Configuration Device Interface

The serial configuration device interface is a straight male, HE10 2x5-pin connector, to receive the Altera FPGA USB Blaster probe for serial EPCS Device programming.

Table 2-11. HE10 2x5-pin Connector Pinout

Pin	Signal Name	Description	Type	Level
1	DCLK	Configuration Clock pin	O	3.3V
3	CONF_DONE	Configuration Status pin	I/O	3.3V open-drain
5	nCONFIG	Configuration Control input	I	3.3V
6	nCE	Configuration Chip enable	I	3.3V (active low)
7	DATA0	Configuration Data input	I	3.3V
8	nCSO	Configuration Chip select	O	3.3V
9	ASDO_FPGA	Configuration Read enable	O	3.3V
4	3V3	3.3V power supply	O	3.3V
2, 10	GND	Electrical ground	-	-

2.3.12 EI12: Manganese-Lithium Coin Battery

The AT91CAP9-STK board implements a coin cell battery holder for 12 mm rechargeable 3V Manganese-Lithium coin battery, Panasonic ML1220 type.

3V non-rechargeable Lithium coin batteries are not supported.

2.3.13 EI13: 64-lead Extension Connector for the AT91CAP9 I/O Lines

A straight male, 2.54 mm-pitch, 64-pin connector is available on the board as a CAP9 extension connector.

Table 2-12. 64-pin Connector Pinout

Pin	Signal Name	Level	Pin	Signal Name	Level
1	5V	5V	2	5V	5V
3	5V	5V	4	GND	-
5	GND	-	6	GND	-
7	3V3	3.3V	8	3V3	3.3V
9	PA2/SPI0_SPCK	3.3V	10	GND	-
11	GND	-	12	PA0/SPI0_MISO	3.3V
13	PA9	3.3V	14	GND	-
15	GND	-	16	PA1/SPI0_MOSI	3.3V
17	PD1/SPI0_NPCS3	3.3V	18	PD0	3.3V
19	GND	-	20	3V3	3.3V
21	TWCK	3.3V open-drain	22	PA10/IRQ0	3.3V
23	GND	-	24	PA14/IRQ1	3.3V
25	TWD	3.3V open-drain	26	PA22/TXD0	VDDIOP1
27	PA24/RTS0	VDDIOP1	28	PA23/ RXD0	VDDIOP1
29	GND	-	30	PB12/SPI1_MISO	3.3V
31	PA27/PCK1	VDDIOP1	32	PB13/SPI1_MOSI	3.3V
33	VDDIOP1	3.3V or 1.8V	34	GND	-
35	PA26	VDDIOP1	36	PB14/SPI1_SPCK	3.3V
37	PA29	VDDIOP1	38	GND	-
39	PA30	VDDIOP1	40	PB15/SPI1_NPCS0	3.3V
41	PA31	VDDIOP1	42	PB16/SPI1_NPCS1	3.3V
43	VDDIOP1	3.3V or 1.8V	44	3V3	3.3V
45	GND	-	46	3V3	3.3V
47	PC12	3.3V	48	PC29	3.3V
49	PC13	3.3V	50	GND	-
51	PD2	3.3V	52	PD5/DMARQ2	3.3V
53	PC3	3.3V	54	GND	-
55	GND	-	56	PD6/NWAIT	1.8V
57	PD8/NCS5	1.8V	58	PD7/NCS4	1.8V
59	PD10/SCK1	1.8V	60	PD9/SCK2	1.8V
61	PD13/A24	1.8V	62	PD12/A23	1.8V
63	PD14 / A25	1.8V	64	1V8_CAP9	1,8V

2.3.14 EI14: Two 64-lead Extension Connectors for the FPGA I/O Lines

Two straight male, 2.54 mm-pitch, 64-pin connectors are available on the board as FPGA extension connectors.

The pinouts for both FPGA connectors are given in Table 2-13 and Table 2-14

Table 2-13. 64-pin Connector Pinout and Bank Assignment

Pin	FPGA IO/Power Name	Bank	Pin	FPGA IO/Power Name	Bank
1	GND	-	2	VCCIO4	BANK4
3	FPGA_IO0	BANK4	4	VCCIO4	BANK4
5	FPGA_IO1	BANK4	6	FPGA_IO2	BANK4
7	FPGA_IO3	BANK4	8	FPGA_IO4	BANK4
9	FPGA_IO5	BANK4	10	GND	-
11	FPGA_IO6	BANK4	12	FPGA_IO7	BANK4
13	FPGA_IO8	BANK4	14	FPGA_IO9	BANK4
15	FPGA_IO10	BANK4	16	FPGA_IO11	BANK4
17	FPGA_IO12	BANK4	18	FPGA_IO13	BANK4
19	GND	-	20	FPGA_IO14	BANK4
21	FPGA_IO15	BANK4	22	FPGA_IO16	BANK4
23	FPGA_IO17	BANK4	24	FPGA_IO18	BANK4
25	FPGA_IO19	BANK4	26	FPGA_IO20	BANK4
27	FPGA_IO21	BANK4	28	GND	-
29	FPGA_IO22	BANK4	30	FPGA_IO23	BANK4
31	FPGA_IO24	BANK4	32	FPGA_IO25	BANK4
33	FPGA_IO26	BANK4	34	FPGA_IO27	BANK4
35	GND	-	36	FPGA_IO28	BANK6
37	FPGA_IO29	BANK6	38	FPGA_IO30	BANK6
39	FPGA_IO31	BANK6	40	FPGA_IO32	BANK6
41	FPGA_IO33	BANK6	42	FPGA_IO34	BANK6
43	FPGA_IO35	BANK6	44	FPGA_IO36	BANK6
45	FPGA_IO37	BANK6	46	GND	-
47	FPGA_IO38	BANK6	48	FPGA_IO39	BANK6
49	FPGA_IO40	BANK6	50	FPGA_IO41	BANK6
51	FPGA_IO42	BANK6	52	FPGA_IO43	BANK6
53	FPGA_IO44	BANK6	54	FPGA_IO45	BANK6
55	GND	-	56	FPGA_IO46	BANK6
57	FPGA_IO47	BANK6	58	FPGA_IO48	BANK6
59	FPGA_IO49	BANK6	60	FPGA_IO50	BANK6
61	VCCIO6	BANK6	62	FPGA_IO51	BANK6
63	VCCIO6	BANK6	64	GND	-

Table 2-14. 64-pin Connector Pinout and Bank Assignment

Pin	FPGA IO/Power Name	Bank	Pin	FPGA IO/Power Name	Bank
1	GND	-	2	VCCIO6	BANK6
3	FPGA_IO	BANK6	4	VCCIO6	BANK6
5	FPGA_IO	BANK6	6	FPGA_IO	BANK6
7	FPGA_IO	BANK6	8	FPGA_IO	BANK6
9	FPGA_IO	BANK6	10	GND	-
11	FPGA_IO	BANK7	12	FPGA_IO	BANK7
13	FPGA_IO	BANK7	14	FPGA_IO	BANK7
15	FPGA_IO	BANK7	16	FPGA_IO	BANK7
17	FPGA_IO	BANK7	18	FPGA_IO	BANK7
19	GND	-	20	FPGA_IO	BANK7
21	FPGA_IO	BANK7	22	VCCIO7	BANK7
23	FPGA_IO	BANK7	24	VCCIO7	BANK7
25	FPGA_IO	BANK7	26	FPGA_IO	BANK7
27	FPGA_IO	BANK7	28	GND	-
29	FPGA_IO	BANK7	30	FPGA_IO	BANK7
31	FPGA_IO	BANK7	32	FPGA_IO	BANK7
33	FPGA_IO	BANK7	34	FPGA_IO	BANK7
35	FPGA_IO	BANK7	36	FPGA_IO	BANK7
37	GND	-	38	FPGA_IO	BANK7
39	FPGA_IO	BANK7	40	FPGA_IO	BANK7
41	FPGA_IO	BANK7	42	FPGA_IO	BANK7
43	VCCIO8	BANK8	44	FPGA_IO	BANK7
45	VCCIO8	BANK8	46	GND	-
47	FPGA_IO	BANK8	48	FPGA_IO	BANK8
49	FPGA_IO	BANK8	50	FPGA_IO	BANK8
51	FPGA_IO	BANK8	52	FPGA_IO	BANK8
53	FPGA_IO	BANK8	54	FPGA_IO	BANK8
55	GND	-	56	FPGA_IO	BANK8
57	FPGA_PLLOUTp	3.3V	58	GND	-
59	GND	-	60	FPGA_IO	BANK8
61	FPGA_PLLOUTn	3.3V	62	GND	-
63	GND	-	64	3V3	3.3V

2.4 Characteristics

2.4.1 Functional Characteristics

2.4.1.1 F1: AT91CAP9 Microcontroller

The AT91CAP9-STK microcontroller core block implements the necessary digital-system core functions.

It's composed of the following elements:

- One 32-bit-ARM9® AT91CAP9 microcontroller core and its power supplies (see below).
- One 1.8V, 512 Mbytes, 8-bit NAND Flash,
- One 1.8V, 64 Mbytes, 32-bit SDRAM Application Volatile Memory
- One optional 3.3V DataFlash® memory from 512 Kbytes to 8 Mbytes
- One Debug and JTAG Test unit (See “F14: Programming and Configuration” on page 2-27.)
- One MPB

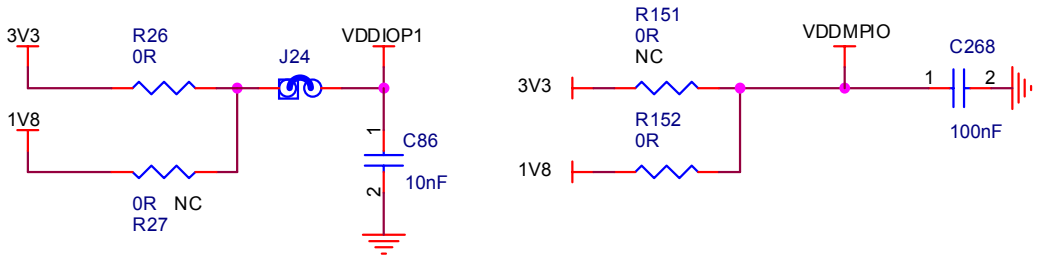
2.4.1.1.1 AT91CAP9 Power Supplies

The power supply of the AT91CAP9 Microcontroller is shown below.

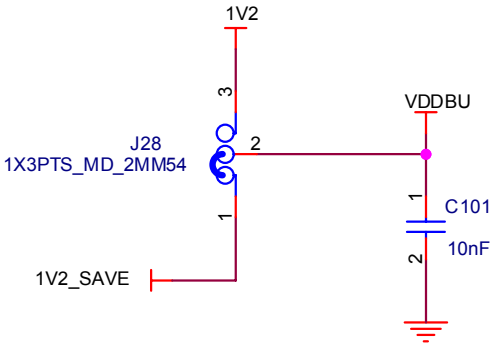
Table 2-15. AT91CAP9 Power Supply

Power Supply Name	Power Supply
VDDCORE	1V2_CAP9
VDDPLL	3V3
VDDUPLL	1V2_CAP9 (RC filtered)
VDDUTMII	3V3
VDDIOP0	3V3
VDDIOP1	3V3 or 1V8_CAP9
VDDUTMIC	1V2_CAP9
VDDIOM	1V8
VDDMPIO	3V3 or 1V8_FPGA
VDDBU	1V2_SAVE or 1V2_CAP9
VDDANA	3V3 filtered
VREFP	VREFP (3V)

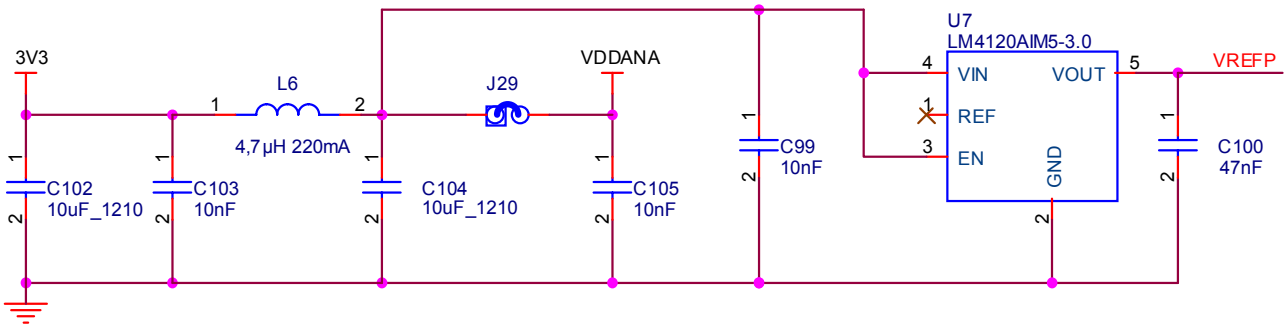
- For VDDIOP1 and VDDMPI0, the choice is made by 0Ω resistors:



- For VDDBU, the choice is made by a jumper on the 3-pin J28 connector:



- The implementation of VDDANA and VREEP is shown below.



2.4.1.1.2 AT91CAP9 Clocks

The internal clocks of the AT91CAP9 are generated by two external quartz sources:

- 12 Mhz quartz for the MAINCK internal clock
- 32,768 kHz quartz for the SLCK internal slow clock

2.4.1.2 F2: FPGA and MPIO Bus

2.4.1.2.1 FPGA Characteristics

This function is performed by an Altera Stratix2, EP2S15F484 FPGA and its EPCS16 serial configuration device.

Stratix2 EP2S,15F484 FPGA characteristics are:

- 15600 equivalent LE (LE is four-input LUT-based architecture),
- 1.2V core power supply, 3.3V or 1.8V I/O bank power supplies,
- 484-pin FBGA,
- -5 speed grade.

The FPGA aims to emulate the logic to be implemented in the MPB through 5 metal layers.

The FPGA also manages the EI14 interface.

2.4.1.2.2 MPIO Bus Characteristics

The FPGA is connected to the AT91CAP9 microcontroller through the two MPIO buses:

- First MPIO bus: MPIOA[0:31], connected to FPGA bank 1
- Second MPIO bus: MPIOB[0:44], connected to FPGA banks 2 and 5
- Bus frequency: 100MHz
- Dedicated MPIO bus clock: MPIOB24

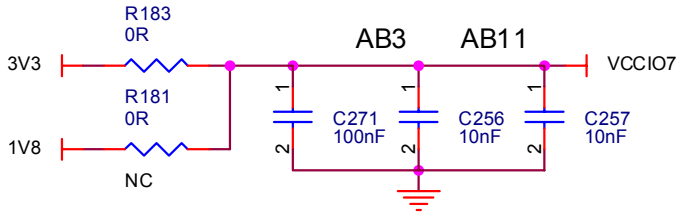
2.4.1.2.3 FPGA Power Supplies

Table 2-16. FPGA Bank Power Supplies

Bank 1	VDDMPIO (default 1V8_FPGA)
Bank 2	VDDMPIO (default 1V8_FPGA)
Bank 3	3V3
Bank 4	VCCIO4 (default 3V3)
Bank 5	VDDMPIO (default 1V8_FPGA)
Bank 6	VCCIO6 (default 1V8_FPGA)
Bank 7	VCCIO7 (default 3V3)
Bank 8	VCCIO8 (default 3V3)
Bank 9	3V3
Bank 10	3V3

Power for VDDMPIO, VCCIO4, VCCIO6, VCCIO7, and VCCIO8 can be supplied either by 3V3 or 1V8 (1V8_CAP9) power supplies. (See “F10: Power Supplies and Low-power Mode” on page 2-22.)

Choice is made by 0Ω resistor as shown below (VCCIO7 example):



Each of the six FPGA PLL blocks have two power supply pins: VCCA_PPLw and VCCD_PPLx (x = from to 6).

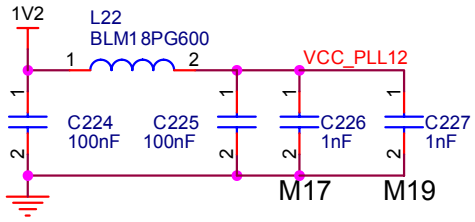
Table 2-17. FPGA PLL Block Power Supply

PLL Supply Pin Name	Power Supply
VCCA_PPL1	VCC_PLL12
VCCA_PPL2	VCC_PLL12
VCCA_PPL3	VCC_PLL34
VCCA_PPL4	VCC_PLL34
VCCA_PPL5	VCC_PLL56

Table 2-17. FPGA PLL Block Power Supply (Continued)

PLL Supply Pin Name	Power Supply
VCCA_PPL6	VCC_PLL56
VCCD_PPL1	1V2_CAP9
VCCD_PPL2	1V2_CAP9
VCCD_PPL3	1V2_CAP9
VCCD_PPL4	1V2_CAP9
VCCD_PPL5	1V2_CAP9
VCCD_PPL6	1V2_CAP9

VCC_PLL12, VCC_PLL34, VCC_PLL56 are 1V2 (1V2_CAP9) ferrite isolated power supplies as shown below (VCC_PLL12 example):

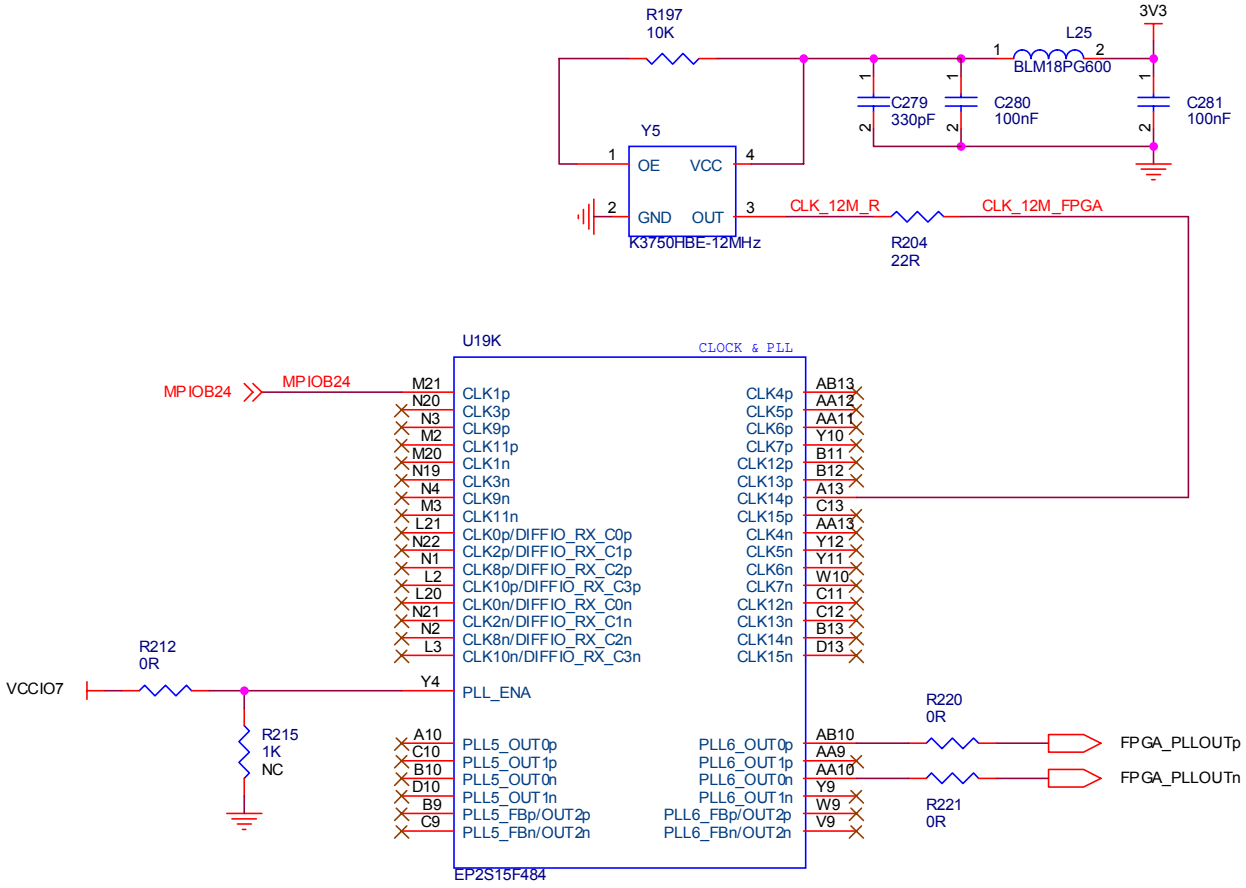


2.4.1.2.4 FPGA Clock

The MPIO Bus clock MPIOB24 is connected to the CLK1p clock input pin of the FPGA. An additional external 12 MHz oscillator generates clock to the CLK14p clock input pin of the FPGA.

Spare clock PLL_OUTp and PLL_OUTn are connected to the EI14 interface.

FPGA clock part electrical connection is shown below.

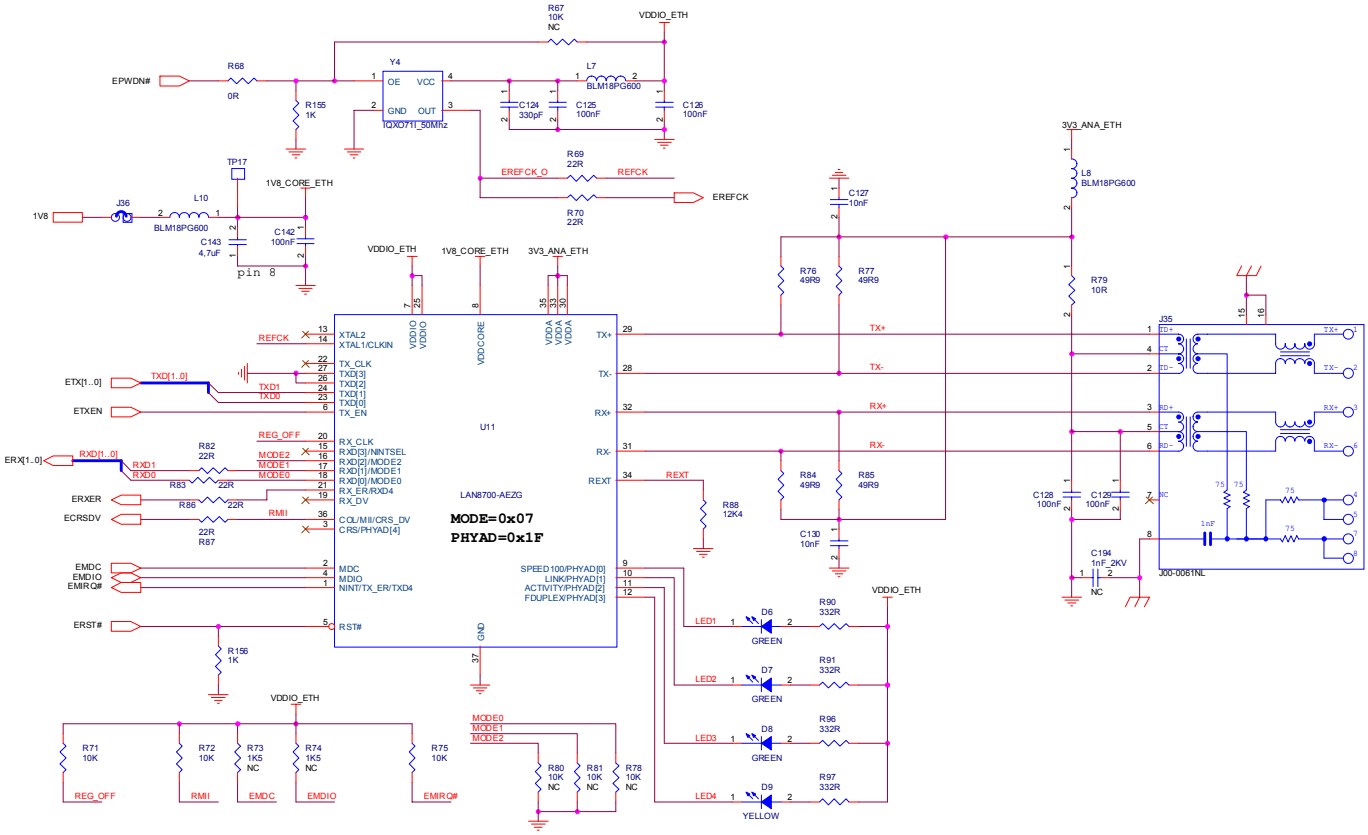


2.4.1.3 F3: RMII 10/100 Base-T Fast-Ethernet PHY Auto-MDIX

The 10/100 Ethernet MAC function is implemented in the AT91CAP9 EMAC module.

This module manages an RMII 10/100 Base-T Fast-Ethernet PHY Auto-MDIX (SMSC LAN8700) to implement a 10/100 Base-T Ethernet port.

The implementation is shown below.



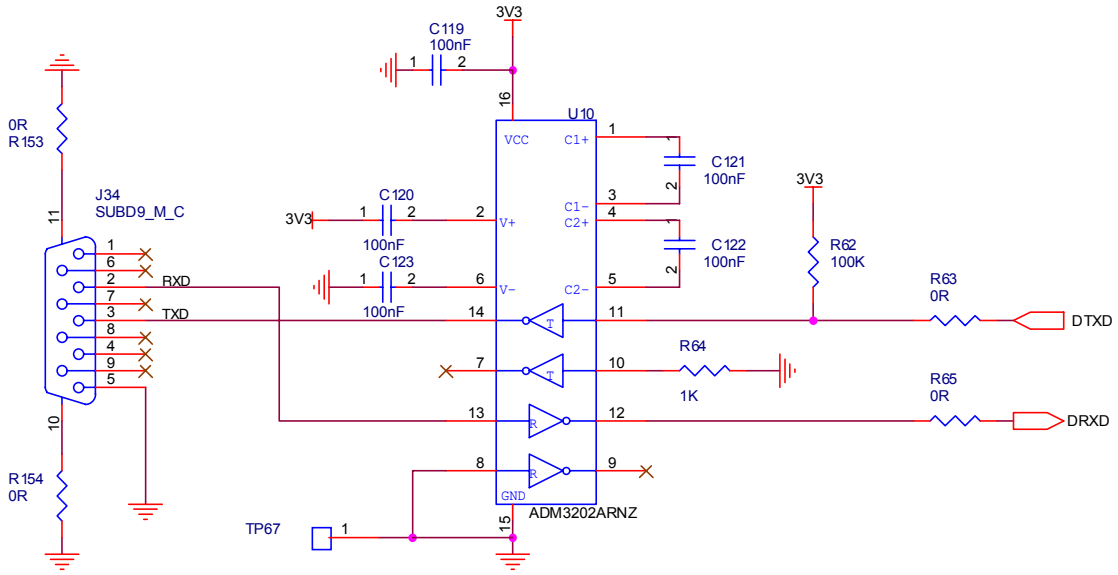
The 1.8V core power supply is external by default, to minimize 3.3V power consumption.

Use of LAN8700 3.3V/1.8V internal regulator can be done by disconnected J36 and R71 REG_OFF Pull-up.

2.4.1.4 F4: RS232 Driver

An ADM3202 RS232 driver is implemented for signal adaptation between RS232 signals (RXD, TXD) on the debug port connector and AT91CAP9 Debug unit 3.3V signals (DRXD, DTXD).

The implementation is shown below:



2.4.1.5 F5: USB Host and Device

2.4.1.5.1 USB Host

The two USB v2.0 Host interfaces are managed by the AT91CAP9 USB Host port, which handles OHCI protocol as well as USB v2.0 Full-speed and Low-speed protocols.

Two NUF2101 USB filters are implemented for ESD protection and line adaptation (26.3Ω to 33.7Ω). One 0603 footprint is implemented on each signal to adjust 39Ω line impedance if necessary.

One 500 mA SMD fuse is added on 5V power supply of each port.