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AT91SAM7A1-EK Evaluation Board

User Guide

Table of Contents

Section 1
Overview

1.1 Scope

The AT91SAM7A1-EK Evaluation Board enables real-time code development and evaluation. It supports the AT91SAM7A1 microcontroller.

1.2 Deliverables

The evaluation board is supplied with:

- an AT91SAM7A1 evaluation board called the AT91SAM7A1-EK
- a bare power lead, a fuse, 2 jumpers
- a 25-pin parallel cable
- the AT91 CD-ROM including:
  - Summary and full datasheets, datasheets with electrical and mechanical characteristics
  - Application notes and Getting Started documents for all development boards and AT91 microcontrollers
  - An AT91 Software package with C and assembly listings is also provided. This allows the user to begin evaluating the AT91 ARM® Thumb® 32-bit microcontroller quickly.

1.3 AT91SAM7A1 Evaluation Board

The board consists of:

- The Atmel AT91SAM7A1 ARM-based microcontroller
- Memories
  - 512 Kbyte 16-bit/8-bit SRAM
  - 2 Mbyte 16-bit Flash
- Footprint for an 8 Kbyte SPI EEPROM
- Communications interface
  - 1 CAN port wired on SubD9 connector
  - 2 LIN ports and 1 RS232 interface
  - 1 LIN port and 2 RS232 interfaces
  - 1 LIN port and 1 RS232 modem-compliant interface

- Main machine interfaces
  - 1 LCD (2 lines x 16 characters with backlight)
  - 1 reset push button
  - 1 piezoelectric buzzer
  - 3 LEDs connected to the PIO/Timer module
  - 3 programmable push buttons
- Miscellaneous
  - Current measurement possibility
  - Temperature measurement
  - Contrast voltage measurement
  - Configurable straps for flexibility
- ICE interface
  - A standard 20-pin ICE interface connector
  - An embedded ICE Interface linked to SubD25 connector
- Power supply features
  - DC power line filtering
  - Diode bridge
  - Adjustable voltage regulators
- Clocks
  - 6 MHz and 32.768 KHz crystals
- Expansion connectors
  - Most chip I/Os accessible via two 50-pin connectors (J17, J18)
  - EBI expansion connector allowing plug-in of memory board or Ethernet board

Section 2

Setting Up the AT91SAM7A1-EK Evaluation Board

2.1 Requirements

In order to set up the AT91SAM7A1-EK Evaluation Board, the following elements are required:

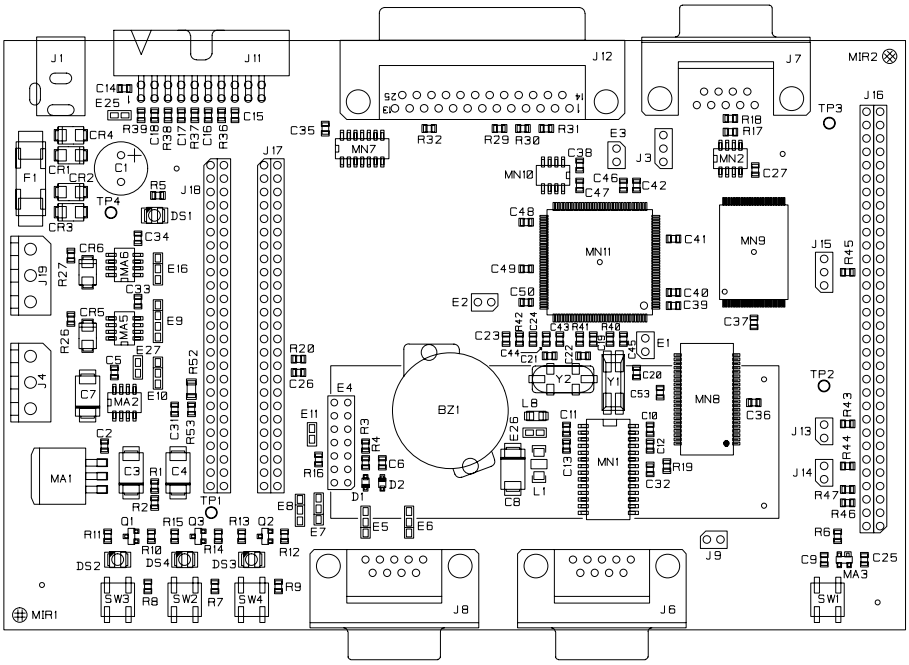
- the AT91SAM7A1-EK Evaluation Board itself
- a DC power supply capable of supplying 7V to 12V @ 400 mA (not supplied)

2.2 Electrostatic Warning

The AT91SAM7A1-EK Evaluation Board is shipped in protective anti-static packaging. The board must not be subjected to high electrostatic potentials. A grounding strap or similar protective device should be worn when handling the board. Avoid touching the component pins or any other metallic element.

2.3 Layout

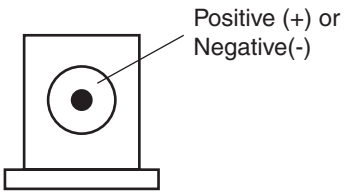
Figure 2-1. Top Level Layout



2.4 Voltage

DC power is supplied to the board via the 2.1 mm connector (J1) shown in Figure 2-2. The polarity of the power supply is not critical. The minimum voltage required is 7V. The supply must be isolated from ground. The 0 volts of the on-board regulated supplies can be connected to ground via any one of the 4 test points, TP1 to TP4.

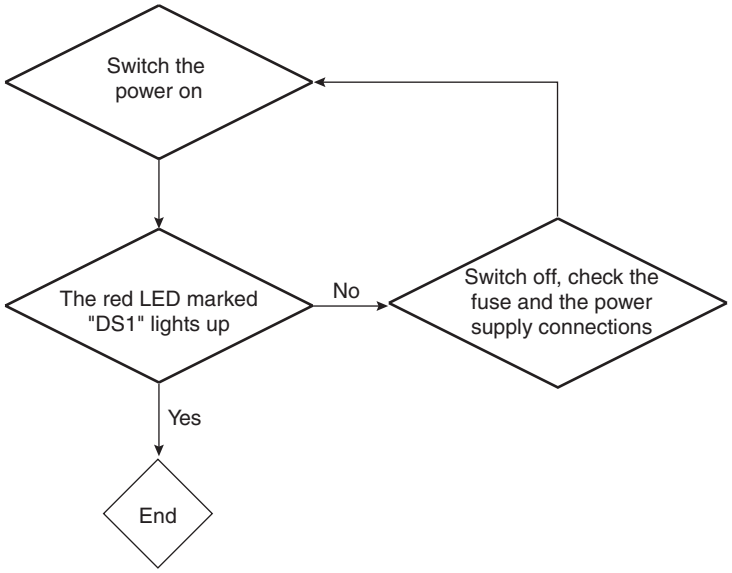
Figure 2-2. 2.1mm Connector



The board has a voltage regulator providing +3.3V and another providing +5V. These regulators allow the input voltage to be from 7V to 12V.

2.5 Powering Up the Board

Figure 2-3. Powering Up the Board



2.6 Measuring Current Consumption on the AT91SAM7A1

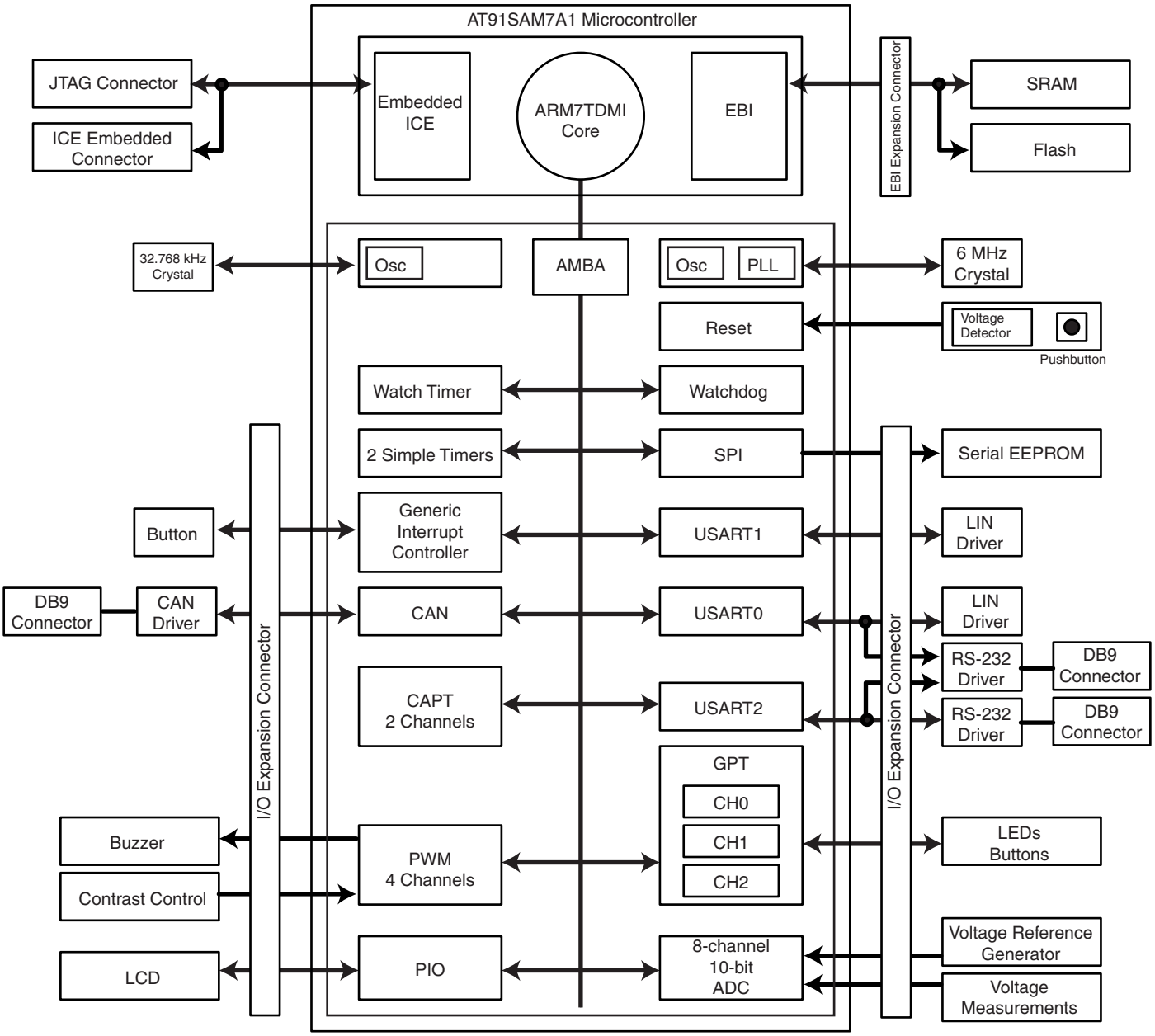
The board is designed to generate the entire power supply of the AT91SAM7A1 device. The PCB power tracks to the ARM7 core, the I/O and the analog cells are independent. This feature enables measurement of the current consumption of the different major parts of the AT91SAM7A1 device.

Table 2-1. Current Consumption Measurement Procedure

Block to Measure	Strap to Unsolder	Action
Core	E1	Connect an ammeter in place of the strap
Analog Cells	E2	
I/O Cells	E3	

2.7 AT91SAM7A1-EK Block Diagram

Figure 2-4. AT91SAM7A1-EK Evaluation Board Block Diagram



Section 3

Board Description

3.1 AT91SAM7A1-EK Top Level

The AT91SAM7A1-EK evaluation board consists of eight main blocks. Each block is described in the sections that follow.

The block diagram is shown in Figure 2-4.

3.2 AT91SAM7A1 Processor

The processor is based on an ARM7TDMI® 32-bit core and provides

- Standard modules (e.g., timers and USART)
- Specific modules (e.g., CAN)

The footprint is for a 144-pin TQFP package.

The jumpers E1, E2 and E3 can be removed to allow measurement of the current required by the microcontroller.

For more details, refer to Figure 4-3.

3.3 Power Supply Block

The voltage regulator provides 3.3V, 5V and analog 3.3V to the board and lights the red LED when operating.

Power can be applied via the 2.1 mm connector to the regulator in either polarity because of the diode rectifying circuit.

The regulators can tolerate supply transients up to 30V although they shut down without damage if they overheat.

The I/O power is configurable. Jumper J3 allows the selection of either 3.3V or 5V. The board also provides jumpers that measure the power of the microcontroller.

By unsoldering straps, an ammeter can be connected. Strap E1 is used to measure core consumption. Strap E3 is used to measure I/O cell consumption; the analog cell consumption is measured by jumper E2.

For more details, refer to Figure 4-3.

3.4 Application Interface

The board provides the following application interfaces:

Table 3-1. Board Application Interfaces

Part	Description
Reset push button	Detects and then resets the board when the 3.3V supply voltage drops below 2.7V. Allows manual reset of both board and microcontroller.
Red LED DS2	Connected to timer (or I/O) pin TIOA0 (GPT module)
Orange LED DS3	Connected to timer (or I/O) pin TIOA1 (GPT module)
Green LED DS4	Connected to timer (or I/O) pin TIOB0 (GPT module)
SW2 push button SW3 push button	Connected to input pins TIOA2 and TIOB1 (or I/O) of the timer (GPT module)
SW4 push button	Connected to GIC (Generic Interrupt Controller) module IRQ0 input. Allows the user to generate interrupts manually.
Buzzer	Connected to the PWM0 output. It demonstrates the PWM (Pulse Width Modulation) features. It is possible to enable/disable the buzzer by opening/closing jumper J10. The PWM0 output signal can be a 3V3 or 5V (jumper J3). The voltage influences the volume of the sound.
LCD connected to PIO	Displays 2 lines of 16 characters each. The LCD is driven by the PIO which can be powered by 3V3 or 5V. The LCD tolerates these two voltages. Users can display messages on the LCD. The contrast voltage is provided by the PWM1 and can be measured by ADC0 channel 0.

For more details, refer to Figure 4-3 and Figure 4-4.

3.5 CAN Bus

The CAN0 module is connected to a female SubD9 connector (J7) via the CAN driver MN2.The pinout is described in Table 3-2.

Figure 3-1. Female DB9 Connector

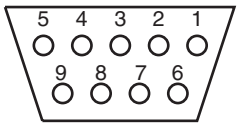


Table 3-2. Pinout

SubD9 Pin	Function
4	CAN-L
3	GND
8	CAN-H
others	Not connected

The CAN bus resistive load is 60 Ohm. It is made up of two 120 Ohm resistors in parallel. The recommended CAN bus load is 60 Ohm. Depending on the external input bus resistor, users can disconnect resistors to achieve the correct bus load.

For more details, refer to Figure 4-5.

3.6 LIN Buses and RS-232 Lines

Via USART modules, the AT91SAM7A1-EK board provides the following:

- 2 LIN buses and 1 RS-232 line

or

- 1 LIN bus and 2 RS-232 lines

or

- 2 LIN and 1 RS-232 modem-compliant interfaces

Table 3-3. 2 LIN Buses and 1 RS-232 Interface

Communication Type	Connector	AT91SAM7A1 Peripheral	Closed Straps	Open Straps
LIN	J19	USART1	No strap	No strap
LIN	J4	USART0	E9: 3 - 4	E9: 2 - 3
RS232	J8	USART2	J9	

Table 3-4. 1 LIN Bus and 2 RS-232 Interfaces

Communication Type	Connector	AT91SAM7A1 Peripheral	Closed Straps	Open Straps
LIN	J19	USART1	No strap	No strap
RS232	J6	USART0	E9: 2 - 3	E9: 3 - 4
			E16: 2 -3	E16: 1 - 2
			E5: 2 -3	E5: 1 - 2
			E6: 2 -3	E6: 1 - 2
RS232	J8	USART2	J9	

Table 3-5. 2 LIN Buses and 1 RS-232 Modem-compliant Interface

Communication Type	Connector	AT91SAM7A1 Peripheral	Closed Straps	Open Straps
LIN	J19	USART1	No strap	No strap
LIN	J4	USART0	E9: 3 - 4	E9: 2 - 3
RS232 Modem	J8	USART2	J9	
		UPIO	E16: 1 - 2	E16: 2 - 3
			E9: 1 - 2	E16: 2 -3
			E5: 1 - 2	E5: 2 -3
			E6: 1 - 2	E6: 2 -3

Note: The UPIO[5:0] are shared between the LCD interface and the RS-232 driver MN1. To avoid signal conflicts, these two devices should not be used at the same time.

The RS-232 interfaces are connected to two SubD9 male connectors:

- Connector J6 for the simple RS-232 interface (RX/TX)
- Connector J8 for the RS-232 modem-compliant interface (RX/TX/DSR/CTS, etc.)

The pinout for the DB9 connector J6 used by the USART0 is described in Table 3-6.

Table 3-6. J6 Pinout

J6 Pin	Function	AT91SAM7A1 Pin (1)
2	RX (Receive Data)	RXD0
3	TX (Transmit Data)	TXD0
5	Ground	GND
Others	Not connected	Not connected

Note: 1. Depends on the strap configuration.

The pinout for the DB9 connector J8 used by the USART0, USART2 and UPIO[5:0] is described in Table 3-7.

Table 3-7. J8 Pinout

J8 Pin	Function	AT91SAM7A1 Pin (1)
1	CD (Carrier Detect)	UPIO1/RXD0
2	RX (Receive Data)	RXD2
3	TX (Transmit Data)	TXD2
4	DTR (Data Terminal Ready)	UPIO0/TXD0
5	Ground	GND
6	DSR (Data Set Ready)	UPIO3
7	RTS (Request to Send)	UPIO2
8	CTS (Clear to Send)	UPIO4
9	RI (Ring Indicator)	UPIO5

Note: 1. Depends on the strap configuration.

Note: Depending on the strap configuration, either SubD9 pin 1 or 4 can be controlled by UPIO or by USART0 pins.
The schematic of these connectors is the same as the one used by the CAN0 module (see Section 3.5).

The LIN interfaces are connected to two three-pin header connectors:

- Connector J19
- Connector J4

The pinout for the connector J19 used by the USART1 is described Table 3-8.

Table 3-8. J19 Pinout

J19 Pin	Function	AT91SAM7A1 Pin (1)
1	Vs (8V - 18V)	
2	LIN (Local Interconnect Network)	TXD1/RXD1
3	Ground	GND

Note: 1. Depends on the strap configuration.

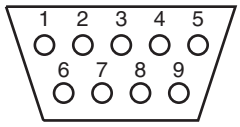
The pin-out for the connector J4 used by the USART0 is described Table 3-9.

Table 3-9. J4 Pinout

J4 Pin	Function	AT91SAM7A1 Pin (1)
1	Vs (8V - 18V)	
2	LIN (Local Interconnect Network)	TXD0/RXD0
3	Ground	GND

Note: 1. Depends on the strap configuration.

Figure 3-2. Male DB9 Connector



For more details, refer to Figure 4-6.

3.7 Crystal Oscillators and Clock Distribution

The system clock is derived from a 6 MHz crystal oscillator mounted on-board. At reset, the on-chip PLL-based frequency multiplier is disabled, using the frequency of the crystal oscillator as the default master clock. The low-frequency clock used for the low-power mode, the Watchtimer module and the Watchdog module can be leaded by a 32 kHz crystal oscillator or a division of the 6 MHz crystal oscillator. At reset, the low-frequency clock is configured on the 32 kHz crystal oscillator mounted on-board.

For more details, refer to Figure 4-2.

3.8 Memory Organization

The Flash memory is an AT49BV1614A (1Mx16-bit). Write-protection for half of the on-board Flash memory is provided. Output 2 of Jumper J15 drives the address pin 20 of the Flash.

To access the whole memory, put a jumper in J5: 1 - 2.

To protect the upper memory and access only the lower memory (from 0x40000000 to 0x40080000: only 1 Mbyte), put a jumper in J5: 2 - 3.

To protect the lower memory and access only the upper memory (from 0x40080000 to 0x40100000: only 1 Mbyte), close the jumper from J5: 2 - 3.

The mapping defined by the boot software is shown in Table 3-10.

Table 3-10. Memory Mapping

Element	Address
Flash	0x40000000
SRAM	0x48000000

3.9 I/O Expansion

Two I/O expansion connectors (J17 and J18) provide the users with the general-purpose I/O (GPIO) lines, analog lines, VDD and ground. The connectors are not fitted at the factory; however, the user can fit any 2 x 25 connector on a 0.1" (2.54 mm) pitch. For connector pin-out details, see Figure 4-10.

3.10 External Bus Interface

Figure 4-8 shows one 2 MByte 16-bit Flash (AT49BV1614A-90TC) and a 512 Kbyte 16-bit SRAM device (Alliance AS7C34098-10TC or equivalent).

Figure 4-9 shows the bus expansion connector (J16) that, like the I/O expansion connector (J17 and J18), is not fitted at the factory. The user can fit any 32 x 2 connector on a 0.1" (2.54 mm) pitch to gain access to the data, address, chip select, read/write, oscillator output and wait state pins. VDD and ground are available on the connector.

On-board jumpers (J13, J14 and J15) allow the user to connect Chip Selects either to on-board memories or to the expansion connector.

In most case, jumpers should be set up as in Table 3-11.

Table 3-11. Board Jumper Configuration

Jumper	Jumper Configuration	Description
J13	1 - 2 closed	On-board Flash driven by NCS0
	1 - 2 left open	On-board Flash always de-selected
J14	1 - 2 closed	On-board SRAM driven by NCS1
	1 - 2 left open	On-board SRAM always de-selected
J15	1 - 2 closed 2 - 3 left open	On-board Flash address line 20 is driven. User can access the whole memory space.
	1 - 2 left open 2 - 3 closed	On-board Flash upper memory protected. User can access only the 1 Mbyte lower space.
	1 - 2 left open 2 - 3 left open	On-board Flash lower memory protected. User can access only the 1 Mbyte upper space.

3.11 ICE Interface

An ARM®-standard 20-pin box header (J11) is provided to enable connection of an ICE interface to the JTAG inputs on the AT91SAM7A1 device. This allows code to be developed on the board without the use of system resources such as memory and serial ports. A mini ICE interface is embedded on the board. It is accessed by a parallel port connector (J12).

Note: To use a standard external ICE interface in target powered mode, it is necessary to close the strap E25 that enables the VCC power supply on the JTAG port.

For more details, refer to Figure 4-7.

3.12 Default Strap Configuration

Table 3-12. Default Strap Configuration

Schematic	Strap/Jumper	Configuration	Description
Figure 4-3	E1	Closed	VDDCORE connected to VDD
	E2	Closed	AVDDCORE connected to AVDD
	E3	Closed	VDDIO connected to VDDPERIPH
	J3	1 - 2 closed 2 - 3 open	VDDPERIPH connected to VDD
	E26	Closed	AGND connected to GND
	E10	1 - 2 closed 2 - 3 open	MA2 EN_pin connected to NRESET
Figure 4-4	E7	1 - 2 closed 2 - 3 open	E4-1 (LCD pin 1) connected to VDDPERIPH
	E8	1 - 2 closed 2 - 3 open	E4-2 (LCD pin 2) connected to GND
Figure 4-6	E9	2 - 3 closed 1 - 2 open 3 - 4 open	1 LIN and 2 RS-232 interfaces
	E16	2 - 3 closed 1 - 2 open	
	E5	2 - 3 closed 1 - 2 open	
	E6	2 - 3 closed 1 - 2 open	
Figure 4-7	J9	Closed	
	E25	Closed	Power on the JTAG connection
Figure 4-8	J13	Closed	NCS-FLASH connected to NCS0
	J14	Closed	NCS-SRAM connected to NCS1
	J15	1 - 2 closed 2 - 3 open	Flash pin A19 connected to signal A20/CS7 (whole memory accessible)

Section 4

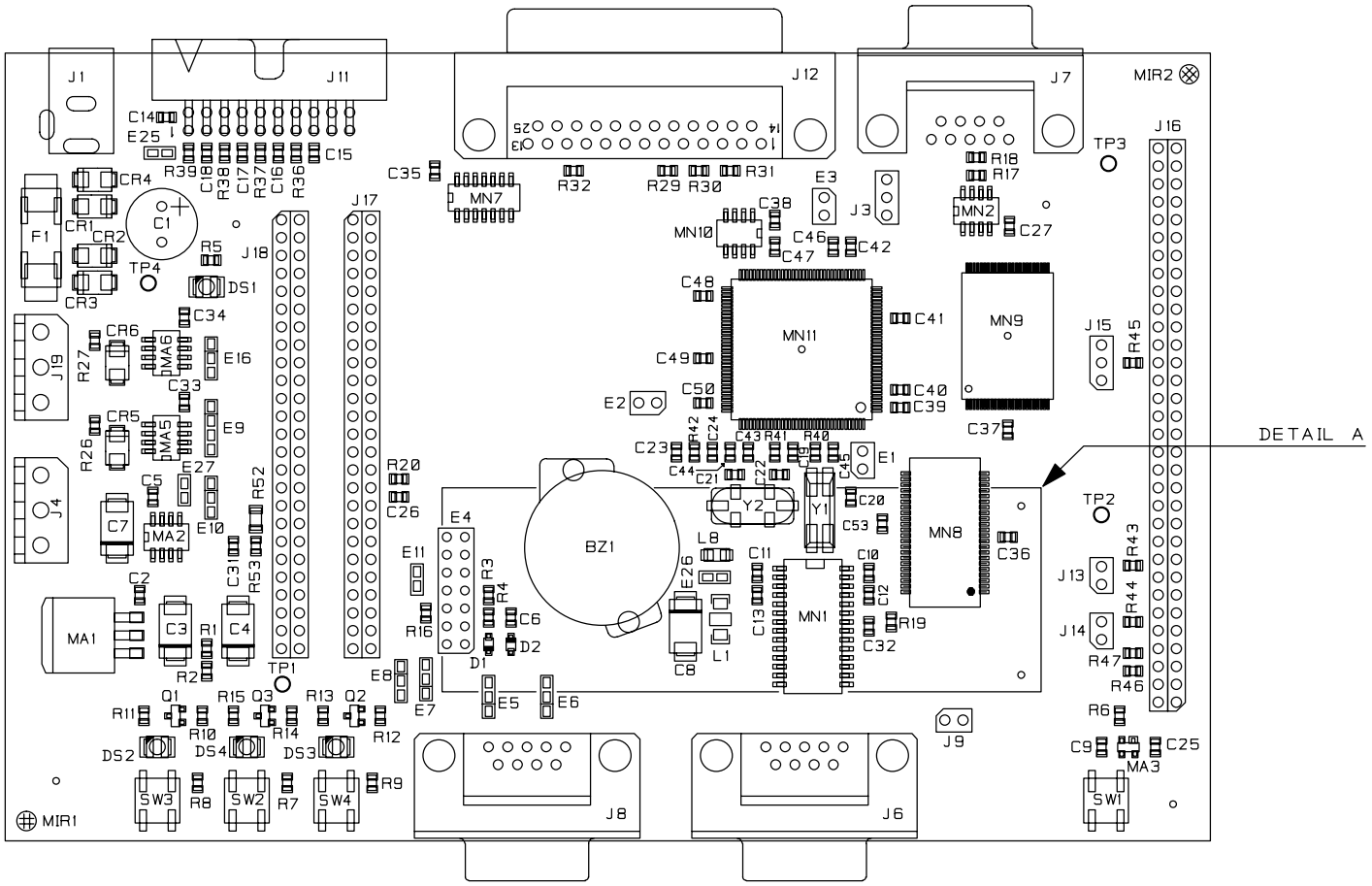
Schematics

4.1 Schematics

Table 4-1. AT91SAM7A1 Schematics

Figure Reference	Denomination
Figure 4-1	Top Level Layout
Figure 4-2	AT91SAM7A1
Figure 4-3	Power
Figure 4-4	Application Interface
Figure 4-5	CAN Interface
Figure 4-6	RS-232 and LIN Interface
Figure 4-7	ICE Interface
Figure 4-8	Memories
Figure 4-9	EBI Expansion
Figure 4-10	Expansion Connector

Figure 4-1. Components Side Assembly



DETAIL A: MONTAGE AFFICHEUR/
LCD ASSEMBLY

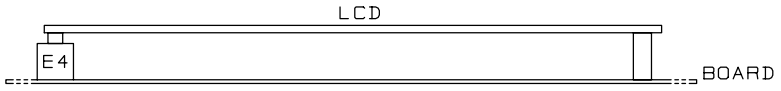


Figure 4-2. AT91SAM7A1

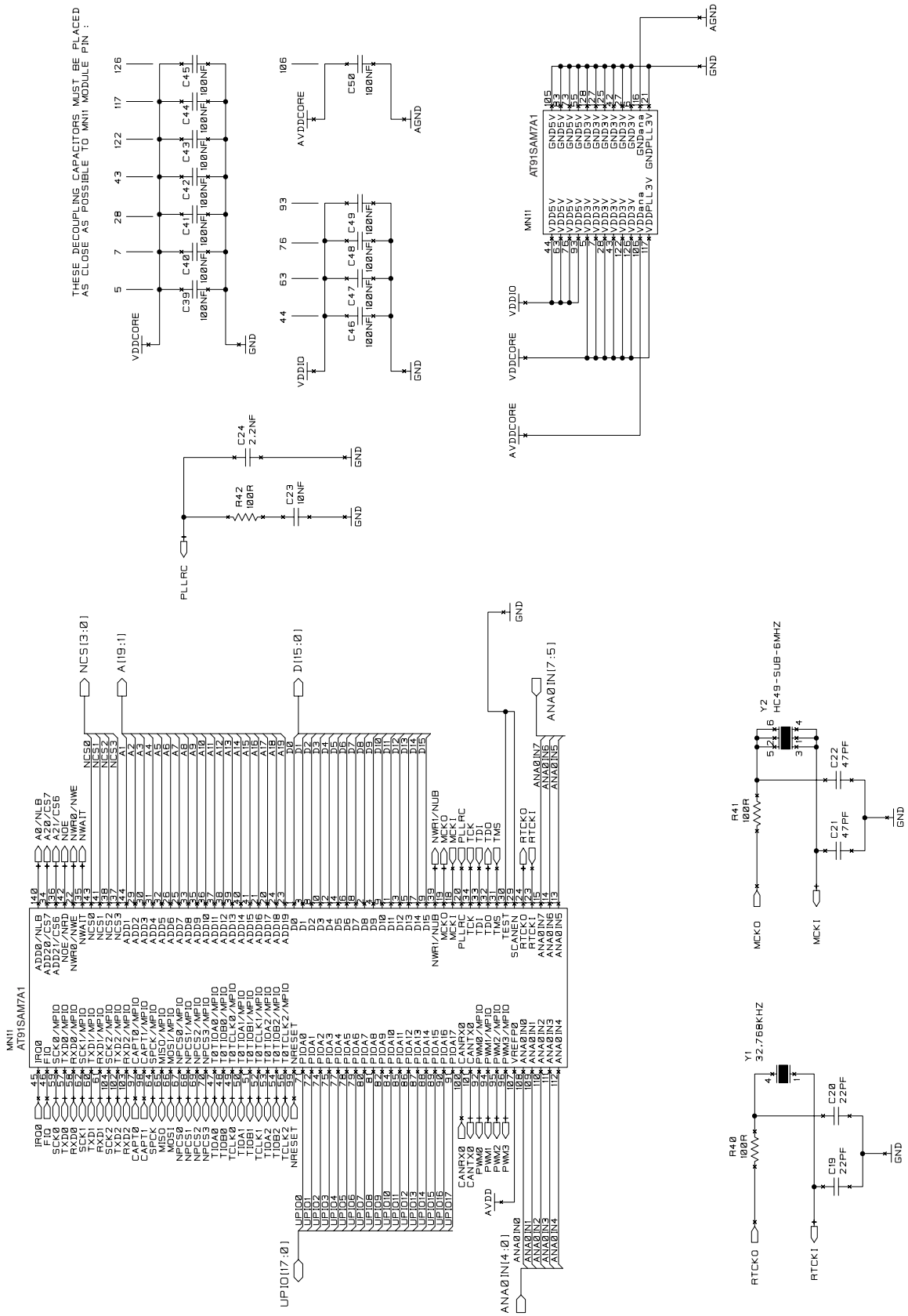


Figure 4-3. Power

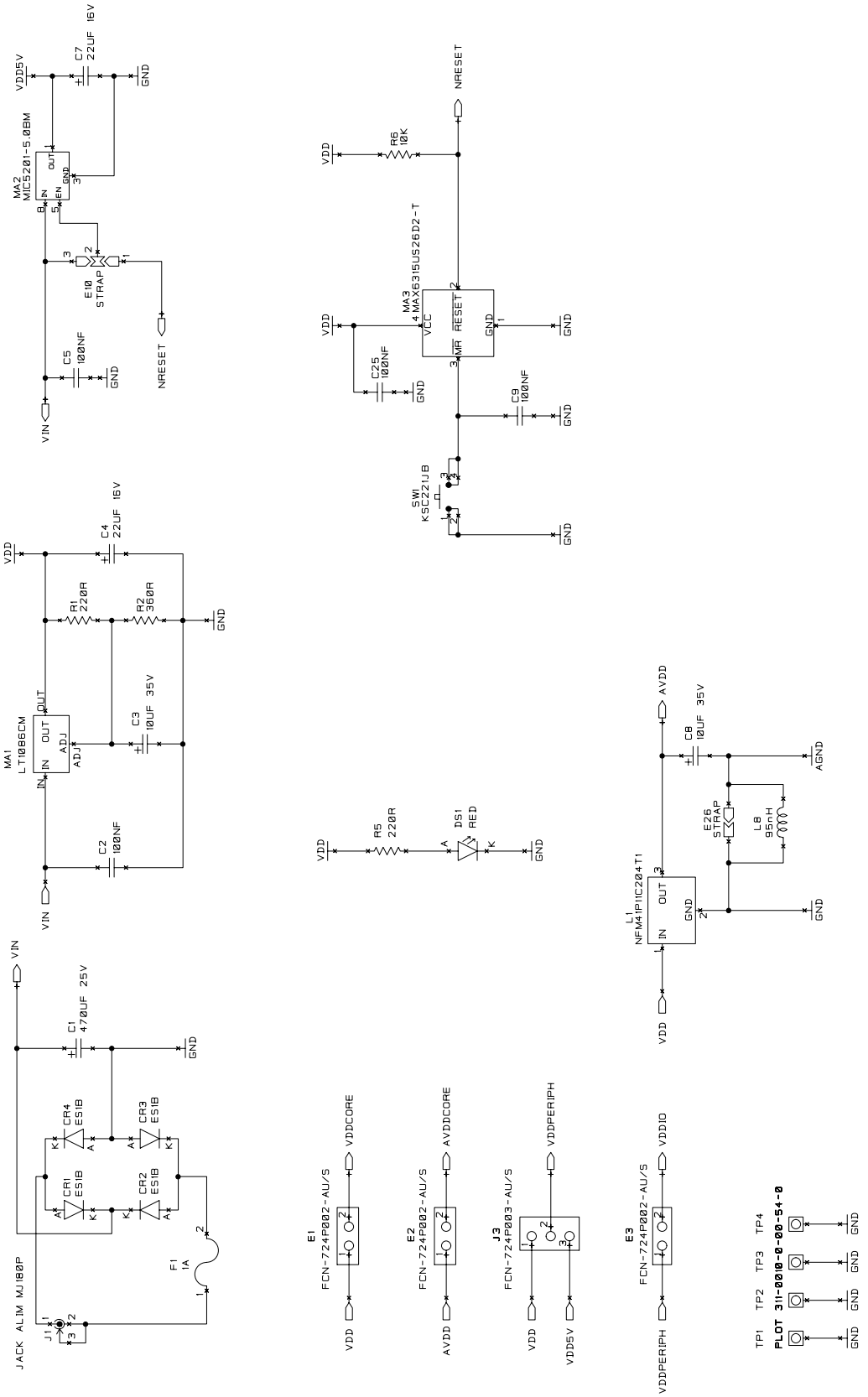


Figure 4-4. Application Interface

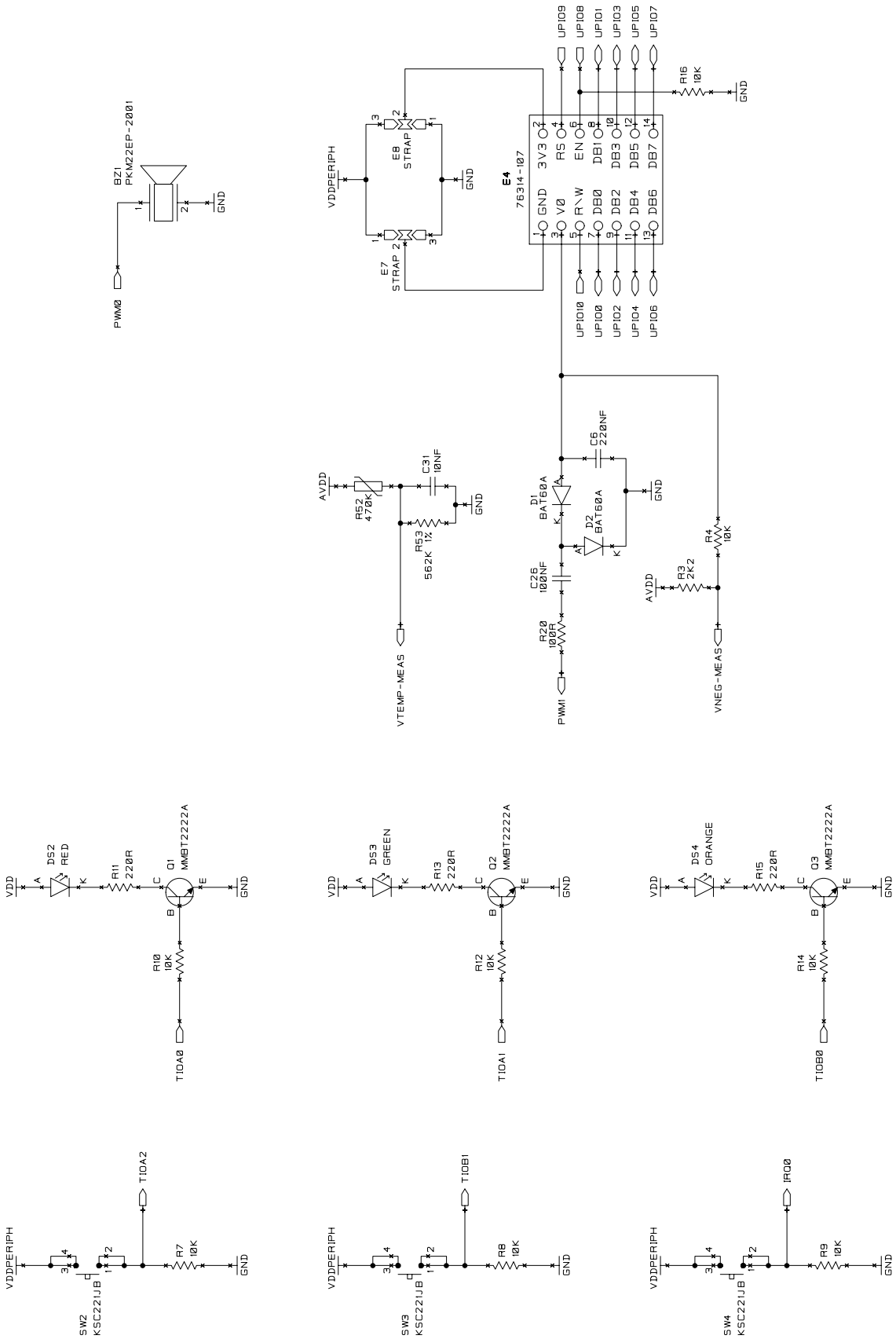


Figure 4-5. CAN Interface

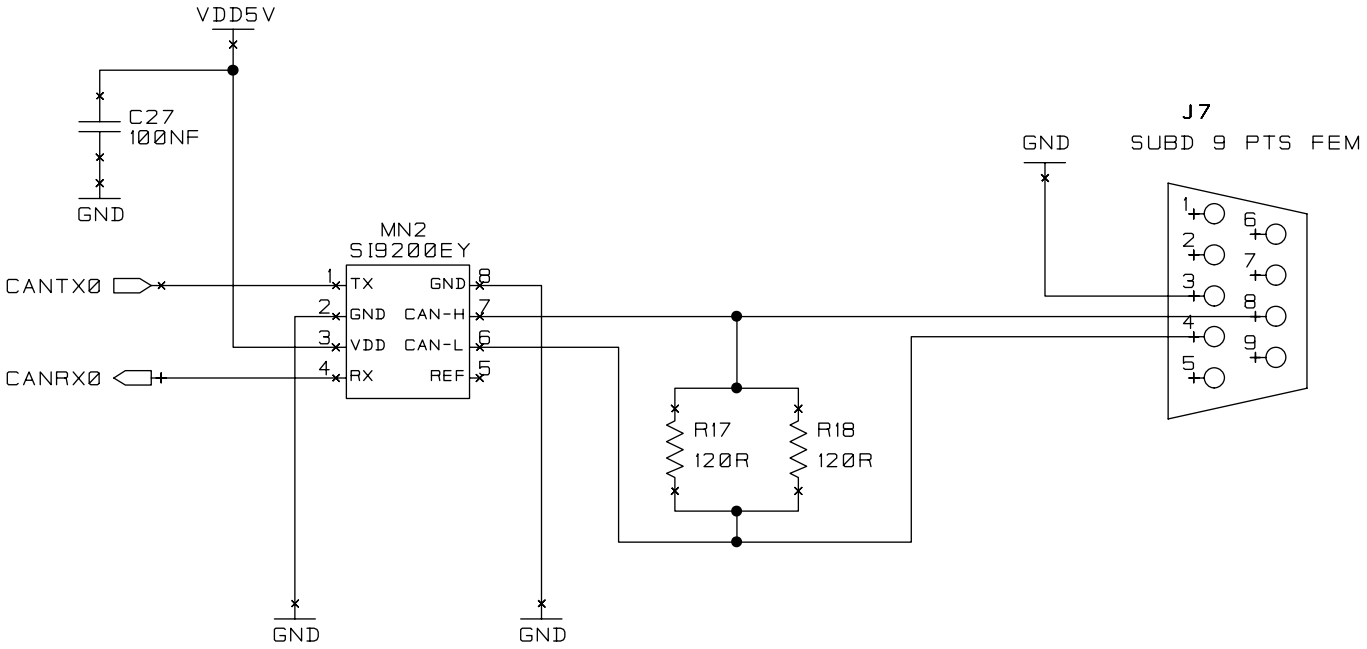


Figure 4-6. RS-232 and LIN Interfaces