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AT91SAM ARM-based Flash MCU

SAM7L128/SAM7L64

DATASHEET

Description

The AT91SAM7L128/64 are low power members of Atmel's Smart ARM Microcontroller family based on the 32-bit ARM7™ RISC processor and high-speed Flash memory.

- AT91SAM7L128 features a 128 Kbyte high-speed Flash and a total of 6 Kbytes SRAM.
- AT91SAM7L64 features a 64 Kbyte high-speed Flash and a total of 6 Kbytes SRAM.

They also embed a large set of peripherals, including a Segment LCD Controller and a complete set of system functions minimizing the number of external components.

These devices provide an ideal migration path for 8-bit microcontroller users looking for additional performance, extended memory and higher levels of system integration with strong constraints on power consumption.

Featuring innovative power reduction modes and ultra-low-power operation, the AT91SAM7L128/64 is tailored for battery operated applications such as calculators, toys, remote controls, medical devices, mobile phone accessories and wireless sensors.

The embedded Flash memory can be programmed in-system via the JTAG-ICE interface or via a parallel interface on a production programmer prior to mounting. Built-in lock bits and a security bit protect the firmware from accidental overwrite and preserve its confidentiality.

The AT91SAM7L128/64 system controller includes a reset controller capable of managing the power-on sequence of the microcontroller and the complete system. Correct device operation can be monitored by a built-in brownout detector and a watchdog running off an integrated oscillator.

By combining the ARM7TDMI processor with on-chip Flash and SRAM, and a wide range of peripheral functions, including USART, SPI, External Bus Timer Counter, RTC and Analog-to-Digital Converters on a monolithic chip, the AT91SAM7L128/64 microcontroller is a powerful device that provides a flexible, cost-effective solution to many embedded control applications.

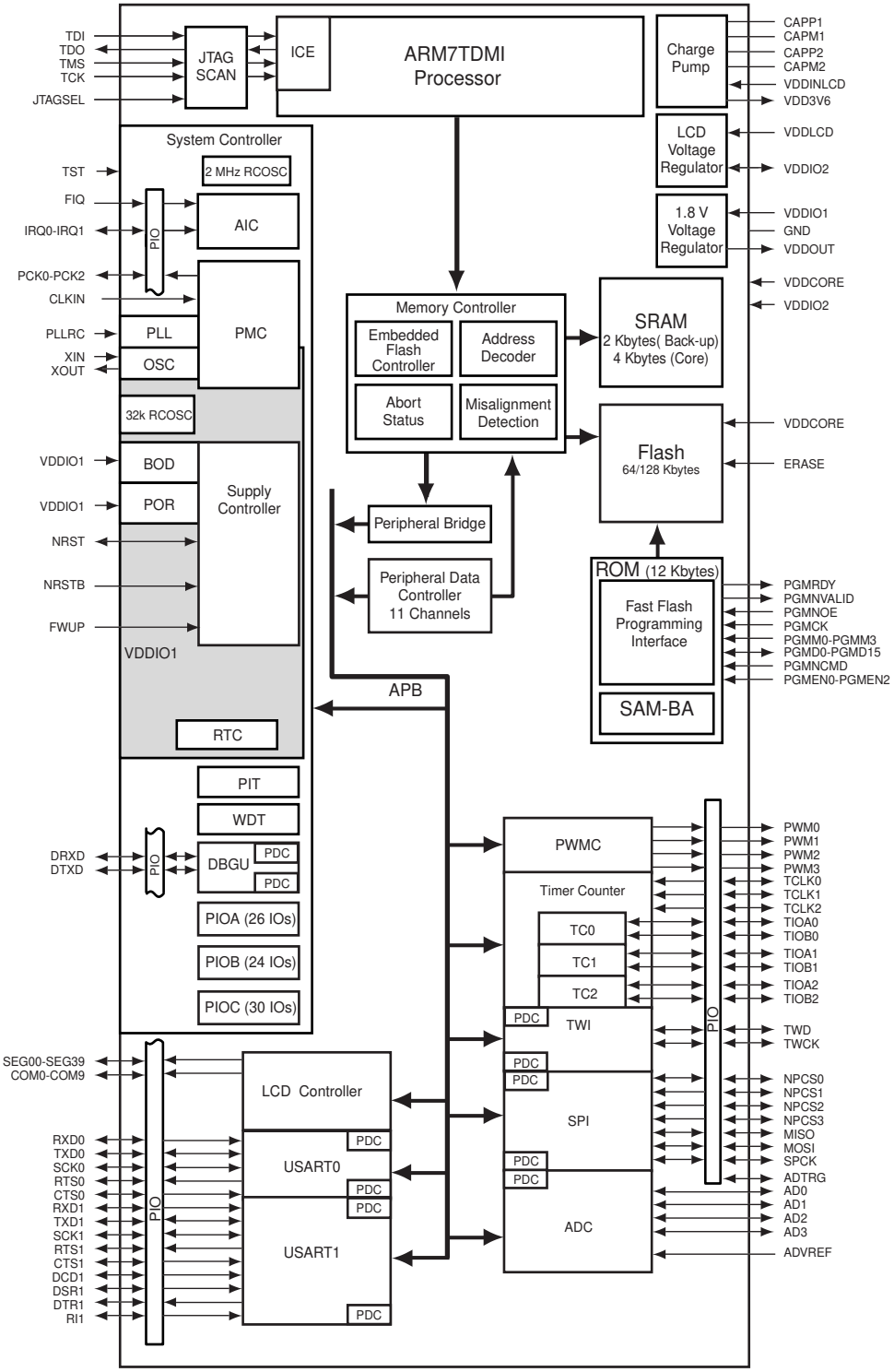
1. Features

- Incorporates the ARM7TDMI® ARM® Thumb® Processor
  - High-performance 32-bit RISC Architecture
  - High-density 16-bit Instruction Set
  - Leader in MIPS/Watt
  - EmbeddedICE™ In-circuit Emulation, Debug Communication Channel Support
- Internal High-speed Flash
  - 128 Kbytes (AT91SAM7L128), Organized in 512 Pages of 256 Bytes Single Plane
  - 64 Kbytes (AT91SAM7L64), Organized In 256 Pages of 256 Bytes Single Plane
  - Single Cycle Access at Up to 15 MHz in Worst Case Conditions
  - 128-bit Read Access
  - Page Programming Time: 4.6 ms, Including Page Auto Erase, Full Erase Time: 10 ms
  - 10,000 Write Cycles, 10-year Data Retention Capability, Sector Lock Capabilities, Flash Security Bit
  - Fast Flash Programming Interface for High Volume Production
- Internal High-speed SRAM, Single-cycle Access at Maximum Speed
  - 6 Kbytes
    - 2 Kbytes Directly on Main Supply That Can Be Used as Backup SRAM
    - 4 Kbytes in the Core
- Memory Controller (MC)
  - Enhanced Embedded Flash Controller, Abort Status and Misalignment Detection
- Enhanced Embedded Flash Controller (EEFC)
  - Interface of the Flash Block with the 32-bit Internal Bus
  - Increases Performance in ARM and Thumb Mode with 128-bit Wide Memory Interface
- Reset Controller (RSTC)
  - Based on Zero-power Power-on Reset and Fully Programmble Brownout Detector
  - Provides External Reset Signal Shaping and Reset Source Status
- Clock Generator (CKGR)
  - Low-power 32 kHz RC Oscillator, 32 kHz On-chip Oscillator, 2 MHz Fast RC Oscillator and one PLL
- Supply Controller (SUPC)
  - Minimizes Device Power Consumption
  - Manages the Different Supplies On Chip
  - Supports Multiple Wake-up Sources
- Power Management Controller (PMC)
  - Software Power Optimization Capabilities, Including Active and Four Low Power Modes:
    - Idle Mode: No Processor Clock
    - Wait Mode: No Processor Clock, Voltage Regulator Output at Minimum
    - Backup Mode: Voltage Regulator and Processor Switched Off
    - Off (Power Down) Mode: Entire Chip Shut Down Except for Force Wake Up Pin (FWUP) that Re-activates the Device. 100 nA Current Consumption.
- In Active Mode, Dynamic Power Consumption <30 mA at 36 MHz
  - Three Programmable External Clock Signals
  - Handles Fast Start Up
- Advanced Interrupt Controller (AIC)
  - Individually Maskable, Eight-level Priority, Vectored Interrupt Sources
  - Two External Interrupt Sources and One Fast Interrupt Source, Spurious Interrupt Protected
- Debug Unit (DBGU)
  - Two-wire UART and Support for Debug Communication Channel interrupt, Programmable ICE Access Prevention
- Periodic Interval Timer (PIT)
  - 20-bit Programmable Counter plus 12-bit Interval Counter

- Windowed Watchdog (WDT)
  - 12-bit Key-protected Programmable Counter
  - Provides Reset or Interrupt Signals to the System
  - Counter may be Stopped While the Processor is in Debug State or in Idle Mode
- Real-time Clock (RTC)
  - Two Hundred Year Calendar with Alarm
  - Runs Off the Internal RC or Crystal Oscillator
- Three Parallel Input/Output Controllers (PIOA, PIOB, PIOC)
  - Eighty Programmable I/O Lines Multiplexed with up to Two Peripheral I/Os
  - Input Change Interrupt Capability on Each I/O Line
  - Individually Programmable Open-drain, Pull-up resistor and Synchronous Output
- Eleven Peripheral DMA Controller (PDC) Channels
- One Segment LCD Controller
  - Display Capacity of Forty Segments and Ten Common Terminals
  - Software Selectable LCD Output Voltage (Contrast)
- Two Universal Synchronous/Asynchronous Receiver Transmitters (USART)
  - Individual Baud Rate Generator, IrDA® Infrared Modulation/Demodulation
  - Support for ISO7816 T0/T1 Smart Card, Hardware Handshaking, RS485 Support
  - Manchester Encoder/Decoder
  - Full Modem Line Support on USART1
- One Master/Slave Serial Peripheral Interface (SPI)
  - 8- to 16-bit Programmable Data Length, Four External Peripheral Chip Selects
- One Three-channel 16-bit Timer/Counter (TC)
  - Three External Clock Inputs, Two Multi-purpose I/O Pins per Channel
  - Double PWM Generation, Capture/Waveform Mode, Up/Down Capability
- One Four-channel 16-bit PWM Controller (PWMC)
- One Two-wire Interface (TWI)
  - Master, Multi-Master and Slave Mode Support, All Atmel® Two-wire EEPROMs and I^2C compatible Devices Supported
  - General Call Supported in Slave Mode
- One 4-channel 10-bit Analog-to-Digital Converter, Four Channels Multiplexed with Digital I/Os
- SAM-BA® Boot Assistant
  - Default Boot Program
  - Interface with SAM-BA Graphic User Interface
  - In Application Programming Function (IAP)
- IEEE® 1149.1 JTAG Boundary Scan on All Digital Pins
- Four High-current Drive I/O lines, Up to 4 mA Each
- Power Supplies
  - Embedded 1.8V Regulator, Drawing up to 60 mA for the Core with Programmable Output Voltage
  - Single Supply 1.8V - 3.6V
- Fully Static Operation: Up to 36 MHz at 85· C, Worst Case Conditions
- Available in a 128-lead LQFP Green and a 144-ball LFBGA Green Package

2. Block Diagram

Figure 2-1. AT91SAM7L128/64 Block Diagram



3. Signal Description

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
Power					
VDDIO1	I/O Lines (PIOC) and Voltage Regulator Power Supply	Power			From 1.80V to 3.6V
VDDOUT	Voltage Regulator Output	Power			
VDDCORE	Core Power Supply	Power			Connected externally to VDDOUT
VDDINLCD	Charge Pump Power Supply	Power			From 1.80V to 3.6V
VDD3V6	Charge Pump Output	Power			
VDDLCD	LCD Voltage Regulator Power Supply	Power			
VDDIO2	LCD Voltage Regulator Output and LCD I/O Lines Power Supply (PIOA and PIOB)	Power			1.80V to 3.6V
CAPP1	Charge pump capacitor 1	Power			Capacitor needed between CAPP1 and CAPM1.
CAPM1	Charge pump capacitor 1	Power			
CAPP2	Charge pump capacitor 2	Power			Capacitor needed between CAPP2 and CAPM2.
CAPM2	Charge pump capacitor 2	Power			
FWUP	Force Wake-up	Input	Low	VDDIO1	Needs external Pull-up.
WKUP0-15	Wake-up inputs used in Backup mode and Fast Start-up inputs in Wait mode	Input		VDDIO1	
GND	Ground	Ground			
Clocks, Oscillators and PLLs					
XIN	32 kHz Oscillator Input	Input		VDDIO1	
XOUT	32 kHz Oscillator Output	Output		VDDIO1	
CLKIN	Main Clock input	Input		VDDIO1	Should be tied low when not used.
PCK0 - PCK2	Programmable Clock Output	Output			
PLLRC	PLL Filter	Input		VDDCORE	
PLLRCGND	PLL RC Filter Ground	Power			Must not be connected to external Ground.
ICE and JTAG					
TCK	Test Clock	Input		VDDIO1	No internal pull-up resistor
TDI	Test Data In	Input		VDDIO1	No internal pull-up resistor
TDO	Test Data Out	Output		VDDIO1	
TMS	Test Mode Select	Input		VDDIO1	No internal pull-up resistor
JTAGSEL	JTAG Selection	Input		VDDIO1	Internal Pull-down resistor
Flash Memory					
ERASE	Flash and NVM Configuration Bits Erase Command	Input	High	VDDIO1	Internal Pull-down (15 kΩ) resistor

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
Reset/Test					
NRST	Microcontroller Reset	I/O	Low	VDDIO1	Internal Pull-up (100 kΩ) resistor
TST	Test Mode Select	Input	High	VDDIO1	Internal Pull-down (15 kΩ) resistor
NRSTB	Asynchronous Master Reset	Input	Low	VDDIO1	Internal Pull-up (15 kΩ) resistor
Debug Unit					
DRXD	Debug Receive Data	Input			
DTXD	Debug Transmit Data	Output			
AIC					
IRQ0 - IRQ1	External Interrupt Inputs	Input			
FIQ	Fast Interrupt Input	Input			
PIO					
PA0 - PA25	Parallel IO Controller A	I/O		VDDIO2	Pulled-up input at reset
PB0 - PB23	Parallel IO Controller B	I/O		VDDIO2	Pulled-up input at reset
PC0 - PC29	Parallel IO Controller C	I/O		VDDIO1	Pulled-up input at reset
USART					
SCK0 - SCK1	Serial Clock	I/O			
TXD0 - TXD1	Transmit Data	I/O			
RXD0 - RXD1	Receive Data	Input			
RTS0 - RTS1	Request To Send	Output			
CTS0 - CTS1	Clear To Send	Input			
DCD1	Data Carrier Detect	Input			
DTR1	Data Terminal Ready	Output			
DSR1	Data Set Ready	Input			
RI1	Ring Indicator	Input			
Timer/Counter					
TCLK0 - TCLK2	External Clock Inputs	Input			
TIOA0 - TIOA2	Timer Counter I/O Line A	I/O			
TIOB0 - TIOB2	Timer Counter I/O Line B	I/O			
PWM Controller					
PWM0 - PWM3	PWM Channels	Output			
Serial Peripheral Interface					
MISO	Master In Slave Out	I/O			
MOSI	Master Out Slave In	I/O			
SPCK	SPI Serial Clock	I/O			
NPCS0	SPI Peripheral Chip Select 0	I/O	Low		
NPCS1-NPCS3	SPI Peripheral Chip Select 1 to 3	Output	Low		

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
Two-Wire Interface					
TWD	Two-wire Serial Data	I/O			
TWCK	Two-wire Serial Clock	I/O			
Analog-to-Digital Converter					
AD0-AD3	Analog Inputs	Input		VDDCORE	
ADTRG	ADC Trigger	Input			
ADVREF	ADC Reference	Analog		VDDCORE	
Fast Flash Programming Interface					
PGMEN0-PGMEN2	Programming Enabling	Input		VDDIO1	
PGMM0-PGMM3	Programming Mode	Input		VDDIO1	
PGMD0-PGMD15	Programming Data	I/O		VDDIO1	
PGMRDY	Programming Ready	Output	High	VDDIO1	
PGMNVALID	Data Direction	Output	Low	VDDIO1	
PGMNOE	Programming Read	Input	Low	VDDIO1	
PGMCK	Programming Clock	Input		VDDIO1	
PGMNCMD	Programming Command	Input	Low	VDDIO1	
Segmented LCD Controller					
COM[9:0]	Common Terminals	Output		VDDIO2	
SEG[39:0]	Segment Terminals	Output		VDDIO2	

4. Package and Pinout

The AT91SAM7L128/64 is available in:

- 20 x 14 mm 128-lead LQFP package with a 0.5 mm lead-pitch
- 10 x 10 mm 144-ball LFBGA package with a 0.8 mm pitch.

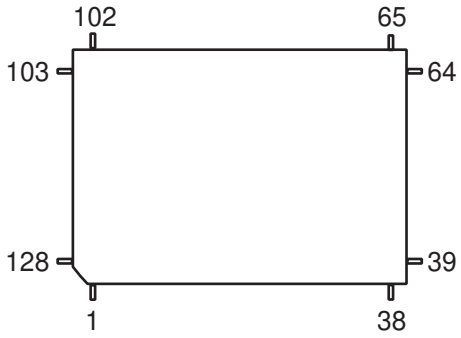
The part is also available in die delivery.

4.1 128-lead LQFP Package Outline

Figure 4-1 shows the orientation of the 128-lead LQFP package.

A detailed mechanical description is given in the Mechanical Characteristics section of the product datasheet.

Figure 4-1. 128-lead LQFP Package Outline (Top View)



4.2 128-lead LQFP Package Pinout

Table 4-1. Pinout for 128-lead LQFP Package

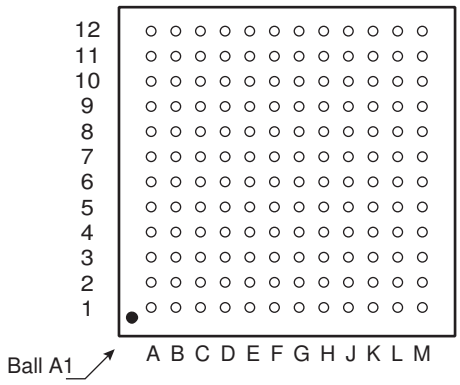
1	TST	33	VDDLCD	65	PB21	97	PC10/PGMM3
2	VDDCORE	34	VDD3V6	66	PB22	98	PC11/PGMD0
3	PA0	35	CAPM2	67	PB23	99	PC12/PGMD1
4	PA1	36	CAPP2	68	GND	100	VDDCORE
5	PA2	37	CAPM1	69	ADVREF	101	PC13/PGMD2
6	PA3	38	CAPP1	70	AD3	102	PC14/PGMD3
7	PA4	39	VDDINLCD	71	AD2	103	PC15/PGMD4
8	PA5	40	GND	72	AD1	104	PC16/PGMD5
9	PA6	41	PB0	73	AD0	105	PC17/PGMD6
10	PA7	42	PB1	74	VDDOUT	106	PC18/PGMD7
11	PA8	43	PB2	75	VDDIO1	107	PC19/PGMD8
12	PA9	44	PB3	76	GND	108	PC20/PGMD9
13	PA10	45	PB4	77	PC28	109	PC21/PGMD10
14	GND	46	PB5	78	PC29	110	PC22/PGMD11
15	VDDIO2	47	PB6	79	NRST	111	PC23/PGMD12
16	PA11	48	PB7	80	ERASE	112	PC24/PGMD13
17	PA12	49	PB8	81	TCK	113	PC25/PGMD14
18	PA13	50	PB9	82	TMS	114	PC26/PGMD15
19	PA14	51	PB10	83	JTAGSEL	115	PC27
20	PA15	52	PB11	84	VDDCORE	116	TDI
21	PA16	53	PB12	85	VDDIO1	117	TDO
22	PA17	54	PB13	86	GND	118	FWUP
23	PA18	55	VDDIO2	87	PC0/PGMEN0	119	VDDIO1
24	PA19	56	GND	88	PC1/PGMEN1	120	GND
25	PA20	57	PB14	89	PC2/PGMEN2	121	PLLRC
26	PA21	58	PB15	90	PC3/PGMNCMD	122	PLLRCGND
27	PA22	59	PB16	91	PC4/PGMRDY	123	GND
28	VDDCORE	60	PB17	92	PC5/PGMNOE	124	VDDCORE
29	PA23	61	PB18	93	PC6/PGMNVALID	125	CLKIN
30	PA24	62	VDDCORE	94	PC7/PGMM0	126	NRSTB
31	PA25	63	PB19	95	PC8/PGMM1	127	XIN/PGMCK
32	VDDIO2	64	PB20	96	PC9/PGMM2	128	XOUT

4.3 144-ball LFBGA Package Outline

Figure 4-2 shows the orientation of the 144-ball LFBGA package.

A detailed mechanical description is given in the Mechanical Characteristics section of the product datasheet.

Figure 4-2. 144-ball LFBGA Package Outline (Top View)



4.4 144-ball LFBGA Pinout

Table 4-2. SAM7L128/64 Pinout for 144-ball LFBGA Package

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	XOUT	D1	PA6	G1	VDD3V6	K1	CAPM1
A2	XIN/PGCMK	D2	PA5	G2	PA17	K2	VDDIO2
A3	VDDCORE	D3	PA7	G3	PA16	K3	VDDIO2
A4	GND	D4	NC	G4	PA15	K4	PA25
A5	PLLRCGND	D5	PC26/PGMD15	G5	GND	K5	PB3
A6	PLLRC	D6	PC25/PGMD14	G6	GND	K6	PB10
A7	PC24/PGMD13	D7	PC21/PGMD10	G7	GND	K7	PB13
A8	PC23//PGMD12	D8	PC18/PGMD7	G8	VDDIO1	K8	PB15
A9	PC17/PGMD6	D9	PC6/PGMNVALID	G9	NRST	K9	PB20
A10	NC	D10	PC7/PGMM0	G10	TMS	K10	VDDCORE
A11	PC14	D11	PC4/PGMRDY	G11	ERASE	K11	VDDCORE
A12	PC12	D12	PC3/PGMNCMD	G12	VDDOUT	K12	AD2
B1	PA1	E1	VDDIO2	H1	CAPM2	L1	CAPP1
B2	PA0	E2	PA10	H2	PA22	L2	VDDIO2
B3	NRSTB	E3	PA9	H3	PA19	L3	VDDIO2
B4	TST	E4	PA11	H4	PA18	L4	PB4
B5	TDO	E5	PA8	H5	GND	L5	PB5
B6	PC27	E6	VDDIO1	H6	GND	L6	PB11
B7	GND	E7	VDDIO1	H7	GND	L7	PB12
B8	NC	E8	VDDIO1	H8	VDDCORE	L8	PB17
B9	PC20/PGMD9	E9	PC5/PGMNOE	H9	PC29	L9	PB19
B10	PC15/PGMD4	E10	PC0/PGMEN0	H10	VDDCORE	L10	PB22
B11	PC13/PGMD2	E11	PC2/PGMEN2	H11	PC28	L11	PB23
B12	PC11/PGMD0	E12	VDDCORE	H12	AD0	L12	AD3
C1	PA3	F1	VDDLCD	J1	CAPP2	M1	VDDINLCD
C2	PA4	F2	PA13	J2	PA23	M2	PB0
C3	PA2	F3	PA14	J3	PA24	M3	PB1
C4	CLKIN	F4	PA12	J4	PA21	M4	PB2
C5	FWUP	F5	GND	J5	PA20	M5	PB6
C6	TDI	F6	GND	J6	PB8	M6	PB7
C7	PC22/PGMD11	F7	GND	J7	PB9	M7	VDDIO2
C8	PC19/PGMD8	F8	VDDIO1	J8	PB14	M8	PB16
C9	PC16/PGMD5	F9	TCK	J9	VDDCORE	M9	PB18
C10	PC9/PGMM2	F10	JTAGSEL	J10	VDDCORE	M10	PB21
C11	PC10/PGMM3	F11	PC1/PGMEN1	J11	VDDCORE	M11	GND
C12	PC8/PGMM1	F12	VDDIO1	J12	AD1	M12	ADVREF

5. Power Considerations

5.1 Power Supplies

The AT91SAM7L128/64 has six types of power supply pins and integrates a voltage regulator, allowing the device to be supplied with only one voltage. The six power supply pin types are:

- VDDOUT pin. It is the output of the voltage regulator. Output voltage can be programmed from 1.55V to 1.80V by steps of 100 mV.
- VDDIO1 pin. It powers the voltage regulator input and all the PIOC IO lines (1.8V-3.6V). VDDIO1 voltage must be above 2.2V to allow the chip to start-up (POR threshold).
- VDDIO2 pin. It powers the PIOA and PIOB I/O lines (1.8V-3.6V). It is also the output of the LCD voltage regulator. The output voltage can be programmed from 2.4V to 3.4V with 16 steps.
- VDDCORE pin. It powers the logic of the device, the PLL, the 2 MHz Fast RC oscillator, the ADC and the Flash memory. It must be connected to the VDDOUT pin with a decoupling capacitor.
- VDDINLCD pin. It powers the charge pump which can be used as LCD Regulator power supply. Voltage ranges from 1.8V to 3.6V.

No separate ground pins are provided for the different power supplies. Only GND pins are provided and should be connected as shortly as possible to the system ground plane.

5.2 Low Power Modes

The various low power modes of the AT91SAM7L128/64 are described below.

5.2.1 Off (Power Down) Mode

In off (power down) mode, the entire chip is shut down. Only a low level on the FWUP pin can wake up the AT91SAM7L128/64 (by a push-button for example). Internally, except for the FWUP pin through VDDIO1, none of the chip is supplied.

Once the internal main power switch has been activated by FWUP, the 32 kHz RC oscillator and the Supply Controller are supplied, then the core and peripherals are reset and the AT91SAM7L128/64 enters in active mode. Refer to the System Controller Block Diagram, Figure 9-1 on page 29.

At first power-up, if FWUP is tied high, the device enters off mode. The PIOA and PIOB pins' states are undefined. PIOC and NRST pins are initialized as high impedance inputs.

Once the device enters active mode, the core and the parallel input/output controller are reset. Then, if the chip enters off mode, PIOA and PIOB pins are configured as inputs with pull-ups and PIOC pins as high impedance inputs.

Current consumption in this mode is typically 100 nA.

5.2.2 Backup Mode

In backup mode, the supply controller, the zero-power power-on reset and the 32 kHz oscillator (software selectable internal RC or external crystal) remain running. The voltage regulator and the core are switched off.

Prior to entering this mode, the RTC, the backup SRAM, the brownout detector, the charge pump, the LCD voltage regulator and the LCD controller can be set on or off separately.

Table 5-1 on page 13 shows an example of backup mode with backup SRAM and RTC running.

When entering this mode, all PIO pins keep their previous states, they are reinitialized as inputs with pull-ups at wake-up.

The AT91SAM7L128/64 can be awakened from this mode through the FWUP pin, an event on WUP0-15 pins, or an RTC alarm or brownout event.

Current consumption is 3.5 µA typical without the LCD controller running.

5.2.3 Wait Mode

In wait mode, the voltage regulator must be set in deep mode. Voltage regulator output voltage should be set at a minimum voltage to decrease leakage in the digital core. No clock is running in the core. From this mode, a fast start-up is available (refer to Section 5.4 "Fast Start-Up").

In this mode, all PIO pins keep their previous states.

5.2.4 Idle Mode

The processor is in idle mode which means that the processor has no clock but the Master clock (MCK) remains running. The processor can also be wakened by an IRQ or FIQ.

5.2.5 Active Mode

The total dynamic power consumption is less than 30 mA at full speed (36 MHz) when running out of the Flash. The power management controller can be used to adapt the frequency and the regulator output voltage can be adjusted to optimize power consumption.

5.2.6 Low Power Mode Summary Table

The modes detailed above are the main modes. In off mode, no options are available but once the shutdown controller is set to on, each part can be set to on, or off, separately and more modes can be active. The table below shows a summary of the configurations of the low power modes.

Table 5-1. Low Power Mode Configuration Summary

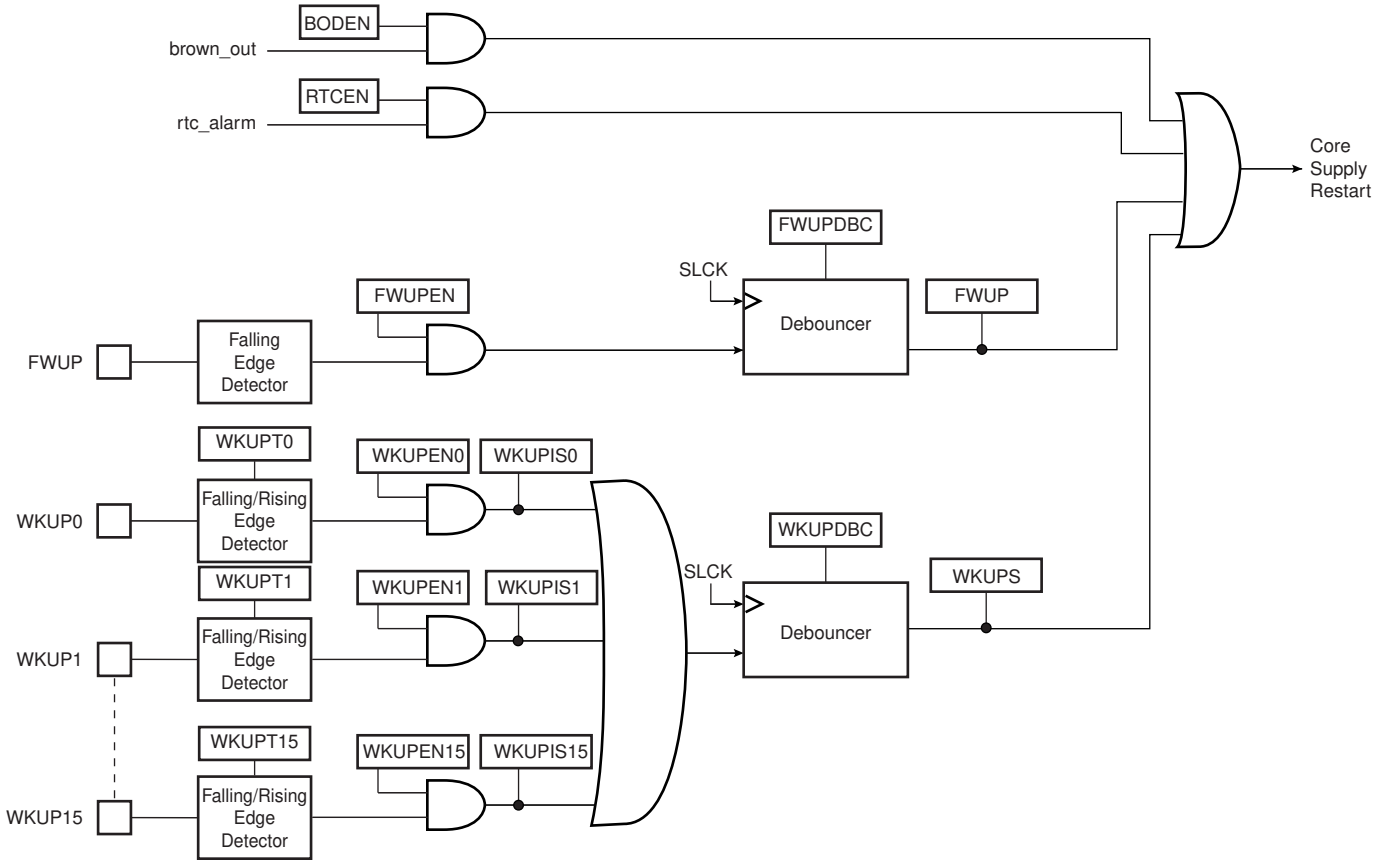
Mode	FWUP	SUPC, 32 kHz Oscillator, POR	RTC	Backup SRAM	Regulator (Deep Mode)	Core	Potential Wake-up Sources	Consumption[2][3]	Wake-up Time[1]
Off Mode	X						FWUP pin	100 nA typ	< 5 ms
Backup Mode (with SRAM and RTC)	X	X	X	X			FWUP pin WUP0-15 pins BOD alarm RTC alarm	3.5 µA typ	< 0.5 ms
Wait Mode (with SRAM and RTC)	X	X	X	X	X	X	Fast start-up through WUP0-15 pins	9 µA typ	< 2 µs (in case of fast start-up)
Idle Mode	X	X		X	X	X	IRQs FIQ	[4]	[4]

Notes:
1. When considering wake-up time, the time required to start the PLL is not taken into account. Once started, the AT91SAM7128/L64 works with the 2 MHz Fast RC oscillator. The user has to add the PLL start-up time if it is needed in the system. The wake-up time is defined as the time taken for wake up until the first instruction is fetched.
2. The external LCD current consumption and the external loads on PIOs are not taken into account in the calculation.
3. BOD current consumption is not included.
4. Depends on MCK frequency.

5.3 Wake-up Sources

The wake-up events allow the device to exit from backup mode. When a wake-up event is detected, the supply controller performs a sequence which automatically reenables the voltage regulator and the backup SRAM power supply, if it is not already enabled.

Figure 5-1. Wake Up Sources

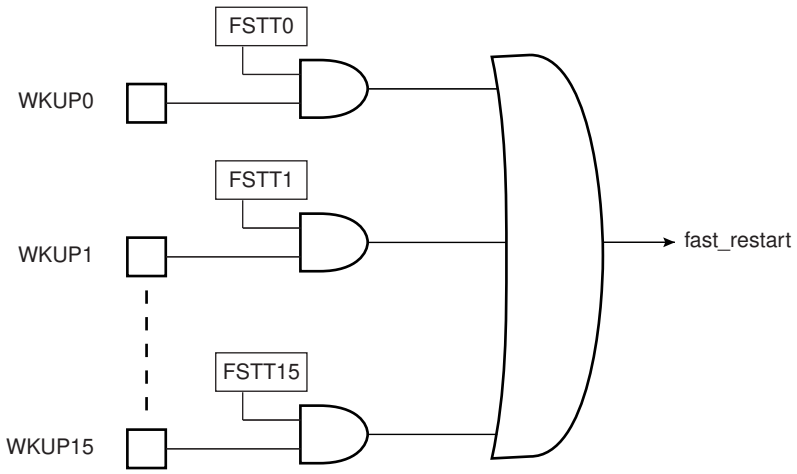


5.4 Fast Start-Up

The SAM7L128/64 allows the processor to restart in a few microseconds while the processor is in wait mode. A fast start up can occur upon detection of a low level on one of the 16 wake-up inputs.

The fast restart circuitry, as shown in Figure 5-2, is fully asynchronous and provides a fast start-up signal to the power management controller. As soon as the fast start-up signal is asserted, the PMC automatically restarts the embedded 2 MHz Fast RC oscillator, switches the master clock on this 2 MHz clock and reenables the processor clock, if it is disabled.

Figure 5-2. Fast Start-Up Circuitry



5.5 Voltage Regulator

The AT91SAM7L128/64 embeds a voltage regulator that is managed by the supply controller. This internal regulator is only intended to supply the internal core of AT91SAM7L128/64. It features three different operating modes:

- In normal mode, the voltage regulator consumes less than 30 µA static current and draws 60 mA of output current.
- In deep mode, the current consumption of the voltage regulator is less than 8.5 µA. It can draw up to 1 mA of output current. The default output voltage is 1.80V and the start-up time to reach normal mode is inferior to 400 µs.
- In shutdown mode, the voltage regulator consumes less than 1 µA while its output is driven internally to GND. The default output voltage is 1.80V and the start-up time to reach normal mode is inferior to 400 µs.

Furthermore, in normal and deep modes, the regulator output voltage can be programmed by software with 4 different steps within the range of 1.55V to 1.80V. The default output voltage is 1.80V in both normal and deep modes. The voltage regulator can regulate 1.80V output voltage as long as the input voltage is above 1.95V. Below 1.95V input voltage, the output voltage remains above 1.65V.

Output voltage adjusting ability allows current consumption reduction on VDDCORE and also enables programming a lower voltage when the input voltage is lower than 1.95V.

At 1.55V, the Flash is still functional but with slower read access time. Programming or erasing the Flash is not possible under these conditions. MCK maximum frequency is 25 MHz with VDDCORE at 1.55V (1.45V minimum).

The regulator has an indicator that can be used by the software to show that the output voltage has the correct value (output voltage has reached at least 80% of the typical voltage). This flag is used by the supply controller. This feature is only possible when the voltage regulator is in normal mode at 1.80V.

Adequate output supply decoupling is mandatory for VDDOUT in order to reduce ripple and avoid oscillations. One external 2.2 µF (or 3.3 µF) X7R capacitor must be connected between VDDOUT and GND.

Adequate input supply decoupling is mandatory for VDDIO1 in order to improve startup stability and reduce source voltage drop. The input decoupling capacitor should be placed close to the chip. For example, two capacitors can be used in parallel, 100 nF NPO and 4.7 µF X7R.

5.6 LCD Power Supply

The AT91SAM7L128/64 embeds an on-chip LCD power supply comprising a regulated charge pump and an adjustable voltage regulator.

The regulated charge pump output delivers 3.6V as long as its input is supplied between 1.8V and 3.6V. The regulated charge pump only requires two external flying capacitors and one external tank capacitor to operate.

Adequate input supply decoupling is mandatory for VDDINLCD in order to improve startup stability and reduce source voltage drop. The input decoupling capacitor should be placed close to the chip.

Current consumption of the charge pump and LCD bias when active is 350 µA (max case).

The regulated charge pump can be used to supply the LCD voltage regulator or as a 3.6V voltage reference delivering up to 4 mA.

The LCD voltage regulator output voltage is software selectable from 2.4V to 3.4V with 16 levels. Its input should be supplied in the range of 2.5 to 3.6V. The LCD voltage regulator can be supplied by the regulated charge pump output or by an external supply.

When the LCD voltage regulator is not used, its output must be connected to an external source in order to supply the PIOA and PIOB I/O lines.

Figure 5-3 below shows the typical schematics needed:

Figure 5-3. The Charge Pump Supplies the LCD Regulator

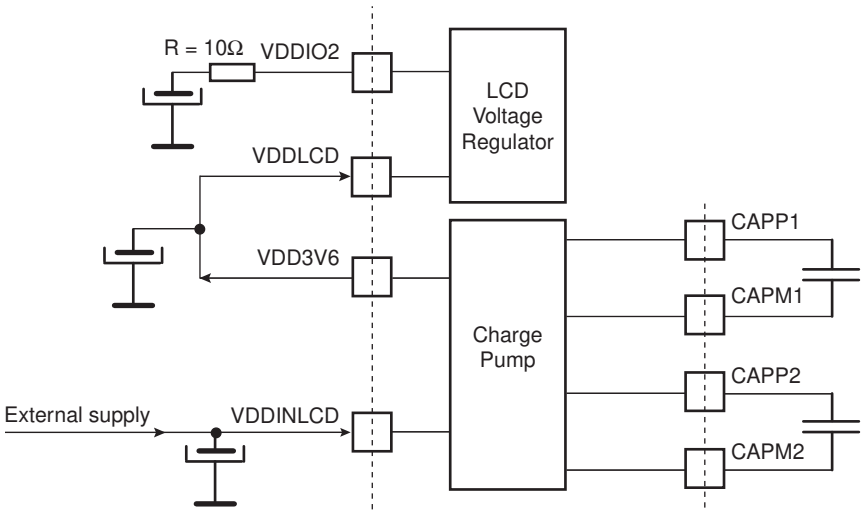
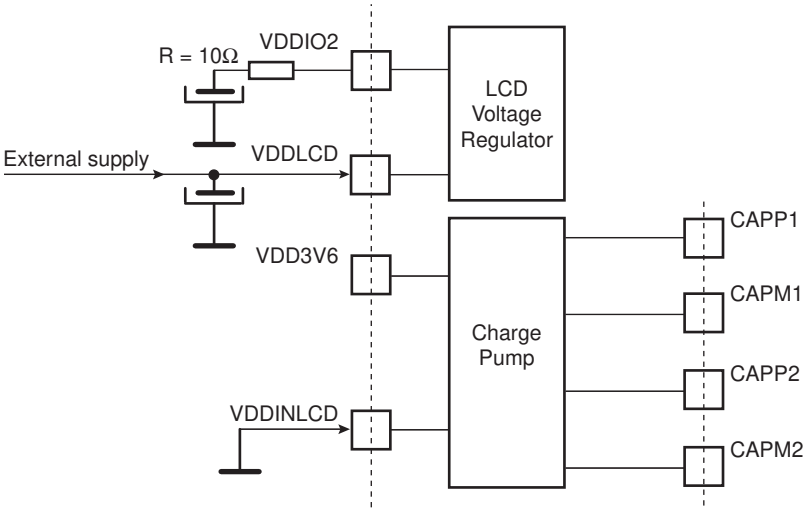
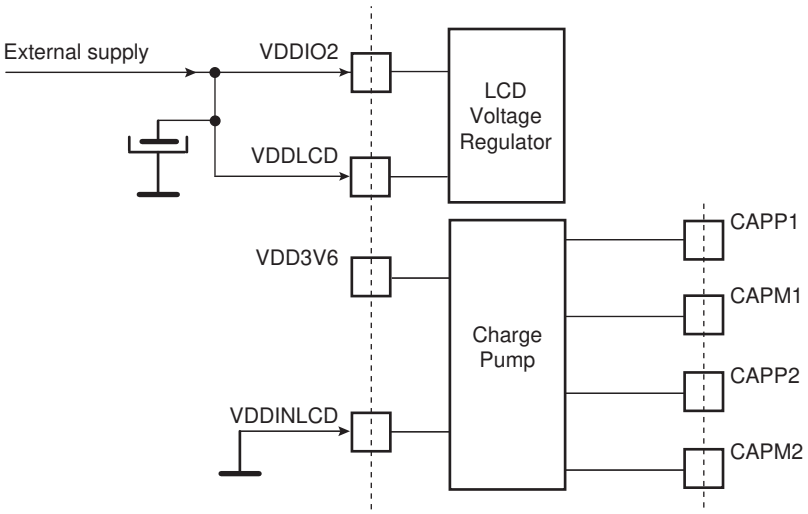


Figure 5-4. The LCD Regulator is Externally Supplied



If the charge pump is not needed, the user can apply an external voltage. See Figure 5-5 below:

Figure 5-5. The Charge Pump and the LCD Regulator are Not Used

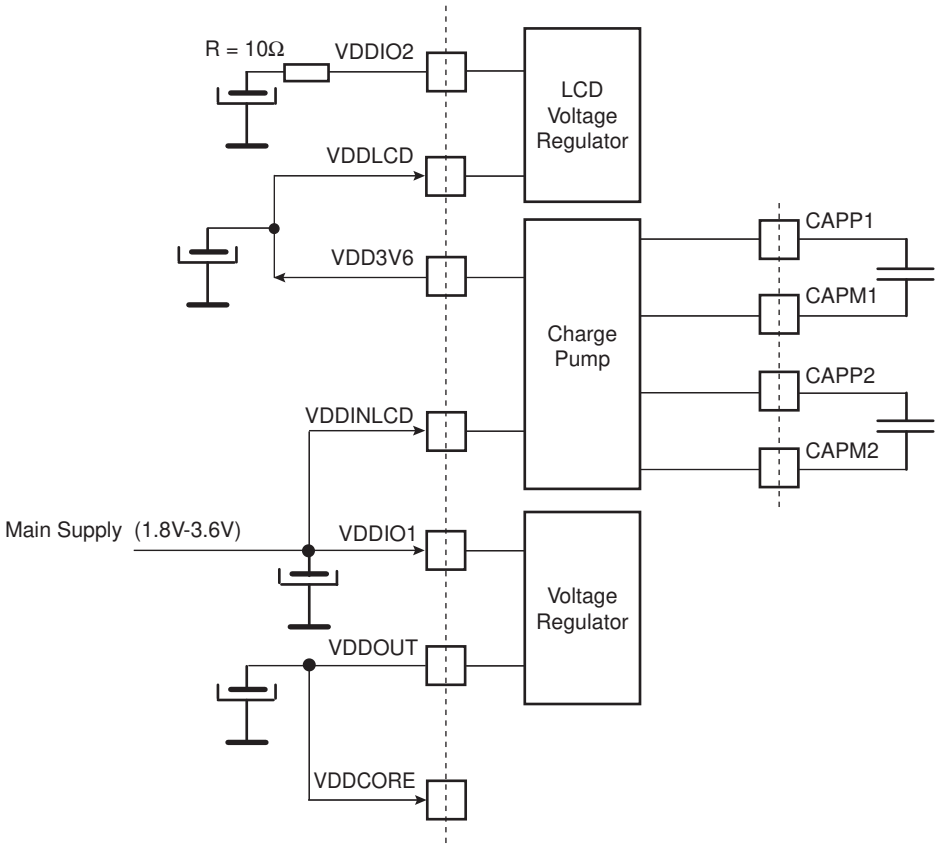


Please note that in this topology, switching time enhancement buffers are not available. (Refer Section 10.13 ”Segment LCD Controller”.)

5.7 Typical Powering Schematics

The AT91SAM7L128/64 supports a 1.8V-3.6V single supply mode. The internal regulator input connected to the source and its output feeds VDDCORE. Figure 5-6 shows the power schematics to be used.

Figure 5-6. 3.3V System Single Power Supply Schematic



6. I/O Line Considerations

6.1 JTAG Port Pins

TMS, TDI and TCK are schmitt trigger inputs. TMS, TDI and TCK do not integrate a pull-up resistor.

TDO is an output, driven at up to VDDIO, and has no pull-up resistor.

The JTAGSEL pin is used to select the JTAG boundary scan when asserted at a high level. The JTAGSEL pin integrates a permanent pull-down resistor of about 15 kΩ to GND, so that it can be left unconnected for normal operations.

6.2 Test Pin

The TST pin is used for manufacturing test or fast programming mode of the AT91SAM7L128/64 when asserted high. The TST pin integrates a permanent pull-down resistor of about 15 kΩ to GND, so that it can be left unconnected for normal operations.

To enter fast programming mode, the TST and CLKIN pins must be tied high while FWUP is tied low.

6.3 NRST Pin

The NRST pin is bidirectional. It is handled by the on-chip reset controller and can be driven low to provide a reset signal to the external components or asserted low externally to reset the microcontroller. There is no constraint on the length of the reset pulse and the reset controller can guarantee a minimum pulse length.

The NRST pin integrates a permanent pull-up resistor to VDDIO1 of about 100 kΩ.

6.4 NRSTB Pin

The NRSTB pin is input only and enables asynchronous reset of the AT91SAM7L128/64 when asserted low. The NRSTB pin integrates a permanent pull-up resistor of about 15 kΩ. This allows connection of a simple push button on the NRBST pin as a system-user reset.

In all modes, this pin will reset the chip. It can be used as an external system reset source.

In harsh environments, it is recommended to add an external capacitor (10 nF) between NRSTB and VDDIO1.

NRSTB pin must not be connected to VDDIO1. There must not be an external pull-up on NRSTB.

6.5 ERASE Pin

The ERASE pin is used to reinitialize the Flash content and some of its NVM bits. It integrates a permanent pull-down resistor of about 15 kΩ to GND, so that it can be left unconnected for normal operations.

This pin is debounced by SCLK to improve the glitch tolerance. When the ERASE pin is tied high during less than 100 ms, it is not taken into account. The pin must be tied high during more than 220 ms to perform the reinitialization of the Flash.

6.6 PIO Controller Lines

All the I/O lines; PA0 to PA25, PB0 to PB23, PC0 to PC29 integrate a programmable pull-up resistor. Programming of this pull-up resistor is performed independently for each I/O line through the PIO controllers. All I/Os have input schmitt triggers.

Typical pull-up value is 100 kΩ.

Maximum frequency is:

- 36 MHz under 25 pF of load on PIOC
- 36 MHz under 25 pF of load on PIOA and PIOB

6.7 I/O Line Current Drawing

The PIO lines PC5 to PC8 are high-drive current capable. Each of these I/O lines can drive up to 4 mA permanently. The remaining I/O lines can draw only 2 mA.

Each I/O is designed to achieve very small leakage. However, the total current drawn by all the I/O lines cannot exceed 150 mA.

7. Processor and Architecture

7.1 ARM7TDMI Processor

- RISC processor based on ARMv4T Von Neumann Architecture
  - Runs at up to 36 MHz, providing 0.9 MIPS/MHz
- Two instruction sets
  - ARM® high-performance 32-bit instruction set
  - Thumb high code density 16-bit instruction set
- Three-stage pipeline architecture
  - Instruction Fetch (F)
  - Instruction Decode (D)
  - Execute (E)

7.2 Debug and Test Features

- Integrated embedded in-circuit emulator
  - Two watchpoint units
  - Test access port accessible through a JTAG protocol
  - Debug communication channel
- Debug Unit
  - Two-pin UART
  - Debug communication channel interrupt handling
  - Chip ID Register
- IEEE1149.1 JTAG Boundary-scan on all digital pins

7.3 Memory Controller

- Programmable Bus Arbiter
  - Handles requests from the ARM7TDMI and the Peripheral DMA Controller
- Address decoder provides selection signals for
  - Five internal 1 Mbyte memory areas
  - One 256 Mbyte embedded peripheral area
- Abort Status Registers
  - Source, Type and all parameters of the access leading to an abort are saved
  - Facilitates debug by detection of bad pointers
- Misalignment Detector
  - Alignment checking of all data accesses
  - Abort generation in case of misalignment
- Remap Command
  - Remaps the SRAM in place of the embedded non-volatile memory
  - Allows handling of dynamic exception vectors
  - Peripheral protection against write and/or user access
- Enhanced Embedded Flash Controller
  - Embedded Flash interface, up to three programmable wait states

  - Prefetch buffer, buffering and anticipating the 16-bit requests, reducing the required wait states
  - Key-protected program, erase and lock/unlock sequencer
  - Single command for erasing, programming and locking operations
  - Interrupt generation in case of forbidden operation

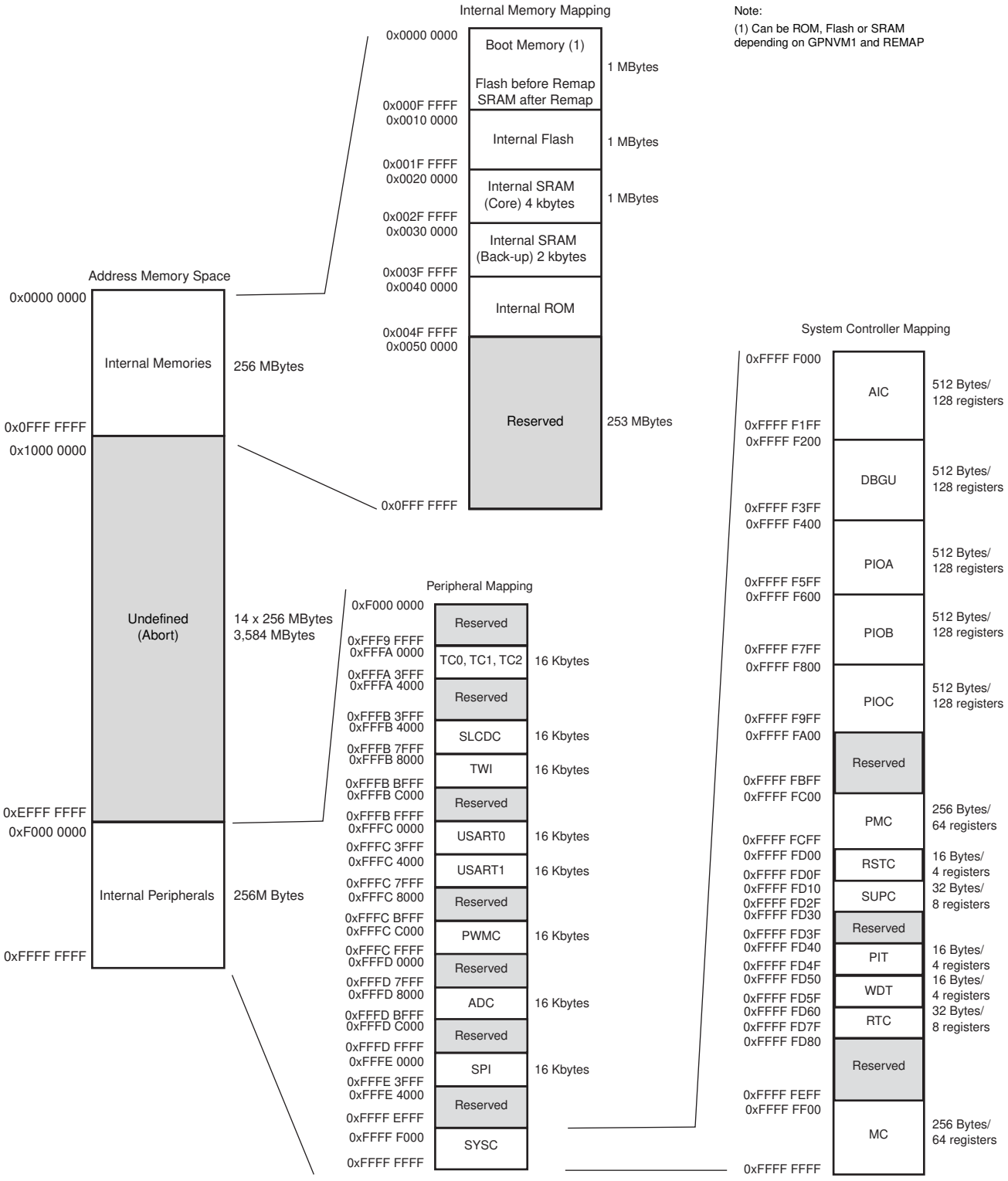
7.4 Peripheral DMA Controller

- Handles data transfer between peripherals and memories
- Eleven channels
  - Two for each USART
  - Two for the Debug Unit
  - Two for the Serial Peripheral Interface
  - Two for the Two Wire Interface
  - One for the Analog-to-digital Converter
- Low bus arbitration overhead
  - One Master Clock cycle needed for a transfer from memory to peripheral
  - Two Master Clock cycles needed for a transfer from peripheral to memory
- Next Pointer management for reducing interrupt latency requirements

8. Memories

- 128 Kbytes of Flash Memory (AT91SAM7L128)
  - Single plane
  - One bank of 512 pages of 256 bytes
  - Fast access time, 15 MHz single-cycle access in Worst Case conditions
  - Page programming time: 4.6 ms, including page auto-erase
  - Page programming without auto-erase: 2.3 ms
  - Full chip erase time: 10 ms
  - 10,000 write cycles, 10-year data retention capability
  - 16 lock bits, each protecting 16 lock regions of 32 pages
  - Protection Mode to secure contents of the Flash
- 64 Kbytes of Flash Memory (AT91SAM7L64)
  - Single plane
  - One bank of 256 pages of 256 bytes
  - Fast access time, 15 MHz single-cycle access in Worst Case conditions
  - Page programming time: 4.6 ms, including page auto-erase
  - Page programming without auto-erase: 2.3 ms
  - Full chip erase time: 10 ms
  - 10,000 write cycles, 10-year data retention capability
  - 8 lock bits, each protecting 8 lock regions of 32 pages
  - Protection Mode to secure contents of the Flash
- 6 Kbytes of Fast SRAM
  - Single-cycle access at full speed
  - 2 Kbytes of Backup SRAM
  - 4 Kbytes of Core SRAM

Figure 8-1. Memory Mapping



8.1 Embedded Memories

8.1.1 Internal Memories

8.1.1.1 Internal SRAM

The AT91SAM7L128/64 embeds a high-speed 4-Kbyte SRAM bank and a 2-Kbyte backup SRAM bank. The backup SRAM is directly supplied on 1.8V-3.6V supply domain.

The 4-Kbyte Core SRAM is supplied by VDDCORE which is connected to the output of the voltage regulator.

After reset and until the Remap Command is performed, the 4-Kbyte Core SRAM is only accessible at address 0x0020 0000. The 2-Kbyte Backup SRAM is accessible at address 0x0030 0000.

After remap, the 4-Kbyte Core SRAM also becomes available at address 0x0.

The user can see the 6 Kbytes of SRAM contiguously at address 0x002F F000.

8.1.1.2 Internal ROM

The AT91SAM7L128/64 embeds an Internal ROM. The ROM is always mapped at address 0x0040 0000. The ROM contains the FFPI and SAM-BA program.

ROM size is 12 Kbytes.

8.1.1.3 Internal Flash

- The AT91SAM7L128 features one bank of 128 Kbytes of Flash.
- The AT91SAM7L64 features one bank of 64 Kbytes of Flash.

At any time, the Flash is mapped to address 0x0010 0000.

A general purpose NVM (GPNVM1) bit is used to boot either on the ROM (default) or from the Flash.

This GPNVM1 bit can be cleared or set respectively through the commands “Clear General-purpose NVM Bit” and “Set General-purpose NVM Bit” of the EEFC User Interface.

Setting the GPNVM Bit 1 selects the boot from the Flash, clearing it selects the boot from the ROM. Asserting ERASE clears the GPNVM Bit 1 and thus selects the boot from the ROM by default.

Figure 8-2. Internal Memory Mapping with GPNVM Bit 1 = 0 (default)