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AT91SAM ARM-based Embedded MPU

SAM9260

Features

- 180 MHz ARM926EJ-S™ ARM® Thumb® Processor
  - 8 KBytes Data Cache, 8 KBytes Instruction Cache, MMU
- Memories
  - 32-bit External Bus Interface supporting 4-bank SDRAM/LPSDR, Static Memories, CompactFlash, SLC NAND Flash with ECC
  - Two 4-kbyte internal SRAM, single-cycle access at system speed
  - One 32-kbyte internal ROM, embedding bootstrap routine
- Peripherals
  - ITU-R BT. 601/656 Image Sensor Interface
  - USB Device and USB Host with dedicated On-Chip Transceiver
  - 10/100 Mbps Ethernet MAC Controller
  - One High Speed Memory Card Host
  - Two Master/Slave Serial Peripheral Interfaces
  - Two Three-channel 32-bit Timer/Counters
  - One Synchronous Serial Controller
  - One Two-wire Interface
  - Four USARTs
  - Two UARTs
  - 4-channel 10-bit ADC
- System
  - 90 MHz six 32-bit layer AHB Bus Matrix
  - 22 Peripheral DMA Channels
  - Boot from NAND Flash, DataFlash® or serial DataFlash
  - Reset Controller with On-Chip Power-on Reset
  - Selectable 32,768 Hz Low-Power and 3-20 MHz Main Oscillator
  - Internal Low-Power 32 kHz RC Oscillator
  - One PLL for the system and one PLL optimized for USB
  - Two Programmable External Clock Signals
  - Advanced Interrupt Controller and Debug Unit
  - Periodic Interval Timer, Watchdog Timer and Real Time Timer
- I/O
  - Three 32-bit Parallel Input/Output Controllers
  - 96 Programmable I/O Lines Multiplexed with up to Two Peripheral I/Os
- Package
  - 217-ball BGA, 0.8 mm pitch
  - 208-pin QFP, 0.5 mm pitch

This is a summary document. The complete document is available on the Atmel website at www.atmel.com.

1. Description

The SAM9260 is based on the integration of an ARM926EJ-S processor with fast ROM and RAM memories and a wide range of peripherals.

The SAM9260 embeds an Ethernet MAC, one USB Device Port, and a USB Host controller. It also integrates several standard peripherals, such as the USART, SPI, TWI, Timer Counters, Synchronous Serial Controller, ADC and MultiMedia Card Interface.

The SAM9260 is architectured on a 6-layer matrix, allowing a maximum internal bandwidth of six 32-bit buses. It also features an External Bus Interface capable of interfacing with a wide range of memory devices.

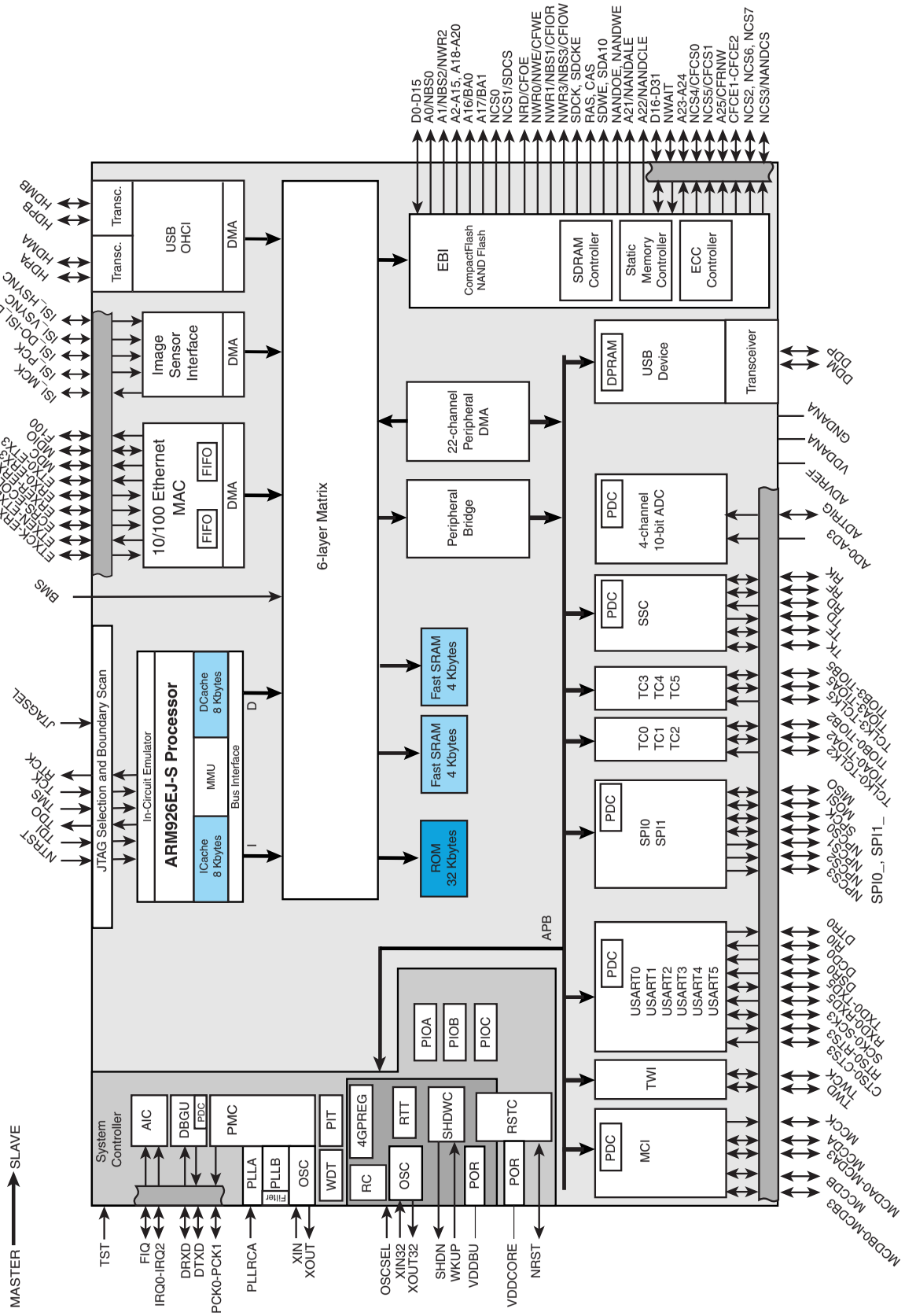
2. SAM9260 Block Diagram

The block diagram shows all the features for the 217-LFBGA package. Some functions are not accessible in the 208-pin PQFP package and the unavailable pins are highlighted in “Multiplexing on PIO Controller A” on page 31, “Multiplexing on PIO Controller B” on page 32, “Multiplexing on PIO Controller C” on page 33. The USB Host Port B is not available in the 208-pin package. Table 2-1 on page 2 defines all the multiplexed and not multiplexed pins not available in the 208-PQFP package.

Table 2-1. Unavailable Signals in 208-lead PQFP Package

PIO	Peripheral A	Peripheral B
-	HDPB	-
-	HDMB	-
PA30	SCK2	RXD4
PA31	SCK0	TXD4
PB12	TXD5	ISI_D10
PB13	RXD5	ISI_D11
PC2	AD2	PCK1
PC3	AD3	SPI1_NPCS3
PC12	IRQ0	NCS7

Figure 2-1. SAM9260 Block Diagram



3. Signal Description

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level	Comments
Power Supplies				
VDDIOM	EBI I/O Lines Power Supply	Power		1.65V to 1.95V or 3.0V to3.6V
VDDIOP0	Peripherals I/O Lines Power Supply	Power		3.0V to 3.6V
VDDIOP1	Peripherals I/O Lines Power Supply	Power		1.65V to 3.6V
VDDBU	Backup I/O Lines Power Supply	Power		1.65V to 1.95V
VDDANA	Analog Power Supply	Power		3.0V to 3.6V
VDDPLL	PLL Power Supply	Power		1.65V to 1.95V
VDDCORE	Core Chip Power Supply	Power		1.65V to 1.95V
GND	Ground	Ground		
GNDPLL	PLL and Oscillator Ground	Ground		
GNDANA	Analog Ground	Ground		
GNDBU	Backup Ground	Ground		
Clocks, Oscillators and PLLs				
XIN	Main Oscillator Input	Input		
XOUT	Main Oscillator Output	Output		
XIN32	Slow Clock Oscillator Input	Input		
XOUT32	Slow Clock Oscillator Output	Output		
OSCSEL	Slow Clock Oscillator Selection	Input		Accepts between 0V and VDDBU.
PLLRCA	PLL A Filter	Input		
PCK0 - PCK1	Programmable Clock Output	Output		
Shutdown, Wakeup Logic				
SHDN	Shutdown Control	Output		Driven at 0V only. Do not tie over VDDBU.
WKUP	Wake-up Input	Input		Accepts between 0V and VDDBU.
ICE and JTAG				
NTRST	Test Reset Signal	Input	Low	Pull-up resistor
TCK	Test Clock	Input		No pull-up resistor
TDI	Test Data In	Input		No pull-up resistor
TDO	Test Data Out	Output		
TMS	Test Mode Select	Input		No pull-up resistor
JTAGSEL	JTAG Selection	Input		Pull-down resistor. Accepts between 0V and VDDBU.
RTCK	Return Test Clock	Output		

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Comments
Reset/Test				
NRST	Microcontroller Reset	I/O	Low	Pull-up resistor
TST	Test Mode Select	Input		Pull-down resistor. Accepts between 0V and VDDBU.
BMS	Boot Mode Select	Input		No pull-up resistor BMS = 0 when tied to GND BMS = 1 when tied to VDDIOP0.
Debug Unit - DBGU				
DRXD	Debug Receive Data	Input		
DTXD	Debug Transmit Data	Output		
Advanced Interrupt Controller - AIC				
IRQ0 - IRQ2	External Interrupt Inputs	Input		
FIQ	Fast Interrupt Input	Input		
PIO Controller - PIOA - PIOB - PIOC				
PA0 - PA31	Parallel IO Controller A	I/O		Pulled-up input at reset
PB0 - PB31	Parallel IO Controller B	I/O		Pulled-up input at reset
PC0 - PC31	Parallel IO Controller C	I/O		Pulled-up input at reset
External Bus Interface - EBI				
D0 - D31	Data Bus	I/O		Pulled-up input at reset
A0 - A25	Address Bus	Output		0 at reset
NWAIT	External Wait Signal	Input	Low	
Static Memory Controller - SMC				
NCS0 - NCS7	Chip Select Lines	Output	Low	
NWR0 - NWR3	Write Signal	Output	Low	
NRD	Read Signal	Output	Low	
NWE	Write Enable	Output	Low	
NBS0 - NBS3	Byte Mask Signal	Output	Low	
CompactFlash Support				
CFCE1 - CFCE2	CompactFlash Chip Enable	Output	Low	
CFOE	CompactFlash Output Enable	Output	Low	
CFWE	CompactFlash Write Enable	Output	Low	
CFIOR	CompactFlash IO Read	Output	Low	
CFIOW	CompactFlash IO Write	Output	Low	
CFRNW	CompactFlash Read Not Write	Output		
CFCS0 - CFCS1	CompactFlash Chip Select Lines	Output	Low	

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Comments
NAND Flash Support				
NANDCS	NAND Flash Chip Select	Output	Low	
NANDOE	NAND Flash Output Enable	Output	Low	
NANDWE	NAND Flash Write Enable	Output	Low	
NANDALE	NAND Flash Address Latch Enable	Output	Low	
NANDCLE	NAND Flash Command Latch Enable	Output	Low	
SDRAM Controller				
SDCK	SDRAM Clock	Output		
SDCKE	SDRAM Clock Enable	Output	High	
SDCS	SDRAM Controller Chip Select	Output	Low	
BA0 - BA1	Bank Select	Output		
SDWE	SDRAM Write Enable	Output	Low	
RAS - CAS	Row and Column Signal	Output	Low	
SDA10	SDRAM Address 10 Line	Output		
Multimedia Card Interface MCI				
MCCK	Multimedia Card Clock	Output		
MCCDA	Multimedia Card Slot A Command	I/O		
MCDA0 - MCDA3	Multimedia Card Slot A Data	I/O		
MCCDB	Multimedia Card Slot B Command	I/O		
MCDB0 - MCDB3	Multimedia Card Slot B Data	I/O		
Universal Synchronous Asynchronous Receiver Transmitter USARTx				
SCKx	USARTx Serial Clock	I/O		
TXDx	USARTx Transmit Data	I/O		
RXDx	USARTx Receive Data	Input		
RTSx	USARTx Request To Send	Output		
CTSx	USARTx Clear To Send	Input		
DTR0	USART0 Data Terminal Ready	Output		
DSR0	USART0 Data Set Ready	Input		
DCD0	USART0 Data Carrier Detect	Input		
RI0	USART0 Ring Indicator	Input		
Synchronous Serial Controller - SSC				
TD	SSC Transmit Data	Output		
RD	SSC Receive Data	Input		
TK	SSC Transmit Clock	I/O		
RK	SSC Receive Clock	I/O		
TF	SSC Transmit Frame Sync	I/O		
RF	SSC Receive Frame Sync	I/O		

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Comments
Timer/Counter - TCx				
TCLKx	TC Channel x External Clock Input	Input		
TIOAx	TC Channel x I/O Line A	I/O		
TIOBx	TC Channel x I/O Line B	I/O		
Serial Peripheral Interface - SPIx_				
SPIx_MISO	Master In Slave Out	I/O		
SPIx_MOSI	Master Out Slave In	I/O		
SPIx_SPCK	SPI Serial Clock	I/O		
SPIx_NPCS0	SPI Peripheral Chip Select 0	I/O	Low	
SPIx_NPCS1-SPIx_NPCS3	SPI Peripheral Chip Select	Output	Low	
Two-Wire Interface				
TWD	Two-wire Serial Data	I/O		
TWCK	Two-wire Serial Clock	I/O		
USB Host Port				
HDPA	USB Host Port A Data +	Analog		
HDMA	USB Host Port A Data -	Analog		
HDPB	USB Host Port B Data +	Analog		
HDMB	USB Host Port B Data +	Analog		
USB Device Port				
DDM	USB Device Port Data -	Analog		
DDP	USB Device Port Data +	Analog		
Ethernet 10/100				
ETXCK	Transmit Clock or Reference Clock	Input		MII only, REFCK in RMII
ERXCK	Receive Clock	Input		MII only
ETXEN	Transmit Enable	Output		
ETX0-ETX3	Transmit Data	Output		ETX0-ETX1 only in RMII
ETXER	Transmit Coding Error	Output		MII only
ERXDV	Receive Data Valid	Input		RXDV in MII, CRSDV in RMII
ERX0-ERX3	Receive Data	Input		ERX0-ERX1 only in RMII
ERXER	Receive Error	Input		
ECRS	Carrier Sense and Data Valid	Input		MII only
ECOL	Collision Detect	Input		MII only
EMDC	Management Data Clock	Output		
EMDIO	Management Data Input/Output	I/O		
EF100	Force 100Mbit/sec.	Output	High	

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Comments
Image Sensor Interface				
ISI_D0-ISI_D11	Image Sensor Data	Input		
ISI_MCK	Image Sensor Reference Clock	Output		Provided by PCK1.
ISI_HSYNC	Image Sensor Horizontal Synchro	Input		
ISI_VSYNC	Image Sensor Vertical Synchro	Input		
ISI_PCK	Image Sensor Data clock	Input		
Analog to Digital Converter				
AD0-AD3	Analog Inputs	Analog		Digital pulled-up inputs at reset
ADVREF	Analog Positive Reference	Analog		
ADTRG	ADC Trigger	Input		

4. Package and Pinout

The SAM9260 is available in two packages:

- 208-pin PQFP Green package (0.5mm pitch).
- 217-ball LFBGA Green package (0.8 mm ball pitch).

4.1 208-pin PQFP Package

Figure 11-3 shows the orientation of the 208-pin PQFP package. A detailed mechanical description is given in the section "SAM9260 Mechanical Characteristics" of the datasheet.

4.2 208-pin PQFP Pinout

Table 4-1. Pinout for 208-pin PQFP Package

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
1	PA24	53	GND	105	RAS	157	ADVREF
2	PA25	54	DDM	106	D0	158	PC0
3	PA26	55	DDP	107	D1	159	PC1
4	PA27	56	PC13	108	D2	160	VDDANA
5	VDDIOP0	57	PC11	109	D3	161	PB10
6	GND	58	PC10	110	D4	162	PB11
7	PA28	59	PC14	111	D5	163	PB20
8	PA29	60	PC9	112	D6	164	PB21
9	PB0	61	PC8	113	GND	165	PB22
10	PB1	62	PC4	114	VDDIOM	166	PB23
11	PB2	63	PC6	115	SDCK	167	PB24
12	PB3	64	PC7	116	SDWE	168	PB25
13	VDDIOP0	65	VDDIOM	117	SDCKE	169	VDDIOP1
14	GND	66	GND	118	D7	170	GND
15	PB4	67	PC5	119	D8	171	PB26
16	PB5	68	NCS0	120	D9	172	PB27
17	PB6	69	CFOE/NRD	121	D10	173	GND
18	PB7	70	CFWE/NWE/NWR0	122	D11	174	VDDCORE
19	PB8	71	NANDOE	123	D12	175	PB28
20	PB9	72	NANDWE	124	D13	176	PB29
21	PB14	73	A22	125	D14	177	PB30
22	PB15	74	A21	126	D15	178	PB31
23	PB16	75	A20	127	PC15	179	PA0
24	VDDIOP0	76	A19	128	PC16	180	PA1
25	GND	77	VDDCORE	129	PC17	181	PA2
26	PB17	78	GND	130	PC18	182	PA3
27	PB18	79	A18	131	PC19	183	PA4
28	PB19	80	BA1/A17	132	VDDIOM	184	PA5
29	TDO	81	BA0/A16	133	GND	185	PA6
30	TDI	82	A15	134	PC20	186	PA7
31	TMS	83	A14	135	PC21	187	VDDIOP0
32	VDDIOP0	84	A13	136	PC22	188	GND
33	GND	85	A12	137	PC23	189	PA8
34	TCK	86	A11	138	PC24	190	PA9
35	NTRST	87	A10	139	PC25	191	PA10
36	NRST	88	A9	140	PC26	192	PA11
37	RTCK	89	A8	141	PC27	193	PA12
38	VDDCORE	90	VDDIOM	142	PC28	194	PA13
39	GND	91	GND	143	PC29	195	PA14
40	BMS	92	A7	144	PC30	196	PA15
41	OSCSEL	93	A6	145	PC31	197	PA16
42	TST	94	A5	146	GND	198	PA17
43	JTAGSEL	95	A4	147	VDDCORE	199	VDDIOP0
44	GNDBU	96	A3	148	VDDPLL	200	GND
45	XOUT32	97	A2	149	XIN	201	PA18
46	XIN32	98	NWR2/NBS2/A1	150	XOUT	202	PA19
47	VDDBU	99	NBS0/A0	151	GNDPLL	203	VDDCORE
48	WKUP	100	SDA10	152	NC	204	GND
49	SHDN	101	CFIOW/NBS3/NWR3	153	GNDPLL	205	PA20
50	HDMA	102	CFIOR/NBS1/NWR1	154	PLLRCA	206	PA21
51	HDPA	103	SDCS/NCS1	155	VDDPLL	207	PA22
52	VDDIOP0	104	CAS	156	GNDANA	208	PA23

4.3 217-ball LFBGA Package

Figure 11-1 shows the orientation of the 217-ball LFBGA package. A detailed mechanical description is given in the section “SAM9260 Mechanical Characteristics” of the datasheet.

4.4 217-ball LFBGA Pinout

Table 4-2. Pinout for 217-ball LFBGA Package

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	CFIOW/NBS3/NWR3	D5	A5	J14	TDO	P17	PB5
A2	NBS0/A0	D6	GND	J15	PB19	R1	NC
A3	NWR2/NBS2/A1	D7	A10	J16	TDI	R2	GNDANA
A4	A6	D8	GND	J17	PB16	R3	PC29
A5	A8	D9	VDDCORE	K1	PC24	R4	VDDANA
A6	A11	D10	GND	K2	PC20	R5	PB12
A7	A13	D11	VDDIOM	K3	D15	R6	PB23
A8	BA0/A16	D12	GND	K4	PC21	R7	GND
A9	A18	D13	DDM	K8	GND	R8	PB26
A10	A21	D14	HDPB	K9	GND	R9	PB28
A11	A22	D15	NC	K10	GND	R10	PA0
A12	CFWE/NWE/NWR0	D16	VDDBU	K14	PB4	R11	PA4
A13	CFOE/NRD	D17	XIN32	K15	PB17	R12	PA5
A14	NCS0	E1	D10	K16	GND	R13	PA10
A15	PC5	E2	D5	K17	PB15	R14	PA21
A16	PC6	E3	D3	L1	GND	R15	PA23
A17	PC4	E4	D4	L2	PC26	R16	PA24
B1	SDCK	E14	HDPA	L3	PC25	R17	PA29
B2	CFIOR/NBS1/NWR1	E15	HDMA	L4	VDDIOP0	T1	PLLRCA
B3	SDCS/NCS1	E16	GNDBU	L14	PA28	T2	GNDPLL
B4	SDA10	E17	XOUT32	L15	PB9	T3	PC0
B5	A3	F1	D13	L16	PB8	T4	PC1
B6	A7	F2	SDWE	L17	PB14	T5	PB10
B7	A12	F3	D6	M1	VDDCORE	T6	PB22
B8	A15	F4	GND	M2	PC31	T7	GND
B9	A20	F14	OSCSEL	M3	GND	T8	PB29
B10	NANDWE	F15	BMS	M4	PC22	T9	PA2
B11	PC7	F16	JTAGSEL	M14	PB1	T10	PA6
B12	PC10	F17	TST	M15	PB2	T11	PA8
B13	PC13	G1	PC15	M16	PB3	T12	PA11
B14	PC11	G2	D7	M17	PB7	T13	VDDCORE
B15	PC14	G3	SDCKE	N1	XIN	T14	PA20
B16	PC8	G4	VDDIOM	N2	VDDPLL	T15	GND
B17	WKUP	G14	GND	N3	PC23	T16	PA22
C1	D8	G15	NRST	N4	PC27	T17	PA27
C2	D1	G16	RTCK	N14	PA31	U1	GNDPLL
C3	CAS	G17	TMS	N15	PA30	U2	ADVREF
C4	A2	H1	PC18	N16	PB0	U3	PC2
C5	A4	H2	D14	N17	PB6	U4	PC3
C6	A9	H3	D12	P1	XOUT	U5	PB20
C7	A14	H4	D11	P2	VDDPLL	U6	PB21
C8	BA1/A17	H8	GND	P3	PC30	U7	PB25
C9	A19	H9	GND	P4	PC28	U8	PB27
C10	NANDOE	H10	GND	P5	PB11	U9	PA12
C11	PC9	H14	VDDCORE	P6	PB13	U10	PA13
C12	PC12	H15	TCK	P7	PB24	U11	PA14
C13	DDP	H16	NTRST	P8	VDDIOP1	U12	PA15
C14	HDMB	H17	PB18	P9	PB30	U13	PA19
C15	NC	J1	PC19	P10	PB31	U14	PA17
C16	VDDIOP0	J2	PC17	P11	PA1	U15	PA16
C17	SHDN	J3	VDDIOM	P12	PA3	U16	PA18
D1	D9	J4	PC16	P13	PA7	U17	VDDIOP0
D2	D2	J8	GND	P14	PA9		
D3	RAS	J9	GND	P15	PA26		
D4	D0	J10	GND	P16	PA25		

5. Power Considerations

5.1 Power Supplies

The SAM9260 has several types of power supply pins:

- VDDCORE pins: Power the core, including the processor, the embedded memories and the peripherals; voltage ranges from 1.65V and 1.95V, 1.8V nominal.
- VDDIOM pins: Power the External Bus Interface I/O lines; voltage ranges between 1.65V and 1.95V (1.8V typical) or between 3.0V and 3.6V (3.3V nominal). The expected voltage range is selectable by software.
- VDDIOP0 pins: Power the Peripheral I/O lines and the USB transceivers; voltage ranges from 3.0V and 3.6V, 3V or 3.3V nominal.
- VDDIOP1 pins: Power the Peripherals I/O lines involving the Image Sensor Interface; voltage ranges from 1.65V and 3.6V, 1.8V, 2.5V, 3V or 3.3V nominal.
- VDDBU pin: Powers the Slow Clock oscillator and a part of the System Controller; voltage ranges from 1.65V to 1.95V, 1.8V nominal.
- VDDPLL pin: Powers the Main Oscillator and PLL cells; voltage ranges from 1.65V and 1.95V, 1.8V nominal.
- VDDANA pin: Powers the Analog to Digital Converter; voltage ranges from 3.0V and 3.6V, 3.3V nominal.

The power supplies VDDIOM, VDDIOP0 and VDDIOP1 are identified in the pinout table and the multiplexing tables. These supplies enable the user to power the device differently for interfacing with memories and for interfacing with peripherals.

Ground pins GND are common to VDDCORE, VDDIOM, VDDIOP0 and VDDIOP1 pins power supplies. Separated ground pins are provided for VDDBU, VDDPLL and VDDANA. These ground pins are respectively GNDBU, GNDPLL and GNDANA.

5.2 Power Consumption

The SAM9260 consumes about 500 µA of static current on VDDCORE at 25°C. This static current rises up to 5 mA if the temperature increases to 85°C.

On VDDBU, the current does not exceed 10 µA in worst case conditions.

For dynamic power consumption, the SAM9260 consumes a maximum of 100 mA on VDDCORE at maximum conditions (1.8V, 25°C, processor running full-performance algorithm out of high speed memories).

5.3 Programmable I/O Lines Power Supplies

The power supplies pins VDDIOM accept two voltage ranges. This allows the device to reach its maximum speed either out of 1.8V or 3.3V external memories.

The target maximum speed is 100 MHz on the pin SDCK (SDRAM Clock) loaded with 30 pF for power supply at 1.8V and 50 pF for power supply at 3.3V. The other signals (control, address and data signals) do not exceed 50 MHz.

The voltage ranges are determined by programming registers in the Chip Configuration registers located in the Matrix User Interface.

At reset, the selected voltage defaults to 3.3V nominal, and power supply pins can accept either 1.8V or 3.3V. Obviously, the device cannot reach its maximum speed if the voltage supplied to the pins is 1.8V only. The user must program the EBI voltage range before getting the device out of its Slow Clock Mode.

6. I/O Line Considerations

6.1 JTAG Port Pins

TMS, TDI and TCK are Schmitt trigger inputs and have no pull-up resistors.

TDO and RTCK are outputs, driven at up to VDDIOP0, and have no pull-up resistors.

The JTAGSEL pin is used to select the JTAG boundary scan when asserted at a high level (tied to VDDBU). It integrates a permanent pull-down resistor of about **15 kΩ** to GNDBU, so that it can be left unconnected for normal operations.

The NTRST signal is described in Section 6.3.

All the JTAG signals are supplied with VDDIOP0.

6.2 Test Pin

The TST pin is used for manufacturing test purposes when asserted high. It integrates a permanent pull-down resistor of about 15 kΩ to GNDBU, so that it can be left unconnected for normal operations. Driving this line at a high level leads to unpredictable results.

This pin is supplied with VDDBU.

6.3 Reset Pins

NRST is a bidirectional with an open-drain output integrating a non-programmable pull-up resistor. It can be driven with voltage at up to VDDIOP0.

NTRST is an input which allows reset of the JTAG Test Access port. It has no action on the processor.

As the product integrates power-on reset cells, which manages the processor and the JTAG reset, the NRST and NTRST pins can be left unconnected.

The NRST and NTRST pins both integrate a permanent pull-up resistor to VDDIOP0. Its value can be found in the table “DC Characteristics” in the section “SAM9260 Electrical Characteristics” in the product datasheet.

The NRST signal is inserted in the Boundary Scan.

6.4 PIO Controllers

All the I/O lines managed by the PIO Controllers integrate a programmable pull-up resistor. Refer to the section on DC Characteristics in “SAM9260 Electrical Characteristics” for more information. Programming of this pull-up resistor is performed independently for each I/O line through the PIO Controllers.

After reset, all the I/O lines default as inputs with pull-up resistors enabled, except those which are multiplexed with the External Bus Interface signals and that must be enabled as Peripheral at reset. This is explicitly indicated in the column “Reset State” of the PIO Controller multiplexing tables.

6.5 I/O Line Drive Levels

The PIO lines are high-drive current capable. Each of these I/O lines can drive up to 16 mA permanently except PC4 to PC31 that are VDDIOM powered.

6.6 Shutdown Logic Pins

The SHDN pin is a tri-state output pin, which is driven by the Shutdown Controller. There is no internal pull-up. An external pull-up tied to VDDBU is needed and its value must be higher than 1 MΩ. The resistor value is calculated according to the regulator enable implementation and the SHDN level.

The pin WKUP is an input-only. It can accept voltages only between 0V and VDDBU.

6.7 Slow Clock Selection

The SAM9260 slow clock can be generated either by an external 32,768 Hz crystal or the on-chip RC oscillator.

Table 6-1 defines the states for OSCSEL signal.

Table 6-1. Slow Clock Selection

OSCSEL	Slow Clock	Startup Time
0	Internal RC	240 µs
1	External 32768 Hz	1200 ms

The startup counter delay for the slow clock oscillator depends on the OSCSEL signal. The 32,768 Hz startup delay is 1200 ms whereas it is 240 µs for the internal RC oscillator (refer to Table 6-1). The pin OSCSEL must be tied either to GND or VDDBU for correct operation of the device.

7. Processor and Architecture

7.1 ARM926EJ-S Processor

- RISC Processor Based on ARM v5TEJ Architecture with Jazelle technology for Java acceleration
- Two Instruction Sets
  - ARM High-performance 32-bit Instruction Set
  - Thumb High Code Density 16-bit Instruction Set
- DSP Instruction Extensions
- 5-Stage Pipeline Architecture:
  - Instruction Fetch (F)
  - Instruction Decode (D)
  - Execute (E)
  - Data Memory (M)
  - Register Write (W)
- 8-Kbyte Data Cache, 8-Kbyte Instruction Cache
  - Virtually-addressed 4-way Associative Cache
  - Eight words per line
  - Write-through and Write-back Operation
  - Pseudo-random or Round-robin Replacement
- Write Buffer
  - Main Write Buffer with 16-word Data Buffer and 4-address Buffer
  - DCache Write-back Buffer with 8-word Entries and a Single Address Entry
  - Software Control Drain
- Standard ARM v4 and v5 Memory Management Unit (MMU)
  - Access Permission for Sections
  - Access Permission for large pages and small pages can be specified separately for each quarter of the page
  - 16 embedded domains
- Bus Interface Unit (BIU)
  - Arbitrates and Schedules AHB Requests
  - Separate Masters for both instruction and data access providing complete Matrix system flexibility
  - Separate Address and Data Buses for both the 32-bit instruction interface and the 32-bit data interface
  - On Address and Data Buses, data can be 8-bit (Bytes), 16-bit (Half-words) or 32-bit (Words)

7.2 Bus Matrix

- 6-layer Matrix, handling requests from 6 masters
- Programmable Arbitration strategy
  - Fixed-priority Arbitration
  - Round-Robin Arbitration, either with no default master, last accessed default master or fixed default master
- Burst Management
  - Breaking with Slot Cycle Limit Support
  - Undefined Burst Length Support
- One Address Decoder provided per Master
  - Three different slaves may be assigned to each decoded memory area: one for internal boot, one for external boot, one after remap

- Boot Mode Select
  - Non-volatile Boot Memory can be internal or external
  - Selection is made by BMS pin sampled at reset
- Remap Command
  - Allows Remapping of an Internal SRAM in Place of the Boot Non-Volatile Memory
  - Allows Handling of Dynamic Exception Vectors

7.2.1 Matrix Masters

The Bus Matrix of the SAM9260 manages six Masters, which means that each master can perform an access concurrently with others, according the slave it accesses is available.

Each Master has its own decoder that can be defined specifically for each master. In order to simplify the addressing, all the masters have the same decodings.

Table 7-1. List of Bus Matrix Masters

Master 0	ARM926™ Instruction
Master 1	ARM926 Data
Master 2	PDC
Master 3	USB Host DMA
Master 4	ISI Controller
Master 5	Ethernet MAC

7.2.2 Matrix Slaves

Each Slave has its own arbiter, thus allowing a different arbitration per Slave to be programmed.

Table 7-2. List of Bus Matrix Slaves

Slave 0	Internal SRAM0 4 KBytes
Slave 1	Internal SRAM1 4 KBytes
Slave 2	Internal ROM
	USB Host User Interface
Slave 3	External Bus Interface
Slave 4	Internal Peripherals

7.2.3 Master to Slave Access

All the Masters can normally access all the Slaves. However, some paths do not make sense, such as allowing access from the Ethernet MAC to the Internal Peripherals. Thus, these paths are forbidden or simply not wired, and shown “-” in the following table.

Table 7-3. SAM9260 Masters to Slaves Access

Master		0 & 1	2	3	4	5
Slave		ARM926 Instruction & Data	Peripheral DMA Controller	USB Host Controller	ISI Controller	Ethernet MAC
0	Internal SRAM 4 KBytes	X	X	X	X	X
1	Internal SRAM 4 KBytes	X	X	X	X	X

Table 7-3. SAM9260 Masters to Slaves Access (Continued)

2	Internal ROM	X	X	X	-	-
	UHP User Interface	X	-	-	-	-
3	External Bus Interface	X	X	X	X	X
4	Internal Peripherals	X	X	X	-	-

7.3 Peripheral DMA Controller

- Acting as one Matrix Master
- Allows data transfers from/to peripheral to/from any memory space without any intervention of the processor.
- Next Pointer Support, forbids strong real-time constraints on buffer management.
- Twenty-two channels
  - Two for each USART
  - Two for the Debug Unit
  - Two for each Serial Synchronous Controller
  - Two for each Serial Peripheral Interface
  - One for Multimedia Card Interface
  - One for Analog-to-Digital Converter

The Peripheral DMA Controller handles transfer requests from the channel according to the following priorities (Low to High priorities):

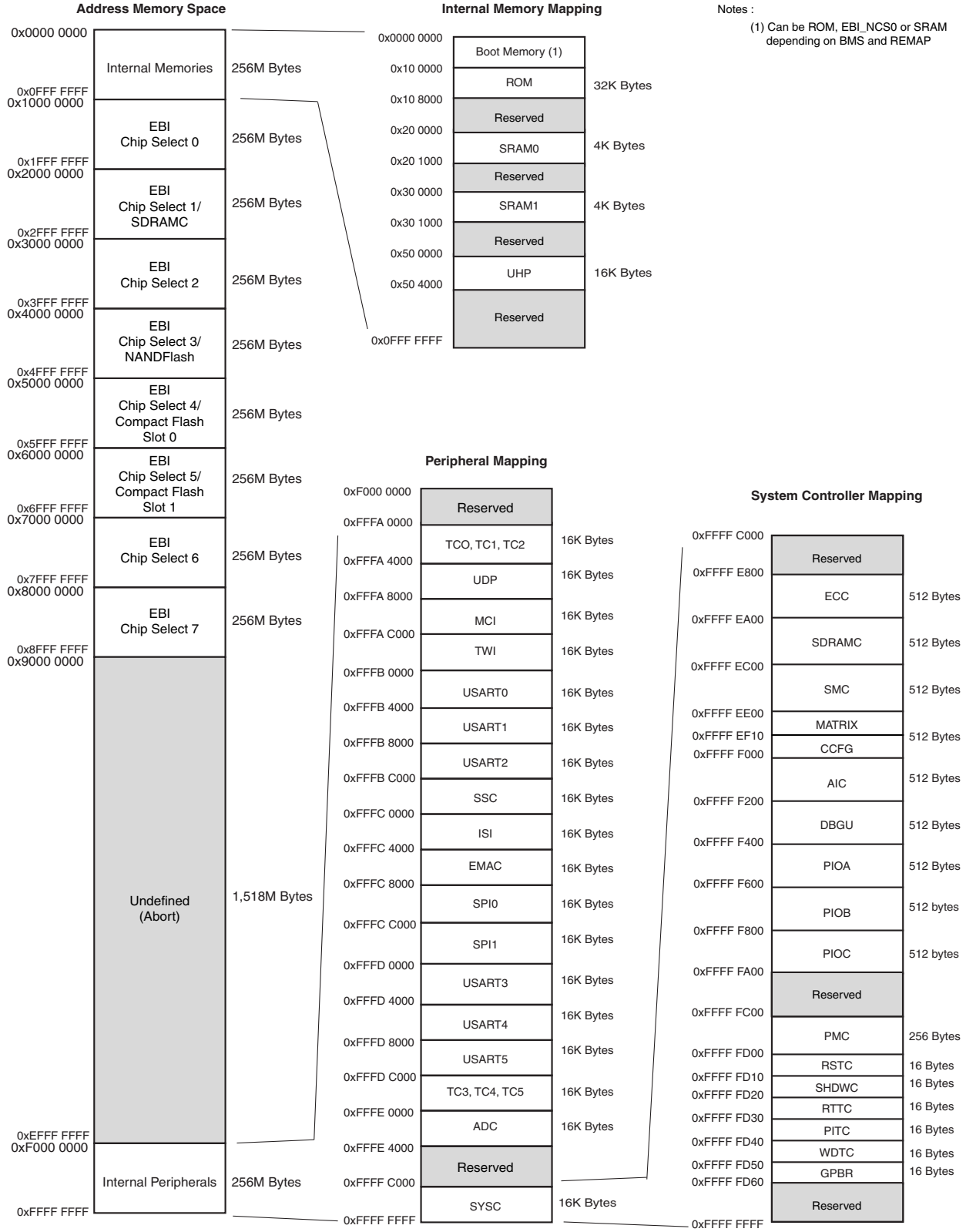
- DBGU Transmit Channel
- USART5 Transmit Channel
- USART4 Transmit Channel
- USART3 Transmit Channel
- USART2 Transmit Channel
- USART1 Transmit Channel
- USART0 Transmit Channel
- SPI1 Transmit Channel
- SPI0 Transmit Channel
- SSC Transmit Channel
- DBGU Receive Channel
- USART5 Receive Channel
- USART4 Receive Channel
- USART3 Receive Channel
- USART2 Receive Channel
- USART1 Receive Channel
- USART0 Receive Channel
- ADC Receive Channel
- SPI1 Receive Channel
- SPI0 Receive Channel
- SSC Receive Channel
- MCI Transmit/Receive Channel

7.4 Debug and Test Features

- ARM926 Real-time In-circuit Emulator
  - Two real-time Watchpoint Units
  - Two Independent Registers: Debug Control Register and Debug Status Register
  - Test Access Port Accessible through JTAG Protocol
  - Debug Communications Channel
- Debug Unit
  - Two-pin UART
  - Debug Communication Channel Interrupt Handling
  - Chip ID Register
- IEEE1149.1 JTAG Boundary-scan on All Digital Pins

8. Memories

Figure 8-1. SAM9260 Memory Mapping



A first level of address decoding is performed by the Bus Matrix, i.e., the implementation of the Advanced High Performance Bus (AHB) for its Master and Slave interfaces with additional features.

Decoding breaks up the 4G bytes of address space into 16 banks of 256 Mbytes. The banks 1 to 7 are directed to the EBI that associates these banks to the external chip selects EBI_NCS0 to EBI_NCS7. Bank 0 is reserved for the addressing of the internal memories, and a second level of decoding provides 1 Mbyte of internal memory area. Bank 15 is reserved for the peripherals and provides access to the Advanced Peripheral Bus (APB).

Other areas are unused and performing an access within them provides an abort to the master requesting such an access.

Each Master has its own bus and its own decoder, thus allowing a different memory mapping per Master. However, in order to simplify the mappings, all the masters have a similar address decoding.

Regarding Master 0 and Master 1 (ARM926 Instruction and Data), three different Slaves are assigned to the memory space decoded at address 0x0: one for internal boot, one for external boot, one after remap. Refer to Table 8-1, “Internal Memory Mapping,” on page 20 for details.

A complete memory map is presented in Figure 8-1 on page 19.

8.1 Embedded Memories

- 32 KB ROM
  - Single Cycle Access at full matrix speed
- Two 4 KB Fast SRAM
  - Single Cycle Access at full matrix speed

8.1.1 Boot Strategies

Table 8-1 summarizes the Internal Memory Mapping for each Master, depending on the Remap status and the BMS state at reset.

Table 8-1. Internal Memory Mapping

Address	REMAP = 0		REMAP = 1
	BMS = 1	BMS = 0	
0x0000 0000	ROM	EBI_NCS0	SRAM0 4K

The system always boots at address 0x0. To ensure a maximum number of possibilities for boot, the memory layout can be configured with two parameters.

REMAP allows the user to lay out the first internal SRAM bank to 0x0 to ease development. This is done by software once the system has booted. Refer to the Bus Matrix Section for more details.

When REMAP = 0, BMS allows the user to lay out to 0x0, at his convenience, the ROM or an external memory. This is done via hardware at reset.

Note: Memory blocks not affected by these parameters can always be seen at their specified base addresses. See the complete memory map presented in Figure 8-1 on page 19.

The SAM9260 matrix manages a boot memory that depends on the level on the BMS pin at reset. The internal memory area mapped between address 0x0 and 0x000F FFFF is reserved for this purpose.

If BMS is detected at 1, the boot memory is the embedded ROM.

If BMS is detected at 0, the boot memory is the memory connected on the Chip Select 0 of the External Bus Interface.

8.1.1.1 BMS = 1, Boot on Embedded ROM

The system boots using the Boot Program.

- Boot on slow clock (On-chip RC or 32,768 Hz)
- Auto baudrate detection

- Downloads and runs an application from external storage media into internal SRAM
- Downloaded code size depends on embedded SRAM size
- Automatic detection of valid application
- Bootloader on a non-volatile memory
  - SPI DataFlash® connected on NPCS0 and NPCS1 of the SPI0
  - 8-bit and/or 16-bit NAND Flash
- SAM-BA® Monitor in case no valid program is detected in external NVM, supporting
  - Serial communication on a DBGU
  - USB Device Port

8.1.1.2 BMS = 0, Boot on External Memory

- Boot on slow clock (On-chip RC or 32,768 Hz)
- Boot with the default configuration for the Static Memory Controller, byte select mode, 16-bit data bus, Read/Write controlled by Chip Select, allows boot on 16-bit non-volatile memory.

The customer-programmed software must perform a complete configuration.

To speed up the boot sequence when booting at 32 kHz EBI CS0 (BMS=0), the user must take the following steps:

1. Program the PMC (main oscillator enable or bypass mode).
2. Program and start the PLL.
3. Reprogram the SMC setup, cycle, hold, mode timings registers for CS0 to adapt them to the new clock.
4. Switch the main clock to the new value.

8.2 External Memories

The external memories are accessed through the External Bus Interface. Each Chip Select line has a 256-Mbyte memory area assigned.

Refer to the memory map in Figure 8-1 on page 19.

8.2.1 External Bus Interface

- Integrates three External Memory Controllers
  - Static Memory Controller
  - SDRAM Controller
  - ECC Controller
- Additional logic for NAND Flash
- Full 32-bit External Data Bus
- Up to 26-bit Address Bus (up to 64MBytes linear)
- Up to 8 chip selects, Configurable Assignment:
  - Static Memory Controller on NCS0
  - SDRAM Controller or Static Memory Controller on NCS1
  - Static Memory Controller on NCS2
  - Static Memory Controller on NCS3, Optional NAND Flash support
  - Static Memory Controller on NCS4 - NCS5, Optional CompactFlash support
  - Static Memory Controller on NCS6-NCS7

8.2.2 Static Memory Controller

- 8-, 16- or 32-bit Data Bus
- Multiple Access Modes supported
  - Byte Write or Byte Select Lines

    - Asynchronous read in Page Mode supported (4- up to 32-byte page size)
- Multiple device adaptability
    - Compliant with LCD Module
    - Control signals programmable setup, pulse and hold time for each Memory Bank
- Multiple Wait State Management
    - Programmable Wait State Generation
    - External Wait Request
    - Programmable Data Float Time
- Slow Clock mode supported

8.2.3 SDRAM Controller

- Supported devices
    - Standard and Low-power SDRAM (Mobile SDRAM)
- Numerous configurations supported
    - 2K, 4K, 8K Row Address Memory Parts
    - SDRAM with two or four Internal Banks
    - SDRAM with 16- or 32-bit Datapath
- Programming facilities
    - Word, half-word, byte access
    - Automatic page break when Memory Boundary has been reached
    - Multibank Ping-pong Access
    - Timing parameters specified by software
    - Automatic refresh operation, refresh rate is programmable
- Energy-saving capabilities
    - Self-refresh, power down and deep power down modes supported
- Error detection
    - Refresh Error Interrupt
- SDRAM Power-up Initialization by software
- CAS Latency of 1, 2 and 3 supported
- Auto Precharge Command not used

8.2.4 Error Corrected Code Controller

- Tracking the accesses to a NAND Flash device by triggering on the corresponding chip select
- Single bit error correction and 2-bit Random detection
- Automatic Hamming Code Calculation while writing
    - ECC value available in a register
- Automatic Hamming Code Calculation while reading
    - Error Report, including error flag, correctable error flag and word address being detected erroneous
    - Support 8- or 16-bit NAND Flash devices with 512-, 1024-, 2048- or 4096-bytes pages

9. System Controller

The System Controller is a set of peripherals that allows handling of key elements of the system, such as power, resets, clocks, time, interrupts, watchdog, etc.

The System Controller User Interface also embeds the registers that configure the Matrix and a set of registers for the chip configuration. The chip configuration registers configure EBI chip select assignment and voltage range for external memories

The System Controller's peripherals are all mapped within the highest 16 Kbytes of address space, between addresses 0xFFFF E800 and 0xFFFF FFFF.

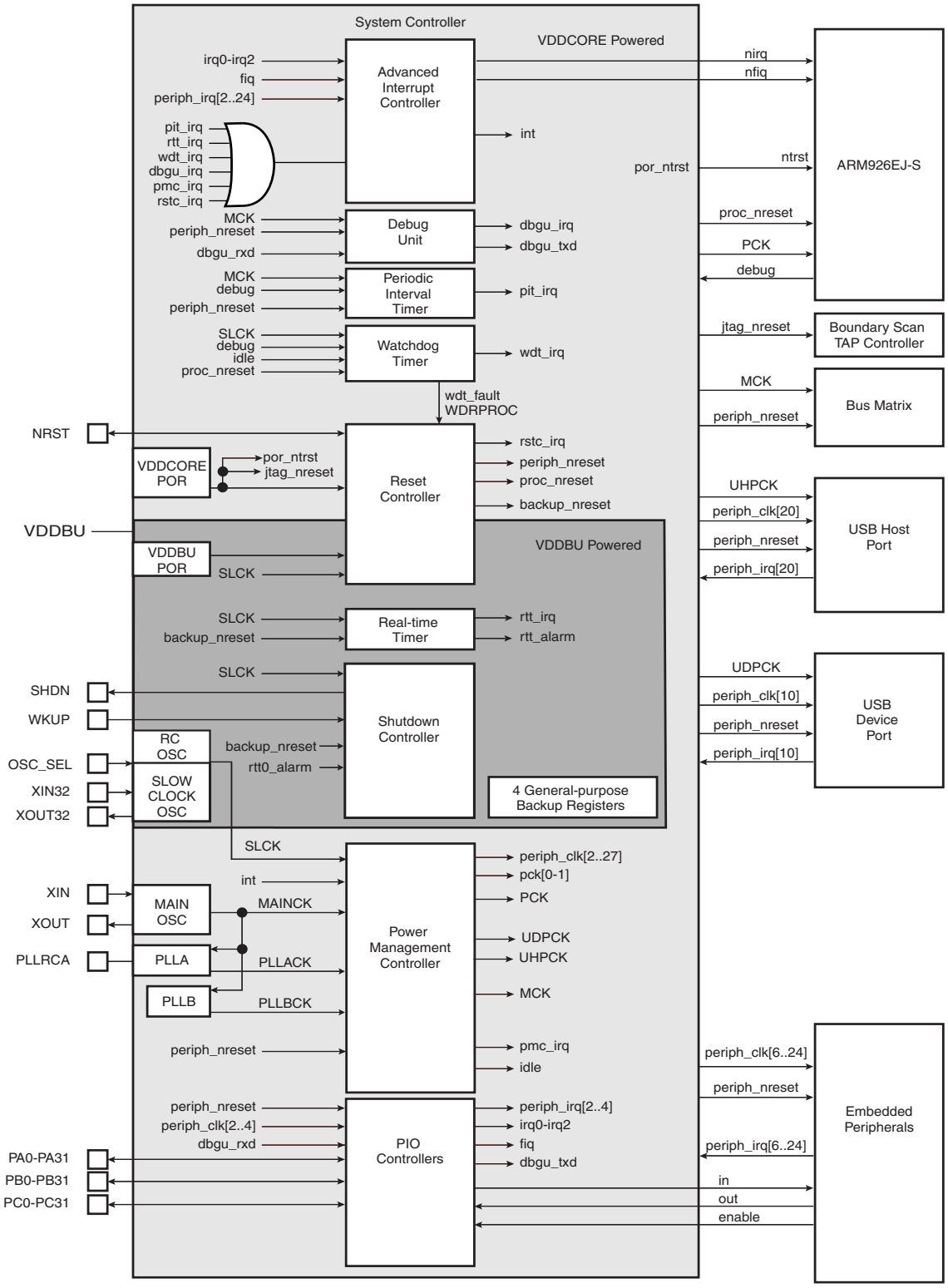
However, all the registers of System Controller are mapped on the top of the address space. All the registers of the System Controller can be addressed from a single pointer by using the standard ARM instruction set, as the Load/Store instruction has an indexing mode of ±4 Kbytes.

Figure 9-1 on page 24 shows the System Controller block diagram.

Figure 8-1 on page 19 shows the mapping of the User Interfaces of the System Controller peripherals.

9.1 System Controller Block Diagram

Figure 9-1. SAM9260 System Controller Block Diagram



9.2 Reset Controller

- Based on two Power-on-reset cells
  - One on VDDBU and one on VDDCORE
- Status of the last reset
  - Either general reset (VDDBU rising), wake-up reset (VDDCORE rising), software reset, user reset or watchdog reset
- Controls the internal resets and the NRST pin output
  - Allows shaping a reset signal for the external devices

9.3 Shutdown Controller

- Shutdown and Wake-up logic
  - Software programmable assertion of the SHDN pin
  - Deassertion Programmable on a WKUP pin level change or on alarm

9.4 Clock Generator

- Embeds a Low-power 32,768 Hz Slow Clock Oscillator and a Low-power RC oscillator selectable with OSCSEL signal
  - Provides the permanent Slow Clock SLCK to the system
- Embeds the Main Oscillator
  - Oscillator bypass feature
  - Supports 3 to 20 MHz crystals
- Embeds 2 PLLs
  - PLLA outputs 80 to 240 MHz clock
  - PLLB outputs 70 to 130 MHz clock
  - Both integrate an input divider to increase output accuracy
  - PLLB embeds its own filter