SAM9260

Atmel | SMART ARM-based Embedded MPU

DATASHEET

Description

The Atmel® | SMART SAM9260 eMPU is based on the integration of an ARM926EJ-S™ processor with fast ROM and RAM memories and a wide range of peripherals.

The SAM9260 embeds an Ethernet MAC, one USB Device Port, and a USB Host controller. It also integrates several standard peripherals, such as the USART, SPI, TWI, Timer Counters, Synchronous Serial Controller, ADC and MultiMedia Card Interface.

The SAM9260 is architectured on a 6-layer matrix, allowing a maximum internal bandwidth of six 32-bit buses. It also features an External Bus Interface capable of interfacing with a wide range of memory devices.

Features

- 180 MHz ARM926EJ-S™ ARM® Thumb® Processor
  - 8 Kbytes Data Cache, 8 Kbytes Instruction Cache, MMU
- Memories
  - 32-bit External Bus Interface supporting 4-bank SDRAM/LPSDR, Static Memories, CompactFlash, SLC NAND Flash with ECC
  - Two 4-Kbyte internal SRAM, single-cycle access at system speed
  - One 32-Kbyte internal ROM, embedding bootstrap routine
- Peripherals
  - ITU-R BT. 601/656 Image Sensor Interface (ISI)
  - USB Device and USB Host with dedicated On-Chip Transceiver
  - 10/100 Mbps Ethernet MAC Controller (EMAC)
  - One High Speed Memory Card Host
  - Two Master/Slave Serial Peripheral Interfaces (SPI)
  - Two 3-channel 32-bit Timer/Counters (TC)
  - One Synchronous Serial Controller (SSC)
  - One Two-wire Interface (TWI)
  - Four USARTs
  - Two UARTs
  - 4-channel 10-bit ADC
- System
  - 90 MHz six 32-bit layer AHB Bus Matrix
  - 22 Peripheral DMA Channels
  - Boot from NAND Flash, DataFlash or serial DataFlash
  - Reset Controller (RSTC) with On-Chip Power-on Reset
  - Selectable 32.768 kHz Low-Power and 3–20 MHz Main Oscillator
  - Internal Low-Power 32 kHz RC Oscillator
  - One PLL for the system and one PLL optimized for USB
  - Two Programmable External Clock Signals
  - Advanced Interrupt Controller (AIC)
  - Debug Unit (DBGU)
  - Periodic Interval Timer (PIT)
  - Watchdog Timer (WDT)
  - Real-time Timer (RTT)
- I/O
  - Three 32-bit Parallel Input/Output Controllers
  - 96 Programmable I/O Lines Multiplexed with up to Two Peripheral I/Os
- Package
  - 217-ball LFBGA – 15 x 15 x 1.4 mm, 0.8 mm pitch
  - 208-pin PQFP – 28 x 28 x 4.1 mm, 0.5 mm pitch

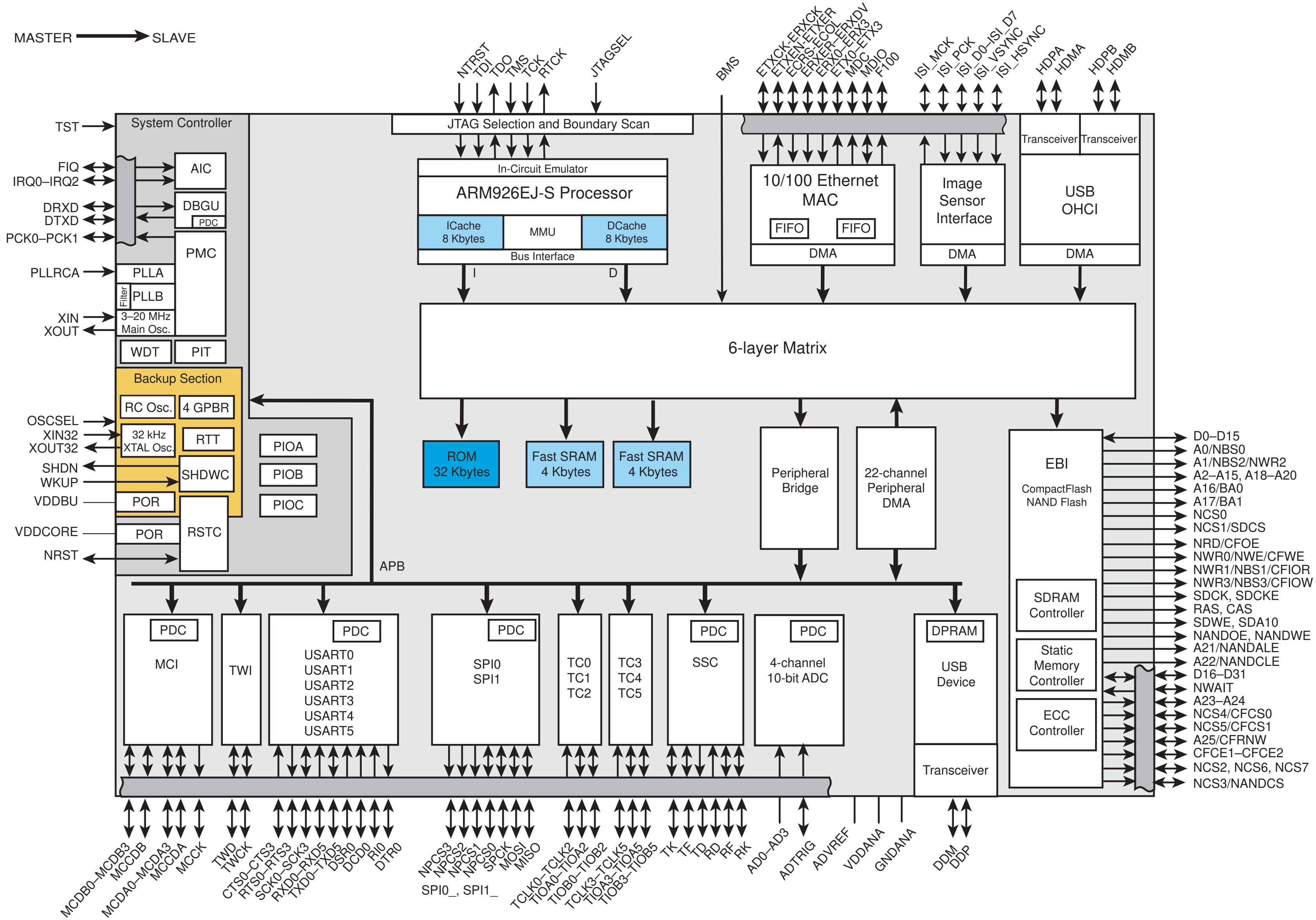
1. SAM9260 Block Diagram

Figure 1-1, "SAM9260 Block Diagram," on page 4 shows all the features for the 217-LFBGA package. Some functions are not accessible in the 208-pin PQFP package and the unavailable pins are highlighted in "Multiplexing on PIO Controller A" on page 29, "Multiplexing on PIO Controller B" on page 30, "Multiplexing on PIO Controller C" on page 31. The USB Host Port B is not available in the 208-pin package. Table 1-1 defines all the multiplexed and not multiplexed pins not available in the 208-PQFP package.

Table 1-1. Unavailable Signals in 208-lead PQFP Package

PIO	Peripheral A	Peripheral B
–	HDPB	–
–	HDMB	–
PA30	SCK2	RXD4
PA31	SCK0	TXD4
PB12	TXD5	ISI_D10
PB13	RXD5	ISI_D11
PC2	AD2	PCK1
PC3	AD3	SPI1_NPCS3
PC12	IRQ0	NCS7

Figure 1-1. SAM9260 Block Diagram



2. Signal Description

Table 2-1. Signal Description List

Signal Name	Function	Type	Active Level	Comments
Power Supplies				
VDDIOM	EBI I/O Lines Power Supply	Power		1.65–1.95 V or 3.0–3.6 V
VDDIOP0	Peripherals I/O Lines Power Supply	Power		3.0–3.6 V
VDDIOP1	Peripherals I/O Lines Power Supply	Power		1.65–3.6 V
VDDBU	Backup I/O Lines Power Supply	Power		1.65–1.95 V
VDDANA	Analog Power Supply	Power		3.0–3.6 V
VDDPLL	PLL Power Supply	Power		1.65–1.95 V
VDDCORE	Core Chip Power Supply	Power		1.65–1.95 V
GND	Ground	Ground		
GNDPLL	PLL and Oscillator Ground	Ground		
GNDANA	Analog Ground	Ground		
GNDBU	Backup Ground	Ground		
Clocks, Oscillators and PLLs				
XIN	Main Oscillator Input	Input		
XOUT	Main Oscillator Output	Output		
XIN32	Slow Clock Oscillator Input	Input		
XOUT32	Slow Clock Oscillator Output	Output		
OSCSEL	Slow Clock Oscillator Selection	Input		Accepts between 0V and VDDBU
PLLRCA	PLL A Filter	Input		
PCK0–PCK1	Programmable Clock Output	Output		
Shutdown, Wakeup Logic				
SHDN	Shutdown Control	Output		Driven at 0V only. Do not tie over VDDBU.
WKUP	Wake-up Input	Input		Accepts between 0V and VDDBU
ICE and JTAG				
NTRST	Test Reset Signal	Input	Low	Pull-up resistor
TCK	Test Clock	Input		No pull-up resistor
TDI	Test Data In	Input		No pull-up resistor
TDO	Test Data Out	Output		
TMS	Test Mode Select	Input		No pull-up resistor
JTAGSEL	JTAG Selection	Input		Pull-down resistor. Accepts between 0V and VDDBU.
RTCK	Return Test Clock	Output		

Table 2-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Comments
Reset/Test				
NRST	Microcontroller Reset	I/O	Low	Pull-up resistor
TST	Test Mode Select	Input		Pull-down resistor. Accepts between 0V and VDDBU.
BMS	Boot Mode Select	Input		No pull-up resistor BMS = 0 when tied to GND BMS = 1 when tied to VDDIOP0
Debug Unit - DBGU				
DRXD	Debug Receive Data	Input		
DTXD	Debug Transmit Data	Output		
Advanced Interrupt Controller - AIC				
IRQ0–IRQ2	External Interrupt Inputs	Input		
FIQ	Fast Interrupt Input	Input		
PIO Controller - PIOA / PIOB / PIOC				
PA0–PA31	Parallel IO Controller A	I/O		Pulled-up input at reset
PB0–PB31	Parallel IO Controller B	I/O		Pulled-up input at reset
PC0–PC31	Parallel IO Controller C	I/O		Pulled-up input at reset
External Bus Interface - EBI				
D0–D31	Data Bus	I/O		Pulled-up input at reset
A0–A25	Address Bus	Output		0 at reset
NWAIT	External Wait Signal	Input	Low	
Static Memory Controller - SMC				
NCS0–NCS7	Chip Select Lines	Output	Low	
NWR0–NWR3	Write Signal	Output	Low	
NRD	Read Signal	Output	Low	
NWE	Write Enable	Output	Low	
NBS0–NBS3	Byte Mask Signal	Output	Low	
CompactFlash Support				
CFCE1–CFCE2	CompactFlash Chip Enable	Output	Low	
CFOE	CompactFlash Output Enable	Output	Low	
CFWE	CompactFlash Write Enable	Output	Low	
CFIOR	CompactFlash IO Read	Output	Low	
CFIOW	CompactFlash IO Write	Output	Low	
CFRNW	CompactFlash Read Not Write	Output		
CFCS0–CFCS1	CompactFlash Chip Select Lines	Output	Low	

Table 2-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Comments
NAND Flash Support				
NANDCS	NAND Flash Chip Select	Output	Low	
NANDOE	NAND Flash Output Enable	Output	Low	
NANDWE	NAND Flash Write Enable	Output	Low	
NANDALE	NAND Flash Address Latch Enable	Output	Low	
NANDCLE	NAND Flash Command Latch Enable	Output	Low	
SDRAM Controller - SDRAMC				
SDCK	SDRAM Clock	Output		
SDCKE	SDRAM Clock Enable	Output	High	
SDCS	SDRAM Controller Chip Select	Output	Low	
BA0–BA1	Bank Select	Output		
SDWE	SDRAM Write Enable	Output	Low	
RAS–CAS	Row and Column Signal	Output	Low	
SDA10	SDRAM Address 10 Line	Output		
MultiMedia Card Interface - MCI				
MCCK	MultiMedia Card Clock	Output		
MCCDA	MultiMedia Card Slot A Command	I/O		
MCDA0–MCDA3	MultiMedia Card Slot A Data	I/O		
MCCDB	MultiMedia Card Slot B Command	I/O		
MCDB0–MCDB3	MultiMedia Card Slot B Data	I/O		
Universal Synchronous Asynchronous Receiver Transmitter - USARTx				
SCKx	USARTx Serial Clock	I/O		
TXDx	USARTx Transmit Data	I/O		
RXDx	USARTx Receive Data	Input		
RTSx	USARTx Request To Send	Output		
CTSx	USARTx Clear To Send	Input		
DTR0	USART0 Data Terminal Ready	Output		
DSR0	USART0 Data Set Ready	Input		
DCD0	USART0 Data Carrier Detect	Input		
RI0	USART0 Ring Indicator	Input		
Synchronous Serial Controller - SSC				
TD	SSC Transmit Data	Output		
RD	SSC Receive Data	Input		
TK	SSC Transmit Clock	I/O		
RK	SSC Receive Clock	I/O		
TF	SSC Transmit Frame Sync	I/O		
RF	SSC Receive Frame Sync	I/O		

Table 2-1. **Signal Description List (Continued)**

Signal Name	Function	Type	Active Level	Comments
Timer/Counter - TCx				
TCLKx	TC Channel x External Clock Input	Input		
TIOAx	TC Channel x I/O Line A	I/O		
TIOBx	TC Channel x I/O Line B	I/O		
Serial Peripheral Interface - SPIx_				
SPIx_MISO	Master In Slave Out	I/O		
SPIx_MOSI	Master Out Slave In	I/O		
SPIx_SPCK	SPI Serial Clock	I/O		
SPIx_NPCS0	SPI Peripheral Chip Select 0	I/O	Low	
SPIx_NPCS1–SPIx_NPCS3	SPI Peripheral Chip Select	Output	Low	
Two-wire Interface - TWI				
TWD	Two-wire Serial Data	I/O		
TWCK	Two-wire Serial Clock	I/O		
USB Host Port - UHP				
HDPA	USB Host Port A Data +	Analog		
HDMA	USB Host Port A Data -	Analog		
HDPB	USB Host Port B Data +	Analog		
HDMB	USB Host Port B Data +	Analog		
USB Device Port - UDP				
DDM	USB Device Port Data -	Analog		
DDP	USB Device Port Data +	Analog		
Ethernet 10/100 - EMAC				
ETXCK	Transmit Clock or Reference Clock	Input		MII only, REFCK in RMII
ERXCK	Receive Clock	Input		MII only
ETXEN	Transmit Enable	Output		
ETX0–ETX3	Transmit Data	Output		ETX0–ETX1 only in RMII
ETXER	Transmit Coding Error	Output		MII only
ERXDV	Receive Data Valid	Input		RXDV in MII, CRSDV in RMII
ERX0–ERX3	Receive Data	Input		ERX0–ERX1 only in RMII
ERXER	Receive Error	Input		
ECRS	Carrier Sense and Data Valid	Input		MII only
ECOL	Collision Detect	Input		MII only
EMDC	Management Data Clock	Output		
EMDIO	Management Data Input/Output	I/O		
EF100	Force 100 Mbit/s	Output	High	

Table 2-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Comments
Image Sensor Interface - ISI				
ISI_D0–ISI_D11	Image Sensor Data	Input		
ISI_MCK	Image Sensor Reference Clock	Output		
ISI_HSYNC	Image Sensor Horizontal Synchro	Input		
ISI_VSYNC	Image Sensor Vertical Synchro	Input		
ISI_PCK	Image Sensor Data clock	Input		
Analog-to-Digital Converter - ADC				
AD0–AD3	Analog Inputs	Analog		Digital pulled-up inputs at reset
ADVREF	Analog Positive Reference	Analog		
ADTRG	ADC Trigger	Input		

3. Package and Pinout

The SAM9260 is available in two Green-compliant packages:

- 208-pin PQFP (0.5 mm pitch)
- 217-ball LFBGA (0.8 mm ball pitch)

A detailed mechanical description and the orientation of the packages are given in Section 40. "SAM9260 Mechanical Characteristics".

3.1 208-pin PQFP Pinout

Table 3-1. Pinout for 208-pin PQFP Package

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
1	PA24	53	GND	105	RAS	157	ADVREF
2	PA25	54	DDM	106	D0	158	PC0
3	PA26	55	DDP	107	D1	159	PC1
4	PA27	56	PC13	108	D2	160	VDDANA
5	VDDIOP0	57	PC11	109	D3	161	PB10
6	GND	58	PC10	110	D4	162	PB11
7	PA28	59	PC14	111	D5	163	PB20
8	PA29	60	PC9	112	D6	164	PB21
9	PB0	61	PC8	113	GND	165	PB22
10	PB1	62	PC4	114	VDDIOM	166	PB23
11	PB2	63	PC6	115	SDCK	167	PB24
12	PB3	64	PC7	116	SDWE	168	PB25
13	VDDIOP0	65	VDDIOM	117	SDCKE	169	VDDIOP1
14	GND	66	GND	118	D7	170	GND
15	PB4	67	PC5	119	D8	171	PB26
16	PB5	68	NCS0	120	D9	172	PB27
17	PB6	69	CFOE/NRD	121	D10	173	GND
18	PB7	70	CFWE/NWE/NWR0	122	D11	174	VDDCORE
19	PB8	71	NANDOE	123	D12	175	PB28
20	PB9	72	NANDWE	124	D13	176	PB29
21	PB14	73	A22	125	D14	177	PB30
22	PB15	74	A21	126	D15	178	PB31
23	PB16	75	A20	127	PC15	179	PA0
24	VDDIOP0	76	A19	128	PC16	180	PA1
25	GND	77	VDDCORE	129	PC17	181	PA2
26	PB17	78	GND	130	PC18	182	PA3
27	PB18	79	A18	131	PC19	183	PA4
28	PB19	80	BA1/A17	132	VDDIOM	184	PA5
29	TDO	81	BA0/A16	133	GND	185	PA6

Table 3-1. Pinout for 208-pin PQFP Package (Continued)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
30	TDI	82	A15	134	PC20	186	PA7
31	TMS	83	A14	135	PC21	187	VDDIOP0
32	VDDIOP0	84	A13	136	PC22	188	GND
33	GND	85	A12	137	PC23	189	PA8
34	TCK	86	A11	138	PC24	190	PA9
35	NTRST	87	A10	139	PC25	191	PA10
36	NRST	88	A9	140	PC26	192	PA11
37	RTCK	89	A8	141	PC27	193	PA12
38	VDDCORE	90	VDDIOM	142	PC28	194	PA13
39	GND	91	GND	143	PC29	195	PA14
40	BMS	92	A7	144	PC30	196	PA15
41	OSCSEL	93	A6	145	PC31	197	PA16
42	TST	94	A5	146	GND	198	PA17
43	JTAGSEL	95	A4	147	VDDCORE	199	VDDIOP0
44	GNDBU	96	A3	148	VDDPLL	200	GND
45	XOUT32	97	A2	149	XIN	201	PA18
46	XIN32	98	NWR2/NBS2/A1	150	XOUT	202	PA19
47	VDDBU	99	NBS0/A0	151	GNDPLL	203	VDDCORE
48	WKUP	100	SDA10	152	NC	204	GND
49	SHDN	101	CFIOW/NBS3/NWR3	153	GNDPLL	205	PA20
50	HDMA	102	CFIOR/NBS1/NWR1	154	PLLRCA	206	PA21
51	HDPA	103	SDCS/NCS1	155	VDDPLL	207	PA22
52	VDDIOP0	104	CAS	156	GNDANA	208	PA23

3.2 217-ball LFBGA Package

A detailed mechanical description and the orientation of the 217-ball LFBGA package is given in Section 40. "SAM9260 Mechanical Characteristics".

3.3 217-ball LFBGA Pinout

Table 3-2. Pinout for 217-ball LFBGA Package

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	CFIOW/NBS3/NWR3	D5	A5	J14	TDO	P17	PB5
A2	NBS0/A0	D6	GND	J15	PB19	R1	NC
A3	NWR2/NBS2/A1	D7	A10	J16	TDI	R2	GNDANA
A4	A6	D8	GND	J17	PB16	R3	PC29
A5	A8	D9	VDDCORE	K1	PC24	R4	VDDANA
A6	A11	D10	GND	K2	PC20	R5	PB12
A7	A13	D11	VDDIOM	K3	D15	R6	PB23
A8	BA0/A16	D12	GND	K4	PC21	R7	GND
A9	A18	D13	DDM	K8	GND	R8	PB26
A10	A21	D14	HDPB	K9	GND	R9	PB28
A11	A22	D15	NC	K10	GND	R10	PA0
A12	CFWE/NWE/NWR0	D16	VDDBU	K14	PB4	R11	PA4
A13	CFOE/NRD	D17	XIN32	K15	PB17	R12	PA5
A14	NCS0	E1	D10	K16	GND	R13	PA10
A15	PC5	E2	D5	K17	PB15	R14	PA21
A16	PC6	E3	D3	L1	GND	R15	PA23
A17	PC4	E4	D4	L2	PC26	R16	PA24
B1	SDCK	E14	HDPA	L3	PC25	R17	PA29
B2	CFIOR/NBS1/NWR1	E15	HDMA	L4	VDDIOP0	T1	PLLRCA
B3	SDCS/NCS1	E16	GNDBU	L14	PA28	T2	GNDPLL
B4	SDA10	E17	XOUT32	L15	PB9	T3	PC0
B5	A3	F1	D13	L16	PB8	T4	PC1
B6	A7	F2	SDWE	L17	PB14	T5	PB10
B7	A12	F3	D6	M1	VDDCORE	T6	PB22
B8	A15	F4	GND	M2	PC31	T7	GND
B9	A20	F14	OSCSEL	M3	GND	T8	PB29
B10	NANDWE	F15	BMS	M4	PC22	T9	PA2
B11	PC7	F16	JTAGSEL	M14	PB1	T10	PA6
B12	PC10	F17	TST	M15	PB2	T11	PA8
B13	PC13	G1	PC15	M16	PB3	T12	PA11
B14	PC11	G2	D7	M17	PB7	T13	VDDCORE
B15	PC14	G3	SDCKE	N1	XIN	T14	PA20

Table 3-2. Pinout for 217-ball LFBGA Package (Continued)

Pin	Signal Name
B16	PC8
B17	WKUP
C1	D8
C2	D1
C3	CAS
C4	A2
C5	A4
C6	A9
C7	A14
C8	BA1/A17
C9	A19
C10	NANDOE
C11	PC9
C12	PC12
C13	DDP
C14	HDMB
C15	NC
C16	VDDIOP0
C17	SHDN
D1	D9
D2	D2
D3	RAS
D4	D0

Pin	Signal Name
G4	VDDIOM
G14	GND
G15	NRST
G16	RTCK
G17	TMS
H1	PC18
H2	D14
H3	D12
H4	D11
H8	GND
H9	GND
H10	GND
H14	VDDCORE
H15	TCK
H16	NTRST
H17	PB18
J1	PC19
J2	PC17
J3	VDDIOM
J4	PC16
J8	GND
J9	GND
J10	GND

Pin	Signal Name
N2	VDDPLL
N3	PC23
N4	PC27
N14	PA31
N15	PA30
N16	PB0
N17	PB6
P1	XOUT
P2	VDDPLL
P3	PC30
P4	PC28
P5	PB11
P6	PB13
P7	PB24
P8	VDDIOP1
P9	PB30
P10	PB31
P11	PA1
P12	PA3
P13	PA7
P14	PA9
P15	PA26
P16	PA25

Pin	Signal Name
T15	GND
T16	PA22
T17	PA27
U1	GNDPLL
U2	ADVREF
U3	PC2
U4	PC3
U5	PB20
U6	PB21
U7	PB25
U8	PB27
U9	PA12
U10	PA13
U11	PA14
U12	PA15
U13	PA19
U14	PA17
U15	PA16
U16	PA18
U17	VDDIOP0

4. Power Considerations

4.1 Power Supplies

The SAM9260 devices have several types of power supply pins. Some supply pins share common ground (GND) pins whereas others have separate grounds. See Table 4-1.

Table 4-1. SAM9260 Power Supply Pins

Pin(s)	Item(s) powered	Range	Typical	Ground
VDDCORE	Core, including the processor Embedded memories Peripherals	1.65–1.95 V	1.8V	GND
VDDIOM	External Bus Interface I/O lines	1.65–1.95 V[1]	1.8V	GND
		3.0–3.6 V[1]	3.3V	GND
VDDIOP0	Peripheral I/O lines USB transceivers	3.0–3.6 V	3.3V	GND
VDDIOP1	Peripherals I/O lines involving the Image Sensor Interface	1.65–3.6 V	1.8V 2.5V 3.3V	GND
VDDBU	Slow Clock oscillator Part of the System Controller	1.65–1.95 V	1.8V	GNDBU
VDDPLL	Main oscillator PLL cells	1.65–1.95 V	1.8V	GNDPLL
VDDANA	Analog-to-Digital Converter	3.0–3.6 V	3.3V	GNDANA

Note: 1. Desired voltage range selectable by software

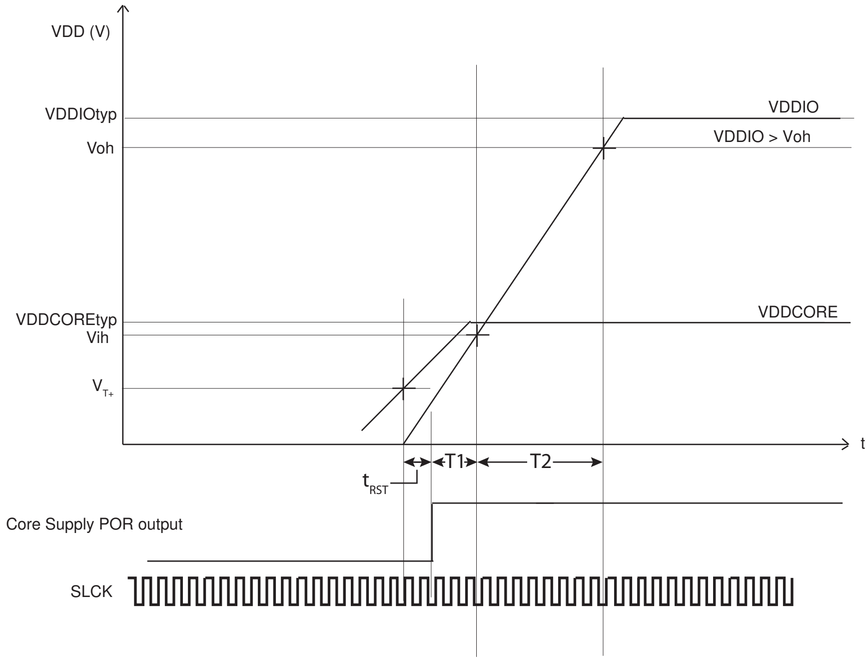
The power supplies VDDIOM, VDDIOP0 and VDDIOP1 are identified in the pinout table and the multiplexing tables. These supplies enable the user to power the device differently for interfacing with memories and for interfacing with peripherals.

4.2 Power Sequence Requirements

The SAM9260 board design must comply with the guidelines described in Section 4.2.1 “Power-up Sequence” and Section 4.2.2 “Power-down Sequence” to guarantee reliable operation of the device. Any deviation from these sequences may lead to preventing the device from booting.

4.2.1 Power-up Sequence

Figure 4-1. V_{DDCORE} and V_{VDDIO} Constraints at Startup



VDDCORE and VDDBU are controlled by internal POR (Power On Reset) to guarantee that these power sources reach their target values prior to the release of POR.

4.2.1.1 VDDBU is Continuously Powered (used with a battery)

- VDDIOM, VDDIOP0 and VDDIOP1 must NOT be powered until VDDCORE has reached a level superior to V_{T+}.
- VDDIOP0 must be ≥ V_{IH} (refer to Table 39-2 “DC Characteristics” for more details) within (t_{RST} + T1) after VDDCORE reached V_{T+}.
- VDDIOM must reach V_{OH} (refer to Table 39-2 “DC Characteristics” for more details) within (t_{RST} + T1 + T2) after VDDCORE has reached V_{T+}.
  - t_{RST} is a POR characteristic
  - $T1 = 3 \times t_{SLCK}$
  - $T2 = 16 \times t_{SLCK}$

The t_{SLCK} min (22 µs) is obtained for the maximum frequency of the internal RC oscillator (44 kHz).

  - t_{RST} = 100 µs
  - T1 = 66 µs
  - T2 = 352 µs

4.2.1.2 VDDBU is not Continuously Powered (no backup features used)

If VDDBU is not used with a battery, the power sequence can be less constrained. The user can power VDDCORE, then VDDIOM, VDDIOP0 and VDDIOP1, with VDDBU following last in the sequence, thus ensuring that BMS is correctly sampled.

4.2.2 Power-down Sequence

Switch-off the VDDIOM, VDDIOP0 and VDDIOP1 power supply prior to or at the same time as VDDCORE.

No power-up or power-down restrictions apply to VDDBU, VDDPLL and VDDANA.

4.3 Programmable I/O Lines Power Supplies

The power supplies pins VDDIOM accept two voltage ranges. This allows the device to reach its maximum speed either out of 1.8V or 3.3V external memories.

The voltage ranges are determined by programming registers in the Chip Configuration registers located in Section 17.6 “Bus Matrix User Interface”.

At reset, the selected voltage defaults to 3.3V nominal, and power supply pins can accept either 1.8V or 3.3V. The device cannot reach its maximum speed if the voltage supplied to the pins is 1.8V only. The user must program the EBI voltage range before getting the device out of its Slow Clock Mode.

5. I/O Line Considerations

5.1 JTAG Port Pins

TMS, TDI and TCK are Schmitt trigger inputs and have no pull-up resistors.

TDO and RTCK are outputs, driven at up to VDDIOP0, and have no pull-up resistors.

The JTAGSEL pin is used to select the JTAG boundary scan when asserted at a high level (tied to VDDBU). It integrates a permanent pull-down resistor of about 15 kΩ to GNDBU, so that it can be left unconnected for normal operations.

The NTRST signal is described in Section 5.3.

All the JTAG signals are supplied with VDDIOP0.

5.2 Test Pin

The TST pin is used for manufacturing test purposes when asserted high. It integrates a permanent pull-down resistor of about 15 kΩ to GNDBU, so that it can be left unconnected for normal operations. Driving this line at a high level leads to unpredictable results.

This pin is supplied with VDDBU.

5.3 Reset Pins

NRST is a bidirectional with an open-drain output integrating a non-programmable pull-up resistor. It can be driven with voltage at up to VDDIOP0.

NTRST is an input which allows reset of the JTAG Test Access port. It has no action on the processor.

As the product integrates power-on reset cells, which manages the processor and the JTAG reset, the NRST and NTRST pins can be left unconnected.

The NRST and NTRST pins both integrate a permanent pull-up resistor to VDDIOP0. Its value can be found in Table 39-2 “DC Characteristics”.

The NRST signal is inserted in the Boundary Scan.

5.4 PIO Controllers

All the I/O lines managed by the PIO Controllers integrate a programmable pull-up resistor. Refer to Section 39.2 “DC Characteristics” for more information. Programming of this pull-up resistor is performed independently for each I/O line through the PIO Controllers.

After reset, all the I/O lines default as inputs with pull-up resistors enabled, except those which are multiplexed with the External Bus Interface signals and that must be enabled as Peripheral at reset. This is explicitly indicated in the column “Reset State” of the PIO Controller multiplexing tables.

5.5 I/O Line Drive Levels

The PIO lines are high-drive current capable. Each of these I/O lines can drive up to 16 mA permanently except PC4 to PC31 that are VDDIOM powered.

5.6 Shutdown Logic Pins

The SHDN pin is a tri-state output pin, which is driven by the Shutdown Controller. There is no internal pull-up. An external pull-up tied to VDDBU is needed and its value must be higher than 1 MΩ. The resistor value is calculated according to the regulator enable implementation and the SHDN level.

The pin WKUP is an input-only. It can accept voltages only between 0V and VDDBU.

5.7 Slow Clock Selection

The SAM9260 slow clock can be generated either by an external 32.768 kHz crystal or the on-chip RC oscillator. Table 5-1 defines the states for OSCSEL signal.

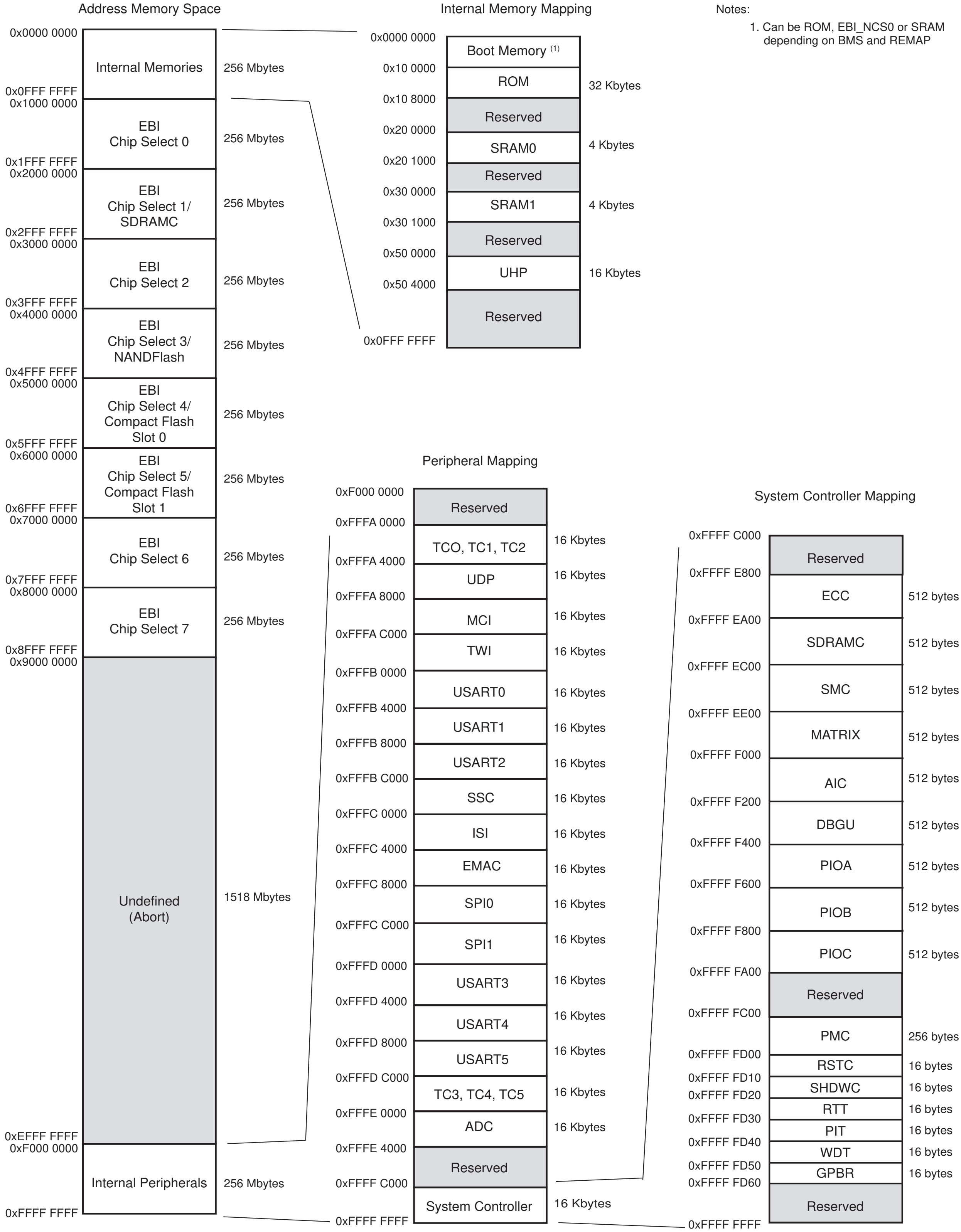
Table 5-1. Slow Clock Selection

OSCSEL	Slow Clock	Startup Time
0	Internal RC	240 µs
1	External 32.768 kHz	1200 ms

The startup counter delay for the slow clock oscillator depends on the OSCSEL signal. The 32.768 kHz startup delay is 1200 ms whereas it is 240 µs for the internal RC oscillator (refer to Table 5-1). The pin OSCSEL must be tied either to GND or VDDBU for correct operation of the device.

6. Memories

Figure 6-1. SAM9260 Memory Mapping



A first level of address decoding is performed by the Bus Matrix, i.e., the implementation of the Advanced High Performance Bus (AHB) for its Master and Slave interfaces with additional features.

Decoding breaks up the 4 Gbytes of address space into 16 banks of 256 Mbytes. The banks 1 to 7 are directed to the EBI that associates these banks to the external chip selects EBI_NCS0 to EBI_NCS7. Bank 0 is reserved for the addressing of the internal memories, and a second level of decoding provides 1 Mbyte of internal memory area. Bank 15 is reserved for the peripherals and provides access to the Advanced Peripheral Bus (APB).

Other areas are unused and performing an access within them provides an abort to the master requesting such an access.

Each Master has its own bus and its own decoder, thus allowing a different memory mapping per Master. However, in order to simplify the mappings, all the masters have a similar address decoding.

Regarding Master 0 and Master 1 (ARM926™ Instruction and Data), three different Slaves are assigned to the memory space decoded at address 0x0: one for internal boot, one for external boot, one after remap. Refer to Table 6-1 "Internal Memory Mapping" for details.

A complete memory map is presented in Figure 6-1 on page 19.

6.1 Embedded Memories

- 32 KB ROM
  - Single Cycle Access at full matrix speed
- Two 4 KB Fast SRAM
  - Single Cycle Access at full matrix speed

6.1.1 Boot Strategies

Table 6-1 summarizes the Internal Memory Mapping for each Master, depending on the Remap status and the BMS state at reset.

Table 6-1. Internal Memory Mapping

Address	REMAP = 0		REMAP = 1
	BMS = 1	BMS = 0	
0x0000 0000	ROM	EBI_NCS0	SRAM0 4K

The system always boots at address 0x0. To ensure a maximum number of possibilities for boot, the memory layout can be configured with two parameters. After reset, the ROM is mapped at both addresses 0x0000_0000 and 0x0010_0000.

REMAP allows the user to lay out the first internal SRAM bank to 0x0 to ease development. This is done by software once the system has booted. Refer to Section 17. "SAM9260 Bus Matrix" for more details.

When REMAP = 0, BMS allows the user to lay out to 0x0, at his convenience, the ROM or an external memory. This is done via hardware at reset.

Note: Memory blocks not affected by these parameters can always be seen at their specified base addresses. See the complete memory map presented in Figure 6-1 on page 19.

The SAM9260 matrix manages a boot memory that depends on the level on the BMS pin at reset. The internal memory area mapped between address 0x0 and 0x000F FFFF is reserved for this purpose.

If BMS is detected at 1, the boot memory is the embedded ROM.

If BMS is detected at 0, the boot memory is the memory connected on the Chip Select 0 of the External Bus Interface.

6.1.1.1 BMS = 1, Boot on Embedded ROM

The system boots using the Boot Program.

- Boot on slow clock (on-chip RC or 32.768 kHz)
- Auto baudrate detection
- Downloads and runs an application from external storage media into internal SRAM
- Downloaded code size depends on embedded SRAM size
- Automatic detection of valid application
- Bootloader on a non-volatile memory
  - SPI DataFlash connected on NPCS0 and NPCS1 of the SPI0
  - 8-bit and/or 16-bit NAND Flash
- SAM-BA® Monitor in case no valid program is detected in external NVM, supporting
  - Serial communication on a DBGU
  - USB Device Port

6.1.1.2 BMS = 0, Boot on External Memory

- Boot on slow clock (on-chip RC or 32.768 kHz)
- Boot with the default configuration for the Static Memory Controller, byte select mode, 16-bit data bus, Read/Write controlled by Chip Select, allows boot on 16-bit non-volatile memory.

The customer-programmed software must perform a complete configuration.

To speed up the boot sequence when booting at 32 kHz EBI CS0 (BMS = 0), the user must take the following steps:

1. Program the PMC (main oscillator enable or bypass mode).
2. Program and start the PLL.
3. Reprogram the SMC setup, cycle, hold, mode timings registers for CS0 to adapt them to the new clock.
4. Switch the main clock to the new value.

6.2 External Memories

The external memories are accessed through the External Bus Interface. Each Chip Select line has a 256-Mbyte memory area assigned. Refer to Figure 6-1, “SAM9260 Memory Mapping,” on page 19.

6.2.1 External Bus Interface

- Integrates three External Memory Controllers
  - Static Memory Controller
  - SDRAM Controller
  - ECC Controller
- Additional logic for NAND Flash
- Full 32-bit External Data Bus
- Up to 26-bit Address Bus (up to 64 Mbytes linear)
- Up to 8 chip selects, Configurable Assignment:
  - Static Memory Controller on NCS0
  - SDRAM Controller or Static Memory Controller on NCS1
  - Static Memory Controller on NCS2
  - Static Memory Controller on NCS3, Optional NAND Flash support
  - Static Memory Controller on NCS4–NCS5, Optional CompactFlash support
  - Static Memory Controller on NCS6–NCS7

6.2.2 Static Memory Controller

- 8-, 16- or 32-bit Data Bus
- Multiple Access Modes supported
  - Byte Write or Byte Select Lines
  - Asynchronous read in Page Mode supported (4- up to 32-byte page size)
- Multiple device adaptability
  - Compliant with LCD Module
  - Control signals programmable setup, pulse and hold time for each Memory Bank
- Multiple Wait State Management
  - Programmable Wait State Generation
  - External Wait Request
  - Programmable Data Float Time
- Slow Clock mode supported

6.2.3 SDRAM Controller

- Supported devices
  - Standard and Low-power SDRAM (Mobile SDRAM)
- Numerous configurations supported
  - 2K, 4K, 8K Row Address Memory Parts
  - SDRAM with two or four Internal Banks
  - SDRAM with 16- or 32-bit Datapath
- Programming facilities
  - Word, half-word, byte access
  - Automatic page break when Memory Boundary has been reached
  - Multibank Ping-pong Access
  - Timing parameters specified by software
  - Automatic refresh operation, refresh rate is programmable
- Energy-saving capabilities
  - Self-refresh, power down and deep power down modes supported
- Error detection
  - Refresh Error Interrupt
- SDRAM Power-up Initialization by software
- CAS Latency of 1, 2 and 3 supported
- Auto Precharge Command not used

6.2.4 Error Correction Code Controller

- Tracking the accesses to a NAND Flash device by trigging on the corresponding chip select
- Single bit error correction and 2-bit Random detection
- Automatic Hamming Code Calculation while writing
  - ECC value available in a register
- Automatic Hamming Code Calculation while reading
  - Error Report, including error flag, correctable error flag and word address being detected erroneous
  - Support 8- or 16-bit NAND Flash devices with 512-, 1024-, 2048- or 4096-bytes pages

7. System Controller

The System Controller is a set of peripherals that allows handling of key elements of the system, such as power, resets, clocks, time, interrupts, watchdog, etc.

The System Controller User Interface also embeds the registers that configure the Matrix and a set of registers for the chip configuration. The chip configuration registers configure EBI chip select assignment and voltage range for external memories

The System Controller's peripherals are all mapped within the highest 16 Kbytes of address space, between addresses 0xFFFF E800 and 0xFFFF FFFF.

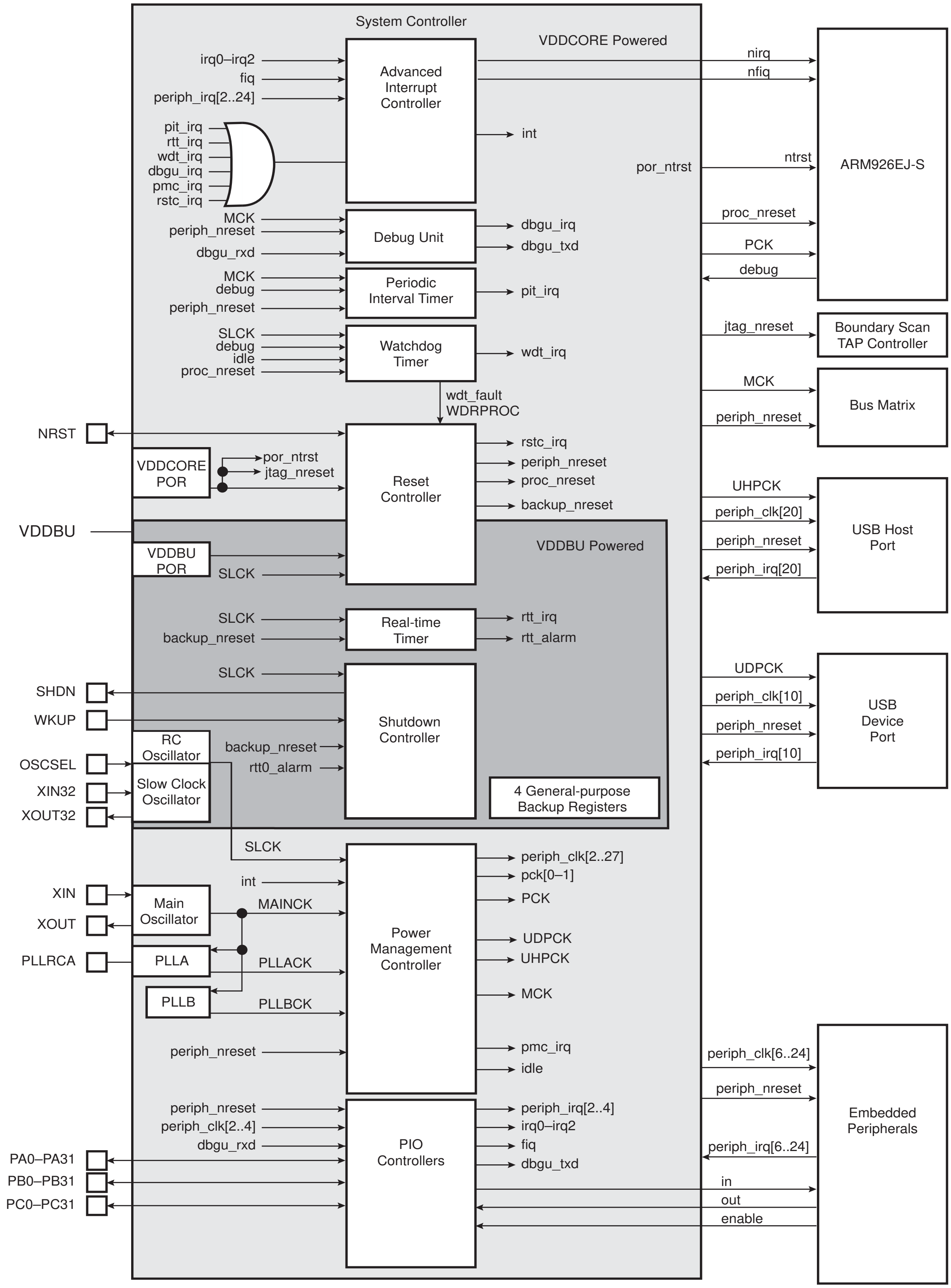
However, all the registers of System Controller are mapped on the top of the address space. All the registers of the System Controller can be addressed from a single pointer by using the standard ARM instruction set, as the Load/Store instruction has an indexing mode of ±4 Kbytes.

Figure 7-1 on page 24 shows the System Controller block diagram.

Figure 6-1 on page 19 shows the mapping of the User Interfaces of the System Controller peripherals.

7.1 System Controller Block Diagram

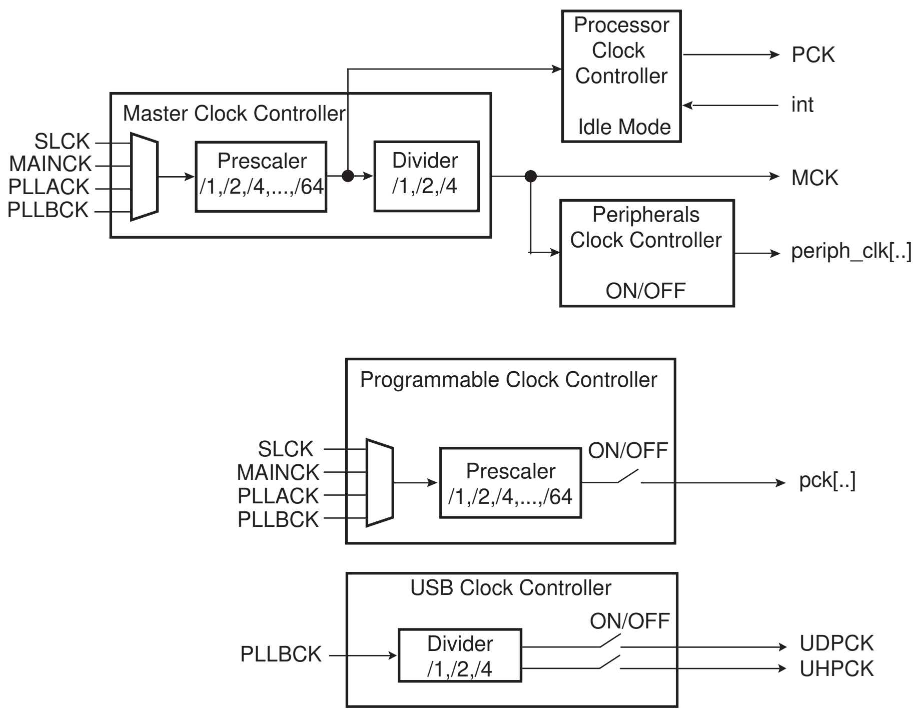
Figure 7-1. SAM9260 System Controller Block Diagram



7.2 Power Management Controller

- Provides:
  – Processor Clock PCK
  – Master Clock MCK, in particular to the Matrix and the memory interfaces
  – USB Device Clock UDPCK
  – independent peripheral clocks, typically at the frequency of MCK
  – 2 programmable clock outputs: PCK0, PCK1
- Five flexible operating modes:
  – Normal Mode, processor and peripherals running at a programmable frequency
  – Idle Mode, processor stopped waiting for an interrupt
  – Slow Clock Mode, processor and peripherals running at low frequency
  – Standby Mode, mix of Idle and Backup Mode, peripheral running at low frequency, processor stopped waiting for an interrupt
  – Backup Mode, Main Power Supplies off, VDDBU powered by a battery

Figure 7-2. SAM9260 Power Management Controller Block Diagram



7.3 General-purpose Backup Registers

- Four 32-bit general-purpose backup registers

7.4 Chip Identification

- Chip ID: 0x019803A2
- JTAG ID: 0x05B1303F
- ARM926 TAP ID: 0x0792603F