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Features

- Incorporates the ARM926EJ-S™ ARM® Thumb® Processor
  - DSP Instruction Extensions
  - ARM Jazelle® Technology for Java® Acceleration
  - 16 Kbyte Data Cache, 16 Kbyte Instruction Cache, Write Buffer
  - 210 MIPS at 190 MHz
  - Memory Management Unit
  - EmbeddedICE™, Debug Communication Channel Support
  - Mid-level implementation Embedded Trace Macrocell™
- Additional Embedded Memories
  - 32 Kbytes of Internal ROM, Single-cycle Access at Maximum Bus Speed
  - 160 Kbytes of Internal SRAM, Single-cycle Access at Maximum Processor or Bus Speed
- External Bus Interface (EBI)
  - Supports SDRAM, Static Memory, NAND Flash and CompactFlash®
- LCD Controller
  - Supports Passive or Active Displays
  - Up to 16-bits per Pixel in STN Color Mode
  - Up to 16M Colors in TFT Mode (24-bit per Pixel), Resolution up to 2048 x 2048
- USB
  - USB 2.0 Full Speed (12 Mbits per second) Host Double Port
    - Dual On-chip Transceivers
    - Integrated FIFOs and Dedicated DMA Channels
  - USB 2.0 Full Speed (12 Mbits per second) Device Port
    - On-chip Transceiver, 2 Kbyte Configurable Integrated FIFOs
- Bus Matrix
  - Handles Five Masters and Five Slaves
  - Boot Mode Select Option
  - Remap Command
- Fully Featured System Controller (SYSC) for Efficient System Management, including
  - Reset Controller, Shutdown Controller, Four 32-bit Battery Backup Registers for a Total of 16 Bytes
  - Clock Generator and Power Management Controller
  - Advanced Interrupt Controller and Debug Unit
  - Periodic Interval Timer, Watchdog Timer and Real-time Timer
  - Three 32-bit PIO Controllers
- Reset Controller (RSTC)
  - Based on Power-on Reset Cells, Reset Source Identification and Reset Output Control
- Shutdown Controller (SHDWC)
  - Programmable Shutdown Pin Control and Wake-up Circuitry
- Clock Generator (CKGR)
  - 32,768 Hz Low-power Oscillator on Battery Backup Power Supply, Providing a Permanent Slow Clock
  - 3 to 20 MHz On-chip Oscillator and two PLLs
- Power Management Controller (PMC)
  - Very Slow Clock Operating Mode, Software Programmable Power Optimization Capabilities
  - Four Programmable External Clock Signals

AT91 ARM Thumb-based Microcontrollers

AT91SAM9261

Preliminary

Summary

NOTE: This is a summary document. The complete document is available on the Atmel website at www.atmel.com.

6062LS–ATARM–23-Mar-09

- Advanced Interrupt Controller (AIC)
  - Individually Maskable, Eight-level Priority, Vectored Interrupt Sources
  - Three External Interrupt Sources and One Fast Interrupt Source, Spurious Interrupt Protected
- Debug Unit (DBGU)
  - 2-wire USART and support for Debug Communication Channel, Programmable ICE Access Prevention
  - Mode for General Purpose Two-wire UART Serial Communication
- Periodic Interval Timer (PIT)
  - 20-bit Interval Timer plus 12-bit Interval Counter
- Watchdog Timer (WDT)
  - Key Protected, Programmable Only Once, Windowed 12-bit Counter, Running at Slow Clock
- Real-Time Timer (RTT)
  - 32-bit Free-running Backup Counter Running at Slow Clock
- Three 32-bit Parallel Input/Output Controllers (PIO) PIOA, PIOB and PIOC
  - 96 Programmable I/O Lines Multiplexed with up to Two Peripheral I/Os
  - Input Change Interrupt Capability on Each I/O Line
  - Individually Programmable Open-drain, Pull-up Resistor and Synchronous Output
- Nineteen Peripheral DMA (PDC) Channels
- Multimedia Card Interface (MCI)
  - SDCard and MultiMediaCard™ Compliant
  - Automatic Protocol Control and Fast Automatic Data Transfers with PDC, MMC and SDCard Compliant
- Three Synchronous Serial Controllers (SSC)
  - Independent Clock and Frame Sync Signals for Each Receiver and Transmitter
  - I²S Analog Interface Support, Time Division Multiplex Support
  - High-speed Continuous Data Stream Capabilities with 32-bit Data Transfer
- Three Universal Synchronous/Asynchronous Receiver Transmitters (USART)
  - Individual Baud Rate Generator, IrDA® Infrared Modulation/Demodulation
  - Support for ISO7816 T0/T1 Smart Card, Hardware and Software Handshaking, RS485 Support
- Two Master/Slave Serial Peripheral Interface (SPI)
  - 8- to 16-bit Programmable Data Length, Four External Peripheral Chip Selects
- One Three-channel 16-bit Timer/Counters (TC)
  - Three External Clock Inputs, Two multi-purpose I/O Pins per Channel
  - Double PWM Generation, Capture/Waveform Mode, Up/Down Capability
- Two-wire Interface (TWI)
  - Master Mode Support, All Two-wire Atmel EEPROMs Supported
- IEEE® 1149.1 JTAG Boundary Scan on All Digital Pins
- Required Power Supplies:
  - 1.08V to 1.32V for VDDCORE and VDDBU
  - 3.0V to 3.6V for VDDOSC and for VDDPLL
  - 2.7V to 3.6V for VDDIOP (Peripheral I/Os)
  - 1.65V to 1.95V and 3.0V to 3.6V for VDDIOM (Memory I/Os)
- Available in a 217-ball LFBGA RoHS-compliant Package

1. Description

The AT91SAM9261 is a complete system-on-chip built around the ARM926EJ-S ARM Thumb processor with an extended DSP instruction set and Jazelle Java accelerator. It achieves 210 MIPS at 190 MHz.

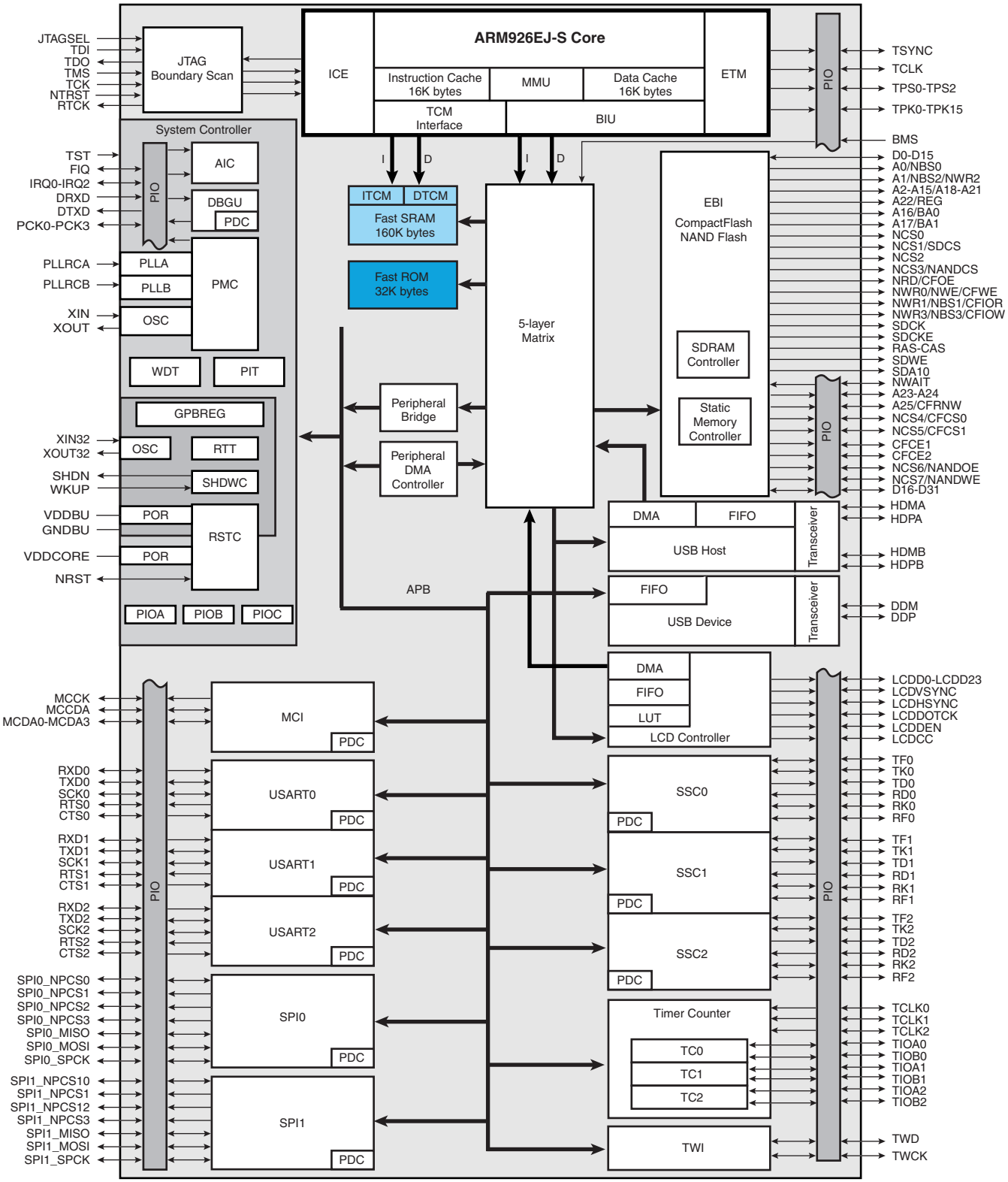
The AT91SAM9261 is an optimized host processor for applications with an LCD display. Its integrated LCD controller supports BW and up to 16M color, active and passive LCD displays. The 160 Kbyte integrated SRAM can be configured as a frame buffer minimizing the impact for LCD refresh on the overall processor performance. The External Bus Interface incorporates controllers for synchronous DRAM (SDRAM) and Static memories and features specific interface circuitry for CompactFlash and NAND Flash.

The AT91SAM9261 integrates a ROM-based Boot Loader supporting code shadowing from, for example, external DataFlash® into external SDRAM. The software controlled Power Management Controller (PMC) keeps system power consumption to a minimum by selectively enabling/disabling the processor and various peripherals and adjustment of the operating frequency.

The AT91SAM9261 also benefits from the integration of a wide range of debug features including JTAG-ICE, a dedicated UART debug channel (DBGU) and an embedded real time trace. This enables the development and debug of all applications, especially those with real-time constraints.

2. Block Diagram

Figure 2-1. AT91SAM9261 Block Diagram



3. Signal Description

Table 3-1. Signal Description by Peripheral

Signal Name	Function	Type	Active Level	Comments
Power				
VDDIOM	EBI I/O Lines Power Supply	Power		1.65 V to 1.95V and 3.0V to 3.6V
VDDIOP	Peripherals I/O Lines Power Supply	Power		2.7V to 3.6V
VDDBU	Backup I/O Lines Power Supply	Power		1.08V to 1.32V
VDDPLL	PLL Power Supply	Power		3.0V to 3.6V
VDDOSC	Oscillator Power Supply	Power		3.0V to 3.6V
VDDCORE	Core Chip Power Supply	Power		1.08V to 1.32V
GND	Ground	Ground		
GNDPLL	PLL Ground	Ground		
GNDOSC	Oscillator Ground	Ground		
GNDBU	Backup Ground	Ground		
Clocks, Oscillators and PLLs				
XIN	Main Oscillator Input	Input		
XOUT	Main Oscillator Output	Output		
XIN32	Slow Clock Oscillator Input	Input		
XOUT32	Slow Clock Oscillator Output	Output		
PLLRCA	PLL Filter	Input		
PLLRCB	PLL Filter	Input		
PCK0 - PCK3	Programmable Clock Output	Output		
Shutdown, Wakeup Logic				
SHDN	Shutdown Control	Output		Do not tie over VDDBU.
WKUP	Wake-Up Input	Input		Accepts between 0V and VDDBU.
ICE and JTAG				
TCK	Test Clock	Input		No pull-up resistor.
RTCK	Returned Test Clock	Output		No pull-up resistor.
TDI	Test Data In	Input		No pull-up resistor.
TDO	Test Data Out	Output		
TMS	Test Mode Select	Input		No pull-up resistor.
NTRST	Test Reset Signal	Input	Low	Pull-up resistor.
JTAGSEL	JTAG Selection	Input		Pull-down resistor. Accepts between 0V and VDDBU.
ETM™				
TSYNC	Trace Synchronization Signal	Output		
TCLK	Trace Clock	Output		
TPS0 - TPS2	Trace ARM Pipeline Status	Output		
TPK0 - TPK15	Trace Packet Port	Output		

Table 3-1. Signal Description by Peripheral (Continued)

Signal Name	Function	Type	Active Level	Comments
Reset/Test				
NRST	Microcontroller Reset	I/O	Low	Pull-up resistor
TST	Test Mode Select	Input		Pull-down resistor.
BMS	Boot Mode Select	Input		
Debug Unit				
DRXD	Debug Receive Data	Input		
DTXD	Debug Transmit Data	Output		
AIC				
IRQ0 - IRQ2	External Interrupt Inputs	Input		
FIQ	Fast Interrupt Input	Input		
PIO				
PA0 - PA31	Parallel IO Controller A	I/O		Pulled-up input at reset
PB0 - PB31	Parallel IO Controller B	I/O		Pulled-up input at reset
PC0 - PC31	Parallel IO Controller C	I/O		Pulled-up input at reset
EBI				
D0 - D31	Data Bus	I/O		Pulled-up input at reset
A0 - A25	Address Bus	Output		0 at reset
NWAIT	External Wait Signal	Input	Low	
SMC				
NCS0 - NCS7	Chip Select Lines	Output	Low	
NWR0 - NWR3	Write Signal	Output	Low	
NRD	Read Signal	Output	Low	
NWE	Write Enable	Output	Low	
NBS0 - NBS3	Byte Mask Signal	Output	Low	
CompactFlash Support				
CFCE1 - CFCE2	CompactFlash Chip Enable	Output	Low	
CFOE	CompactFlash Output Enable	Output	Low	
CFWE	CompactFlash Write Enable	Output	Low	
CFIOR	CompactFlash IO Read	Output	Low	
CFIOW	CompactFlash IO Write	Output	Low	
CFRNW	CompactFlash Read Not Write	Output		
CFCS0 - CFCS1	CompactFlash Chip Select Lines	Output	Low	
NAND Flash Support				
NANDOE	NAND Flash Output Enable	Output	Low	
NANDWE	NAND Flash Write Enable	Output	Low	
NANDCS	NAND Flash Chip Select	Output	Low	

Table 3-1. Signal Description by Peripheral (Continued)

Signal Name	Function	Type	Active Level	Comments
SDRAM Controller				
SDCK	SDRAM Clock	Output		
SDCKE	SDRAM Clock Enable	Output	High	
SDCS	SDRAM Controller Chip Select	Output	Low	
BA0 - BA1	Bank Select	Output		
SDWE	SDRAM Write Enable	Output	Low	
RAS - CAS	Row and Column Signal	Output	Low	
SDA10	SDRAM Address 10 Line	Output		
Multimedia Card Interface				
MCCK	Multimedia Card Clock	Output		
MCCDA	Multimedia Card A Command	I/O		
MCDA0 - MCDA3	Multimedia Card A Data	I/O		
USART				
SCK0 - SCK2	Serial Clock	I/O		
TXD0 - TXD2	Transmit Data	Output		
RXD0 - RXD2	Receive Data	Input		
RTS0 - RTS2	Request To Send	Output		
CTS0 - CTS2	Clear To Send	Input		
Synchronous Serial Controller				
TD0 - TD2	Transmit Data	Output		
RD0 - RD2	Receive Data	Input		
TK0 - TK2	Transmit Clock	I/O		
RK0 - RK2	Receive Clock	I/O		
TF0 - TF2	Transmit Frame Sync	I/O		
RF0 - RF2	Receive Frame Sync	I/O		
Timer/Counter				
TCLK0 - TCLK2	External Clock Input	Input		
TIOA0 - TIOA2	I/O Line A	I/O		
TIOB0 - TIOB2	I/O Line B	I/O		
SPI				
SPI0_MISO - SPI1_MISO	Master In Slave Out	I/O		
SPI0_MOSI - SPI1_MOSI	Master Out Slave In	I/O		
SPI0_SPCK - SPI1_SPCK	SPI Serial Clock	I/O		
SPI0_NPCS0, SPI1_NPCS0	SPI Peripheral Chip Select 0	I/O	Low	
SPI0_NPCS1 - SPI0_NPCS3 SPI1_NPCS1 - SPI1_NPCS3	SPI Peripheral Chip Select	Output	Low	

Table 3-1. Signal Description by Peripheral (Continued)

Signal Name	Function	Type	Active Level	Comments
Two-Wire Interface				
TWD	Two-wire Serial Data	I/O		
TWCK	Two-wire Serial Clock	I/O		
LCD Controller				
LCDD0 - LCDD23	LCD Data Bus	Output		
LCDVSYNC	LCD Vertical Synchronization	Output		
LCDHSYNC	LCD Horizontal Synchronization	Output		
LCDDOTCK	LCD Dot Clock	Output		
LCDDEN	LCD Data Enable	Output		
LCDCC	LCD Contrast Control	Output		
USB Device Port				
DDM	USB Device Port Data -	Analog		
DDP	USB Device Port Data +	Analog		
USB Host Port				
HDMA	USB Host Port A Data -	Analog		
HDPA	USB Host Port A Data +	Analog		
HDMB	USB Host Port B Data -	Analog		
HDPB	USB Host Port B Data +	Analog		

4. Package and Pinout

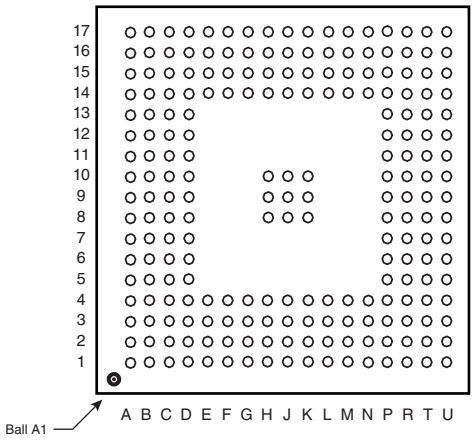
The AT91SAM9261 is available in a 217-ball LFBGA RoHS-compliant package, 15 x 15 mm, 0.8 mm ball pitch

4.1 217-ball LFBGA Package Outline

Figure 4-1 shows the orientation of the 217-ball LFBGA Package.

A detailed mechanical description is given in the section “AT91SAM9261 Mechanical Characteristics” of the product datasheet.

Figure 4-1. 217-ball LFBGA Package Outline (Top View)



4.2 Pinout

Table 4-1. AT91SAM9261 Pinout for 217-ball LFBGA Package [1]

Pin	Signal Name
A1	A19
A2	A16/BA0
A3	A14
A4	A12
A5	A9
A6	A6
A7	A3
A8	A2
A9	NC
A10	XOUT32
A11	XIN32
A12	DDP
A13	HDPB
A14	HDMB
A15	PB27
A16	GND
A17	PB24
B1	A20
B2	A18
B3	A15
B4	A13
B5	A11
B6	A7
B7	A4
B8	A1/NBS2/NWR2
B9	VDDBU
B10	JTAGSEL
B11	WKUP
B12	DDM
B13	PB31
B14	HDMA
B15	PB26
B16	PB25
B17	PB19
C1	A22
C2	A21
C3	VDDIOM
C4	A17/BA1
C5	VDDIOM
C6	A8
C7	GND
C8	VDDIOM
C9	GNDBU
C10	TST
C11	GND
C12	HDPA
C13	PB30
C14	NC
C15	VDDIOP
C16	PB21
C17	TMS
D1	NCS2
D2	NCS1/SDCS
D3	GND
D4	VDDIOM
D5	VDDCORE
D6	A10
D7	A5
D8	A0/NBS0
D9	SHDN
D10	NC
D11	VDDIOP
D12	PB29
D13	PB28
D14	PB23
D15	PB20
D16	PB17
D17	TCK
E1	NWR1/NBS1/CFIOR
E2	NWR0/NWE/CFWE
E3	NRD/CFOE
E4	SDA10
E14	PB22
E15	PB18
E16	PB15
E17	TDI
F1	SDCKE
F2	RAS
F3	NWR3/NBS3/CFIOW
F4	NCS0
F14	PB16
F15	NRST
F16	TDO
F17	NTRST
G1	D0
G2	D1
G3	SDWE
G4	NCS3/NANDCS
G14	PB14
G15	PB12
G16	PB11
G17	PB8
H1	D2
H2	D3
H3	VDDIOM
H4	SDCK
H8	GND
H9	GND
H10	GND
H14	PB10
H15	PB13
H16	PB7
H17	PB5
J1	D4
J2	D5
J3	GND
J4	CAS
J8	GND
J9	GND
J10	GND
J14	VDDIOP
J15	PB9
J16	PB6
J17	PB4
K1	D6
K2	D8
K3	D10
K4	D7
K8	GND
K9	GND
K10	GND
K14	VDDCORE
K15	PB3/BMS
K16	PB1
K17	PB2
L1	D9
L2	D11
L3	D12
L4	VDDIOM
L14	PA30
L15	PA27
L16	PA31
L17	PB0
M1	D13
M2	D15
M3	PC18
M4	VDDCORE
M14	PA25
M15	PA26
M16	PA28
M17	PA29
N1	D14
N2	PC17
N3	PC31
N4	VDDIOM
N14	PA22
N15	PA21
N16	PA23
N17	PA24
P1	PC16
P2	PC30
P3	PC22
P4	PC24
P5	PC28
P6	PC1
P7	PC7
P8	PC11
P9	GNDPLL
P10	PA3
P11	VDDIOP
P12	VDDCORE
P13	PA15
P14	PA16
P15	VDDIOP
P16	PA19
P17	PA20
R1	PC19
R2	PC21
R3	GND
R4	PC27
R5	PC29
R6	PC4
R7	PC8
R8	PC12
R9	PC14
R10	VDDPLL
R11	PA0
R12	PA7
R13	PA10
R14	PA13
R15	PA17
R16	GND
R17	PA18
T1	PC20
T2	PC23
T3	PC26
T4	PC2
T5	VDDIOP
T6	PC5
T7	PC9
T8	PC10
T9	PC15
T10	VDDOSC
T11	GNDOSC
T12	PA1
T13	PA4
T14	PA6
T15	PA8
T16	PA11
T17	PA14
U1	PC25
U2	PC0
U3	PC3
U4	GND
U5	PC6
U6	VDDIOP
U7	GND
U8	PC13
U9	PLLRCB
U10	PLLRCA
U11	XIN
U12	XOUT
U13	PA2
U14	PA5
U15	PA12
U16	PA9
U17	RTCK

Note: 1. Shaded cells define the pins powered by VDDIOM.

5. Power Considerations

5.1 Power Supplies

The AT91SAM9261 has six types of power supply pins:

- VDDCORE pins: Power the core, including the processor, the memories and the peripherals; voltage ranges from 1.08V and 1.32V, 1.2V nominal.
- VDDIOM pins: Power the External Bus Interface I/O lines; voltage ranges from 1.65V to 1.95V and 3.0V to 3.6V, 1.8V and 3.3V nominal.
- VDDIOP pins: Power the Peripheral I/O lines and the USB transceivers; voltage ranges from 2.7V and 3.6V, 3.3V nominal.
- VDDBU pin: Powers the Slow Clock oscillator and a part of the System Controller; voltage ranges from 1.08V and 1.32V, 1.2V nominal.
- VDDPLL pin: Powers the PLL cells; voltage ranges from 3.0V and 3.6V, 3.3V nominal.
- VDDOSC pin: Powers the Main Oscillator cells; voltage ranges from 3.0V and 3.6V, 3.3V nominal.

The double power supplies VDDIOM and VDDIOP are identified in Table 4-1 on page 10. These supplies enable the user to power the device differently for interfacing with memories and for interfacing with peripherals.

Ground pins GND are common to VDDCORE, VDDIOM and VDDIOP pins power supplies. Separated ground pins are provided for VDDBU, VDDOSC and VDDPLL. The ground pins are GNDBU, GNDOSC and GNDPLL, respectively.

5.2 Power Consumption

The AT91SAM9261 consumes about 550 µA of static current on VDDCORE at 25°C. This static current rises at up to 5.5 mA if the temperature increases to 85°C.

On VDDBU, the current does not exceed 3 µA @25°C, but can rise at up to 20 µA @85°C.

For dynamic power consumption, the AT91SAM9261 consumes a maximum of 50 mA on VDDCORE at maximum speed in typical conditions (1.2V, 25°C), processor running full-performance algorithm.

6. I/O Line Considerations

6.1 JTAG Port Pins

TMS, TDI and TCK are Schmitt trigger inputs and have no pull-up resistors.

TDO and RTCK are outputs, driven at up to VDDIOP, and have no pull-up resistor.

The JTAGSEL pin is used to select the JTAG boundary scan when asserted at a high level (tied to VDDBU). It integrates a permanent pull-down resistor of about 15 kΩ to GNDBU, so that it can be left unconnected for normal operations.

The NTRST pin is used to initialize the embedded ICE TAP Controller when asserted at a low level. It integrates a permanent pull-up resistor of about 15 kΩ to VDDIOP, so that it can be left unconnected for normal operations.

6.2 Test Pin

The TST pin is used for manufacturing test purposes when asserted high. It integrates a permanent pull-down resistor of about 15 kΩ to GNDBU, so that it can be left unconnected for normal operations. Driving this line at a high level leads to unpredictable results.

6.3 Reset Pin

NRST is an open-drain output integrating a non-programmable pull-up resistor. It can be driven with voltage at up to VDDIOP. As the product integrates power-on reset cells, the NRST pin can be left unconnected in case no reset from the system needs to be applied to the product.

The NRST pin integrates a permanent pull-up resistor of 100 kΩ minimum to VDDIOP.

The NRST signal is inserted in the Boundary Scan.

6.4 PIO Controller A, B and C Lines

All the I/O lines PA0 to PA31, PB0 to PB31, and PC0 to PC31 integrate a programmable pull-up resistor of 100 kΩ. Programming of this pull-up resistor is performed independently for each I/O line through the PIO Controllers.

After reset, all the I/O lines default as inputs with pull-up resistors enabled, except those which are multiplexed with the External Bus Interface signals that require to be enabled as Peripherals at reset. This is explicitly indicated in the column “Reset State” of the PIO Controller multiplexing tables.

6.5 Shutdown Logic Pins

The SHDN pin is an output only, driven by Shutdown Controller.

The pin WKUP is an input only. It can accept voltages only between 0V and VDDBU.

7. Processor and Architecture

7.1 ARM926EJ-S Processor

- RISC Processor Based on ARM v5TEJ Architecture with Jazelle technology for Java acceleration
- Two Instruction Sets
  - ARM High-performance 32-bit Instruction Set
  - Thumb High Code Density 16-bit Instruction Set
- DSP Instruction Extensions
- 5-Stage Pipeline Architecture:
  - Instruction Fetch (F)
  - Instruction Decode (D)
  - Execute (E)
  - Data Memory (M)
  - Register Write (W)
- 16 Kbyte Data Cache, 16 Kbyte Instruction Cache
  - Virtually-addressed 4-way Associative Cache
  - Eight words per line
  - Write-through and Write-back Operation
  - Pseudo-random or Round-robin Replacement
- Write Buffer
  - Main Write Buffer with 16-word Data Buffer and 4-address Buffer
  - DCache Write-back Buffer with 8-word Entries and a Single Address Entry
  - Software Control Drain
- Standard ARM v4 and v5 Memory Management Unit (MMU)
  - Access Permission for Sections
  - Access Permission for large pages and small pages can be specified separately for each quarter of the page
  - 16 embedded domains
- Bus Interface Unit (BIU)
  - Arbitrates and Schedules AHB Requests
  - Separate Masters for both instruction and data access providing complete AHB system flexibility
  - Separate Address and Data Buses for both the 32-bit instruction interface and the 32-bit data interface
  - On Address and Data Buses, data can be 8-bit (Bytes), 16-bit (Half-words) or 32-bit (Words)

7.2 Debug and Test Features

- Integrated Embedded In-circuit Emulator Real-Time
  - Two real-time Watchpoint Units
  - Two Independent Registers: Debug Control Register and Debug Status Register
  - Test Access Port Accessible through JTAG Protocol
  - Debug Communications Channel
- Debug Unit
  - Two-pin UART
  - Debug Communication Channel Interrupt Handling
  - Chip ID Register
- Embedded Trace Macrocell: ETM9™
  - Medium+ Level Implementation
  - Half-rate Clock Mode
  - Four Pairs of Address Comparators
  - Two Data Comparators
  - Eight Memory Map Decoder Inputs
  - Two 16-bit Counters
  - One 3-stage Sequencer
  - One 45-byte FIFO
- IEEE1149.1 JTAG Boundary-scan on All Digital Pins

7.3 Bus Matrix

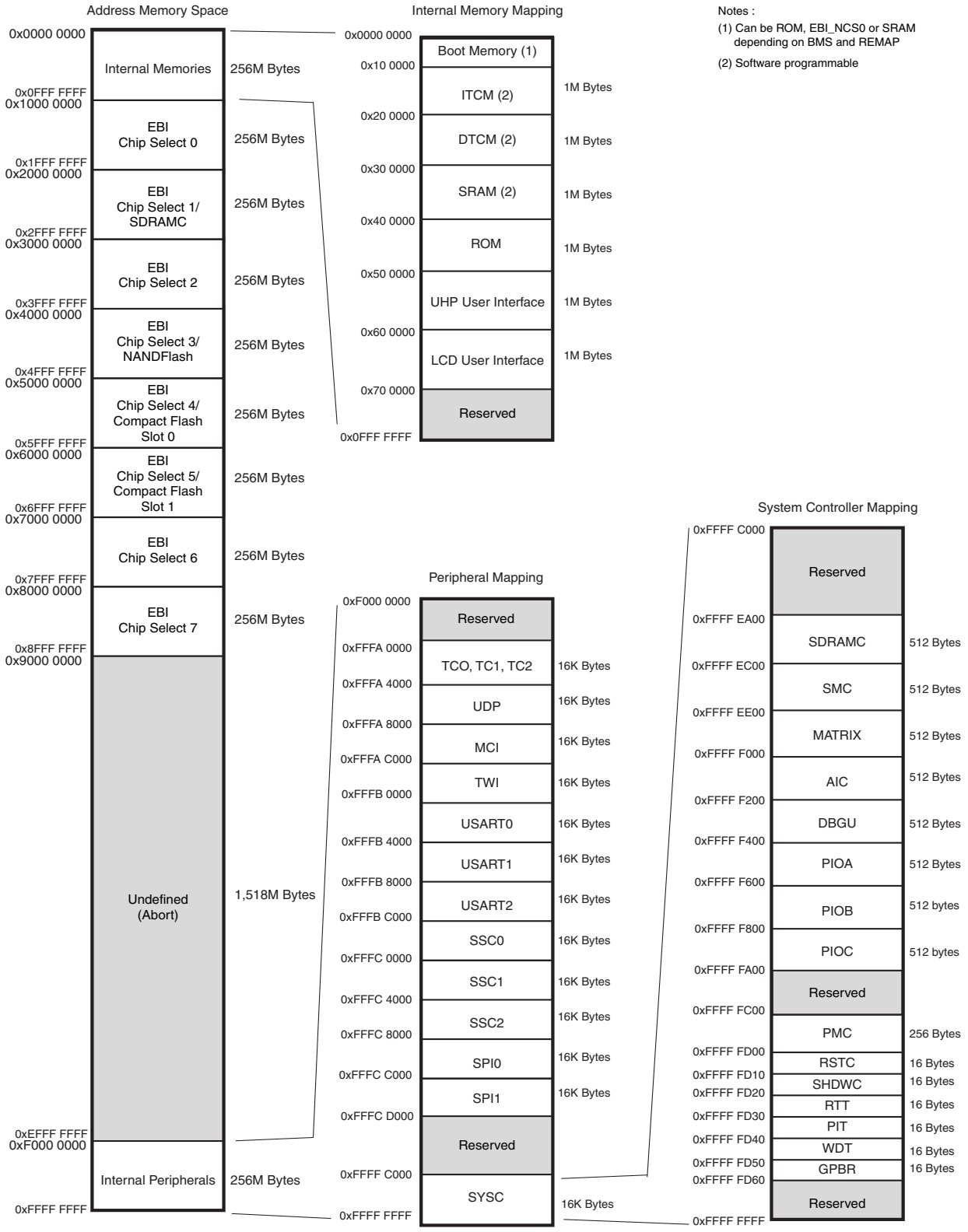
- Five Masters and Five Slaves handled
  - Handles Requests from the ARM926EJ-S, USB Host Port, LCD Controller and the Peripheral DMA Controller to internal ROM, internal SRAM, EBI, APB, LCD Controller and USB Host Port.
  - Round-Robin Arbitration (three modes supported: no default master, last accessed default master, fixed default master)
  - Burst Breaking with Slot Cycle Limit
- One Address Decoder Provided per Master
  - Three different slaves may be assigned to each decoded memory area: one for internal boot, one for external boot, one after remap.
- Boot Mode Select Option
  - Non-volatile Boot Memory can be Internal or External.
  - Selection is made by BMS pin sampled at reset.
- Remap Command
  - Allows Remapping of an Internal SRAM in Place of the Boot Non-Volatile Memory
  - Allows Handling of Dynamic Exception Vectors

7.4 Peripheral DMA Controller

- Transfers from/to peripheral to/from any memory space without intervention of the processor.
- Next Pointer Support, forbids strong real-time constraints on buffer management.
- Nineteen channels
  - Two for each USART
  - Two for the Debug Unit
  - Two for each Serial Synchronous Controller
  - Two for each Serial Peripheral Interface
  - One for the Multimedia Card Interface

8. Memories

Figure 8-1. AT91SAM9261 Memory Mapping



A first level of address decoding is performed by the Bus Matrix, i.e., the implementation of the Advanced High performance Bus (AHB) for its Master and Slave interfaces with additional features.

Decoding breaks up the 4 Gbytes of address space into 16 areas of 256 Mbytes. The areas 1 to 8 are directed to the EBI that associates these areas to the external chip selects NCS0 to NCS7. The area 0 is reserved for the addressing of the internal memories, and a second level of decoding provides 1 Mbyte of internal memory area. The area 15 is reserved for the peripherals and provides access to the Advanced Peripheral Bus (APB).

Other areas are unused and performing an access within them provides an abort to the master requesting such an access.

The Bus Matrix manages five Masters and five Slaves.

Each Master has its own bus and its own decoder, thus allowing a different memory mapping per Master.

Regarding Master 0 and Master 1 (ARM926™ Instruction and Data), three different Slaves are assigned to the memory space decoded at address 0x0: one for internal boot, one for external boot, one after remap. Refer to Table 8-3 for details.

Table 8-1. List of Bus Matrix Masters

Master 0	ARM926 Instruction
Master 1	ARM926 Data
Master 2	PDC
Master 3	LCD Controller
Master 4	USB Host

Each Slave has its own arbiter, thus allowing a different arbitration per Slave.

Table 8-2. List of Bus Matrix Slaves

Slave 0	Internal SRAM
Slave 1	Internal ROM
Slave 2	LCD Controller and USB Host Port Interfaces
Slave 3	External Bus Interface
Slave 4	Internal Peripherals

8.1 Embedded Memories

- 32 KB ROM
  - Single Cycle Access at full bus speed
- 160 KB Fast SRAM
  - Single Cycle Access at full bus speed
  - Supports ARM926EJ-S TCM interface at full processor speed

8.1.1 Internal Memory Mapping

Table 8-3 summarizes the Internal Memory Mapping for each Master, depending on the Remap status and the BMS state at reset.

Table 8-3. Internal Memory Mapping

Address	Master 0: ARM926 Instruction			Master 1: ARM926 Data		
	REMAP(RCB0) = 0		REMAP (RCB0) = 1	REMAP (RCB1) = 0		REMAP (RCB1) = 1
	BMS = 1	BMS = 0		BMS = 1	BMS = 0	
0x0000 0000	Int. ROM	EBI NCS0[1]	Int. RAM C	Int. ROM	EBI NCS0[1]	Int. RAM C

Note: 1. EBI NCS0 is to be connected to a 16-bit non-volatile memory. The access configuration is defined by the reset state of SMC Setup, SMC Pulse, SMC Cycle and SMC Mode CS0 registers.

8.1.1.1 Internal SRAM

The AT91SAM9261 embeds a high-speed 160 Kbyte SRAM. This Internal SRAM is split into three areas. Its Memory Mapping is detailed in Table 8-3 above.

- Internal SRAM A is the ARM926EJ-S Instruction TCM and the user can map this SRAM block anywhere in the ARM926 instruction memory space using CP15 instructions. This SRAM block is also accessible by the ARM926 Data Master and by the AHB Masters through the AHB bus at address 0x0010 0000.
- Internal SRAM B is the ARM926EJ-S Data TCM and the user can map this SRAM block anywhere in the ARM926 data memory space using CP15 instructions. This SRAM block is also accessible by the ARM926 Data Master and by the AHB Masters through the AHB bus at address 0x0020 0000.
- Internal SRAM C is only accessible by all the AHB Masters.
  After reset and until the Remap Command is performed, this SRAM block is accessible through the AHB bus at address 0x0030 0000 by all the AHB Masters.
  After Remap, this SRAM block also becomes accessible through the AHB bus at address 0x0 by the ARM926 Instruction and the ARM926 Data Masters.

Within the 160 Kbyte SRAM size available, the amount of memory assigned to each block is software programmable as a multiple of 16 Kbytes according to Table 8-4. This table provides the size of the Internal SRAM C according to the size of the Internal SRAM A and the Internal SRAM B.

Table 8-4. Internal SRAM Block Size

Internal SRAM C		Internal SRAM A (ITCM)			
		0	16 Kbytes	32 Kbytes	64 Kbytes
Internal SRAM B (DCTM)	0	160 Kbytes	144 Kbytes	128 Kbytes	96 Kbytes
	16 Kbytes	144 Kbytes	128 Kbytes	112 Kbytes	80 Kbytes
	32 Kbytes	128 Kbytes	112 Kbytes	96 Kbytes	64 Kbytes
	64 Kbytes	96 Kbytes	80 Kbytes	64 Kbytes	32 Kbytes

Note that among the ten 16 Kbyte blocks making up the Internal SRAM, two are permanently assigned to Internal SRAM C.

At reset, the whole memory (160 Kbytes) is assigned to Internal SRAM C.

The memory blocks assigned to SRAM A, SRAM B and SRAM C areas are not contiguous and when the user dynamically changes the Internal SRAM configuration, the new 16 Kbyte block organization may affect the previous configuration from a software point of view.

Table 8-5 illustrates different configurations and the related 16 Kbyte blocks (RB0 to RB9) assignments.

Table 8-5. 16 Kbyte Block Allocation

Decoded Area	Address	Configuration Examples and Related 16 Kbyte Block Assignments			
		ITCM = 0 Kbyte DTCM = 0 Kbyte AHB = 160 Kbytes (1)	**ITCM = 64 Kbytes DTCM = 64 Kbytes AHB = 32 Kbytes**	**ITCM = 32 Kbytes DTCM = 64 Kbytes AHB = 64 Kbytes**	**ITCM = 32 Kbytes DTCM = 16 Kbytes AHB = 112 Kbytes**
Internal SRAM A (ITCM)	0x0010 0000		RB3	RB3	RB3
	0x0010 4000		RB2	RB2	RB2
	0x0010 8000		RB1		
	0x0010 C000		RB0		
Internal SRAM B (DTCM)	0x0020 0000		RB7	RB7	RB7
	0x0020 4000		RB6	RB6	
	0x0020 8000		RB5	RB5	
	0x0020 C000		RB4	RB4	
Internal SRAM C (AHB)	0x0030 0000	RB9	RB9	RB9	RB9
	0x0030 4000	RB8	RB8	RB8	RB8
	0x0030 8000	RB7		RB1	RB6
	0x0030 C000	RB6		RB0	RB5
	0x0031 0000	RB5			RB4
	0x0031 4000	RB4			RB1
	0x0031 8000	RB3			RB0
	0x0031 C000	RB2			
	0x0032 0000	RB1			
	0x0032 4000	RB0			

Note: 1. Configuration after reset.

8.1.1.2 Internal ROM

The AT91SAM9261 integrates a 32 Kbyte Internal ROM mapped at address 0x0040 0000. It is also accessible at address 0x0 after reset and before remap if the BMS is tied high during reset.

8.1.1.3 USB Host Port

The AT91SAM9261 integrates a USB Host Port Open Host Controller Interface (OHCI). The registers of this interface are directly accessible on the AHB Bus and are mapped like a standard internal memory at address 0x0050 0000.

8.1.1.4 LCD Controller

The AT91SAM9261 integrates an LCD Controller. The interface is directly accessible on the AHB Bus and is mapped like a standard internal memory at address 0x0060 0000.

8.1.2 Boot Strategies

The system always boots at address 0x0. To ensure a maximum number of possibilities for boot, the memory layout can be configured with two parameters.

REMAP allows the user to lay out the first internal SRAM bank to 0x0 to ease development. This is done by software once the system has booted for each Master of the Bus Matrix. Refer to the Bus Matrix Section for more details.

When REMAP = 0, BMS allows the user to lay out to 0x0, at his convenience, the ROM or an external memory. This is done via hardware at reset.

Note: Memory blocks not affected by these parameters can always be seen at their specified base addresses. See the complete memory map presented in Figure 8-1 on page 16.

The AT91SAM9261 Bus Matrix manages a boot memory that depends on the level on the BMS pin at reset. The internal memory area mapped between address 0x0 and 0x000F FFFF is reserved for this purpose.

If BMS is detected at 1, the boot memory is the embedded ROM.

If BMS is detected at 0, the boot memory is the memory connected on the Chip Select 0 of the External Bus Interface.

8.1.2.1 BMS = 1, Boot on Embedded ROM

The system boots using the Boot Program.

- Downloads and runs an application from external storage media into internal SRAM
- Downloaded code size depends on embedded SRAM size
- Automatic detection of valid application
- Bootloader on a non-volatile memory
  - SDCard
  - NAND Flash
  - SPI DataFlash connected on NPCS0 of the SPI
- SAM-BA® boot in case no valid program is detected in external NVM, supporting:
  - Serial communication on a DBGU
  - USB Device HS Port

8.1.2.2 BMS = 0, Boot on External Memory

- Boot on slow clock (32,768 Hz)
- Boot with the default configuration for the Static Memory Controller, byte select mode, 16-bit data bus, Read/Write controlled by Chip Select, allows boot on 16-bit non-volatile memory.

The customer-programmed software must perform a complete configuration.

To speed up the boot sequence when booting at 32 kHz EBI CS0 (BMS=0), the user must take the following steps:

1. Program the PMC (main oscillator enable or bypass mode).
2. Program and start the PLL.
3. Reprogram the SMC setup, cycle, hold, mode timings registers for CS0 to adapt them to the new clock
4. Switch the main clock to the new value.

8.1.3 ETM™ Memories

The eight ETM9 Medium+ memory map decoder inputs are connected to custom address decoders and the resulting memory mapping is summarized in Table 8-6.

Table 8-6. ETM9 Memory Mapping

Product Resource	Area	Access Type	Start Address	End Address
SRAM	Internal	Data	0x0000 0000	0x002F FFFF
SRAM	Internal	Fetch	0x0000 0000	0x002F FFFF
ROM	Internal	Data	0x0040 0000	0x004F FFFF
ROM	Internal	Fetch	0x0040 0000	0x004F FFFF
External Bus Interface	External	Data	0x1000 0000	0x8FFF FFFF
External Bus Interface	External	Fetch	0x1000 0000	0x8FFF FFFF
User Peripherals	Internal	Data	0xF000 0000	0xFFFF BFFF
System Peripherals	Internal	Data	0xFFFF C000	0xFFFF FFFF

8.2 External Memories

The external memories are accessed through the External Bus Interface (Bus Matrix Slave 3).

Refer to the memory map in Figure 8-1 on page 16.

9. System Controller

The System Controller manages all vital blocks of the microcontroller: interrupts, clocks, power, time, debug and reset.

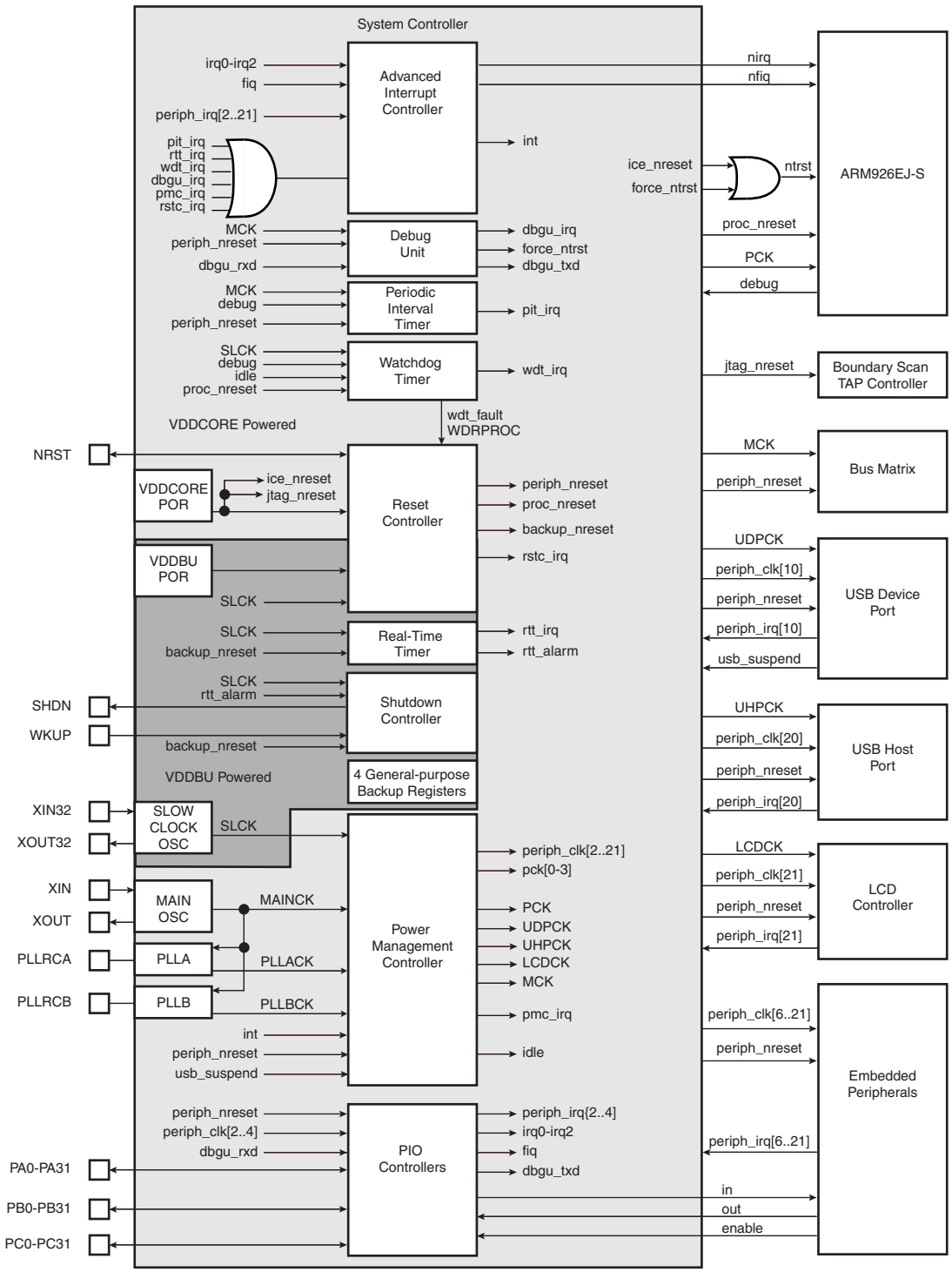
The System Peripherals are all mapped within the highest 6 Kbytes of address space, between addresses 0xFFFF EA00 and 0xFFFF FFFF. Each peripheral has an address space of 256 or 512 Bytes, representing 64 or 128 registers.

Figure 9-1 on page 23 shows the System Controller block diagram.

Figure 8-1 on page 16 shows the mapping of the User Interfaces of the System Controller peripherals.

9.1 Block Diagram

Figure 9-1. System Controller Block Diagram



9.2 Reset Controller

- Based on two Power-on-Reset cells
- Status of the last reset
  - Either cold reset, first reset, soft reset, user reset, watchdog reset, wake-up reset
- Controls the internal resets and the NRST pin output

9.3 Shutdown Controller

- Shutdown and Wake-up logic:
  - Software programmable assertion of the SHDN pin
  - Deassertion Programmable on a WKUP pin level change or on alarm

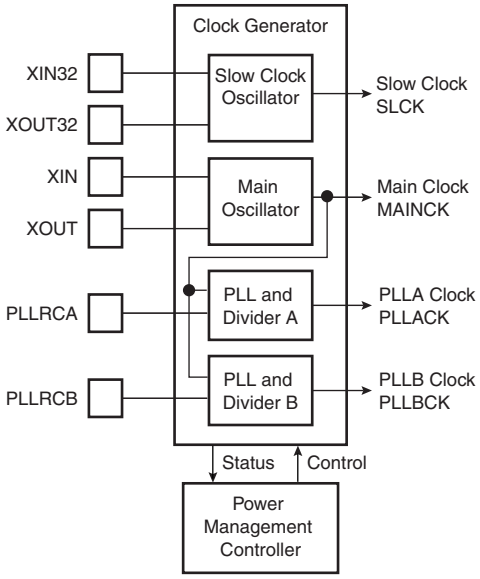
9.4 General-purpose Backup Registers

- Four 32-bit general-purpose backup registers

9.5 Clock Generator

- Embeds the Low-power 32768 Hz Slow Clock Oscillator
  - Provides the permanent Slow Clock to the system
- Embeds the Main Oscillator
  - Oscillator bypass feature
  - Supports 3 to 20 MHz crystals
- Embeds Two PLLs
  - Outputs 80 to 240 MHz clocks
  - Integrates an input divider to increase output accuracy
  - 1 MHz minimum input frequency
- Provides SLCK, MAINCK, PLLACK and PLLBCK.

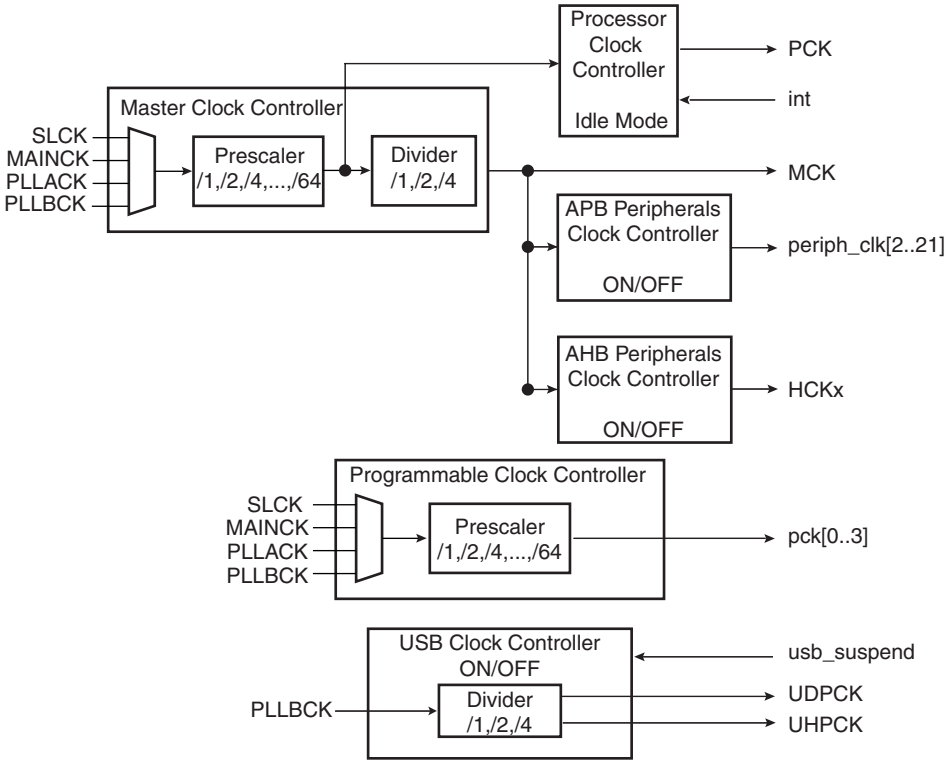
Figure 9-2. Clock Generator Block Diagram



9.6 Power Management Controller

- The Power Management Controller provides:
  - the Processor Clock PCK
  - the Master Clock MCK
  - the USB Clock USBCK (HCK0)
  - the LCD Controller Clock LCDCK (HCK1)
  - up to thirty peripheral clocks
  - four programmable clock outputs: PCK0 to PCK3

Figure 9-3. Power Management Controller Block Diagram



9.7 Periodic Interval Timer

- Includes a 20-bit Periodic Counter with less than 1 µs accuracy
- Includes a 12-bit Interval Overlay Counter
- Real time OS or Linux®/WindowsCE® compliant tick generator

9.8 Watchdog Timer

- 12-bit key-protected only-once programmable counter
- Windowed, prevents the processor to be in a dead-lock on the watchdog access

9.9 Real-time Timer

- 32-bit Free-running backup counter
- Alarm Register capable to generate a wake-up of the system