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## Description

The AT91SAM9263 32-bit microcontroller, based on the ARM926EJ-S processor, is architected on a 9-layer matrix, allowing a maximum internal bandwidth of nine 32-bit buses. It also features two independent external memory buses, EBIO and EBI1, capable of interfacing with a wide range of memory devices and an IDE hard disk. Two external buses prevent bottlenecks, thus guaranteeing maximum performance.

The AT91SAM9263 embeds an LCD Controller supported by a Two D Graphics Controller and a 2-channel DMA Controller, and one Image Sensor Interface. It also integrates several standard peripherals, such as USART, SPI, TWI, Timer Counters, PWM Generators, Multimedia Card interface and one CAN Controller.

When coupled with an external GPS engine, the AT91SAM9263 provides the ideal solution for navigation systems.

**This is a summary document.  
The complete document is  
available on the Atmel website  
at [www.atmel.com](http://www.atmel.com).**

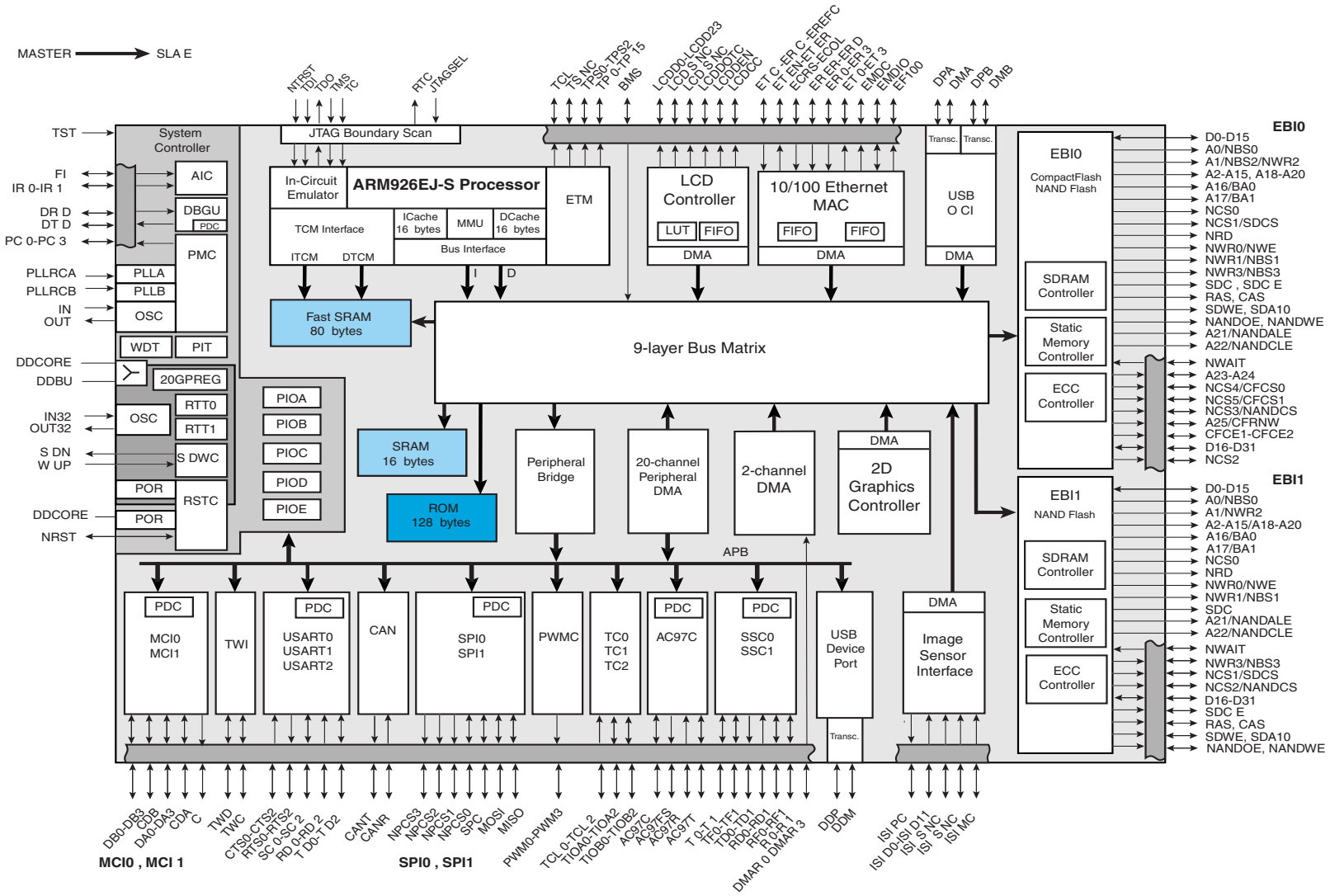
# 1. Features

- Incorporates the ARM926EJ-S™ ARM® Thumb® Processor
  - DSP Instruction Extensions, Jazelle® Technology for Java® Acceleration
  - 16 Kbyte Data Cache, 16 Kbyte Instruction Cache, Write Buffer
  - 220 MIPS at 200 MHz
  - Memory Management Unit
  - EmbeddedICE™, Debug Communication Channel Support
  - Mid-level Implementation Embedded Trace Macrocell™
- Bus Matrix
  - Nine 32-bit-layer Matrix, Allowing a Total of 28.8 Gbps of On-chip Bus Bandwidth
  - Boot Mode Select Option, Remap Command
- Embedded Memories
  - One 128 Kbyte Internal ROM, Single-cycle Access at Maximum Bus Matrix Speed
  - One 80 Kbyte Internal SRAM, Single-cycle Access at Maximum Processor or Bus Matrix Speed
  - One 16 Kbyte Internal SRAM, Single-cycle Access at Maximum Bus Matrix Speed
- Dual External Bus Interface (EBI0 and EBI1)
  - EBI0 Supports SDRAM, Static Memory, ECC-enabled NAND Flash and CompactFlash®
  - EBI1 Supports SDRAM, Static Memory and ECC-enabled NAND Flash
- DMA Controller (DMAC)
  - Acts as one Bus Matrix Master
  - Embeds 2 Unidirectional Channels with Programmable Priority, Address Generation, Channel Buffering and Control
- Twenty Peripheral DMA Controller Channels (PDC)
- LCD Controller
  - Supports Passive or Active Displays
  - Up to 24 bits per Pixel in TFT Mode, Up to 16 bits per Pixel in STN Color Mode
  - Up to 16M Colors in TFT Mode, Resolution Up to 2048x2048, Supports Virtual Screen Buffers
- Two D Graphics Accelerator
  - Line Draw, Block Transfer, Clipping, Commands Queuing
- Image Sensor Interface
  - ITU-R BT. 601/656 External Interface, Programmable Frame Capture Rate
  - 12-bit Data Interface for Support of High Sensibility Sensors
  - SAV and EAV Synchronization, Preview Path with Scaler, YCbCr Format
- USB 2.0 Full Speed (12 Mbits per second) Host Double Port
  - Dual On-chip Transceivers
  - Integrated FIFOs and Dedicated DMA Channels
- USB 2.0 Full Speed (12 Mbits per second) Device Port
  - On-chip Transceiver, 2,432-byte Configurable Integrated DPRAM
- Ethernet MAC 10/100 Base-T
  - Media Independent Interface or Reduced Media Independent Interface
  - 28-byte FIFOs and Dedicated DMA Channels for Receive and Transmit
- Fully-featured System Controller, including
  - Reset Controller, Shutdown Controller
  - Twenty 32-bit Battery Backup Registers for a Total of 80 Bytes
  - Clock Generator and Power Management Controller
  - Advanced Interrupt Controller and Debug Unit
  - Periodic Interval Timer, Watchdog Timer and Double Real-time Timer
- Reset Controller (RSTC)
  - Based on Two Power-on Reset Cells, Reset Source Identification and Reset Output Control
- Shutdown Controller (SHDWC)
  - Programmable Shutdown Pin Control and Wake-up Circuitry
- Clock Generator (CKGR)
  - 32768Hz Low-power Oscillator on Battery Backup Power Supply, Providing a Permanent Slow Clock

- 3 to 20 MHz On-chip Oscillator and Two Up to 240 MHz PLLs
- Power Management Controller (PMC)
  - Very Slow Clock Operating Mode, Software Programmable Power Optimization Capabilities
  - Four Programmable External Clock Signals
- Advanced Interrupt Controller (AIC)
  - Individually Maskable, Eight-level Priority, Vectored Interrupt Sources
  - Two External Interrupt Sources and One Fast Interrupt Source, Spurious Interrupt Protected
- Debug Unit (DBGU)
  - 2-wire UART and Support for Debug Communication Channel, Programmable ICE Access Prevention
  - Mode for General Purpose Two-wire UART Serial Communication
- Periodic Interval Timer (PIT)
  - 20-bit Interval Timer plus 12-bit Interval Counter
- Watchdog Timer (WDT)
  - Key-protected, Programmable Only Once, Windowed 16-bit Counter Running at Slow Clock
- Two Real-time Timers (RTT)
  - 32-bit Free-running Backup Counter Running at Slow Clock with 16-bit Prescaler
- Five 32-bit Parallel Input/Output Controllers (PIOA, PIOB, PIOC, PIOD and PIOE)
  - 160 Programmable I/O Lines Multiplexed with Up to Two Peripheral I/Os
  - Input Change Interrupt Capability on Each I/O Line
  - Individually Programmable Open-drain, Pull-up Resistor and Synchronous Output
- One Part 2.0A and Part 2.0B-compliant CAN Controller
  - 16 Fully-programmable Message Object Mailboxes, 16-bit Time Stamp Counter
- Two Multimedia Card Interface (MCI)
  - SDCard/SDIO and MultiMediaCard™ Compliant
  - Automatic Protocol Control and Fast Automatic Data Transfers with PDC
  - Two SDCard Slots Support on eAch Controller
- Two Synchronous Serial Controllers (SSC)
  - Independent Clock and Frame Sync Signals for Each Receiver and Transmitter
  - I<sup>2</sup>S Analog Interface Support, Time Division Multiplex Support
  - High-speed Continuous Data Stream Capabilities with 32-bit Data Transfer
- One AC97 Controller (AC97C)
  - 6-channel Single AC97 Analog Front End Interface, Slot Assigner
- Three Universal Synchronous/Asynchronous Receiver Transmitters (USART)
  - Individual Baud Rate Generator, IrDA® Infrared Modulation/Demodulation, Manchester Encoding/Decoding
  - Support for ISO7816 T0/T1 Smart Card, Hardware Handshaking, RS485 Support
- Two Master/Slave Serial Peripheral Interface (SPI)
  - 8- to 16-bit Programmable Data Length, Four External Peripheral Chip Selects
- One Three-channel 16-bit Timer/Counters (TC)
  - Three External Clock Inputs, Two Multi-purpose I/O Pins per Channel
  - Double PWM Generation, Capture/Waveform Mode, Up/Down Capability
- One Four-channel 16-bit PWM Controller (PWMC)
- One Two-wire Interface (TWI)
  - Master Mode Support, All Two-wire Atmel® EEPROMs Supported
- IEEE® 1149.1 JTAG Boundary Scan on All Digital Pins
- Required Power Supplies
  - 1.08V to 1.32V for VDDCORE and VDDBU
  - 3.0V to 3.6V for VDDOSC and VDDPLL
  - 2.7V to 3.6V for VDDIOP0 (Peripheral I/Os)
  - 1.65V to 3.6V for VDDIOP1 (Peripheral I/Os)
  - Programmable 1.65V to 1.95V or 3.0V to 3.6V for VDDIOM0/VDDIOM1 (Memory I/Os)
- Available in a 324-ball TFBGA Green Package

## 2. AT91SAM9263 Block Diagram

Figure 2-1. AT91SAM9263 Block Diagram



### 3. Signal Description

Table 3-1 gives details on the signal name classified by peripheral.

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level	Comments
<b>Power Supplies</b>				
VDDIOM0	EBI0 I/O Lines Power Supply	Power		1.65V to 3.6V
VDDIOM1	EBI1 I/O Lines Power Supply	Power		1.65V to 3.6V
VDDIOP0	Peripherals I/O Lines Power Supply	Power		2.7V to 3.6V
VDDIOP1	Peripherals I/O Lines Power Supply	Power		1.65V to 3.6V
VDDDBU	Backup I/O Lines Power Supply	Power		1.08V to 1.32V
VDDPLL	PLL Power Supply	Power		3.0V to 3.6V
VDDOSC	Oscillator Power Supply	Power		3.0V to 3.6V
VDDCORE	Core Chip Power Supply	Power		1.08V to 1.32V
GND	Ground	Ground		
GNDPLL	PLL Ground	Ground		
GNDDBU	Backup Ground	Ground		
<b>Clocks, Oscillators and PLLs</b>				
XIN	Main Oscillator Input	Input		
XOUT	Main Oscillator Output	Output		
XIN32	Slow Clock Oscillator Input	Input		
XOUT32	Slow Clock Oscillator Output	Output		
PLLRCA	PLL A Filter	Input		
PLLRCB	PLL B Filter	Input		
PCK0 - PCK3	Programmable Clock Output	Output		
<b>Shutdown, Wakeup Logic</b>				
SHDN	Shutdown Control	Output		Driven at 0V only. Do not tie over VDDDBU.
WKUP	Wake-up Input	Input		Accepts between 0V and VDDDBU.
<b>ICE and JTAG</b>				
NTRST	Test Reset Signal	Input	Low	Pull-up resistor
TCK	Test Clock	Input		No pull-up resistor
TDI	Test Data In	Input		No pull-up resistor
TDO	Test Data Out	Output		
TMS	Test Mode Select	Input		No pull-up resistor
JTAGSEL	JTAG Selection	Input		Pull-down resistor. Accepts between 0V and VDDDBU.
RTCK	Return Test Clock	Output		

**Table 3-1. Signal Description List (Continued)**

Signal Name	Function	Type	Active Level	Comments
<b>Embedded Trace Module - ETM</b>				
TSYNC	Trace Synchronization Signal	Output		
TCLK	Trace Clock	Output		
TPS0 - TPS2	Trace ARM Pipeline Status	Output		
TPK0 - TPK15	Trace Packet Port	Output		
<b>Reset/Test</b>				
NRST	Microcontroller Reset	I/O	Low	Pull-up resistor
TST	Test Mode Select	Input		Pull-down resistor
BMS	Boot Mode Select	Input		
<b>Debug Unit - DBGU</b>				
DRXD	Debug Receive Data	Input		
DTXD	Debug Transmit Data	Output		
<b>Advanced Interrupt Controller - AIC</b>				
IRQ0 - IRQ1	External Interrupt Inputs	Input		
FIQ	Fast Interrupt Input	Input		
<b>PIO Controller - PIOA - PIOB - PIOC - PIOD - PIOE</b>				
PA0 - PA31	Parallel IO Controller A	I/O		Pulled-up input at reset
PB0 - PB31	Parallel IO Controller B	I/O		Pulled-up input at reset
PC0 - PC31	Parallel IO Controller C	I/O		Pulled-up input at reset
PD0 - PD31	Parallel IO Controller D	I/O		Pulled-up input at reset
PE0 - PE31	Parallel IO Controller E	I/O		Pulled-up input at reset
<b>Direct Memory Access Controller - DMA</b>				
DMARQ0-DMARQ3	DMA Requests	Input		
<b>External Bus Interface - EBIO - EBI1</b>				
EBIx_D0 - EBIx_D31	Data Bus	I/O		Pulled-up input at reset
EBIx_A0 - EBIx_A25	Address Bus	Output		0 at reset
EBIx_NWAIT	External Wait Signal	Input	Low	
<b>Static Memory Controller - SMC</b>				
EBI0_NCS0 - EBI0_NCS5, EBI1_NCS0 - EBI1_NCS2	Chip Select Lines	Output	Low	
EBIx_NWR0 -EBIx_NWR3	Write Signal	Output	Low	
EBIx_NRD	Read Signal	Output	Low	
EBIx_NWE	Write Enable	Output	Low	
EBIx_NBS0 - EBIx_NBS3	Byte Mask Signal	Output	Low	

**Table 3-1. Signal Description List (Continued)**

Signal Name	Function	Type	Active Level	Comments
<b>CompactFlash Support</b>				
EBI0_CFCE1 - EBI0_CFCE2	CompactFlash Chip Enable	Output	Low	
EBI0_CFOE	CompactFlash Output Enable	Output	Low	
EBI0_CFWE	CompactFlash Write Enable	Output	Low	
EBI0_CFIOR	CompactFlash IO Read	Output	Low	
EBI0_CFIOW	CompactFlash IO Write	Output	Low	
EBI0_CFRNW	CompactFlash Read Not Write	Output		
EBI0_CFCS0 - EBI0_CFCS1	CompactFlash Chip Select Lines	Output	Low	
<b>NAND Flash Support</b>				
EBIx_NANDCS	NAND Flash Chip Select	Output	Low	
EBIx_NANDOE	NAND Flash Output Enable	Output	Low	
EBIx_NANDWE	NAND Flash Write Enable	Output	Low	
<b>SDRAM Controller</b>				
EBIx_SDCK	SDRAM Clock	Output		
EBIx_SDCKE	SDRAM Clock Enable	Output	High	
EBIx_SDCS	SDRAM Controller Chip Select	Output	Low	
EBIx_BA0 - EBIx_BA1	Bank Select	Output		
EBIx_SDWE	SDRAM Write Enable	Output	Low	
EBIx_RAS - EBIx_CAS	Row and Column Signal	Output	Low	
EBIx_SDA10	SDRAM Address 10 Line	Output		
<b>Multimedia Card Interface</b>				
MCIx_CK	Multimedia Card Clock	Output		
MCIx_CDA	Multimedia Card Slot A Command	I/O		
MCIx_CDB	Multimedia Card Slot B Command	I/O		
MCIx_DA0 - MCIx_DA3	Multimedia Card Slot A Data	I/O		
MCIx_DB0 - MCIx_DB3	Multimedia Card Slot B Data	I/O		
<b>Universal Synchronous Asynchronous Receiver Transmitter USART</b>				
SCKx	USARTx Serial Clock	I/O		
TXDx	USARTx Transmit Data	I/O		
RXDx	USARTx Receive Data	Input		
RTSx	USARTx Request To Send	Output		
CTSx	USARTx Clear To Send	Input		
<b>Synchronous Serial Controller SSC</b>				
TDx	SSCx Transmit Data	Output		
RDx	SSCx Receive Data	Input		
TKx	SSCx Transmit Clock	I/O		



**Table 3-1. Signal Description List (Continued)**

Signal Name	Function	Type	Active Level	Comments
RKx	SSCx Receive Clock	I/O		
TFx	SSCx Transmit Frame Sync	I/O		
RFx	SSCx Receive Frame Sync	I/O		
<b>AC97 Controller - AC97C</b>				
AC97RX	AC97 Receive Signal	Input		
AC97TX	AC97 Transmit Signal	Output		
AC97FS	AC97 Frame Synchronization Signal	Output		
AC97CK	AC97 Clock signal	Input		
<b>Timer/Counter - TC</b>				
TCLKx	TC Channel x External Clock Input	Input		
TIOAx	TC Channel x I/O Line A	I/O		
TIOBx	TC Channel x I/O Line B	I/O		
<b>Pulse Width Modulation Controller- PWMC</b>				
PWMx	Pulse Width Modulation Output	Output		
<b>Serial Peripheral Interface - SPI</b>				
SPIx_MISO	Master In Slave Out	I/O		
SPIx_MOSI	Master Out Slave In	I/O		
SPIx_SPCK	SPI Serial Clock	I/O		
SPIx_NPCS0	SPI Peripheral Chip Select 0	I/O	Low	
SPIx_NPCS1 - SPIx_NPCS3	SPI Peripheral Chip Select	Output	Low	
<b>Two-Wire Interface</b>				
TWD	Two-wire Serial Data	I/O		
TWCK	Two-wire Serial Clock	I/O		
<b>CAN Controllers</b>				
CANRX	CAN Input	Input		
CANTX	CAN Output	Output		
<b>LCD Controller - LCDC</b>				
LCDD0 - LCDD23	LCD Data Bus	Output		
LCDVSYNC	LCD Vertical Synchronization	Output		
LCDHSYNC	LCD Horizontal Synchronization	Output		
LCDDOTCK	LCD Dot Clock	Output		
LCDDEN	LCD Data Enable	Output		
LCDDCC	LCD Contrast Control	Output		

**Table 3-1. Signal Description List (Continued)**

Signal Name	Function	Type	Active Level	Comments
<b>Ethernet 10/100</b>				
ETXCK	Transmit Clock or Reference Clock	Input		MII only, REFCK in RMII
ERXCK	Receive Clock	Input		MII only
ETXEN	Transmit Enable	Output		
ETX0-ETX3	Transmit Data	Output		ETX0-ETX1 only in RMII
ETXER	Transmit Coding Error	Output		MII only
ERXDV	Receive Data Valid	Input		RXDV in MII, CRSDV in RMII
ERX0-ERX3	Receive Data	Input		ERX0-ERX1 only in RMII
ERXER	Receive Error	Input		
ECRS	Carrier Sense and Data Valid	Input		MII only
ECOL	Collision Detect	Input		MII only
EMDC	Management Data Clock	Output		
EMDIO	Management Data Input/Output	I/O		
EF100	Force 100Mbit/sec.	Output	High	RMII only
<b>USB Device Port</b>				
DDM	USB Device Port Data -	Analog		
DDP	USB Device Port Data +	Analog		
<b>USB Host Port</b>				
HDP A	USB Host Port A Data +	Analog		
HDP A	USB Host Port A Data -	Analog		
HDP B	USB Host Port B Data +	Analog		
HDP B	USB Host Port B Data -	Analog		
<b>Image Sensor Interface - ISI</b>				
ISI_D0-ISI_D11	Image Sensor Data	Input		
ISI_MCK	Image Sensor Reference Clock	Output		Provided by PCK3
ISI_HSYNC	Image Sensor Horizontal Synchro	Input		
ISI_VSYNC	Image Sensor Vertical Synchro	Input		
ISI_PCK	Image Sensor Data Clock	Input		

## 4. Package and Pinout

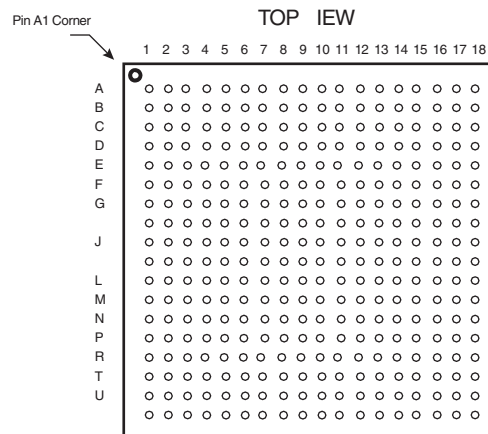
The AT91SAM9263 is available in a 324-ball TFBGA Green package, 15 x 15 mm, 0.8mm ball pitch.

### 4.1 324-ball TFBGA Package Outline

Figure 4-1 shows the orientation of the 324-ball TFBGA package.

A detailed mechanical description is given in the section “AT91SAM9263 Mechanical Characteristics” in the product datasheet.

Figure 4-1. 324-ball TFBGA Pinout (Top View)



## 4.2 324-ball TFBGA Package Pinout

Table 4-1. AT91SAM9263 Pinout for 324-ball TFBGA Package

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	EBIO_D2	E10	PC31	K1	PE6	P10	EBI1_NCS0
A2	EBIO_SDCKE	E11	PC22	K2	PD28	P11	EBI1_NWE_NWR0
A3	EBIO_NWE_NWR0	E12	PC15	K3	PE0	P12	EBI1_D4
A4	EBIO_NCS1_SDCS	E13	PC11	K4	PE1	P13	EBI1_D10
A5	EBIO_A19	E14	PC4	K5	PD27	P14	PA3
A6	EBIO_A11	E15	PB30	K6	PD31	P15	PA2
A7	EBIO_A10	E16	PC0	K7	PD29	P16	PE28
A8	EBIO_A5	E17	PB31	K8	PD25	P17	TDI
A9	EBIO_A1_NBS2_NWR2	E18	HDPA	K9	GND	P18	PLLRCB
A10	PD4	F1	PD7	K10	VDDIOM0	R1	XOUT32
A11	PC30	F2	EBIO_D13	K11	GND	R2	TST
A12	PC26	F3	EBIO_D9	K12	VDDIOM0	R3	PA18
A13	PC24	F4	EBIO_D11	K13	PB3/BMS	R4	PA25
A14	PC19	F5	EBIO_D12	K14	PA14	R5	PA30
A15	PC12	F6	EBIO_NCS0	K15	PA15	R6	EBI1_A2
A16	VDDCORE	F7	EBIO_A16_BA0	K16	PB1	R7	EBI1_A14
A17	VDDIOP0	F8	EBIO_A12	K17	PB0	R8	EBI1_A13
A18	DDP	F9	EBIO_A6	K18	PB2	R9	EBI1_A17_BA1
B1	EBIO_D4	F10	PD3	L1	PE10	R10	EBI1_D1
B2	EBIO_NANDOE	F11	PC27	L2	PE4	R11	EBI1_D8
B3	EBIO_CAS	F12	PC18	L3	PE9	R12	EBI1_D12
B4	EBIO_RAS	F13	PC13	L4	PE7	R13	EBI1_D15
B5	EBIO_NBS3_NWR3	F14	PB26	L5	PE5	R14	PE26
B6	EBIO_A22	F15	PB25	L6	PE2	R15	EBI1_SDCK
B7	EBIO_A15	F16	PB29	L7	PE3	R16	PE30
B8	EBIO_A7	F17	PB27	L8	VDDIOP1	R17	TCK
B9	EBIO_A4	F18	HDMA	L9	VDDIOM1	R18	XOUT
B10	PD0	G1	PD17	L10	VDDIOM0	T1	VDDOSC
B11	PC28	G2	PD12	L11	VDDIOP0	T2	VDDIOM1
B12	PC21	G3	PD6	L12	GNDBU	T3	PA19
B13	PC17	G4	EBIO_D14	L13	PA13	T4	PA21
B14	PC9	G5	PD5	L14	PB4	T5	PA26
B15	PC7	G6	PD8	L15	PA9	T6	PA31
B16	PC5	G7	PD10	L16	PA12	T7	EBI1_A7
B17	PB16	G8	GND	L17	PA10	T8	EBI1_A12
B18	DDM	G9	NC <sup>(1)</sup>	L18	PA11	T9	EBI1_A18
C1	EBIO_D6	G10	GND	M1	PE18	T10	EBI1_D0
C2	EBIO_D0	G11	GND	M2	PE14	T11	EBI1_D7
C3	EBIO_NANDWE	G12	GND	M3	PE15	T12	EBI1_D14
C4	EBIO_SDWE	G13	PB21	M4	PE11	T13	PE23
C5	EBIO_SDCK	G14	PB20	M5	PE13	T14	PE25
C6	EBIO_A21	G15	PB23	M6	PE12	T15	PE29
C7	EBIO_A13	G16	PB28	M7	PE8	T16	PE31
C8	EBIO_A8	G17	PB22	M8	VDDBU	T17	GNDPLL
C9	EBIO_A3	G18	PB18	M9	EBI1_A21	T18	XIN
C10	PD2	H1	PD24	M10	VDDIOM1	U1	PA17
C11	PC29	H2	PD13	M11	GND	U2	PA20
C12	PC23	H3	PD15	M12	GND	U3	PA23
C13	PC14	H4	PD9	M13	VDDIOM1	U4	PA24
C14	PC8	H5	PD11	M14	PA6	U5	PA28
C15	PC3	H6	PD14	M15	PA4	U6	EBI1_A0_NBS0

**Table 4-1. AT91SAM9263 Pinout for 324-ball TFBGA Package (Continued)**

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
C16	GND	H7	PD16	M16	PA7	U7	EBI1_A5
C17	VDDIOP0	H8	VDDIOM0	M17	PA5	U8	EBI1_A10
C18	HDPB	H9	GND	M18	PA8	U9	EBI1_A16_BA0
D1	EBI0_D10	H10	VDDCORE	N1	NC	U10	EBI1_NRD
D2	EBI0_D3	H11	GND	N2	NC	U11	EBI1_D3
D3	NC <sup>(1)</sup>	H12	PB19	N3	PE19	U12	EBI1_D13
D4	EBI0_D1	H13	PB17	N4	NC <sup>(1)</sup>	U13	PE22
D5	EBI0_A20	H14	PB15	N5	PE17	U14	PE27
D6	EBI0_A17_BA1	H15	PB13	N6	PE16	U15	RTCK
D7	EBI0_A18	H16	PB24	N7	EBI1_A6	U16	NTRST
D8	EBI0_A9	H17	PB14	N8	EBI1_A11	U17	VDDPLLA
D9	EBI0_A2	H18	PB12	N9	EBI1_A22	U18	PLLRC
D10	PD1	J1	PD30	N10	EBI1_D2	V1	VDDCORE
D11	PC25	J2	PD26	N11	EBI1_D6	V2	PA22
D12	PC20	J3	PD22	N12	EBI1_D9	V3	PA27
D13	PC6	J4	PD19	N13	GND	V4	PA29
D14	PC16	J5	PD18	N14	GNDPLL	V5	EBI1_A1_NWR2
D15	PC10	J6	PD23	N15	PA1	V6	EBI1_A3
D16	PC2	J7	PD21	N16	PA0	V7	EBI1_A9
D17	PC1	J8	PD20	N17	TMS	V8	EBI1_A15
D18	HDMB	J9	GND	N18	TDO	V9	EBI1_A20
E1	EBI0_D15	J10	GND	P1	XIN32	V10	EBI1_NBS1_NWR1
E2	EBI0_D7	J11	GND	P2	SHDN	V11	EBI1_D5
E3	EBI0_D5	J12	PB11	P3	PA16	V12	EBI1_D11
E4	EBI0_D8	J13	PB9	P4	WKUP	V13	PE21
E5	EBI0_NBS1_NWR1	J14	PB10	P5	JTAGSEL	V14	PE24
E6	EBI0_NRD	J15	PB5	P6	PE20	V15	NRST
E7	EBI0_A14	J16	PB6	P7	EBI1_A8	V16	GND
E8	EBI0_SDA10	J17	PB7	P8	EBI1_A4	V17	GND
E9	EBI0_A0_NBS0	J18	PB8	P9	EBI1_A19	V18	VDDPLLB

Note: 1. NC pins must be left unconnected.

## 5. Power Considerations

### 5.1 Power Supplies

AT91SAM9263 has several types of power supply pins:

- VDDCORE pins: Power the core, including the processor, the embedded memories and the peripherals; voltage ranges from 1.08V to 1.32V, 1.2V nominal.
- VDDIOM0 and VDDIOM1 pins: Power the External Bus Interface 0 I/O lines and the External Bus Interface 1 I/O lines, respectively; voltage ranges between 1.65V and 1.95V (1.8V nominal) or between 3.0V and 3.6V (3.3V nominal).
- VDDIOP0 pins: Power the Peripheral I/O lines and the USB transceivers; voltage ranges from 2.7V to 3.6V, 3.3V nominal.
- VDDIOP1 pins: Power the Peripheral I/O lines involving the Image Sensor Interface; voltage ranges from 1.65V to 3.6V, 1.8V, 2.5V, 3V or 3.3V nominal.
- VDDDBU pin: Powers the Slow Clock oscillator and a part of the System Controller; voltage ranges from 1.08V to 1.32V, 1.2V nominal.
- VDDPLL pin: Powers the PLL cells; voltage ranges from 3.0V to 3.6V, 3.3V nominal.
- VDDOSC pin: Powers the Main Oscillator cells; voltage ranges from 3.0V to 3.6V, 3.3V nominal.

The power supplies VDDIOM0, VDDIOM1 and VDDIOP0, VDDIOP1 are identified in the pinout table and the multiplexing tables. These supplies enable the user to power the device differently for interfacing with memories and for interfacing with peripherals.

Ground pins GND are common to VDDOSC, VDDCORE, VDDIOM0, VDDIOM1, VDDIOP0 and VDDIOP1 pins power supplies. Separated ground pins are provided for VDDDBU and VDDPLL. These ground pins are respectively GNDBU and GNDPLL.

### 5.2 Power Consumption

The AT91SAM9263 consumes about 700  $\mu\text{A}$  (worst case) of static current on VDDCORE at 25°C. This static current rises at up to 7 mA if the temperature increases to 85°C.

On VDDDBU, the current does not exceed 3  $\mu\text{A}$  @25°C, but can rise at up to 20  $\mu\text{A}$  @85°C. An automatic switch to VDDCORE guarantees low power consumption on the battery when the system is on.

For dynamic power consumption, the AT91SAM9263 consumes a maximum of 70 mA on VDDCORE at maximum conditions (1.2V, 25°C, processor running full-performance algorithm).

### 5.3 Programmable I/O Lines Power Supplies

The power supply pins VDDIOM0 and VDDIOM1 accept two voltage ranges. This allows the device to reach its maximum speed, either out of 1.8V or 3.0V external memories.

The maximum speed is 100 MHz on the pin SDCK (SDRAM Clock) loaded with 10 pF. The other signals (control, address and data signals) do not go over 50 MHz, loaded with 30 pF for power supply at 1.8V and 50 pF for power supply at 3.3V.

The voltage ranges are determined by programming registers in the Chip Configuration registers located in the Matrix User Interface.

At reset, the selected voltage defaults to 3.3V nominal and power supply pins can accept either 1.8V or 3.3V. However, the device cannot reach its maximum speed if the voltage supplied to the pins is only 1.8V without reprogramming the EBIO voltage range. The user must be sure to program the EBIO voltage range before getting the device out of its Slow Clock Mode.

## 6. I/O Line Considerations

### 6.1 JTAG Port Pins

TMS, TDI and TCK are Schmitt trigger inputs and have no pull-up resistors.

TDO and RTCK are outputs, driven at up to VDDIOP0, and have no pull-up resistors.

The JTAGSEL pin is used to select the JTAG boundary scan when asserted at a high level (VDDBU). It integrates a permanent pull-down resistor of about 15 k $\Omega$  to GNDBU, so that it can be left unconnected for normal operations.

The NTRST signal is described in [Section 6.3](#).

All JTAG signals except JTAGSEL (VDDBU) are supplied with VDDIOP0.

### 6.2 Test Pin

The TST pin is used for manufacturing test purposes when asserted high. It integrates a permanent pull-down resistor of about 15 k $\Omega$  to GNDBU, so that it can be left unconnected for normal operations. Driving this line at a high level leads to unpredictable results.

This pin is supplied with VDDBU.

### 6.3 Reset Pins

NRST is an open-drain output integrating a non-programmable pull-up resistor. It can be driven with voltage at up to VDDIOP0.

NTRST is an input which allows reset of the JTAG Test Access port. It has no action on the processor.

As the product integrates power-on reset cells, which manage the processor and the JTAG reset, the NRST and NTRST pins can be left unconnected.

The NRST and NTRST pins both integrate a permanent pull-up resistor of 100 k $\Omega$  minimum to VDDIOP0.

The NRST signal is inserted in the Boundary Scan.

### 6.4 PIO Controllers

All the I/O lines managed by the PIO Controllers integrate a programmable pull-up resistor of 100 k $\Omega$  typical. Programming of this pull-up resistor is performed independently for each I/O line through the PIO Controllers.

After reset, all the I/O lines default as inputs with pull-up resistors enabled, except those which are multiplexed with the External Bus Interface signals that require to be enabled as Peripheral at reset. This is explicitly indicated in the column "Reset State" of the PIO Controller multiplexing tables on [page 33](#) and following.

### 6.5 Shutdown Logic Pins

The SHDN pin is a tri-state output only pin, which is driven by the Shutdown Controller. There is no internal pull-up. An external pull-up to VDDBU is needed and its value must be higher than 1 M $\Omega$ . The resistor value is calculated according to the regulator enable implementation and the SHDN level.

The pin WKUP is an input-only. It can accept voltages only between 0V and VDDBU.

## 7. Processor and Architecture

### 7.1 ARM926EJ-S Processor

- RISC Processor based on ARM v5TEJ Harvard Architecture with Jazelle technology for Java acceleration
- Two Instruction Sets
  - ARM High-performance 32-bit Instruction Set
  - Thumb High Code Density 16-bit Instruction Set
- DSP Instruction Extensions
- 5-stage Pipeline Architecture
  - Instruction Fetch (F)
  - Instruction Decode (D)
  - Execute (E)
  - Data Memory (M)
  - Register Write (W)
- 16 Kbyte Data Cache, 16 Kbyte Instruction Cache
  - Virtually-addressed 4-way Associative Cache
  - Eight words per line
  - Write-through and Write-back Operation
  - Pseudo-random or Round-robin Replacement
- Write Buffer
  - Main Write Buffer with 16-word Data Buffer and 4-address Buffer
  - DCache Write-back Buffer with 8-word Entries and a Single Address Entry
  - Software Control Drain
- Standard ARM v4 and v5 Memory Management Unit (MMU)
  - Access Permission for Sections
  - Access Permission for large pages and small pages can be specified separately for each quarter of the page
  - 16 embedded domains
- Bus Interface Unit (BIU)
  - Arbitrates and Schedules AHB Requests
  - Separate Masters for both instruction and data access providing complete Matrix system flexibility
  - Separate Address and Data Buses for both the 32-bit instruction interface and the 32-bit data interface
  - On Address and Data Buses, data can be 8-bit (Bytes), 16-bit (Half-words) or 32-bit (Words)

### 7.2 Bus Matrix

- 9-layer Matrix, handling requests from 9 masters
- Programmable Arbitration strategy
  - Fixed-priority Arbitration
  - Round-Robin Arbitration, either with no default master, last accessed default master or fixed default master
- Burst Management
  - Breaking with Slot Cycle Limit Support
  - Undefined Burst Length Support
- One Address Decoder provided per Master
  - Three different slaves may be assigned to each decoded memory area: one for internal boot, one for external boot, one after remap



- Boot Mode Select
  - Non-volatile Boot Memory can be internal or external
  - Selection is made by BMS pin sampled at reset
- Remap Command
  - Allows Remapping of an Internal SRAM in Place of the Boot Non-Volatile Memory
  - Allows Handling of Dynamic Exception Vectors

### 7.3 Matrix Masters

The Bus Matrix of the AT91SAM9263 manages nine masters, thus each master can perform an access concurrently with others to an available slave peripheral or memory.

Each master has its own decoder, which is defined specifically for each master.

**Table 7-1. List of Bus Matrix Masters**

Master 0	OHCI USB Host Controller
Master 1	Image Sensor Interface
Master 2	Two D Graphic Controller
Master 3	DMA Controller
Master 4	Ethernet MAC
Master 5	LCD Controller
Master 6	Peripheral DMA Controller
Master 7	ARM926 Data
Master 8	ARM926™ Instruction

### 7.4 Matrix Slaves

The Bus Matrix of the AT91SAM9263 manages eight slaves. Each slave has its own arbiter, thus allowing to program a different arbitration per slave.

The LCD Controller, the DMA Controller, the USB OTG and the USB Host have a user interface mapped as a slave on the Matrix. They share the same layer, as programming them does not require a high bandwidth.

**Table 7-2. List of Bus Matrix Slaves**

Slave 0	Internal ROM
Slave 1	Internal 80 Kbyte SRAM
Slave 2	Internal 16 Kbyte SRAM
Slave 3	LCD Controller User Interface
	DMA Controller User Interface
	USB Host User Interface
Slave 4	External Bus Interface 0
Slave 5	External Bus Interface 1
Slave 6	Peripheral Bridge

## 7.5 Master to Slave Access

In most cases, all the masters can access all the slaves. However, some paths do not make sense, for example, allowing access from the Ethernet MAC to the Internal Peripherals. Thus, these paths are forbidden or simply not wired, and are shown as “-” in [Table 7-3](#).

**Table 7-3. Masters to Slaves Access**

Master		0	1	2	3	4	5	6	7&8
Slave		OHCI USB Host Controller	Image Sensor Interface	Two D Graphics Controller	DMA Controller	Ethernet MAC	LCD Controller	Peripheral DMA Controller	ARM926 Data & Instruction
0	Internal ROM	X	X	X	X	X	X	X	X
1	Internal 80 Kbyte SRAM	X	X	X	X	X	X	X	X
2	Internal 16 Kbyte SRAM Bank	X	X	X	X	X	X	X	X
3	LCD Controller User Interface	-	-	-	-	-	-	-	X
	DMA Controller User Interface	-	-	-	-	-	-	-	X
	USB Host User Interface	-	-	-	-	-	-	-	X
4	External Bus Interface 0	X	X	X	X	X	X	X	X
5	External Bus Interface 1	X	X	X	X	X	X	X	X
6	Peripheral Bridge	-	-	-	X	-	-	X	X

## 7.6 Peripheral DMA Controller

- Acts as one Matrix Master
- Allows data transfers between a peripheral and memory without any intervention of the processor
- Next Pointer support, removes heavy real-time constraints on buffer management.
- Twenty channels
  - Two for each USART
  - Two for the Debug Unit
  - Two for each Serial Synchronous Controller
  - Two for each Serial Peripheral Interface
  - Two for the AC97 Controller
  - One for each Multimedia Card Interface

The Peripheral DMA Controller handles transfer requests from the channel according to the following priorities (low to high priorities):

- DBGU Transmit Channel
- USART2 Transmit Channel
- USART1 Transmit Channel
- USART0 Transmit Channel
- AC97 Transmit Channel

- SPI1 Transmit Channel
- SPI0 Transmit Channel
- SSC1 Transmit Channel
- SSC0 Transmit Channel
- DBGU Receive Channel
- USART2 Receive Channel
- USART1 Receive Channel
- USART0 Receive Channel
- AC97 Receive Channel
- SPI1 Receive Channel
- SPI0 Receive Channel
- SSC1 Receive Channel
- SSC0 Receive Channel
- MCI1 Transmit/Receive Channel
- MCI0 Transmit/Receive Channel

## 7.7 DMA Controller

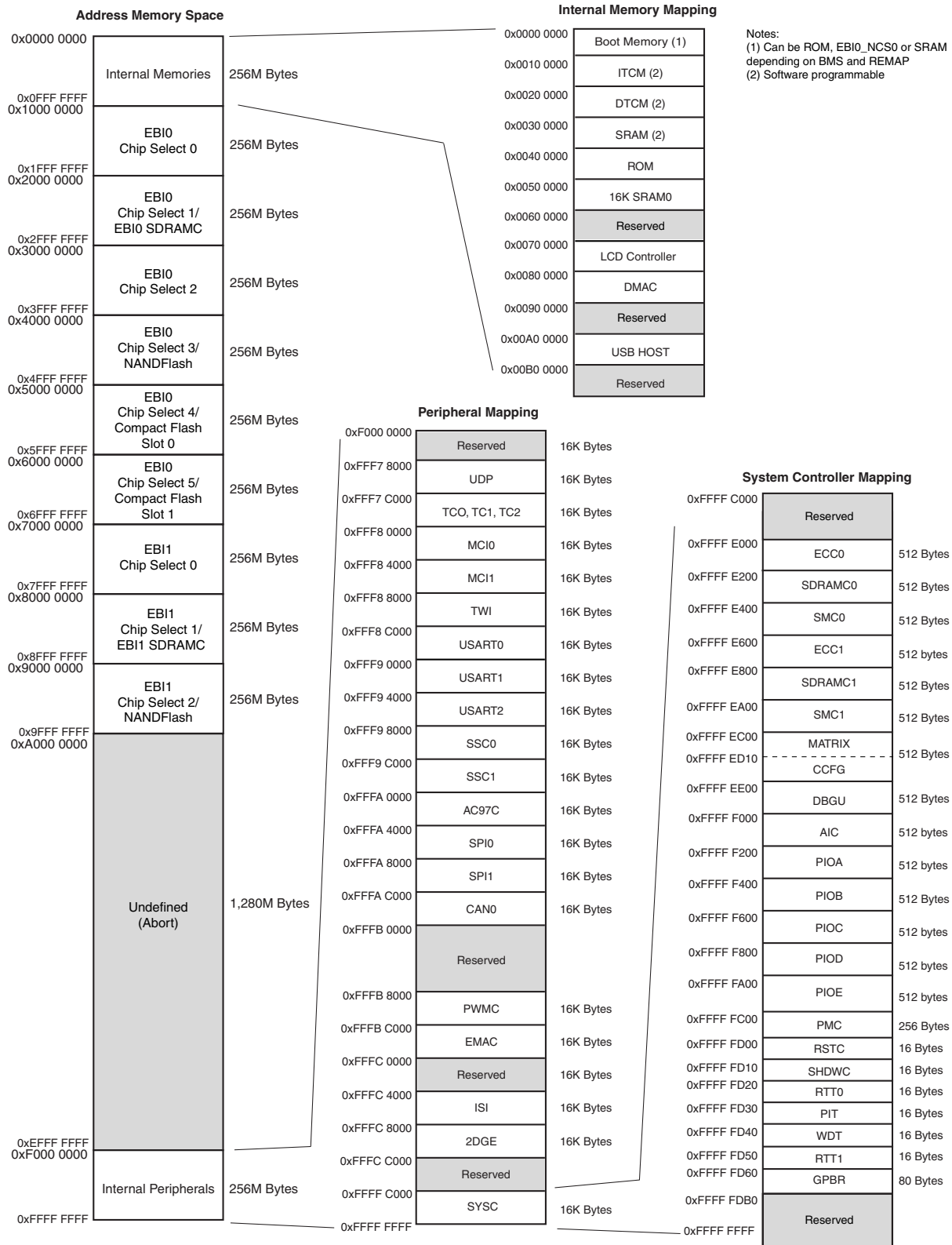
- Acts as one Matrix Master
- Embeds 2 unidirectional channels with programmable priority
- Address Generation
  - Source/destination address programming
  - Address increment, decrement or no change
  - DMA chaining support for multiple non-contiguous data blocks through use of linked lists
  - Scatter support for placing fields into a system memory area from a contiguous transfer. Writing a stream of data into non-contiguous fields in system memory.
  - Gather support for extracting fields from a system memory area into a contiguous transfer
  - User enabled auto-reloading of source, destination and control registers from initially programmed values at the end of a block transfer
  - Auto-loading of source, destination and control registers from system memory at end of block transfer in block chaining mode
  - Unaligned system address to data transfer width supported in hardware
- Channel Buffering
  - Two 8-word FIFOs
  - Automatic packing/unpacking of data to fit FIFO width
- Channel Control
  - Programmable multiple transaction size for each channel
  - Support for cleanly disabling a channel without data loss
  - Suspend DMA operation
  - Programmable DMA lock transfer support.
- Transfer Initiation
  - Supports four external DMA Requests
  - Support for software handshaking interface. Memory mapped registers can be used to control the flow of a DMA transfer in place of a hardware handshaking interface
- Interrupt
  - Programmable interrupt generation on DMA transfer completion, Block transfer completion, Single/Multiple transaction completion or Error condition

## 7.8 Debug and Test Features

- ARM926 Real-time In-circuit Emulator
  - Two real-time Watchpoint Units
  - Two Independent Registers: Debug Control Register and Debug Status Register
  - Test Access Port Accessible through JTAG Protocol
  - Debug Communications Channel
- Debug Unit
  - Two-pin UART
  - Debug Communication Channel Interrupt Handling
  - Chip ID Register
- Embedded Trace Macrocell: ETM9™
  - Medium+ Level Implementation
  - Half-rate Clock Mode
  - Four Pairs of Address Comparators
  - Two Data Comparators
  - Eight Memory Map Decoder Inputs
  - Two 16-bit Counters
  - One 3-stage Sequencer
  - One 45-byte FIFO
- IEEE1149.1 JTAG Boundary-scan on All Digital Pins

# 8. Memories

Figure 8-1. AT91SAM9263 Memory Mapping



A first level of address decoding is performed by the Bus Matrix, i.e., the implementation of the Advanced High Performance Bus (AHB) for its master and slave interfaces with additional features.

Decoding breaks up the 4G bytes of address space into 16 banks of 256M bytes. The banks 1 to 9 are directed to the EBIO that associates these banks to the external chip selects EBIO\_NCS0 to EBIO\_NCS5 and EB11\_NCS0 to EB11\_NCS2. The bank 0 is reserved for the addressing of the internal memories, and a second level of decoding provides 1M bytes of internal memory area. Bank 15 is reserved for the peripherals and provides access to the Advanced Peripheral Bus (APB).

Other areas are unused and performing an access within them provides an abort to the master requesting such an access.

Each master has its own bus and its own decoder, thus allowing a different memory mapping for each master. However, in order to simplify the mappings, all the masters have a similar address decoding.

Regarding Master 0 and Master 1 (ARM926 Instruction and Data), three different slaves are assigned to the memory space decoded at address 0x0: one for internal boot, one for external boot and one after remap. Refer to [Table 8-1, “Internal Memory Mapping,” on page 21](#) for details.

A complete memory map is presented in [Figure 8-1 on page 20](#).

## 8.1 Embedded Memories

- 128 Kbyte ROM
  - Single Cycle Access at full matrix speed
- One 80 Kbyte Fast SRAM
  - Single Cycle Access at full matrix speed
  - Supports ARM926EJ-S TCM interface at full processor speed
  - Allows internal Frame Buffer for up to 1/4 VGA 8 bpp screen
- 16 Kbyte Fast SRAM
  - Single Cycle Access at full matrix speed

### 8.1.1 Internal Memory Mapping

[Table 8-1](#) summarizes the Internal Memory Mapping, depending on the Remap status and the BMS state at reset.

**Table 8-1. Internal Memory Mapping**

Address	REMAP = 0		REMAP = 1
	BMS = 1	BMS = 0	
0x0000 0000	ROM	EBIO_NCS0	SRAM C

#### 8.1.1.1 Internal 80 Kbyte Fast SRAM

The AT91SAM9263 device embeds a high-speed 80 Kbyte SRAM. This internal SRAM is split into three areas. Its memory mapping is presented in [Figure 8-1 on page 20](#).

- Internal SRAM A is the ARM926EJ-S Instruction TCM. The user can map this SRAM block anywhere in the ARM926 instruction memory space using CP15 instructions and the TCR configuration register located in the Chip Configuration User Interface. This SRAM block is also accessible by the ARM926 Data Master and by the AHB Masters through the AHB bus at address 0x0010 0000.
- Internal SRAM B is the ARM926EJ-S Data TCM. The user can map this SRAM block anywhere in the ARM926 data memory space using CP15 instructions. This SRAM block is also accessible by the ARM926 Data Master and by the AHB Masters through the AHB bus at address 0x0020 0000.
- Internal SRAM C is only accessible by all the AHB Masters. After reset and until the Remap Command is performed, this SRAM block is accessible through the AHB bus at address 0x0030 0000 by all the AHB Masters. After Remap, this SRAM block also becomes accessible through the AHB bus at address 0x0 by the ARM926 Instruction and the ARM926 Data Masters.

Within the 80 Kbytes of SRAM available, the amount of memory assigned to each block is software programmable as a multiple of 16 Kbytes as shown in [Table 8-2](#). This table provides the size of the Internal SRAM C according to the size of the internal SRAM A and the internal SRAM B.

**Table 8-2. Internal SRAM Block Size**

Internal SRAM C		Internal SRAM A (ITCM) Size		
		0	16 Kbytes	32 Kbytes
Internal SRAM B (DTCM) size	0	80 Kbytes	64 Kbytes	48 Kbytes
	16 Kbytes	64 Kbytes	48 Kbytes	32 Kbytes
	32 Kbytes	48 Kbytes	32 Kbytes	16 Kbytes

Note that among the five 16 Kbyte blocks making up the Internal SRAM, one is permanently assigned to Internal SRAM C.

At reset, the whole memory (80 Kbytes) is assigned to Internal SRAM C.

The memory blocks assigned to SRAM A, SRAM B and SRAM C areas are not contiguous and when the user dynamically changes the Internal SRAM configuration, the new 16 Kbyte block organization may affect the previous configuration from a software point of view.

[Table 8-3](#) illustrates different configurations and the related 16 Kbyte blocks assignments (RB0 to RB4).

**Table 8-3. 16 Kbyte Block Allocation**

Decoded Area	Address	Configuration examples and related 16 Kbyte block assignments				
		ITCM = 0 Kbyte DTCM = 0 Kbyte AHB = 80 Kbytes <sup>(1)</sup>	ITCM = 32 Kbytes DTCM = 32 Kbytes AHB = 16 Kbytes	ITCM = 16 Kbytes DTCM = 32 Kbytes AHB = 32 Kbytes	ITCM = 32 Kbytes DTCM = 16 Kbytes AHB = 32 Kbytes	ITCM = 16 Kbytes DTCM = 16 Kbytes AHB = 48 Kbytes
Internal SRAM A (ITCM)	0x0010 0000		RB1	RB1	RB1	RB1
	0x0010 4000		RB0		RB0	
Internal SRAM B (DTCM)	0x0020 0000		RB3	RB3	RB3	RB3
	0x0020 4000		RB2	RB2		
Internal SRAM C (AHB)	0x0030 0000	RB4	RB4	RB4	RB4	RB4
	0x0030 4000	RB3		RB0	RB2	RB2
	0x0030 8000	RB2				RB0
	0x0030 C000	RB1				
	0x0031 0000	RB0				

Note: 1. Configuration after reset.

When accessed from the Bus Matrix, the internal 80 Kbytes of Fast SRAM is single cycle accessible at full matrix speed (MCK). When accessed from the processor's TCM Interface, they are also single cycle accessible at full processor speed.

### 8.1.1.2 Internal 16 Kbyte Fast SRAM

The AT91SAM9263 integrates a 16 Kbyte SRAM, mapped at address 0x0050 0000. This SRAM is single cycle accessible at full Bus Matrix speed.

## 8.1.2 Boot Strategies

The system always boots at address 0x0. To ensure maximum boot possibilities, the memory layout can be changed with two parameters.

REMAP allows the user to layout the internal SRAM bank to 0x0. This is done by software once the system has booted. Refer to the section “AT91SAM9263 Bus Matrix” in the product datasheet for more details.

When REMAP = 0, BMS allows the user to layout at address 0x0 either the ROM or an external memory. This is done via hardware at reset.

Note: Memory blocks not affected by these parameters can always be seen at their specified base addresses. See the complete memory map presented in [Figure 8-1 on page 20](#).

The AT91SAM9263 Bus Matrix manages a boot memory that depends on the level on the pin BMS at reset. The internal memory area mapped between address 0x0 and 0x000F FFFF is reserved to this effect.

If BMS is detected at 1, the boot memory is the embedded ROM.

If BMS is detected at 0, the boot memory is the memory connected on the Chip Select 0 of the External Bus Interface.

### 8.1.2.1 BMS = 1, Boot on Embedded ROM

The system boots on Boot Program.

- Boot at slow clock
- Auto baudrate detection
- Downloads and runs an application from external storage media into internal SRAM
- Downloaded code size depends on embedded SRAM size
- Automatic detection of valid application
- Bootloader on a non-volatile memory
  - SD Card
  - NAND Flash
  - SPI DataFlash<sup>®</sup> and Serial Flash connected on NPCS0 of the SPI0
- Interface with SAM-BA<sup>®</sup> Graphic User Interface to enable code loading via:
  - Serial communication on a DBGU
  - USB Bulk Device Port

### 8.1.2.2 BMS = 0, Boot on External Memory

- Boot at slow clock
- Boot with the default configuration for the Static Memory Controller, byte select mode, 16-bit data bus, Read/Write controlled by Chip Select, allows boot on 16-bit non-volatile memory.

The customer-programmed software must perform a complete configuration.

To speed up the boot sequence when booting at 32 kHz EBIO CS0 (BMS=0) the user must:

1. Program the PMC (main oscillator enable or bypass mode).
2. Program and Start the PLL.
3. Reprogram the SMC setup, cycle, hold, mode timings registers for CS0 to adapt them to the new clock.
4. Switch the main clock to the new value.

## 8.2 External Memories

The external memories are accessed through the External Bus Interfaces 0 and 1. Each Chip Select line has a 256 Mbyte memory area assigned.

Refer to [Figure 8-1 on page 20](#).

### 8.2.1 External Bus Interfaces

The AT91SAM9263 features two External Bus Interfaces to offer more bandwidth to the system and to prevent bottlenecks while accessing external memories.



### 8.2.1.1 External Bus Interface 0

- Integrates three External Memory Controllers:
  - Static Memory Controller
  - SDRAM Controller
  - ECC Controller
- Additional logic for NAND Flash and CompactFlash
- Optional Full 32-bit External Data Bus
- Up to 26-bit Address Bus (up to 64 Mbytes linear per chip select)
- Up to 6 Chip Selects, Configurable Assignment:
  - Static Memory Controller on NCS0
  - SDRAM Controller or Static Memory Controller on NCS1
  - Static Memory Controller on NCS2
  - Static Memory Controller on NCS3, Optional NAND Flash support
  - Static Memory Controller on NCS4 - NCS5, Optional CompactFlash support
- Optimized for Application Memory Space

### 8.2.1.2 External Bus Interface 1

- Integrates three External Memory Controllers:
  - Static Memory Controller
  - SDRAM Controller
  - ECC Controller
- Additional logic for NAND Flash
- Optional Full 32-bit External Data Bus
- Up to 23-bit Address Bus (up to 8 Mbytes linear)
- Up to 3 Chip Selects, Configurable Assignment:
  - Static Memory Controller on NCS0
  - SDRAM Controller or Static Memory Controller on NCS1
  - Static Memory Controller on NCS2, Optional NAND Flash support
- Allows supporting an external Frame Buffer for the embedded LCD Controller without impacting processor performance.

### 8.2.2 Static Memory Controller

- 8-, 16- or 32-bit Data Bus
- Multiple Access Modes supported
  - Byte Write or Byte Select Lines
  - Asynchronous read in Page Mode supported (4- up to 32-byte page size)
- Multiple device adaptability
  - Compliant with LCD Module
  - Control signals programmable setup, pulse and hold time for each Memory Bank
- Multiple Wait State Management
  - Programmable Wait State Generation
  - External Wait Request
  - Programmable Data Float Time
- Slow Clock mode supported

### 8.2.3 SDRAM Controller

- Supported devices

- Standard and Low-power SDRAM (Mobile SDRAM)
- Numerous configurations supported
  - **2K, 4K, 8K Row Address Memory Parts**
  - **SDRAM with two or four Internal Banks**
  - **SDRAM with 16- or 32-bit Data Path**
- Programming facilities
  - **Word, half-word, byte access**
  - **Automatic page break when Memory Boundary has been reached**
  - **Multibank Ping-pong Access**
  - **Timing parameters specified by software**
  - **Automatic refresh operation, refresh rate is programmable**
- Energy-saving capabilities
  - **Self-refresh, power down and deep power down modes supported**
- Error detection
  - **Refresh Error Interrupt**
- **SDRAM Power-up Initialization by software**
- **CAS Latency of 1, 2 and 3 supported**
- **Auto Precharge Command not used**

#### 8.2.4 Error Corrected Code Controller

- Tracking the accesses to a NAND Flash device by triggering on the corresponding chip select
- Single-bit error correction and two-bit random detection
- Automatic Hamming Code Calculation while writing
  - ECC value available in a register
- Automatic Hamming Code Calculation while reading
  - Error Report, including error flag, correctable error flag and word address being detected erroneous
  - Support 8- or 16-bit NAND Flash devices with 512-, 1024-, 2048- or 4096-byte pages

## 9. System Controller

The System Controller is a set of peripherals that allow handling of key elements of the system, such as power, resets, clocks, time, interrupts, watchdog, etc.

The System Controller User Interface also embeds registers that are used to configure the Bus Matrix and a set of registers for the chip configuration. The chip configuration registers can be used to configure:

- EBI0 and EBI1 chip select assignment and voltage range for external memories
- ARM Processor Tightly Coupled Memories

The System Controller peripherals are all mapped within the highest 16 Kbytes of address space, between addresses 0xFFFF C000 and 0xFFFF FFFF.

However, all the registers of the System Controller are mapped on the top of the address space. This allows all the registers of the System Controller to be addressed from a single pointer by using the standard ARM instruction set, as the Load/Store instructions have an indexing mode of  $\pm 4$  Kbytes.

[Figure 9-1 on page 26](#) shows the System Controller block diagram.

[Figure 8-1 on page 20](#) shows the mapping of the User Interfaces of the System Controller peripherals.