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32-BIT ARM-BASED MICROPROCESSORS

SAM9N12/SAM9CN11/SAM9CN12

Description

The SAM9N and SAM9CN Arm926EJ-S™-based embedded MPUs offer the frequently-requested combination of user interface functionality and high data rate connectivity, with LCD controller, resistive touchscreen, multiple UARTs, SPI, I2C, full-speed USB Host and Device and SDIO.

These eMPUs support the latest generation of LPDDR/DDR2 and NAND Flash memory interfaces for program and data storage. An internal 133 MHz multi-layer bus architecture associated with eight DMA channels and distributed memory—including a 32-Kbyte SRAM—sustains the high bandwidth required by the processor and the high-speed peripherals.

The SAM9CN devices offer on-chip hardware accelerators with DMA support that enable high-speed data encryption and authentication of transferred data or applications. Supported standards are up to 256-bit AES, and FIPS Publication 180-2 compliant SHA1 and SHA256. A True Random Number Generator is embedded for key generation and exchange protocols. The devices also feature fuse bits for crypto key (SAM9CN12), user configuration (SAM9N12 and SAM9CN11) and device configuration (all). The SAM9CN12 includes a secure Boot ROM; the SAM9N12 and SAM9CN11 include a standard Boot ROM.

The I/Os support 1.8V or 3.3V operation and are independently configurable for the memory interface and peripheral I/Os. This feature eliminates the need for any external level shifters, while 0.8mm ball pitch packages lower PCB cost and complexity.

The SAM9N and SAM9CN power management controllers feature efficient clock gating and a battery backup section that minimizes power consumption in active and standby modes. The following table presents the embedded features of each device.

- Device Configuration

Feature	SAM9N12	SAM9CN11 (for evaluation only)	SAM9CN12
Standard Boot with BSC	✓	✓	–
Secure Boot	–	–	✓
TRNG	✓	✓	✓
AES	–	✓	✓
SHA	–	✓	✓
JTAG Access	✓	✓	–

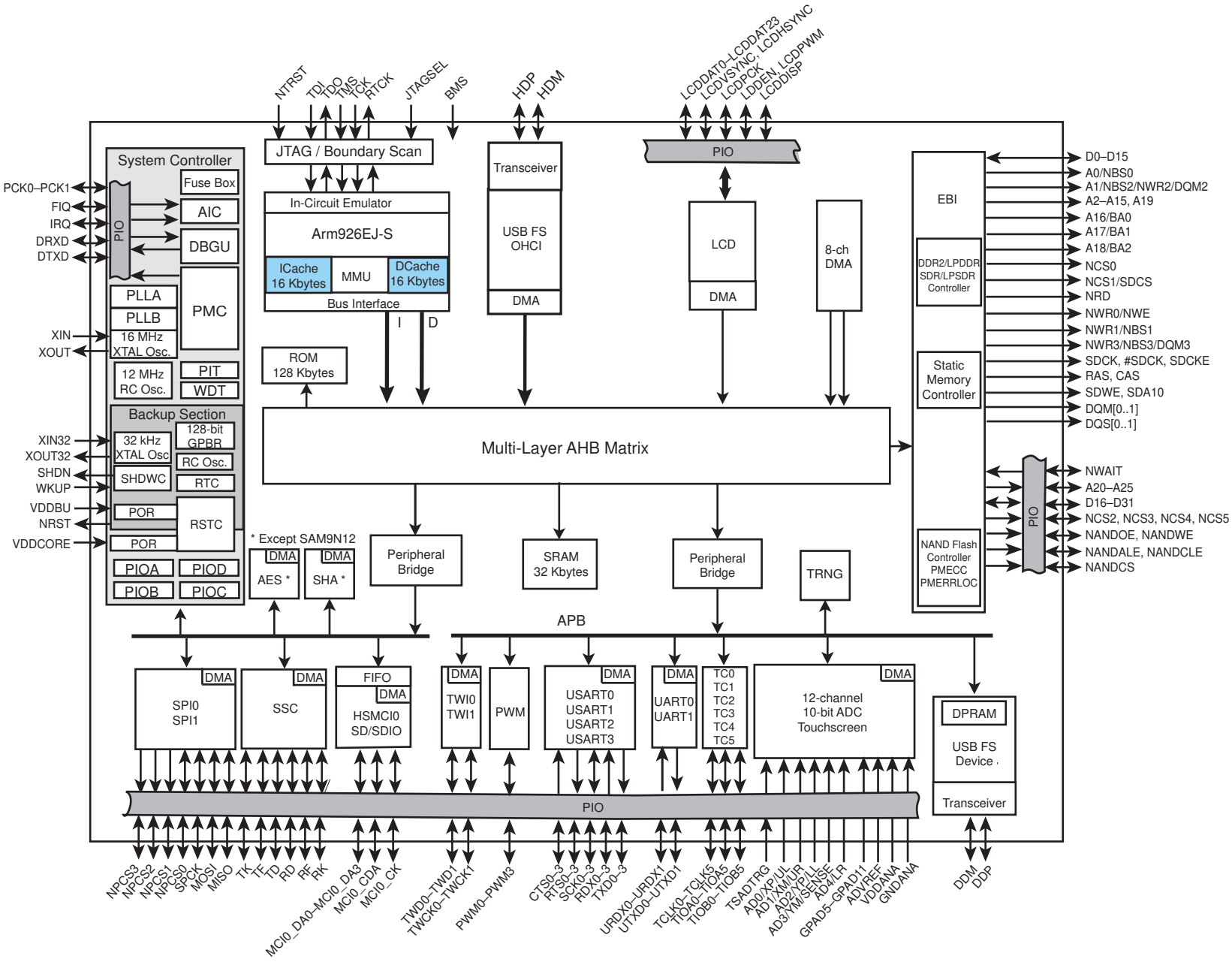
Features

- Core
  - Arm926EJ-S Arm® Thumb® Processor running up to 400 MHz
  - 16 Kbytes Data Cache, 16 Kbytes Instruction Cache, Memory Management Unit
- Memories
  - One 128-Kbyte internal ROM embedding standard or secure bootstrap routine
  - One 32-Kbyte internal SRAM, single-cycle access at system speed
  - 32-bit External Bus Interface supporting 8-bank DDR2/LPDDR, SDR/LPSDR, Static Memories
  - MLC/SLC NAND Controller, with up to 24-bit Programmable Multibit Error Correction Code (PMECC)

- System running up to 133 MHz
  - Power-on Reset, Reset Controller, Shutdown Controller, Periodic Interval Timer, Watchdog Timer and Real Time Clock
  - Boot Mode Select Option, Remap Command
  - Internal Low Power 32 kHz RC and Fast 12 MHz RC Oscillators
  - Selectable 32768 Hz Low-power Oscillator, 16 MHz Oscillator, one PLL for the system and one PLL optimized for USB
  - Six 32-bit-layer AHB Bus Matrix
  - Dual Peripheral Bridge with dedicated programmable clock
  - One dual port 8-channel DMA Controller
  - Advanced Interrupt Controller (AIC)
  - Two Programmable External Clock Signals
- Low-power Mode
  - Shutdown Controller with four 32-bit General-purpose Backup Registers
  - Clock Generator and Power Management Controller
  - Very Slow Clock Operating Mode, Software Programmable Power Optimization Capabilities
- Peripherals
  - LCD Controller
  - USB Device Full Speed with dedicated On-chip Transceiver
  - USB Host Full Speed with dedicated On-chip Transceiver
  - One High speed SD card and SDIO Host Controller
  - Two Master/Slave Serial Peripheral Interfaces (SPI)
  - Two 3-channel 32-bit Timer/Counters (TC)
  - One Synchronous Serial Controller (SSC)
  - One 4-channel 16-bit PWM Controller
  - Two 2-wire Interfaces (TWI)
  - Four Universal Synchronous Asynchronous Receiver Transmitters (USART)
  - Two Universal Asynchronous Receiver Transmitters (UART)
  - One Debug Unit (DBGU)
  - One 12-channel 10-bit Analog-to-Digital Converter with up to 5-wire resistive Touchscreen support
- Safety
  - Crystal Failure Detection
  - Independent Watchdog
  - Power-on Reset Cells
  - Register Write Protection
  - SHA (SHA1 and SHA256) Compliant with FIPS Publication 180-2 (SAM9CN11/SAM9CN12 devices)
- Cryptography
  - True Random Number Generator (TRNG) compliant with NIST Special Publication 800-22
  - AES 256-, 192-, 128-bit Key Algorithm compliant with FIPS Publication 197 (SAM9CN11/SAM9CN12 devices)
  - 256 Fuse bits for crypto key and 64 Fuse bits for device configuration, including JTAG disable and forced boot from the on-chip ROM
- I/O
  - Four 32-bit Parallel Input/Output Controllers
  - 105 Programmable I/O Lines Multiplexed with up to Three Peripheral I/Os
  - Input Change Interrupt Capability on Each I/O Line, optional Schmitt Trigger input
  - Individually Programmable Open-drain, Pull-up and Pull-down Resistor, Synchronous Output
- Packages
  - 217-ball BGA, pitch 0.8 mm
  - 247-ball BGA, pitch 0.5 mm

1. Block Diagram

Figure 1-1: SAM9N12/CN11/CN12 Block Diagram



2. Signal Description

Table 2-1 gives details on the signal names classified by peripheral.

Table 2-1: Signal Description List

Signal Name	Function	Type	Active Level
Clocks, Oscillators and PLLs			
XIN	Main Oscillator Input	Input	–
XOUT	Main Oscillator Output	Output	–
XIN32	Slow Clock Oscillator Input	Input	–
XOUT32	Slow Clock Oscillator Output	Output	–
PCK0–PCK1	Programmable Clock Output	Output	–
Shutdown, Wakeup Logic			
SHDN	Shut-Down Control	Output	–
WKUP	Wake-Up Input	Input	–
ICE and JTAG			
TCK	Test Clock	Input	–
TDI	Test Data In	Input	–
TDO	Test Data Out	Output	–
TMS	Test Mode Select	Input	–
JTAGSEL	JTAG Selection	Input	–
RTCK	Return Test Clock	Output	–
Reset/Test			
NRST	Microcontroller Reset	I/O	Low
NTRST	Test Reset Signal	Input	–
BMS	Boot Mode Select	**Input**	–
Debug Unit - DBGU			
DRXD	Debug Receive Data	Input	–
DTXD	Debug Transmit Data	Output	–
Advanced Interrupt Controller - AIC			
IRQ	External Interrupt Input	Input	–
FIQ	Fast Interrupt Input	Input	–
PIO Controller - PIOA / PIOB / PIOC / PIOD			
PA0–PA31	Parallel IO Controller A	I/O	–
PB0–PB18	Parallel IO Controller B	I/O	–
PC0–PC31	Parallel IO Controller C	I/O	–
PD0–PD21	Parallel IO Controller D	I/O	–

Table 2-1: Signal Description List (Continued)

Signal Name	Function	Type	Active Level
External Bus Interface - EBI			
D0–D15	Data Bus	I/O	–
D16–D31	Data Bus	I/O	–
A0–A25	Address Bus	Output	–
NWAIT	External Wait Signal	Input	Low
Static Memory Controller - SMC			
NCS0–NCS5	Chip Select Lines	Output	Low
NWR0–NWR3	Write Signal	Output	Low
NRD	Read Signal	Output	Low
NWE	Write Enable	Output	Low
NBS0–NBS3	Byte Mask Signal	Output	Low
NAND Flash Support			
NFD0–NFD15	NAND Flash I/O	I/O	–
NANDCS	NAND Flash Chip Select	Output	Low
NANDOE	NAND Flash Output Enable	Output	Low
NANDWE	NAND Flash Write Enable	Output	Low
DDR2/SDRAM/LPDDR Controller			
SDCK,#SDCK	DDR2/SDRAM differential clock	Output	–
SDCKE	DDR2/SDRAM Clock Enable	Output	High
SDCS	DDR2/SDRAM Controller Chip Select	Output	Low
BA[0..2]	Bank Select	Output	Low
SDWE	DDR2/SDRAM Write Enable	Output	Low
RAS - CAS	Row and Column Signal	Output	Low
SDA10	SDRAM Address 10 Line	Output	–
DQS[0..1]	Data Strobe	I/O	–
DQM[0..3]	Write Data Mask	Output	–
High Speed Multimedia Card Interface - HSMCI			
MCI_CK	Multimedia Card Clock	I/O	–
MCI_CDA	Multimedia Card Slot Command	I/O	–
MCI_DA0–MCI_DA7	Multimedia Card Slot Data	I/O	–
Universal Synchronous Asynchronous Receiver Transmitter - USARTx			
SCKx	USARTx Serial Clock	I/O	–
TXDx	USARTx Transmit Data	Output	–
RXDx	USARTx Receive Data	Input	–
RTSx	USARTx Request To Send	Output	–
CTSx	USARTx Clear To Send	Input	–

Table 2-1: Signal Description List (Continued)

Signal Name	Function	Type	Active Level
Universal Asynchronous Receiver Transmitter - UARTx			
UTXDx	UARTx Transmit Data	Output	–
URXDx	UARTx Receive Data	Input	–
Synchronous Serial Controller - SSC			
TD	SSC Transmit Data	Output	–
RD	SSC Receive Data	Input	–
TK	SSC Transmit Clock	I/O	–
RK	SSC Receive Clock	I/O	–
TF	SSC Transmit Frame Sync	I/O	–
RF	SSC Receive Frame Sync	I/O	–
Timer Counter - TCx (x=0..5)			
TCLKx	TC Channel x External Clock Input	Input	–
TIOAx	TC Channel x I/O Line A	I/O	–
TIOBx	TC Channel x I/O Line B	I/O	–
Serial Peripheral Interface - SPIx			
SPIx_MISO	Master In Slave Out	I/O	–
SPIx_MOSI	Master Out Slave In	I/O	–
SPIx_SPCK	SPI Serial Clock	I/O	–
SPIx_NPCS0	SPI Peripheral Chip Select 0	I/O	Low
SPIx_NPCS1–SPIx_NPCS3	SPI Peripheral Chip Select	Output	Low
Two-wire Interface - TWIx			
TWDx	Two-wire Serial Data	I/O	–
TWCKx	Two-wire Serial Clock	I/O	–
Pulse Width Modulation Controller - PWM			
PWM0–PWM3	Pulse Width Modulation Output	Output	–
USB Device Full Speed Port - UDP			
DDP	USB Device Data +	Analog	–
DDM	USB Device Data -	Analog	–
USB Host Full Speed Port - UHP			
HDP	USB Host Data +	Analog	–
HDM	USB Host Data -	Analog	–

Table 2-1: Signal Description List (Continued)

Signal Name	Function	Type	Active Level
LCD Controller - LCDC			
LCDDAT 0–23	LCD Data Bus	Output	–
LCDVSYNC	LCD Vertical Synchronization	Output	–
LCDHSYNC	LCD Horizontal Synchronization	Output	–
LCDPCK	LCD Pixel Clock	Output	–
LCDDEN	LCD Data Enable	Output	–
LCDPWM	LCD Contrast Control	Output	–
LCDDISP	LCD Display Enable	Output	–
Analog-to-Digital Converter - ADC			
AD0/XP/UL	Top/Upper Left Channel	Analog	–
AD1/XM/UR	Bottom/Upper Right Channel	Analog	–
AD2/YP/LL	Right/Lower Left Channel	Analog	–
AD3/YM/SENSE	Left/Sense Channel	Analog	–
AD4/LR	Lower Right Channel	Analog	–
AD5–AD11	7 Analog Inputs	Analog	–
ADTRG	ADC Trigger	Input	–
ADVREF	ADC Reference	Analog	–

Table 2-2: SAM9N12/CN11/CN12 I/O Type Description

I/O Type	Signal Name	Voltage Range	Analog	Pull-up[1]	Pull-up Value (Ohm)	Pull-down[1]	Pull-down Value (Ohm)	Schmitt Trigger[1]
GPIO	All PIO lines except the lines indicated further on in this table	1.65–3.6V	–	Switchable	50–100K	Switchable	50–100K	Switchable
GPIO_CLK	MCICK, SPI0SPCK, SPI1SPCK	1.65–3.6V	–	Switchable	50–100K	Switchable	50–100K	Switchable
GPIO_CLK2	LCDDOTCK	1.65–3.6V	–	Switchable	50–100K	Switchable	50–100K	Switchable
GPIO_ANA	ADx, GPADx	3.0–3.6V	I	Switchable	50–100K			Switchable
EBI	All data lines (input/output) except the lines indicated further on in this table	1.65–1.95V, 3.0–3.6V	–	Switchable	50–100K	Switchable	50–100K	–
EBI_O	All address and control lines (output only) except the lines indicated further on in this table	1.65–1.95V, 3.0–3.6V	–	Reset State	50–100K	Reset State	50–100K	–

Table 2-2: SAM9N12/CN11/CN12 I/O Type Description (Continued)

I/O Type	Signal Name	Voltage Range	Analog	Pull-up[1]	Pull-up Value (Ohm)	Pull-down[1]	Pull-down Value (Ohm)	Schmitt Trigger[1]
EBI_CLK	SDCK, #SDCK	1.65–1.95V, 3.0–3.6V	–	–	–	–	–	–
RSTJTAG	NRST, NTRST, BMS, TCK, TDI, TMS, TDO, RTCK	3.0–3.6V	–	Reset State	100K	Reset State	100K	Reset State
SYSC	WKUP, SHDN, JTAGSEL	1.65–3.6V	–	Reset State	100k	Reset State	15K	Reset State
USBFS	HDP, HDM, DDP, DDM	3.0–3.6V	I/O	–	–	–	–	–
CLOCK	XIN, XOUT, XIN32, XOUT32	1.65–3.6V	I/O	–	–	–	–	–

Note 1: When “Reset State” is stated, the configuration is defined by the “Reset State” column of the Pin Description table.

3. Package and Pinout

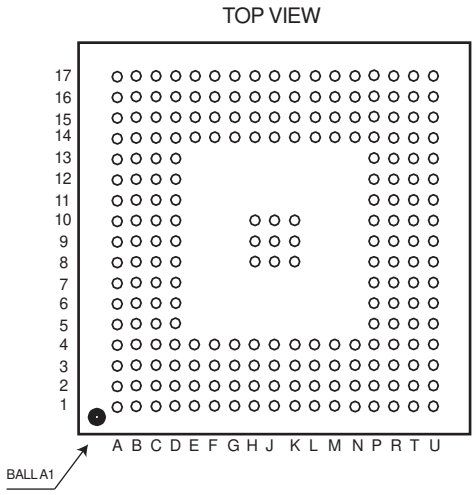
The SAM9N12/SAM9CN11/SAM9CN12 is available in the following Green-compliant packages:

- 217-ball BGA, pitch 0.8 mm
- 247-ball BGA, pitch 0.5 mm

3.1 217-ball BGA Package Outline

Figure 3-1 shows the orientation of the 217-ball BGA package.

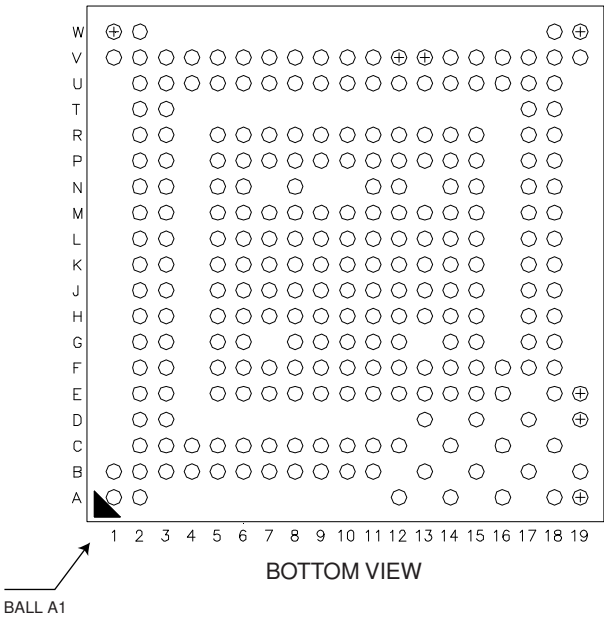
Figure 3-1: Orientation of the 217-ball BGA Package



3.2 247-ball BGA Package Outline

Figure 3-2 shows the orientation of the 247-ball BGA package.

Figure 3-2: Orientation of the 247-ball BGA Package



3.3 217-ball BGA Package Pinout

Table 3-1: BGA217 Pin Description

Ball	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State
			Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, ST
T3	VDDIOP0	GPIO	PA0	I/O	–	–	TXD0	O	SPI1_NPCS1	O	–	–	PIO, I, PU, ST
U2	VDDIOP0	GPIO	PA1	I/O	–	–	RXD0	I	SPI0_NPCS2	O	–	–	PIO, I, PU, ST
U3	VDDIOP0	GPIO	PA2	I/O	–	–	RTS0	O	–	–	–	–	PIO, I, PU, ST
P4	VDDIOP0	GPIO	PA3	I/O	–	–	CTS0	I	–	–	–	–	PIO, I, PU, ST
T4	VDDIOP0	GPIO	PA4	I/O	–	–	SCK0	I/O	–	–	–	–	PIO, I, PU, ST
U4	VDDIOP0	GPIO	PA5	I/O	–	–	TXD1	O	–	–	–	–	PIO, I, PU, ST
P5	VDDIOP0	GPIO	PA6	I/O	–	–	RXD1	I	–	–	–	–	PIO, I, PU, ST
R4	VDDIOP0	GPIO	PA7	I/O	–	–	TXD2	O	SPI0_NPCS1	O	–	–	PIO, I, PU, ST
U6	VDDIOP0	GPIO	PA8	I/O	–	–	RXD2	I	SPI1_NPCS0	I/O	–	–	PIO, I, PU, ST
R5	VDDIOP0	GPIO	PA9	I/O	–	–	DRXD	I	–	–	–	–	PIO, I, PU, ST
R6	VDDIOP0	GPIO	PA10	I/O	–	–	DTXD	O	–	–	–	–	PIO, I, PU, ST
T5	VDDIOP0	GPIO	PA11	I/O	–	–	SPI0_MISO	I/O	MCDA4	I/O	–	–	PIO, I, PU, ST
T6	VDDIOP0	GPIO	PA12	I/O	–	–	SPI0_MOSI	I/O	MCDA5	I/O	–	–	PIO, I, PU, ST
U5	VDDIOP0	GPIO_CLK	PA13	I/O	–	–	SPI0_SPCK	I/O	MCDA6	I/O	–	–	PIO, I, PU, ST
U7	VDDIOP0	GPIO	PA14	I/O	–	–	SPI0_NPCS0	I/O	MCDA7	I/O	–	–	PIO, I, PU, ST
T7	VDDIOP0	GPIO	PA15	I/O	–	–	MCDA0	I/O	–	–	–	–	PIO, I, PU, ST
R7	VDDIOP0	GPIO	PA16	I/O	–	–	MCCDA	I/O	–	–	–	–	PIO, I, PU, ST
U8	VDDIOP0	GPIO_CLK	PA17	I/O	–	–	MCCK	I/O	–	–	–	–	PIO, I, PU, ST
P8	VDDIOP0	GPIO	PA18	I/O	–	–	MCDA1	I/O	–	–	–	–	PIO, I, PU, ST
T8	VDDIOP0	GPIO	PA19	I/O	–	–	MCDA2	I/O	–	–	–	–	PIO, I, PU, ST
R8	VDDIOP0	GPIO	PA20	I/O	–	–	MCDA3	I/O	–	–	–	–	PIO, I, PU, ST
U9	VDDIOP0	GPIO	PA21	I/O	–	–	TIOA0	I/O	SPI1_MISO	I/O	–	–	PIO, I, PU, ST
U10	VDDIOP0	GPIO	PA22	I/O	–	–	TIOA1	I/O	SPI1_MOSI	I/O	–	–	PIO, I, PU, ST
T9	VDDIOP0	GPIO_CLK	PA23	I/O	–	–	TIOA2	I/O	SPI1_SPCK	I/O	–	–	PIO, I, PU, ST
U11	VDDIOP0	GPIO	PA24	I/O	–	–	TCLK0	I	TK	I/O	–	–	PIO, I, PU, ST
T10	VDDIOP0	GPIO	PA25	I/O	–	–	TCLK1	I	TF	I/O	–	–	PIO, I, PU, ST
R9	VDDIOP0	GPIO	PA26	I/O	–	–	TCLK2	I	TD	O	–	–	PIO, I, PU, ST
U12	VDDIOP0	GPIO	PA27	I/O	–	–	TIOB0	I/O	RD	I	–	–	PIO, I, PU, ST
T11	VDDIOP0	GPIO	PA28	I/O	–	–	TIOB1	I/O	RK	I/O	–	–	PIO, I, PU, ST
U13	VDDIOP0	GPIO	PA29	I/O	–	–	TIOB2	I/O	RF	I/O	–	–	PIO, I, PU, ST
R10	VDDIOP0	GPIO	PA30	I/O	–	–	TWD0	I/O	SPI1_NPCS3	O	–	–	PIO, I, PU, ST
T12	VDDIOP0	GPIO	PA31	I/O	–	–	TWCK0	O	SPI1_NPCS2	O	–	–	PIO, I, PU, ST
E4	VDDANA	GPIO	PB0	I/O	–	–	–	–	RTS2	O	–	–	PIO, I, PU, ST
F3	VDDANA	GPIO	PB1	I/O	–	–	–	–	CTS2	I	–	–	PIO, I, PU, ST
F4	VDDANA	GPIO	PB2	I/O	–	–	–	–	SCK2	I/O	–	–	PIO, I, PU, ST
F2	VDDANA	GPIO	PB3	I/O	–	–	–	–	SPI0_NPCS3	O	–	–	PIO, I, PU, ST
G4	VDDANA	GPIO_CLK	PB4	I/O	–	–	–	–	–	–	–	–	PIO, I, PU, ST
G3	VDDANA	GPIO	PB5	I/O	–	–	–	–	–	–	–	–	PIO, I, PU, ST

Table 3-1: BGA217 Pin Description (Continued)

Ball	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State
			Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, ST
D2	VDDANA	GPIO_ANA	PB6	I/O	AD7	I	–	–	–	–	–	–	PIO, I, PU, ST
E2	VDDANA	GPIO_ANA	PB7	I/O	AD8	I	–	–	–	–	–	–	PIO, I, PU, ST
D1	VDDANA	GPIO_ANA	PB8	I/O	AD9	I	–	–	–	–	–	–	PIO, I, PU, ST
F1	VDDANA	GPIO_ANA	PB9	I/O	AD10	I	–	–	PCK1	O	–	–	PIO, I, PU, ST
E1	VDDANA	GPIO_ANA	PB10	I/O	AD11	I	–	–	PCK0	O	–	–	PIO, I, PU, ST
A1	VDDANA	GPIO_ANA	PB11	I/O	AD0	I	–	–	PWM0	O	–	–	PIO, I, PU, ST
C3	VDDANA	GPIO_ANA	PB12	I/O	AD1	I	–	–	PWM1	O	–	–	PIO, I, PU, ST
B1	VDDANA	GPIO_ANA	PB13	I/O	AD2	I	–	–	PWM2	O	–	–	PIO, I, PU, ST
C2	VDDANA	GPIO_ANA	PB14	I/O	AD3	I	–	–	PWM3	O	–	–	PIO, I, PU, ST
D3	VDDANA	GPIO_ANA	PB15	I/O	AD4	I	–	–	–	–	–	–	PIO, I, PU, ST
C1	VDDANA	GPIO_ANA	PB16	I/O	AD5	I	–	–	–	–	–	–	PIO, I, PU, ST
E3	VDDANA	GPIO_ANA	PB17	I/O	AD6	I	–	–	–	–	–	–	PIO, I, PU, ST
D4	VDDANA	GPIO	PB18	I/O	–	–	IRQ	I	ADTRG	I	–	–	PIO, I, PU, ST
G2	VDDIOP1	GPIO	PC0	I/O	–	–	LCDDAT0	O	–	–	TWD1	I/O	PIO, I, PU, ST
G1	VDDIOP1	GPIO	PC1	I/O	–	–	LCDDAT1	O	–	–	TWCK1	O	PIO, I, PU, ST
H4	VDDIOP1	GPIO	PC2	I/O	–	–	LCDDAT2	O	–	–	TIOA3	I/O	PIO, I, PU, ST
J1	VDDIOP1	GPIO	PC3	I/O	–	–	LCDDAT3	O	–	–	TIOB3	I/O	PIO, I, PU, ST
H3	VDDIOP1	GPIO	PC4	I/O	–	–	LCDDAT4	O	–	–	TCLK3	I	PIO, I, PU, ST
J3	VDDIOP1	GPIO	PC5	I/O	–	–	LCDDAT5	O	–	–	TIOA4	I/O	PIO, I, PU, ST
H2	VDDIOP1	GPIO	PC6	I/O	–	–	LCDDAT6	O	–	–	TIOB4	I/O	PIO, I, PU, ST
H1	VDDIOP1	GPIO	PC7	I/O	–	–	LCDDAT7	O	–	–	TCLK4	I	PIO, I, PU, ST
K2	VDDIOP1	GPIO	PC8	I/O	–	–	LCDDAT8	O	–	–	UTXD0	O	PIO, I, PU, ST
J2	VDDIOP1	GPIO	PC9	I/O	–	–	LCDDAT9	O	–	–	URXD0	I	PIO, I, PU, ST
L1	VDDIOP1	GPIO	PC10	I/O	–	–	LCDDAT10	O	–	–	PWM0	O	PIO, I, PU, ST
K1	VDDIOP1	GPIO	PC11	I/O	–	–	LCDDAT11	O	–	–	PWM1	O	PIO, I, PU, ST
L2	VDDIOP1	GPIO	PC12	I/O	–	–	LCDDAT12	O	–	–	TIOA5	I/O	PIO, I, PU, ST
K3	VDDIOP1	GPIO	PC13	I/O	–	–	LCDDAT13	O	–	–	TIOB5	I/O	PIO, I, PU, ST
M1	VDDIOP1	GPIO	PC14	I/O	–	–	LCDDAT14	O	–	–	TCLK5	I	PIO, I, PU, ST
M2	VDDIOP1	GPIO_CLK	PC15	I/O	–	–	LCDDAT15	O	–	–	PCK0	O	PIO, I, PU, ST
K4	VDDIOP1	GPIO	PC16	I/O	–	–	LCDDAT16	O	–	–	UTXD1	O	PIO, I, PU, ST
M3	VDDIOP1	GPIO	PC17	I/O	–	–	LCDDAT17	O	–	–	URXD1	I	PIO, I, PU, ST
N1	VDDIOP1	GPIO	PC18	I/O	–	–	LCDDAT18	O	–	–	PWM0	O	PIO, I, PU, ST
N2	VDDIOP1	GPIO	PC19	I/O	–	–	LCDDAT19	O	–	–	PWM1	O	PIO, I, PU, ST
N3	VDDIOP1	GPIO	PC20	I/O	–	–	LCDDAT20	O	–	–	PWM2	O	PIO, I, PU, ST
P1	VDDIOP1	GPIO	PC21	I/O	–	–	LCDDAT21	O	–	–	PWM3	O	PIO, I, PU, ST
P2	VDDIOP1	GPIO	PC22	I/O	–	–	LCDDAT22	O	TXD3	O	–	–	PIO, I, PU, ST
P3	VDDIOP1	GPIO	PC23	I/O	–	–	LCDDAT23	O	RXD3	I	–	–	PIO, I, PU, ST
R1	VDDIOP1	GPIO	PC24	I/O	–	–	LCDDISP	O	RTS3	O	–	–	PIO, I, PU, ST
R3	VDDIOP1	GPIO	PC25	I/O	–	–	–		CTS3	I	–	–	PIO, I, PU, ST
R2	VDDIOP1	GPIO	PC26	I/O	–	–	LCDPWM	O	SCK3	I/O			PIO, I, PU, ST

Table 3-1: BGA217 Pin Description (Continued)

Ball	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State
			Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, ST
T1	VDDIOP1	GPIO	PC27	I/O	–	–	LCDVSYNC	O	–	–	RTS1	O	PIO, I, PU, ST
M4	VDDIOP1	GPIO	PC28	I/O	–	–	LCDHSYNC	O	–	–	CTS1	I	PIO, I, PU, ST
N4	VDDIOP1	GPIO_CLK	PC29	I/O	–	–	LCDDEN	O	–	–	SCK1	I/O	PIO, I, PU, ST
T2	VDDIOP1	GPIO_CLK2	PC30	I/O	–	–	LCDPCK	O	–	–	–	–	PIO, I, PU, ST
U1	VDDIOP1	GPIO	PC31	I/O	–	–	FIQ	I	–	–	PCK1	O	PIO, I, PU, ST
P15	VDDNF	EBI	PD0	I/O	–	–	NANDOE	O	–	–	–	–	PIO, I, PU
N14	VDDNF	EBI	PD1	I/O	–	–	NANDWE	O	–	–	–	–	PIO, I, PU
M15	VDDNF	EBI	PD2	I/O	–	–	A21/NANDALE	O	–	–	–	–	A21,O, PD
M14	VDDNF	EBI	PD3	I/O	–	–	A22/NANDCLE	O	–	–	–	–	A22,O, PD
P16	VDDNF	EBI	PD4	I/O	–	–	NCS3	O	–	–	–	–	PIO, I, PU
M17	VDDNF	EBI	PD5	I/O	–	–	NWAIT	I	–	–	–	–	PIO, I, PU
L15	VDDNF	EBI	PD6	I/O	–	–	D16	O	–	–	–	–	PIO, I, PU
L16	VDDNF	EBI	PD7	I/O	–	–	D17	O	–	–	–	–	PIO, I, PU
L17	VDDNF	EBI	PD8	I/O	–	–	D18	O	–	–	–	–	PIO, I, PU
K17	VDDNF	EBI	PD9	I/O	–	–	D19	O	–	–	–	–	PIO, I, PU
K16	VDDNF	EBI	PD10	I/O	–	–	D20	O	–	–	–	–	PIO, I, PU
K15	VDDNF	EBI	PD11	I/O	–	–	D21	O	–	–	–	–	PIO, I, PU
J17	VDDNF	EBI	PD12	I/O	–	–	D22	O	–	–	–	–	PIO, I, PU
J16	VDDNF	EBI	PD13	I/O	–	–	D23	O	–	–	–	–	PIO, I, PU
H17	VDDNF	EBI	PD14	I/O	–	–	D24	O	–	–	–	–	PIO, I, PU
J15	VDDNF	EBI	PD15	I/O	–	–	D25	O	A20	O	–	–	A20, O, PD
G17	VDDNF	EBI	PD16	I/O	–	–	D26	O	A23	O	–	–	A23, O, PD
H16	VDDNF	EBI	PD17	I/O	–	–	D27	O	A24	O	–	–	A24, O, PD
H15	VDDNF	EBI	PD18	I/O	–	–	D28	O	A25	O	–	–	A25, O, PD
F17	VDDNF	EBI	PD19	I/O	–	–	D29	O	NCS2	O	–	–	PIO, I, PU
G16	VDDNF	EBI	PD20	I/O	–	–	D30	O	NCS4	O	–	–	PIO, I, PU
E17	VDDNF	EBI	PD21	I/O	–	–	D31	O	NCS5	O	–	–	PIO, I, PU
H8 H9 H10	VDDIOM	POWER	VDDIOM	I	–	–	–	–	–	–	–	–	I
J14 K14 L14	VDDNF	POWER	VDDNF	I	–	–	–	–	–	–	–	–	I
J8 J9 J10 K9 K10	GNDIOM	GND	GNDIOM	I	–	–	–	–	–	–	–	–	I
P9 P12	VDDIOP0	POWER	VDDIOP0	I	–	–	–	–	–	–	–	–	I
L3 L4	VDDIOP1	POWER	VDDIOP1	I	–	–	–	–	–	–	–	–	I
P6 P7 P13	GNDIOP	GND	GNDIOP	I	–	–	–	–	–	–	–	–	I

Table 3-1: BGA217 Pin Description (Continued)

Ball	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State
			Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, ST
D6	VDDBU	POWER	VDDBU	I	–	–	–	–	–	–	–	–	I
D5 B3	GNDBU	GND	GNDBU	I	–	–	–	–	–	–	–	–	I
C4	VDDANA	POWER	VDDANA	I	–	–	–	–	–	–	–	–	I
B2	GNDANA	GND	GNDANA	I	–	–	–	–	–	–	–	–	I
T16	VDDPLL	POWER	VDDPLL	I	–	–	–	–	–	–	–	–	I
P14	GNDPLL	GND	GNDPLL	I	–	–	–	–	–	–	–	–	I
R14	VDDOSC	POWER	VDDOSC	I	–	–	–	–	–	–	–	–	I
R15	VDDUSB	POWER	VDDUSB	I	–	–	–	–	–	–	–	–	I
N16	VDDFUSE	POWER	VDDFUSE	I	–	–	–	–	–	–	–	–	I
M16	GNDFUSE	GND	GNDFUSE	I	–	–	–	–	–	–	–	–	I
T17	GNDUSB	GND	GNDUSB	I	–	–	–	–	–	–	–	–	I
C8 G15 J4 P10	VDDCORE	POWER	VDDCORE	I	–	–	–	–	–	–	–	–	I
D8 H14 K8 P11	GNDCORE	GND	GNDCORE	I	–	–	–	–	–	–	–	–	I
B14	VDDIOM	EBI	D0	I/O	–	–	–	–	–	–	–	–	O, PD
A14	VDDIOM	EBI	D1	I/O	–	–	–	–	–	–	–	–	O, PD
C14	VDDIOM	EBI	D2	I/O	–	–	–	–	–	–	–	–	O, PD
D13	VDDIOM	EBI	D3	I/O	–	–	–	–	–	–	–	–	O, PD
C13	VDDIOM	EBI	D4	I/O	–	–	–	–	–	–	–	–	O, PD
B13	VDDIOM	EBI	D5	I/O	–	–	–	–	–	–	–	–	O, PD
A13	VDDIOM	EBI	D6	I/O	–	–	–	–	–	–	–	–	O, PD
C12	VDDIOM	EBI	D7	I/O	–	–	–	–	–	–	–	–	O, PD
D12	VDDIOM	EBI	D8	I/O	–	–	–	–	–	–	–	–	O, PD
B12	VDDIOM	EBI	D9	I/O	–	–	–	–	–	–	–	–	O, PD
C11	VDDIOM	EBI	D10	I/O	–	–	–	–	–	–	–	–	O, PD
D11	VDDIOM	EBI	D11	I/O	–	–	–	–	–	–	–	–	O, PD
A12	VDDIOM	EBI	D12	I/O	–	–	–	–	–	–	–	–	O, PD
B11	VDDIOM	EBI	D13	I/O	–	–	–	–	–	–	–	–	O, PD
A11	VDDIOM	EBI	D14	I/O	–	–	–	–	–	–	–	–	O, PD
C10	VDDIOM	EBI	D15	I/O	–	–	–	–	–	–	–	–	O, PD
D17	VDDIOM	EBI_O	A0	O	NBS0	O	–	–	–	–	–	–	O, PD
C17	VDDIOM	EBI_O	A1	O	NBS2/ DQM2/ NWR2	O	–	–	–	–	–	–	O, PD
F16	VDDIOM	EBI_O	A2	O	–	–	–	–	–	–	–	–	O, PD
B17	VDDIOM	EBI_O	A3	O	–	–	–	–	–	–	–	–	O, PD
A17	VDDIOM	EBI_O	A4	O	–	–	–	–	–	–	–	–	O, PD

Table 3-1: BGA217 Pin Description (Continued)

Ball	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State
			Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, ST
F15	VDDIOM	EBI_O	A5	O	–	–	–	–	–	–	–	–	O, PD
E16	VDDIOM	EBI_O	A6	O	–	–	–	–	–	–	–	–	O, PD
D16	VDDIOM	EBI_O	A7	O	–	–	–	–	–	–	–	–	O, PD
E15	VDDIOM	EBI_O	A8	O	–	–	–	–	–	–	–	–	O, PD
G14	VDDIOM	EBI_O	A9	O	–	–	–	–	–	–	–	–	O, PD
C16	VDDIOM	EBI_O	A10	O	–	–	–	–	–	–	–	–	O, PD
F14	VDDIOM	EBI_O	A11	O	–	–	–	–	–	–	–	–	O, PD
B16	VDDIOM	EBI_O	A12	O	–	–	–	–	–	–	–	–	O, PD
A16	VDDIOM	EBI_O	A13	O	–	–	–	–	–	–	–	–	O, PD
C15	VDDIOM	EBI_O	A14	O	–	–	–	–	–	–	–	–	O, PD
D15	VDDIOM	EBI_O	A15	O	–	–	–	–	–	–	–	–	O, PD
B15	VDDIOM	EBI_O	A16	O	BA0	O	–	–	–	–	–	–	O, PD
E14	VDDIOM	EBI_O	A17	O	BA1	O	–	–	–	–	–	–	O, PD
A15	VDDIOM	EBI_O	A18	O	BA2	O	–	–	–	–	–	–	O, PD
D14	VDDIOM	EBI_O	A19	O	–	–	–	–	–	–	–	–	O, PD
B7	VDDIOM	EBI_O	NCS0	O	–	–	–	–	–	–	–	–	O, PU
C5	VDDIOM	EBI_O	NCS1	O	SDCS	O	–	–	–	–	–	–	O, PU
C7	VDDIOM	EBI_O	NRD	O	–	–	–	–	–	–	–	–	O, PU
A6	VDDIOM	EBI_O	NWR0	O	NWRE	O	–	–	–	–	–	–	O, PU
C6	VDDIOM	EBI_O	NWR1	O	NBS1	O	–	–	–	–	–	–	O, PU
D7	VDDIOM	EBI_O	NWR3	O	NBS3/ DQM3	O	–	–	–	–	–	–	O, PU
A10	VDDIOM	EBI_CLK	SDCK	O	–	–	–	–	–	–	–	–	O
A9	VDDIOM	EBI_CLK	#SDCK	O	–	–	–	–	–	–	–	–	O
D10	VDDIOM	EBI_O	SDCKE	O	–	–	–	–	–	–	–	–	O, PU
B9	VDDIOM	EBI_O	RAS	O	–	–	–	–	–	–	–	–	O, PU
D9	VDDIOM	EBI_O	CAS	O	–	–	–	–	–	–	–	–	O, PU
B10	VDDIOM	EBI_O	SDWE	O	–	–	–	–	–	–	–	–	O, PU
B6	VDDIOM	EBI_O	SDA10	O	–	–	–	–	–	–	–	–	O, PU
C9	VDDIOM	EBI_O	DQM0	O	–	–	–	–	–	–	–	–	O, PU
A8	VDDIOM	EBI_O	DQM1	O	–	–	–	–	–	–	–	–	O, PU
B8	VDDIOM	EBI	DQS0	I/O	–	–	–	–	–	–	–	–	O, PD
A7	VDDIOM	EBI	DQS1	I/O	–	–	–	–	–	–	–	–	O, PD
A2	VDDANA	POWER	ADVREF	I	–	–	–	–	–	–	–	–	I
P17	VDDUSB	USBFS	HDP	I/O	–	–	–	–	–	–	–	–	O, PD
N17	VDDUSB	USBFS	HDM	I/O	–	–	–	–	–	–	–	–	O, PD
R17	VDDUSB	USBFS	DDP	I/O	–	–	–	–	–	–	–	–	O, PD
R16	VDDUSB	USBFS	DDM	I/O	–	–	–	–	–	–	–	–	O, PD
A5	VDDBU	SYSC	WKUP	I	–	–	–	–	–	–	–	–	I, ST
B5	VDDBU	SYSC	SHDN	O	–	–	–	–	–	–	–	–	O, PU

Table 3-1: BGA217 Pin Description (Continued)

Ball	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State
			Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, ST
U15	VDDIOP0	RSTJTAG	BMS	I	–	–	–	–	–	–	–	–	I, PU, ST
B4	VDDBU	SYSC	JTAGSEL	I	–	–	–	–	–	–	–	–	I, PD
R12	VDDIOP0	RSTJTAG	TCK	I	–	–	–	–	–	–	–	–	I, ST
R11	VDDIOP0	RSTJTAG	TDI	I	–	–	–	–	–	–	–	–	I, ST
U14	VDDIOP0	RSTJTAG	TDO	O	–	–	–	–	–	–	–	–	O
T13	VDDIOP0	RSTJTAG	TMS	I	–	–	–	–	–	–	–	–	I, ST
T14	VDDIOP0	RSTJTAG	RTCK	O	–	–	–	–	–	–	–	–	O
R13	VDDIOP0	RSTJTAG	NRST	I/O	–	–	–	–	–	–	–	–	I, PU, ST
T15	VDDIOP0	RSTJTAG	NTRST	I	–	–	–	–	–	–	–	–	I, PU, ST
A4	VDDBU	CLOCK	XIN32	I	–	–	–	–	–	–	–	–	I
A3	VDDBU	CLOCK	XOUT32	O	–	–	–	–	–	–	–	–	O
U17	VDDIOP0	CLOCK	XIN	I	–	–	–	–	–	–	–	–	I
U16	VDDIOP0	CLOCK	XOUT	O	–	–	–	–	–	–	–	–	O
N15	NC	–	–	–	–	–	–	–	–	–	–	–	–

3.4 247-ball BGA Package Pinout

Table 3-2: BGA247 Pin Description

			Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State
Ball	Power Rail	I/O Type	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, ST
P3	VDDIOP0	GPIO	PA0	I/O	–	–	TXD0	O	SPI1_NPCS1	O	–	–	PIO, I, PU, ST
R2	VDDIOP0	GPIO	PA1	I/O	–	–	RXD0	I	SPI0_NPCS2	O	–	–	PIO, I, PU, ST
R9	VDDIOP0	GPIO	PA2	I/O	–	–	RTS0	O	–	–	–	–	PIO, I, PU, ST
N5	VDDIOP0	GPIO	PA3	I/O	–	–	CTS0	I	–	–	–	–	PIO, I, PU, ST
P10	VDDIOP0	GPIO	PA4	I/O	–	–	SCK0	I/O	–	–	–	–	PIO, I, PU, ST
R3	VDDIOP0	GPIO	PA5	I/O	–	–	TXD1	O	–	–	–	–	PIO, I, PU, ST
R10	VDDIOP0	GPIO	PA6	I/O	–	–	RXD1	I	–	–	–	–	PIO, I, PU, ST
T2	VDDIOP0	GPIO	PA7	I/O	–	–	TXD2	O	SPI0_NPCS1	O	–	–	PIO, I, PU, ST
P6	VDDIOP0	GPIO	PA8	I/O	–	–	RXD2	I	SPI1_NPCS0	I/O	–	–	PIO, I, PU, ST
T3	VDDIOP0	GPIO	PA9	I/O	–	–	DRXD	I	–	–	–	–	PIO, I, PU, ST
U2	VDDIOP0	GPIO	PA10	I/O	–	–	DTXD	O	–	–	–	–	PIO, I, PU, ST
P5	VDDIOP0	GPIO	PA11	I/O	–	–	SPI0_MISO	I/O	MCDA4	I/O	–	–	PIO, I, PU, ST
V2	VDDIOP0	GPIO	PA12	I/O	–	–	SPI0_MOSI	I/O	MCDA5	I/O	–	–	PIO, I, PU, ST
V1	VDDIOP0	GPIO_CLK	PA13	I/O	–	–	SPI0_SPCK	I/O	MCDA6	I/O	–	–	PIO, I, PU, ST
W2	VDDIOP0	GPIO	PA14	I/O	–	–	SPI0_NPCS0	I/O	MCDA7	I/O	–	–	PIO, I, PU, ST
W1	VDDIOP0	GPIO	PA15	I/O	–	–	MCDA0	I/O	–	–	–	–	PIO, I, PU, ST
V3	VDDIOP0	GPIO	PA16	I/O	–	–	MCCDA	I/O	–	–	–	–	PIO, I, PU, ST
R5	VDDIOP0	GPIO_CLK	PA17	I/O	–	–	MCCK	I/O	–	–	–	–	PIO, I, PU, ST
U3	VDDIOP0	GPIO	PA18	I/O	–	–	MCDA1	I/O	–	–	–	–	PIO, I, PU, ST
V4	VDDIOP0	GPIO	PA19	I/O	–	–	MCDA2	I/O	–	–	–	–	PIO, I, PU, ST
U4	VDDIOP0	GPIO	PA20	I/O	–	–	MCDA3	I/O	–	–	–	–	PIO, I, PU, ST
V5	VDDIOP0	GPIO	PA21	I/O	–	–	TIOA0	I/O	SPI1_MISO	I/O	–	–	PIO, I, PU, ST
U5	VDDIOP0	GPIO	PA22	I/O	–	–	TIOA1	I/O	SPI1_MOSI	I/O	–	–	PIO, I, PU, ST
R6	VDDIOP0	GPIO_CLK	PA23	I/O	–	–	TIOA2	I/O	SPI1_SPCK	I/O	–	–	PIO, I, PU, ST
R7	VDDIOP0	GPIO	PA24	I/O	–	–	TCLK0	I	TK	I/O	–	–	PIO, I, PU, ST
U6	VDDIOP0	GPIO	PA25	I/O	–	–	TCLK1	I	TF	I/O	–	–	PIO, I, PU, ST
V6	VDDIOP0	GPIO	PA26	I/O	–	–	TCLK2	I	TD	O	–	–	PIO, I, PU, ST
R8	VDDIOP0	GPIO	PA27	I/O	–	–	TIOB0	I/O	RD	I	–	–	PIO, I, PU, ST
U7	VDDIOP0	GPIO	PA28	I/O	–	–	TIOB1	I/O	RK	I/O	–	–	PIO, I, PU, ST
P11	VDDIOP0	GPIO	PA29	I/O	–	–	TIOB2	I/O	RF	I/O	–	–	PIO, I, PU, ST
V7	VDDIOP0	GPIO	PA30	I/O	–	–	TWD0	I/O	SPI1_NPCS3	O	–	–	PIO, I, PU, ST
N12	VDDIOP0	GPIO	PA31	I/O	–	–	TWCK0	O	SPI1_NPCS2	O	–	–	PIO, I, PU, ST
G6	VDDANA	GPIO	PB0	I/O	–	–	–	–	RTS2	O	–	–	PIO, I, PU, ST
E3	VDDANA	GPIO	PB1	I/O	–	–	–	–	CTS2	I	–	–	PIO, I, PU, ST
G5	VDDANA	GPIO	PB2	I/O	–	–	–	–	SCK2	I/O	–	–	PIO, I, PU, ST
F2	VDDANA	GPIO	PB3	I/O	–	–	–	–	SPI0_NPCS3	O	–	–	PIO, I, PU, ST
E2	VDDANA	GPIO_CLK	PB4	I/O	–	–	–	–	–	–	–	–	PIO, I, PU, ST
E5	VDDANA	GPIO	PB5	I/O			–	–	–	–	–	–	PIO, I, PU, ST

Table 3-2: BGA247 Pin Description (Continued)

Ball	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State
			Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, ST
C2	VDDANA	GPIO_ANA	PB6	I/O	AD7	I	–	–	–	–	–	–	PIO, I, PU, ST
B2	VDDANA	GPIO_ANA	PB7	I/O	AD8	I	–	–	–	–	–	–	PIO, I, PU, ST
A2	VDDANA	GPIO_ANA	PB8	I/O	AD9	I	–	–	–	–	–	–	PIO, I, PU, ST
B1	VDDANA	GPIO_ANA	PB9	I/O	AD10	I	–	–	PCK1	O	–	–	PIO, I, PU, ST
A1	VDDANA	GPIO_ANA	PB10	I/O	AD11	I	–	–	PCK0	O	–	–	PIO, I, PU, ST
C7	VDDANA	GPIO_ANA	PB11	I/O	AD0	I	–	–	PWM0	O	–	–	PIO, I, PU, ST
C8	VDDANA	GPIO_ANA	PB12	I/O	AD1	I	–	–	PWM1	O	–	–	PIO, I, PU, ST
D3	VDDANA	GPIO_ANA	PB13	I/O	AD2	I	–	–	PWM2	O	–	–	PIO, I, PU, ST
F5	VDDANA	GPIO_ANA	PB14	I/O	AD3	I	–	–	PWM3	O	–	–	PIO, I, PU, ST
E6	VDDANA	GPIO_ANA	PB15	I/O	AD4	I	–	–	–	–	–	–	PIO, I, PU, ST
C9	VDDANA	GPIO_ANA	PB16	I/O	AD5	I	–	–	–	I	–	–	PIO, I, PU, ST
D2	VDDANA	GPIO_ANA	PB17	I/O	AD6	I	–	–	–	I	–	–	PIO, I, PU, ST
E7	VDDANA	GPIO	PB18	I/O	–	–	IRQ	I	ADTRG	I	–	–	PIO, I, PU, ST
F3	VDDIOP1	GPIO	PC0	I/O	–	–	LCDDAT0	O	–	–	TWD1	I/O	PIO, I, PU, ST
G2	VDDIOP1	GPIO	PC1	I/O	–	–	LCDDAT1	O	–	–	TWCK1	O	PIO, I, PU, ST
L7	VDDIOP1	GPIO	PC2	I/O	–	–	LCDDAT2	O	–	–	TIOA3	I/O	PIO, I, PU, ST
G3	VDDIOP1	GPIO	PC3	I/O	–	–	LCDDAT3	O	–	–	TIOB3	I/O	PIO, I, PU, ST
H5	VDDIOP1	GPIO	PC4	I/O	–	–	LCDDAT4	O	–	–	TCLK3	I	PIO, I, PU, ST
M7	VDDIOP1	GPIO	PC5	I/O	–	–	LCDDAT5	O	–	–	TIOA4	I/O	PIO, I, PU, ST
H3	VDDIOP1	GPIO	PC6	I/O	–	–	LCDDAT6	O	–	–	TIOB4	I/O	PIO, I, PU, ST
H2	VDDIOP1	GPIO	PC7	I/O	–	–	LCDDAT7	O	–	–	TCLK4	I	PIO, I, PU, ST
J3	VDDIOP1	GPIO	PC8	I/O	–	–	LCDDAT8	O	–	–	UTXD0	O	PIO, I, PU, ST
M8	VDDIOP1	GPIO	PC9	I/O	–	–	LCDDAT9	O	–	–	URXD0	I	PIO, I, PU, ST
J5	VDDIOP1	GPIO	PC10	I/O	–	–	LCDDAT10	O	–	–	PWM0	O	PIO, I, PU, ST
K6	VDDIOP1	GPIO	PC11	I/O	–	–	LCDDAT11	O	–	–	PWM1	O	PIO, I, PU, ST
P9	VDDIOP1	GPIO	PC12	I/O	–	–	LCDDAT12	O	–	–	TIOA5	I/O	PIO, I, PU, ST
L6	VDDIOP1	GPIO	PC13	I/O	–	–	LCDDAT13	O	–	–	TIOB5	I/O	PIO, I, PU, ST
J2	VDDIOP1	GPIO	PC14	I/O	–	–	LCDDAT14	O	–	–	TCLK5	I	PIO, I, PU, ST
K3	VDDIOP1	GPIO_CLK	PC15	I/O	–	–	LCDDAT15	O	–	–	PCK0	O	PIO, I, PU, ST
K2	VDDIOP1	GPIO	PC16	I/O	–	–	LCDDAT16	O	–	–	UTXD1	O	PIO, I, PU, ST
K5	VDDIOP1	GPIO	PC17	I/O	–	–	LCDDAT17	O	–	–	URXD1	I	PIO, I, PU, ST
L3	VDDIOP1	GPIO	PC18	I/O	–	–	LCDDAT18	O	–	–	PWM0	O	PIO, I, PU, ST
N8	VDDIOP1	GPIO	PC19	I/O	–	–	LCDDAT19	O	–	–	PWM1	O	PIO, I, PU, ST
L2	VDDIOP1	GPIO	PC20	I/O	–	–	LCDDAT20	O	–	–	PWM2	O	PIO, I, PU, ST
P8	VDDIOP1	GPIO	PC21	I/O	–	–	LCDDAT21	O	–	–	PWM3	O	PIO, I, PU, ST
M3	VDDIOP1	GPIO	PC22	I/O	–	–	LCDDAT22	O	TXD3	O	–	–	PIO, I, PU, ST
L5	VDDIOP1	GPIO	PC23	I/O	–	–	LCDDAT23	O	RXD3	I	–	–	PIO, I, PU, ST
N6	VDDIOP1	GPIO	PC24	I/O	–	–	LCDDISP	O	RTS3	O	–	–	PIO, I, PU, ST
N2	VDDIOP1	GPIO	PC25	I/O	–	–	–	–	CTS3	I	–	–	PIO, I, PU, ST
P7	VDDIOP1	GPIO	PC26	I/O	–	–	LCDPWM	O	SCK3	I/O	–	–	PIO, I, PU, ST

Table 3-2: BGA247 Pin Description (Continued)

Ball	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State
			Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, ST
M2	VDDIOP1	GPIO	PC27	I/O	–	–	LCDVSYNC	O	–	–	RTS1	O	PIO, I, PU, ST
M5	VDDIOP1	GPIO	PC28	I/O	–	–	LCDHSYNC	O	–	–	CTS1	I	PIO, I, PU, ST
N3	VDDIOP1	GPIO_CLK	PC29	I/O	–	–	LCDDEN	O	–	–	SCK1	I/O	PIO, I, PU, ST
M6	VDDIOP1	GPIO_CLK2	PC30	I/O	–	–	LCDPCK	O	–	–	–	–	PIO, I, PU, ST
P2	VDDIOP1	GPIO	PC31	I/O	–	–	FIQ	I	–	–	PCK1	O	PIO, I, PU, ST
R14	VDDNF	EBI	PD0	I/O	–	–	NANDOE	O	–	–	–	–	PIO, I, PU
R15	VDDNF	EBI	PD1	I/O	–	–	NANDWE	O	–	–	–	–	PIO, I, PU
T17	VDDNF	EBI	PD2	I/O	–	–	A21/NANDALE	O	–	–	–	–	A21,O, PD
P15	VDDNF	EBI	PD3	I/O	–	–	A22/NANDCLE	O	–	–	–	–	A22,O, PD
R17	VDDNF	EBI	PD4	I/O	–	–	NCS3	O	–	–	–	–	PIO, I, PU
M15	VDDNF	EBI	PD5	I/O	–	–	NWAIT	I	–	–	–	–	PIO, I, PU
N15	VDDNF	EBI	PD6	I/O	–	–	D16	O	–	–	–	–	PIO, I, PU
V13	VDDNF	EBI	PD7	I/O	–	–	D17	O	–	–	–	–	PIO, I, PU
L14	VDDNF	EBI	PD8	I/O	–	–	D18	O	–	–	–	–	PIO, I, PU
W18	VDDNF	EBI	PD9	I/O	–	–	D19	O	–	–	–	–	PIO, I, PU
V18	VDDNF	EBI	PD10	I/O	–	–	D20	O	–	–	–	–	PIO, I, PU
W19	VDDNF	EBI	PD11	I/O	–	–	D21	O	–	–	–	–	PIO, I, PU
V19	VDDNF	EBI	PD12	I/O	–	–	D22	O	–	–	–	–	PIO, I, PU
N18	VDDNF	EBI	PD13	I/O	–	–	D23	O	–	–	–	–	PIO, I, PU
L15	VDDNF	EBI	PD14	I/O	–	–	D24	O	–	–	–	–	PIO, I, PU
N17	VDDNF	EBI	PD15	I/O	–	–	D25	O	A20	O	–	–	A20, O, PD
M18	VDDNF	EBI	PD16	I/O	–	–	D26	O	A23	O	–	–	A23, O, PD
M17	VDDNF	EBI	PD17	I/O	–	–	D27	O	A24	O	–	–	A24, O, PD
P17	VDDNF	EBI	PD18	I/O	–	–	D28	O	A25	O	–	–	A25, O, PD
L18	VDDNF	EBI	PD19	I/O	–	–	D29	O	NCS2	O	–	–	PIO, I, PU
K15	VDDNF	EBI	PD20	I/O	–	–	D30	O	NCS4	O	–	–	PIO, I, PU
L17	VDDNF	EBI	PD21	I/O	–	–	D31	O	NCS5	O	–	–	PIO, I, PU
E8 E9 E13 F7 F8 F9 G14	VDDIOM	POWER	VDDIOM	I	–	–	–	–	–	–	–	–	I
M14 P13 U10 V9 V10 V11	VDDNF	POWER	VDDNF	I	–	–	–	–	–	–	–	–	I

Table 3-2: BGA247 Pin Description (Continued)

Ball	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State
			Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, ST
H6 H7 J6 J7 J8 F10 F11 F12 F13 F14 F15 F16	GNDIOM	GND	GNDIOM	I	–	–	–	–	–	–	–	–	I
N11 M12 M13	VDDIOP0	POWER	VDDIOP0	I	–	–	–	–	–	–	–	–	I
M9 M10 M11	VDDIOP1	POWER	VDDIOP1	I	–	–	–	–	–	–	–	–	I
L10 L11 L12 L13 V14	GNDIOP	GND	GNDIOP	I	–	–	–	–	–	–	–	–	I
B6	VDDBU	POWER	VDDBU	I	–	–	–	–	–	–	–	–	I
B7	GNDBU	GND	GNDBU	I	–	–	–	–	–	–	–	–	I
F6	VDDANA	POWER	VDDANA	I	–	–	–	–	–	–	–	–	I
C3	GNDANA	GND	GNDANA	I	–	–	–	–	–	–	–	–	I
V17	VDDPLL	POWER	VDDPLL	I	–	–	–	–	–	–	–	–	I
U16	GNDPLL	GND	GNDPLL	I	–	–	–	–	–	–	–	–	I
P14	VDDFUSE	POWER	VDDFUSE	I	–	–	–	–	–	–	–	–	I
N14	GNDFUSE	GND	GNDFUSE	I	–	–	–	–	–	–	–	–	I
R12	VDDOSC	POWER	VDDOSC	I	–	–	–	–	–	–	–	–	I
U13	VDDUSB	POWER	VDDUSB	I	–	–	–	–	–	–	–	–	I
U17	GNDUSB	GND	GNDUSB	I	–	–	–	–	–	–	–	–	I
J12 J13 J14 K10 K11 K12 K13 K14 U15	VDDCORE	POWER	VDDCORE	I	–	–	–	–	–	–	–	–	I
H9 J9 J10 J11 K7 K8 K9 L8 L9	GNDCORE	GND	GNDCORE	I	–	–	–	–	–	–	–	–	I
A19	VDDIOM	EBI	D0	I/O	–	–	–	–	–	–	–	–	O, PD
E15	VDDIOM	EBI	D1	I/O	–	–	–	–	–	–	–	–	O, PD

Table 3-2: BGA247 Pin Description (Continued)

Ball	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State
			Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, ST
C18	VDDIOM	EBI	D2	I/O	–	–	–	–	–	–	–	–	O, PD
D15	VDDIOM	EBI	D3	I/O	–	–	–	–	–	–	–	–	O, PD
B17	VDDIOM	EBI	D4	I/O	–	–	–	–	–	–	–	–	O, PD
E14	VDDIOM	EBI	D5	I/O	–	–	–	–	–	–	–	–	O, PD
C16	VDDIOM	EBI	D6	I/O	–	–	–	–	–	–	–	–	O, PD
A18	VDDIOM	EBI	D7	I/O	–	–	–	–	–	–	–	–	O, PD
B15	VDDIOM	EBI	D8	I/O	–	–	–	–	–	–	–	–	O, PD
G12	VDDIOM	EBI	D9	I/O	–	–	–	–	–	–	–	–	O, PD
C14	VDDIOM	EBI	D10	I/O	–	–	–	–	–	–	–	–	O, PD
D13	VDDIOM	EBI	D11	I/O	–	–	–	–	–	–	–	–	O, PD
A16	VDDIOM	EBI	D12	I/O	–	–	–	–	–	–	–	–	O, PD
A14	VDDIOM	EBI	D13	I/O	–	–	–	–	–	–	–	–	O, PD
B13	VDDIOM	EBI	D14	I/O	–	–	–	–	–	–	–	–	O, PD
H13	VDDIOM	EBI	D15	I/O	–	–	–	–	–	–	–	–	O, PD
J15	VDDIOM	EBI_O	A0	O	NBS0	O	–	–	–	–	–	–	O
K18	VDDIOM	EBI_O	A1	O	NBS2/ DQM2/ NWR2	O	–	–	–	–	–	–	O
K17	VDDIOM	EBI_O	A2	O	–	–	–	–	–	–	–	–	O
H15	VDDIOM	EBI_O	A3	O	–	–	–	–	–	–	–	–	O
J18	VDDIOM	EBI_O	A4	O	–	–	–	–	–	–	–	–	O
J17	VDDIOM	EBI_O	A5	O	–	–	–	–	–	–	–	–	O
G17	VDDIOM	EBI_O	A6	O	–	–	–	–	–	–	–	–	O
H17	VDDIOM	EBI_O	A7	O	–	–	–	–	–	–	–	–	O
H18	VDDIOM	EBI_O	A8	O	–	–	–	–	–	–	–	–	O
H14	VDDIOM	EBI_O	A9	O	–	–	–	–	–	–	–	–	O
G18	VDDIOM	EBI_O	A10	O	–	–	–	–	–	–	–	–	O
F18	VDDIOM	EBI_O	A11	O	–	–	–	–	–	–	–	–	O
F17	VDDIOM	EBI_O	A12	O	–	–	–	–	–	–	–	–	O
E19	VDDIOM	EBI_O	A13	O	–	–	–	–	–	–	–	–	O
D19	VDDIOM	EBI_O	A14	O	–	–	–	–	–	–	–	–	O
E18	VDDIOM	EBI_O	A15	O	–	–	–	–	–	–	–	–	O
G15	VDDIOM	EBI_O	A16	O	BA0	O	–	–	–	–	–	–	O
E16	VDDIOM	EBI_O	A17	O	BA1	O	–	–	–	–	–	–	O
B19	VDDIOM	EBI_O	A18	O	BA2	O	–	–	–	–	–	–	O
D17	VDDIOM	EBI_O	A19	O	–	–	–	–	–	–	–	–	O
B9	VDDIOM	EBI_O	NCS0	O	–	–	–	–	–	–	–	–	O, PU
B8	VDDIOM	EBI_O	NCS1	O	SDCS	O	–	–	–	–	–	–	O, PU
E10	VDDIOM	EBI_O	NRD	O	–	–	–	–	–	–	–	–	O, PU
G10	VDDIOM	EBI_O	NWR0	O	NWRE	O	–	–	–	–	–	–	O, PU
C10	VDDIOM	EBI_O	NWR1	O	NBS1	O	–	–	–	–	–	–	O, PU

Table 3-2: BGA247 Pin Description (Continued)

Ball	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State
			Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, ST
G9	VDDIOM	EBI_O	NWR3	O	NBS3/ DQM3	O	–	–	–	–	–	–	O, PU
B10	VDDIOM	EBI_CLK	SDCK	O	–	–	–	–	–	–	–	–	O
B11	VDDIOM	EBI_CLK	#SDCK	O	–	–	–	–	–	–	–	–	O
C12	VDDIOM	EBI_O	SDCKE	O	–	–	–	–	–	–	–	–	O, PU
G11	VDDIOM	EBI_O	RAS	O	–	–	–	–	–	–	–	–	O, PU
E12	VDDIOM	EBI_O	CAS	O	–	–	–	–	–	–	–	–	O, PU
H12	VDDIOM	EBI_O	SDWE	O	–	–	–	–	–	–	–	–	O, PU
H10	VDDIOM	EBI_O	SDA10	O	–	–	–	–	–	–	–	–	O, PU
A12	VDDIOM	EBI_O	DQM0	O	–	–	–	–	–	–	–	–	O, PU
C11	VDDIOM	EBI_O	DQM1	O	–	–	–	–	–	–	–	–	O, PU
H11	VDDIOM	EBI	DQS0	I/O	–	–	–	–	–	–	–	–	I, PD
E11	VDDIOM	EBI	DQS1	I/O	–	–	–	–	–	–	–	–	I, PD
B3	VDDANA	POWER	ADVREF	I	–	–	–	–	–	–	–	–	I
T18	VDDUSB	USBFS	HDP	I/O	–	–	–	–	–	–	–	–	O, PD
U18	VDDUSB	USBFS	HDM	I/O	–	–	–	–	–	–	–	–	O, PD
P18	VDDUSB	USBFS	DDP	I/O	–	–	–	–	–	–	–	–	O, PD
R18	VDDUSB	USBFS	DDM	I/O	–	–	–	–	–	–	–	–	O, PD
C6	VDDBU	SYSC	WKUP	I	–	–	–	–	–	–	–	–	I, ST
G8	VDDBU	SYSC	SHDN	O	–	–	–	–	–	–	–	–	O, PU
U14	VDDIOP0	RSTJTAG	BMS	I	–	–	–	–	–	–	–	–	I, PU, ST
C4	VDDBU	SYSC	JTAGSEL	I	–	–	–	–	–	–	–	–	I, PD
C5	VDDBU	SYSC	TST	I	–	–	–	–	–	–	–	–	I, PD, ST
V8	VDDIOP0	RSTJTAG	TCK	I	–	–	–	–	–	–	–	–	I, ST
U8	VDDIOP0	RSTJTAG	TDI	I	–	–	–	–	–	–	–	–	I, ST
P12	VDDIOP0	RSTJTAG	TDO	O	–	–	–	–	–	–	–	–	O
R11	VDDIOP0	RSTJTAG	TMS	I	–	–	–	–	–	–	–	–	I, ST
V12	VDDIOP0	RSTJTAG	RTCK	O	–	–	–	–	–	–	–	–	O
U11	VDDIOP0	RSTJTAG	NRST	I/O	–	–	–	–	–	–	–	–	I, PU, ST
U9	VDDIOP0	RSTJTAG	NTRST	I	–	–	–	–	–	–	–	–	I, PU, ST
B4	VDDBU	CLOCK	XIN32	I	–	–	–	–	–	–	–	–	I
B5	VDDBU	CLOCK	XOUT32	O	–	–	–	–	–	–	–	–	O
V16	VDDIOP0	CLOCK	XIN	I	–	–	–	–	–	–	–	–	I
V15	VDDIOP0	CLOCK	XOUT	O	–	–	–	–	–	–	–	–	O
H8	–	–	NC	–	–	–	–	–	–	–	–	–	–
U12	–	–	NC	–	–	–	–	–	–	–	–	–	–
R13	–	–	NC	–	–	–	–	–	–	–	–	–	–

4. Power Considerations

4.1 Power Supplies

The SAM9N12/CN11/CN12 has several types of power supply pins.

Table 4-1 defines the different power supplies rails and the estimated power consumption at typical voltage. For details about power-up and power-down sequences, refer to Section 4.2 ”Power Sequence Requirements”.

Table 4-1: SAM9N12/CN11/CN12 Power Supplies

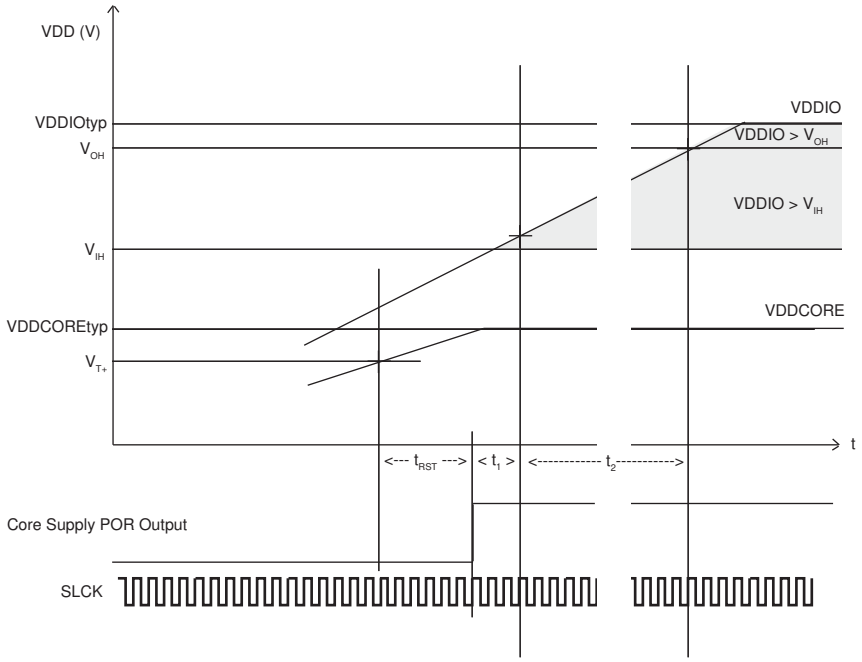
Name	Voltage Range, Nominal	Associated Ground	Powers
VDDCORE	0.9–1.1V, 1.0V	GNDCORE	Core, including the processor, the embedded memories and the peripherals, the internal 12 MHz RC
VDDIOM	1.65–1.95V, 1.8V 3.0–3.6V, 3.3V	GNDIOM	External Memory Interface I/O lines
VDDNF	1.65–1.95V, 1.8V 3.0–3.6V, 3.3V	GNDIOM	NAND Flash I/O and control, D16–D32 and multiplexed SMC lines
VDDIOP0	1.65–3.6V	GNDIOP	Part of Peripherals I/O lines
VDDIOP1	1.65–3.6V	GNDIOP	Part of Peripherals I/O lines
VDDBU	1.65–3.6V	GNDBU	Slow Clock oscillator, the internal 32 Kbyte RC and a part of the System Controller
VDDUSB	3.0–3.6V, 3.3V	GNDUSB	USB interface
VDDPLL	0.9–1.1V, 1.0V	GNDPLL	PLL cells
VDDOSC	1.65–3.6V	GNDPLL	Main Oscillator cells
VDDANA	3.0–3.6V, 3.3V	GNDANA	Analog to Digital Converter
VDDFUSE	3.0–3.6V, 3.3V	GNDFUSE	Fuse box for programming

4.2 Power Sequence Requirements

The AT91 board design must comply with the power-up guidelines below to guarantee reliable operation of the device. Any deviation from these sequences may prevent the device from booting.

4.2.1 Power-Up Sequence

Figure 4-1: VDDCORE and VDDIO Constraints at Startup



VDDCORE and VDDBU are controlled by internal POR (Power-On-Reset) to guarantee that these power sources reach their target values prior to the release of POR.

- VDDIOP must be ≥ V_{IH} (refer to Table 47-2 “DC Characteristics”, for more details), (t_{RST} + t_1) at the latest, after VDDCORE has reached V_{T+}.
- VDDIOM must reach V_{OH} (refer to Table 47-2 “DC Characteristics”, for more details), (t_{RST} + t_1 + t_2) at the latest, after VDDCORE has reached V_{T+}
  - t_{RST} is a POR characteristic
  - $t_1 = 3 \times t_{SLCK}$
  - $t_2 = 16 \times t_{SLCK}$

The t_{SLCK} min (22 µs) is obtained for the maximum frequency of the internal RC oscillator (44 kHz).

  - t_{RST} = 30 µs
  - t_1 = 66 µs
  - t_2 = 352 µs
- VDDPLL is to be established prior to VDDCORE to ensure the PLL is powered once enabled into the ROM code.

As a conclusion, establish VDDIOP and VDDIOM first, then VDDPLL, and VDDCORE at last, to ensure a reliable operation of the device.

4.2.2 Power-Down Sequence

To ensure that the device does not operate outside the operating conditions defined in Table 4-1 “SAM9N12/CN11/CN12 Power Supplies”, it is good practice to first place the device in reset state before removing its power supplies. No specific sequencing is required with respect to its supply channels as long as the NRST line is held active during the the power-down phase.

Figure 4-2: Recommended Power-Down Sequence

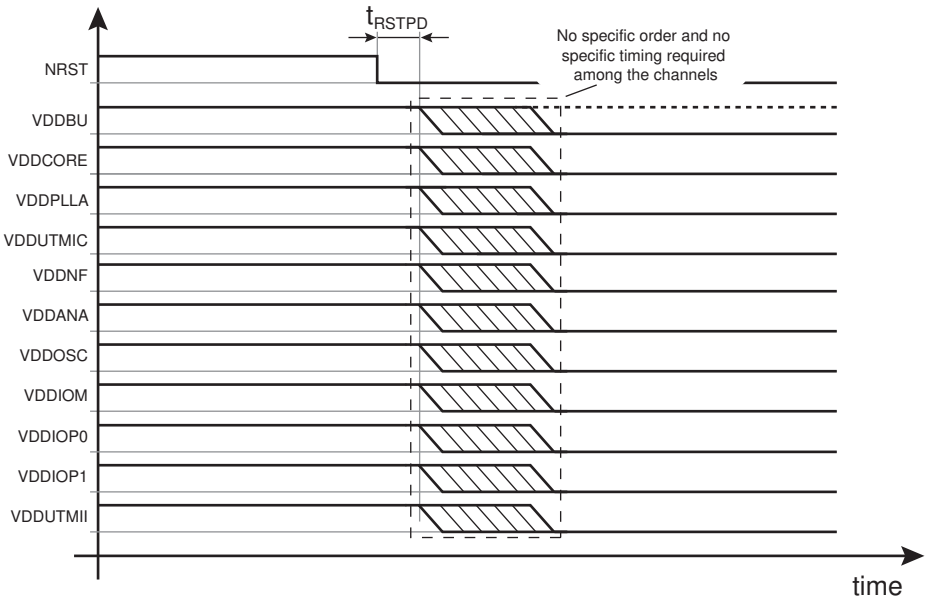


Table 4-2: Power-down Timing Specification

Symbol	Parameter	Conditions	Min	Max	Unit
t_{RSTPD}	Reset Delay at Power-Down	From NRST low to the first supply turn-off	0	–	ms

5. Memories

5.1 Memory Mapping

Figure 5-1 provides the device memory map.

A first level of address decoding is performed by the AHB Bus Matrix, i.e., the implementation of the Advanced High performance Bus (AHB) for its Master and Slave interfaces with additional features.

Decoding breaks up the 4 Gbytes of address space into 16 banks of 256 Mbytes. The banks 1 to 6 are directed to the EBI that associates these banks to the external chip selects EBI_NCS0 to EBI_NCS5. The bank 0 is reserved for the addressing of the internal memories, and a second level of decoding provides 1 Mbyte of internal memory area. Bank 15 is reserved for the peripherals and provides access to the Advanced Peripheral Bus (APB).

Other areas are unused and performing an access within them provides an abort to the master requesting such an access.