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SAM9G15

Atmel | SMART ARM-based Embedded MPU

DATASHEET

Description

The SAM9G15 is a member of the Atmel® | SMART series of 400 MHz ARM926EJ-S™ embedded microprocessor units. This MPU integrates a rich set of peripherals to support embedded industrial applications that require advanced user interfaces and high-speed communication.

The SAM9G15 features a graphics LCD controller with 4-layer overlay and 2D acceleration (picture-in-picture, alpha-blending, scaling, rotation, color conversion), and a 10-bit ADC that supports 4-wire or 5-wire resistive touchscreen panels. Multiple communication interfaces include a soft modem supporting exclusively the Conexant SmartDAA line driver, HS USB Host and Device and FS USB Host with dedicated on-chip transceivers, two HS SDCard/SDIO/MMC interfaces, USARTs, SPIs, I2S and TWIs.

The 10-layer bus matrix coupled with multiple DMA channels ensures uninterrupted data transfers with minimal processor overhead.

The External Bus Interface incorporates controllers for 4-bank and 8-bank DDR2/LPDDR, SDRAM/LPSDRAM, static memories, as well as specific circuitry for MLC/SLC NAND Flash with integrated ECC up to 24 bits.

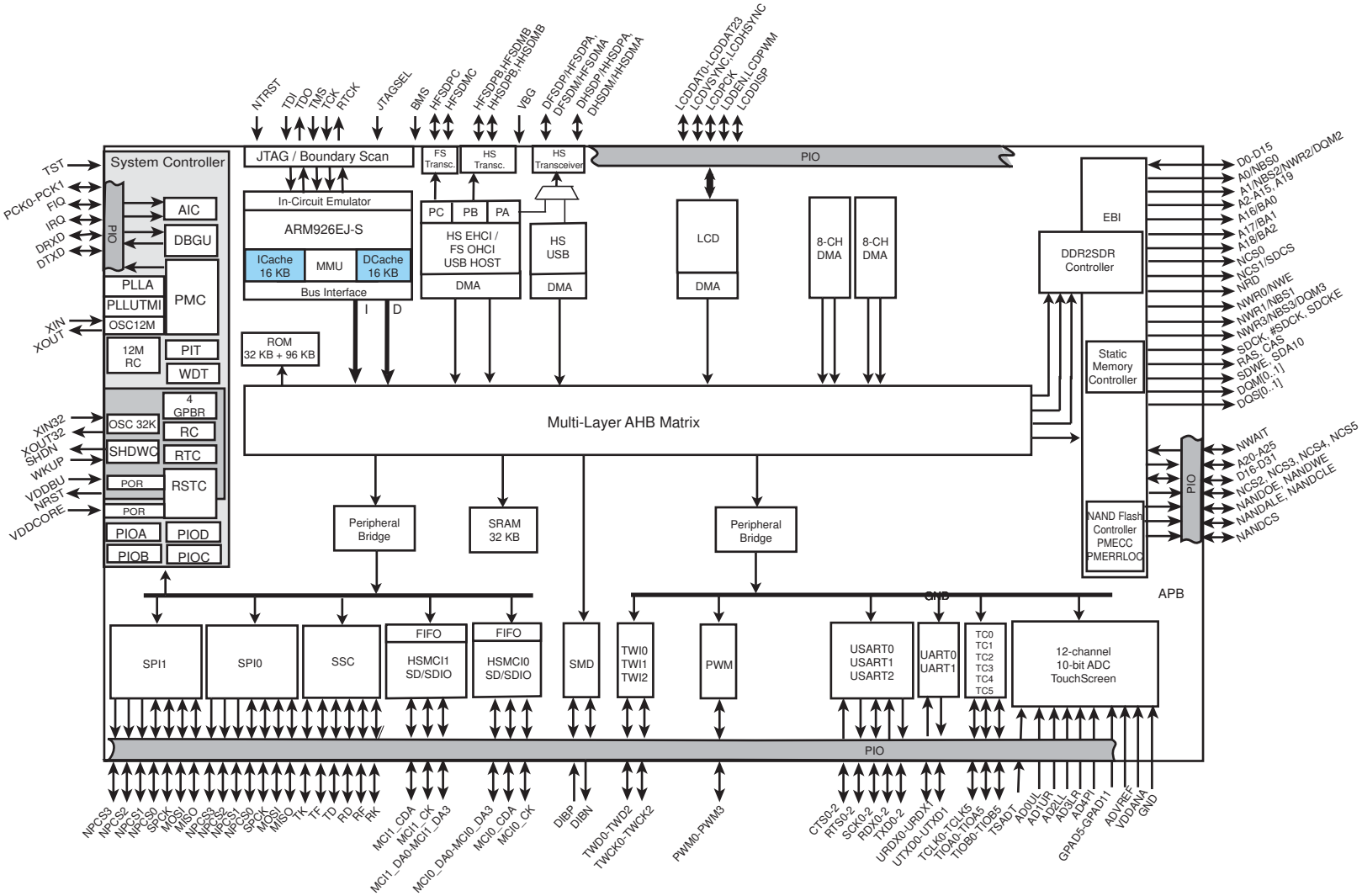
The SAM9G15 is available in a 217-ball BGA package with 0.8 mm ball pitch.

Features

- Core
  - ARM926EJ-S™ ARM® Thumb® Processor running at up to 400 MHz @ 1.0V +/- 10%
  - 16 Kbytes Data Cache, 16 Kbytes Instruction Cache, Memory Management Unit
- Memories
  - One 64-Kbyte internal ROM embedding bootstrap routine: Boot on NAND Flash, SDCard, DataFlash or serial DataFlash. Programmable order.
  - One 32-Kbyte internal SRAM, single-cycle access at system speed
  - High Bandwidth Multi-port DDR SDR SDRAM Controller (DDRSDRC)
  - 32-bit External Bus Interface supporting 4-bank and 8-bank DDR2/LPDDR, SDR/LPSDR, Static Memories
  - MLC/SLC 8-bit NAND Controller, with up to 24-bit Programmable Multi-bit Error Correcting Code (PMECC)
- System running at up to 133 MHz
  - Power-on Reset Cells, Reset Controller, Shutdown Controller, Periodic Interval Timer, Watchdog Timer and Real Time Clock
  - Boot Mode Select Option, Remap Command
  - Internal Low Power 32 kHz RC and Fast 12 MHz RC Oscillators
  - Selectable 32768 Hz Low-power Oscillator and 12 MHz Oscillator
  - One PLL for the system and one PLL at 480 MHz optimized for USB High Speed
  - Twelve 32-bit-layer AHB Bus Matrix for large Bandwidth transfers
  - Dual Peripheral Bridge with dedicated programmable clock for best performances
  - Two dual port 8-channel DMA Controllers (DMAC)
  - Advanced Interrupt Controller (AIC) and Debug Unit (DBGU)
  - Two Programmable External Clock Signals
- Low Power Mode
  - Shutdown Controller with four 32-bit Battery Backup Registers
  - Clock Generator and Power Management Controller
  - Very Slow Clock Operating Mode, Software Programmable Power Optimization Capabilities
- Peripherals
  - LCD Controller (LCDC)with overlay, alpha-blending, rotation, scaling and color conversion
  - USB Device High Speed, USB Host High Speed and USB Host Full Speed with dedicated On-Chip Transceiver
  - Two High Speed Memory Card Hosts
  - Two Master/Slave Serial Peripheral Interfaces (SPI)
  - Two 3-channel 32-bit Timer/Counters (TC)
  - One Synchronous Serial Controller (SSC)
  - One 4-channel 16-bit PWM Controller
  - 3 Two-wire Interfaces (TWI)
  - Three USARTs, two UARTs, one DBGU
  - One 12-channel 10-bit Touchscreen Analog-to-Digital Converter
  - Software Modem Device (SMD)
  - Write Protected Registers
- I/O
  - Four 32-bit Parallel Input/Output Controllers
  - 105 Programmable I/O Lines Multiplexed with up to Three Peripheral I/Os
  - Input Change Interrupt Capability on Each I/O Line, optional Schmitt trigger input
  - Individually Programmable Open-drain, Pull-up and pull-down resistor, Synchronous Output
- Package
  - 217-ball BGA, pitch 0.8 mm

1. Block Diagram

Figure 1-1. SAM9G15 Block Diagram



2. Signal Description

Table 2-1 gives details on the signal name classified by peripheral.

Table 2-1. Signal Description List

Signal Name	Function	Type	Active Level
Clocks, Oscillators and PLLs			
XIN	Main Oscillator Input	Input	
XOUT	Main Oscillator Output	Output	
XIN32	Slow Clock Oscillator Input	Input	
XOUT32	Slow Clock Oscillator Output	Output	
VBG	Bias Voltage Reference for USB	Analog	
PCK0–PCK1	Programmable Clock Output	Output	
Shutdown, Wakeup Logic			
SHDN	Shutdown Control	Output	
WKUP	Wake-Up Input	Input	
ICE and JTAG			
TCK	Test Clock	Input	
TDI	Test Data In	Input	
TDO	Test Data Out	Output	
TMS	Test Mode Select	Input	
JTAGSEL	JTAG Selection	Input	
RTCK	Return Test Clock	Output	
Reset/Test			
NRST	Microcontroller Reset	I/O	Low
TST	Test Mode Select	Input	
NTRST	Test Reset Signal	Input	
BMS	Boot Mode Select	Input	
Debug Unit - DBGU			
DRXD	Debug Receive Data	Input	
DTXD	Debug Transmit Data	Output	
Advanced Interrupt Controller - AIC			
IRQ	External Interrupt Input	Input	
FIQ	Fast Interrupt Input	Input	
PIO Controller - PIOA - PIOB - PIOC - PIOD			
PA0–PA31	Parallel IO Controller A	I/O	
PB0–PB18	Parallel IO Controller B	I/O	
PC0–PC31	Parallel IO Controller C	I/O	
PD0–PD21	Parallel IO Controller D	I/O	

Table 2-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level
External Bus Interface - EBI			
D0–D15	Data Bus	I/O	
D16–D31	Data Bus	I/O	
A0–A25	Address Bus	Output	
NWAIT	External Wait Signal	Input	Low
Static Memory Controller - SMC			
NCS0–NCS5	Chip Select Lines	Output	Low
NWR0–NWR3	Write Signal	Output	Low
NRD	Read Signal	Output	Low
NWE	Write Enable	Output	Low
NBS0–NBS3	Byte Mask Signal	Output	Low
NAND Flash Support			
NFD0–NFD16	NAND Flash I/O	I/O	
NANDCS	NAND Flash Chip Select	Output	Low
NANDOE	NAND Flash Output Enable	Output	Low
NANDWE	NAND Flash Write Enable	Output	Low
DDR2/SDRAM/LPDDR Controller			
SDCK,#SDCK	DDR2/SDRAM Differential Clock	Output	
SDCKE	DDR2/SDRAM Clock Enable	Output	High
SDCS	DDR2/SDRAM Controller Chip Select	Output	Low
BA[0..2]	Bank Select	Output	Low
SDWE	DDR2/SDRAM Write Enable	Output	Low
RAS-CAS	Row and Column Signal	Output	Low
SDA10	SDRAM Address 10 Line	Output	
DQS[0..1]	Data Strobe	I/O	
DQM[0..3]	Write Data Mask	Output	
High Speed MultiMedia Card Interface - HSMCI0–1			
MCI0_CK, MCI1_CK	Multimedia Card Clock	I/O	
MCI0_CDA, MCI1_CDA	Multimedia Card Slot Command	I/O	
MCI0_DA0–MCI0_DA3	Multimedia Card 0 Slot A Data	I/O	
MCI1_DA0–MCI1_DA3	Multimedia Card 1 Slot A Data	I/O	
Universal Synchronous Asynchronous Receiver Transmitter - USARTx			
SCKx	USARTx Serial Clock	I/O	
TXDx	USARTx Transmit Data	Output	
RXDx	USARTx Receive Data	Input	
RTSx	USARTx Request To Send	Output	
CTSx	USARTx Clear To Send	Input	

Table 2-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level
Universal Asynchronous Receiver Transmitter - UARTx			
UTXDx	UARTx Transmit Data	Output	
URXDx	UARTx Receive Data	Input	
Synchronous Serial Controller - SSC			
TD	SSC Transmit Data	Output	
RD	SSC Receive Data	Input	
TK	SSC Transmit Clock	I/O	
RK	SSC Receive Clock	I/O	
TF	SSC Transmit Frame Sync	I/O	
RF	SSC Receive Frame Sync	I/O	
Timer/Counter - TCx (x = 0..5)			
TCLKx	TC Channel x External Clock Input	Input	
TIOAx	TC Channel x I/O Line A	I/O	
TIOBx	TC Channel x I/O Line B	I/O	
Serial Peripheral Interface - SPIx			
SPIx_MISO	Master In Slave Out	I/O	
SPIx_MOSI	Master Out Slave In	I/O	
SPIx_SPCK	SPI Serial Clock	I/O	
SPIx_NPCS0	SPI Peripheral Chip Select 0	I/O	Low
SPIx_NPCS1–SPIx_NPCS3	SPI Peripheral Chip Select	Output	Low
Two-Wire Interface - TWIx			
TWDx	Two-wire Serial Data	I/O	
TWCKx	Two-wire Serial Clock	I/O	
Pulse Width Modulation Controller - PWMC			
PWM0–PWM3	Pulse Width Modulation Output	Output	
USB Device High Speed Port - UDPHS			
DFSDM	USB Device Full Speed Data -	Analog	
DFSDP	USB Device Full Speed Data +	Analog	
DHSDM	USB Device High Speed Data -	Analog	
DHSDP	USB Device High Speed Data +	Analog	
USB Host High Speed Port - UHPHS			
HFSDPA	USB Host Port A Full Speed Data +	Analog	
HFSDMA	USB Host Port A Full Speed Data -	Analog	
HHSDPA	USB Host Port A High Speed Data +	Analog	
HHSDMA	USB Host Port A High Speed Data -	Analog	
HFSDPB	USB Host Port B Full Speed Data +	Analog	
HFSDMB	USB Host Port B Full Speed Data -	Analog	

Table 2-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level
HHSDPB	USB Host Port B High Speed Data +	Analog	
HHSDMB	USB Host Port B High Speed Data -	Analog	
HFSDMC	USB Host Port C Full Speed Data -	Analog	
HFSDPC	USB Host Port C Full Speed Data +	Analog	
LCD Controller - LCDC			
LCDDAT 0–23	LCD Data Bus	Output	
LCDVSYNC	LCD Vertical Synchronization	Output	
LCDHSYNC	LCD Horizontal Synchronization	Output	
LCDPCK	LCD Pixel Clock	Output	
LCDDEN	LCD Data Enable	Output	
LCDPWM	LCD Contrast Control	Output	
LCDDISP	LCD Display Enable	Output	
Analog-to-Digital Converter - ADC			
$AD0_{XP\_UL}$	Top/Upper Left Channel	Analog	
$AD1_{XM\_UR}$	Bottom/Upper Right Channel	Analog	
$AD2_{YP\_LL}$	Right/Lower Left Channel	Analog	
$AD3_{YM\_SENSE}$	Left/Sense Channel	Analog	
$AD4_{LR}$	Lower Right Channel	Analog	
AD5–AD11	7 Analog Inputs	Analog	
ADTRG	ADC Trigger	Input	
ADVREF	ADC Reference	Analog	
Soft Modem Device - SMD			
DIBN	Soft Modem Signal	I/O	
DIBP	Soft Modem Signal	I/O	

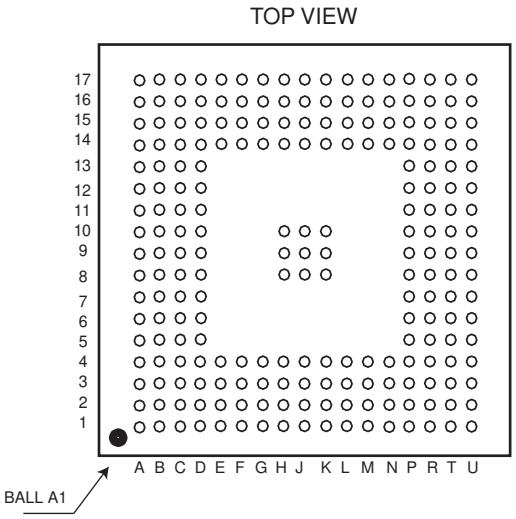
3. Package and Pinout

The SAM9G15 is available in a 217-ball BGA package.

3.1 Overview of the 217-ball BGA Package

Figure 3-1 shows the orientation of the 217-ball BGA Package.

Figure 3-1. Orientation of the 217-ball BGA Package



3.2 I/O Description

Table 3-1. I/O Type Description

I/O Type	Voltage Range	Analog	Pull-up	Pull-down	Schmitt Trigger
GPIO	1.65–3.6V		Switchable	Switchable	Switchable
GPIO_CLK	1.65–3.6V		Switchable	Switchable	Switchable
GPIO_CLK2	1.65–3.6V		Switchable	Switchable	Switchable
GPIO_ANA	3.0–3.6V	I	Switchable		Switchable
EBI	1.65–1.95V, 3.0–3.6V		Switchable	Switchable	
EBI_O	1.65–1.95V, 3.0–3.6V		Reset State	Reset State	
EBI_CLK	1.65–1.95V, 3.0–3.6V				
RSTJTAG	3.0–3.6V		Reset State	Reset State	Reset State
SYSC	1.65–3.6V		Reset State	Reset State	Reset State
VBG	1.15–1.25V	I			
USBFS	3.0–3.6V	I/O			
USBHS	3.0–3.6V	I/O			
CLOCK	1.65–3.6V	I/O			
DIB	3.0–3.6V	I/O			

When “Reset State” is mentioned, the configuration is defined by the “Reset State” column of the Pin Description table.

Table 3-2. I/O Type Assignment and Frequency

I/O Type	I/O Frequency (MHz)	Charge Load (pF)	Output Current	Signal Name
CLOCK	50	50		XIN, XOUT, XIN32, XOUT32
DIB	25	25		DIBN, DIBP
EBI	133	50 (3.3V) 30 (1.8V)		All Data lines (Input/output)
EBI_CLK	133	10		CK, #CK
EBI_O	66	50 (3.3V) 30 (1.8V)		All Address and control lines (output only) except EBI_CLK
GPIO	40	10		All PIO lines except GPIO_CLK, GPIO_CLK2, and GPIO_ANA
GPIO_ANA	25	10	16 mA, 40 mA (peak)	ADx, GPADx
GPIO_CLK	54	10		MCI0CK, MCI1CK, SPI0SPCK, SPI1SPCK
GPIO_CLK2	75	10		LCDDOTCK
RSTJTAG	10	10		NRST, NTRST, BMS, TCK, TDI, TMS, TDO, RTCK
SYSC	0.25	10		WKUP, SHDN, JTAGSEL, TST, SHDN
USBFS	12	10		HFSDPA, HFSDPB/DFSDP, HFSDPC, HFSDMA, HFSDMB/DFSDM, HFSDMC
USBHS	480	10		HHSDPA, HHSDPB/DHSDP, HHSDMA, HHSDMB/DHSDM
VBG	0.25	10		VBG

3.2.1 Reset State

In the tables that follow, the column “Reset State” indicates the reset state of the line with mnemonics.

- “PIO” “/” signal

Indicates whether the PIO Line resets in I/O mode or in peripheral mode. If “PIO” is mentioned, the PIO Line is maintained in a static state as soon as the reset is released. As a result, the bit corresponding to the PIO Line in the register PIO_PSR (Peripheral Status Register) resets low.

If a signal name is mentioned in the “Reset State” column, the PIO Line is assigned to this function and the corresponding bit in PIO_PSR resets high. This is the case of pins controlling memories, in particular the address lines, which require the pin to be driven as soon as the reset is released.

- “I”/“O”

Indicates whether the signal is input or output state.

- “PU”/“PD”

Indicates whether Pull-Up, Pull-Down or nothing is enabled.

- “ST”

Indicates if Schmitt Trigger is enabled.

Example: The PB18 “Reset State” column shows “PIO, I, PU, ST”. That means the line PIO18 is configured as an Input with Pull-Up and Schmitt Trigger enabled. PD14 reset state is “PIO, I, PU”. That means PIO Input with Pull-Up. PD15 reset state is “A20, O, PD” which means output address line 20 with Pull-Down.

3.3 217-ball BGA Package Pinout

Table 3-3. Pin Description BGA217

Ball	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State
			Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, ST
L3	VDDIOP0	GPIO	PA0	I/O			TXD0	O	SPI1_NPCS1	O			PIO, I, PU, ST
P1	VDDIOP0	GPIO	PA1	I/O			RXD0	I	SPI0_NPCS2	O			PIO, I, PU, ST
L4	VDDIOP0	GPIO	PA2	I/O			RTS0	O	MCI1_DA1	I/O			PIO, I, PU, ST
N4	VDDIOP0	GPIO	PA3	I/O			CTS0	I	MCI1_DA2	I/O			PIO, I, PU, ST
T3	VDDIOP0	GPIO	PA4	I/O			SCK0	I/O	MCI1_DA3	I/O			PIO, I, PU, ST
R1	VDDIOP0	GPIO	PA5	I/O			TXD1	O					PIO, I, PU, ST
R4	VDDIOP0	GPIO	PA6	I/O			RXD1	I					PIO, I, PU, ST
R3	VDDIOP0	GPIO	PA7	I/O			TXD2	O	SPI0_NPCS1	O			PIO, I, PU, ST
P4	VDDIOP0	GPIO	PA8	I/O			RXD2	I	SPI1_NPCS0	I/O			PIO, I, PU, ST
U3	VDDIOP0	GPIO	PA9	I/O			DRXD	I					PIO, I, PU, ST
T1	VDDIOP0	GPIO	PA10	I/O			DTXD	O					PIO, I, PU, ST
U1	VDDIOP0	GPIO	PA11	I/O			SPI0_MISO	I/O	MCI1_DA0	I/O			PIO, I, PU, ST
T2	VDDIOP0	GPIO	PA12	I/O			SPI0_MOSI	I/O	MCI1_CDA	I/O			PIO, I, PU, ST
T4	VDDIOP0	GPIO_CLK	PA13	I/O			SPI0_SPCK	I/O	MCI1_CK	I/O			PIO, I, PU, ST
U2	VDDIOP0	GPIO	PA14	I/O			SPI0_NPCS0	I/O					PIO, I, PU, ST
U4	VDDIOP0	GPIO	PA15	I/O			MCI0_DA0	I/O					PIO, I, PU, ST
P5	VDDIOP0	GPIO	PA16	I/O			MCI0_CDA	I/O					PIO, I, PU, ST
R5	VDDIOP0	GPIO_CLK	PA17	I/O			MCI0_CK	I/O					PIO, I, PU, ST
U5	VDDIOP0	GPIO	PA18	I/O			MCI0_DA1	I/O					PIO, I, PU, ST
T5	VDDIOP0	GPIO	PA19	I/O			MCI0_DA2	I/O					PIO, I, PU, ST
U6	VDDIOP0	GPIO	PA20	I/O			MCI0_DA3	I/O					PIO, I, PU, ST
T6	VDDIOP0	GPIO	PA21	I/O			TIOA0	I/O	SPI1_MISO	I/O			PIO, I, PU, ST
R6	VDDIOP0	GPIO	PA22	I/O			TIOA1	I/O	SPI1_MOSI	I/O			PIO, I, PU, ST
U7	VDDIOP0	GPIO_CLK	PA23	I/O			TIOA2	I/O	SPI1_SPCK	I/O			PIO, I, PU, ST
T7	VDDIOP0	GPIO	PA24	I/O			TCLK0	I	TK	I/O			PIO, I, PU, ST
T8	VDDIOP0	GPIO	PA25	I/O			TCLK1	I	TF	I/O			PIO, I, PU, ST
R7	VDDIOP0	GPIO	PA26	I/O			TCLK2	I	TD	O			PIO, I, PU, ST
P8	VDDIOP0	GPIO	PA27	I/O			TIOB0	I/O	RD	I			PIO, I, PU, ST
U8	VDDIOP0	GPIO	PA28	I/O			TIOB1	I/O	RK	I/O			PIO, I, PU, ST
R9	VDDIOP0	GPIO	PA29	I/O			TIOB2	I/O	RF	I/O			PIO, I, PU, ST
R8	VDDIOP0	GPIO	PA30	I/O			TWD0	I/O	SPI1_NPCS3	O			PIO, I, PU, ST
U9	VDDIOP0	GPIO	PA31	I/O			TWCK0	O	SPI1_NPCS2	O			PIO, I, PU, ST
D3	VDDANA	GPIO	PB0	I/O					RTS2	O			PIO, I, PU, ST
D4	VDDANA	GPIO	PB1	I/O					CTS2	I			PIO, I, PU, ST
D2	VDDANA	GPIO	PB2	I/O					SCK2	I/O			PIO, I, PU, ST
E4	VDDANA	GPIO	PB3	I/O					SPI0_NPCS3	O			PIO, I, PU, ST

Table 3-3. Pin Description BGA217 (Continued)

Ball	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State
			Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, ST
D1	VDDANA	GPIO_CLK	PB4	I/O					TWD2	I/O			PIO, I, PU, ST
E3	VDDANA	GPIO	PB5	I/O					TWCK2	O			PIO, I, PU, ST
B3	VDDANA	GPIO_ANA	PB6	I/O	AD7	I							PIO, I, PU, ST
C2	VDDANA	GPIO_ANA	PB7	I/O	AD8	I							PIO, I, PU, ST
C5	VDDANA	GPIO_ANA	PB8	I/O	AD9	I							PIO, I, PU, ST
C1	VDDANA	GPIO_ANA	PB9	I/O	AD10	I			PCK1	O			PIO, I, PU, ST
B2	VDDANA	GPIO_ANA	PB10	I/O	AD11	I			PCK0	O			PIO, I, PU, ST
A3	VDDANA	GPIO_ANA	PB11	I/O	AD0	I			PWM0	O			PIO, I, PU, ST
B4	VDDANA	GPIO_ANA	PB12	I/O	AD1	I			PWM1	O			PIO, I, PU, ST
A2	VDDANA	GPIO_ANA	PB13	I/O	AD2	I			PWM2	O			PIO, I, PU, ST
C4	VDDANA	GPIO_ANA	PB14	I/O	AD3	I			PWM3	O			PIO, I, PU, ST
C3	VDDANA	GPIO_ANA	PB15	I/O	AD4	I							PIO, I, PU, ST
A1	VDDANA	GPIO_ANA	PB16	I/O	AD5	I							PIO, I, PU, ST
B1	VDDANA	GPIO_ANA	PB17	I/O	AD6	I							PIO, I, PU, ST
D5	VDDANA	GPIO	PB18	I/O			IRQ	I	ADTRG	I			PIO, I, PU, ST
E2	VDDIOP1	GPIO	PC0	I/O			LCDDAT0	O			TWD1	I/O	PIO, I, PU, ST
F4	VDDIOP1	GPIO	PC1	I/O			LCDDAT1	O			TWCK1	O	PIO, I, PU, ST
F3	VDDIOP1	GPIO	PC2	I/O			LCDDAT2	O			TIOA3	I/O	PIO, I, PU, ST
H2	VDDIOP1	GPIO	PC3	I/O			LCDDAT3	O			TIOB3	I/O	PIO, I, PU, ST
E1	VDDIOP1	GPIO	PC4	I/O			LCDDAT4	O			TCLK3	I	PIO, I, PU, ST
G4	VDDIOP1	GPIO	PC5	I/O			LCDDAT5	O			TIOA4	I/O	PIO, I, PU, ST
F2	VDDIOP1	GPIO	PC6	I/O			LCDDAT6	O			TIOB4	I/O	PIO, I, PU, ST
F1	VDDIOP1	GPIO	PC7	I/O			LCDDAT7	O			TCLK4	I	PIO, I, PU, ST
G1	VDDIOP1	GPIO	PC8	I/O			LCDDAT8	O			UTXD0	O	PIO, I, PU, ST
G3	VDDIOP1	GPIO	PC9	I/O			LCDDAT9	O			URXD0	I	PIO, I, PU, ST
G2	VDDIOP1	GPIO	PC10	I/O			LCDDAT10	O			PWM0	O	PIO, I, PU, ST
H3	VDDIOP1	GPIO	PC11	I/O			LCDDAT11	O			PWM1	O	PIO, I, PU, ST
J3	VDDIOP1	GPIO	PC12	I/O			LCDDAT12	O			TIOA5	I/O	PIO, I, PU, ST
L2	VDDIOP1	GPIO	PC13	I/O			LCDDAT13	O			TIOB5	I/O	PIO, I, PU, ST
H1	VDDIOP1	GPIO	PC14	I/O			LCDDAT14	O			TCLK5	I	PIO, I, PU, ST
J2	VDDIOP1	GPIO_CLK	PC15	I/O			LCDDAT15	O			PCK0	O	PIO, I, PU, ST
J1	VDDIOP1	GPIO	PC16	I/O			LCDDAT16	O			UTXD1	O	PIO, I, PU, ST
L1	VDDIOP1	GPIO	PC17	I/O			LCDDAT17	O			URXD1	I	PIO, I, PU, ST
K2	VDDIOP1	GPIO	PC18	I/O			LCDDAT18	O			PWM0	O	PIO, I, PU, ST
N3	VDDIOP1	GPIO	PC19	I/O			LCDDAT19	O			PWM1	O	PIO, I, PU, ST
K1	VDDIOP1	GPIO	PC20	I/O			LCDDAT20	O			PWM2	O	PIO, I, PU, ST
M3	VDDIOP1	GPIO	PC21	I/O			LCDDAT21	O			PWM3	O	PIO, I, PU, ST
P3	VDDIOP1	GPIO	PC22	I/O			LCDDAT22	O					PIO, I, PU, ST

Table 3-3. Pin Description BGA217 (Continued)

Ball	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State
			Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, ST
J4	VDDIOP1	GPIO	PC23	I/O			LCDDAT23	O					PIO, I, PU, ST
K3	VDDIOP1	GPIO	PC24	I/O			LCDDISP	O					PIO, I, PU, ST
M2	VDDIOP1	GPIO	PC25	I/O									PIO, I, PU, ST
P2	VDDIOP1	GPIO	PC26	I/O			LCDPWM	O					PIO, I, PU, ST
M1	VDDIOP1	GPIO	PC27	I/O			LCDVSYNC	O			RTS1	O	PIO, I, PU, ST
K4	VDDIOP1	GPIO	PC28	I/O			LCDHSYNC	O			CTS1	I	PIO, I, PU, ST
N1	VDDIOP1	GPIO_CLK	PC29	I/O			LCDDEN	O			SCK1	I/O	PIO, I, PU, ST
R2	VDDIOP1	GPIO_CLK2	PC30	I/O			LCDPCK	O					PIO, I, PU, ST
N2	VDDIOP1	GPIO	PC31	I/O			FIQ	I			PCK1	O	PIO, I, PU, ST
P13	VDDNF	EBI	PD0	I/O			NANDOE	O					PIO, I, PU
R14	VDDNF	EBI	PD1	I/O			NANDWE	O					PIO, I, PU
R13	VDDNF	EBI	PD2	I/O			A21/NANDALE	O					A21,O, PD
P15	VDDNF	EBI	PD3	I/O			A22/NANDCLE	O					A22,O, PD
P12	VDDNF	EBI	PD4	I/O			NCS3	O					PIO, I, PU
P14	VDDNF	EBI	PD5	I/O			NWAIT	I					PIO, I, PU
N14	VDDNF	EBI	PD6	I/O			D16	I/O					PIO, I, PU
R15	VDDNF	EBI	PD7	I/O			D17	I/O					PIO, I, PU
M14	VDDNF	EBI	PD8	I/O			D18	I/O					PIO, I, PU
N16	VDDNF	EBI	PD9	I/O			D19	I/O					PIO, I, PU
N17	VDDNF	EBI	PD10	I/O			D20	I/O					PIO, I, PU
N15	VDDNF	EBI	PD11	I/O			D21	I/O					PIO, I, PU
K15	VDDNF	EBI	PD12	I/O			D22	I/O					PIO, I, PU
M15	VDDNF	EBI	PD13	I/O			D23	I/O					PIO, I, PU
L14	VDDNF	EBI	PD14	I/O			D24	I/O					PIO, I, PU
M16	VDDNF	EBI	PD15	I/O			D25	I/O	A20	O			A20, O, PD
L16	VDDNF	EBI	PD16	I/O			D26	I/O	A23	O			A23, O, PD
L15	VDDNF	EBI	PD17	I/O			D27	I/O	A24	O			A24, O, PD
K17	VDDNF	EBI	PD18	I/O			D28	I/O	A25	O			A25, O, PD
J17	VDDNF	EBI	PD19	I/O			D29	I/O	NCS2	O			PIO, I, PU
K16	VDDNF	EBI	PD20	I/O			D30	I/O	NCS4	O			PIO, I, PU
J16	VDDNF	EBI	PD21	I/O			D31	I/O	NCS5	O			PIO, I, PU
D10 D13 F14	VDDIOM	POWER	VDDIOM	I									I
J14 K14	VDDNF	POWER	VDDNF	I									I
H9 H10 J9 J10	GNDIOM	GND	GNDIOM	I									I

Table 3-3. Pin Description BGA217 (Continued)

Ball	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State
			Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, ST
P7	VDDIOP0	POWER	VDDIOP0	I									I
H4	VDDIOP1	POWER	VDDIOP1	I									I
M4 P6	GNDIOP	GND	GNDIOP	I									I
B5	VDDBU	POWER	VDDBU	I									I
B6	GNDBU	GND	GNDBU	I									I
C6	VDDANA	POWER	VDDANA	I									I
D6	GNDANA	GND	GNDANA	I									I
R12	VDDPLLA	POWER	VDDPLLA	I									I
T13	VDDOSC	POWER	VDDOSC	I									I
U13	GNDOSC	GND	GNDOSC	I									I
H14 K8 K9	VDDCORE	POWER	VDDCORE	I									I
H8 J8 K10	GNDCORE	GND	GNDCORE	I									I
U16	VDDUTMII	POWER	VDDUTMII	I									I
T17	VDDUTMIC	POWER	VDDUTMIC	I									I
T16	GNDUTMI	GND	GNDUTMI	I									I
D14	VDDIOM	EBI	D0	I/O									O, PD
D15	VDDIOM	EBI	D1	I/O									O, PD
A16	VDDIOM	EBI	D2	I/O									O, PD
B16	VDDIOM	EBI	D3	I/O									O, PD
A17	VDDIOM	EBI	D4	I/O									O, PD
B15	VDDIOM	EBI	D5	I/O									O, PD
C14	VDDIOM	EBI	D6	I/O									O, PD
B14	VDDIOM	EBI	D7	I/O									O, PD
A15	VDDIOM	EBI	D8	I/O									O, PD
C15	VDDIOM	EBI	D9	I/O									O, PD
D12	VDDIOM	EBI	D10	I/O									O, PD
C13	VDDIOM	EBI	D11	I/O									O, PD
A14	VDDIOM	EBI	D12	I/O									O, PD
B13	VDDIOM	EBI	D13	I/O									O, PD
A13	VDDIOM	EBI	D14	I/O									O, PD
C12	VDDIOM	EBI	D15	I/O									O, PD
J15	VDDIOM	EBI_O	A0	O	NBS0	O							O, PD
H16	VDDIOM	EBI_O	A1	O	NBS2/DQM/ NWR2	O							O, PD
H15	VDDIOM	EBI_O	A2	O									O, PD

Table 3-3. Pin Description BGA217 (Continued)

Ball	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State
			Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, ST
H17	VDDIOM	EBI_O	A3	O									O, PD
G17	VDDIOM	EBI_O	A4	O									O, PD
G16	VDDIOM	EBI_O	A5	O									O, PD
F17	VDDIOM	EBI_O	A6	O									O, PD
E17	VDDIOM	EBI_O	A7	O									O, PD
F16	VDDIOM	EBI_O	A8	O									O, PD
G15	VDDIOM	EBI_O	A9	O									O, PD
G14	VDDIOM	EBI_O	A10	O									O, PD
F15	VDDIOM	EBI_O	A11	O									O, PD
D17	VDDIOM	EBI_O	A12	O									O, PD
C17	VDDIOM	EBI_O	A13	O									O, PD
E16	VDDIOM	EBI_O	A14	O									O, PD
D16	VDDIOM	EBI_O	A15	O									O, PD
C16	VDDIOM	EBI_O	A16	O	BA0	O							O, PD
B17	VDDIOM	EBI_O	A17	O	BA1	O							O, PD
E15	VDDIOM	EBI_O	A18	O	BA2	O							O, PD
E14	VDDIOM	EBI_O	A19	O									O, PD
B9	VDDIOM	EBI_O	NCS0	O									O, PU
B8	VDDIOM	EBI_O	NCS1	O	SDCS	O							O, PU
D9	VDDIOM	EBI_O	NRD	O									O, PU
C9	VDDIOM	EBI_O	NWR0	O	NWRE	O							O, PU
C7	VDDIOM	EBI_O	NWR1	O	NBS1	O							O, PU
A8	VDDIOM	EBI_O	NWR3	O	NBS3/DQM3	O							O, PU
D11	VDDIOM	EBI_CLK	SDCK	O									O
C11	VDDIOM	EBI_CLK	#SDCK	O									O
B12	VDDIOM	EBI_O	SDCKE	O									O, PU
B11	VDDIOM	EBI_O	RAS	O									O, PU
C10	VDDIOM	EBI_O	CAS	O									O, PU
A12	VDDIOM	EBI_O	SDWE	O									O, PU
C8	VDDIOM	EBI_O	SDA10	O									O, PU
A10	VDDIOM	EBI_O	DQM0	O									O, PU
B10	VDDIOM	EBI_O	DQM1	O									O, PU
A11	VDDIOM	EBI	DQS0	I/O									O, PD
A9	VDDIOM	EBI	DQS1	I/O									O, PD
A4	VDDANA	POWER	ADVREF	I									I
U17	VDDUTMIC	VBG	VBG	I									I
T14	VDDUTMII	USBFS	HFSDPA	I/O	DFSDP	I/O							O, PD
T15	VDDUTMII	USBFS	HFSDMA	I/O	DFSDM	I/O							O, PD

Table 3-3. Pin Description BGA217 (Continued)

Ball	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State
			Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, ST
U14	VDDUTMII	USBHS	HHSDPA	I/O	DHSDP	I/O							O, PD
U15	VDDUTMII	USBHS	HHSDMA	I/O	DHSDM	I/O							O, PD
R16	VDDUTMII	USBFS	HFSDPB	I/O									O, PD
P16	VDDUTMII	USBFS	HFSDMB	I/O									O, PD
R17	VDDUTMII	USBHS	HHSDPB	I/O									O, PD
P17	VDDUTMII	USBHS	HHSDMB	I/O									O, PD
L17	VDDUTMII	USBFS	HFSDPC	I/O									O, PD
M17	VDDUTMII	USBFS	HFSDMC	I/O									O, PD
R11	VDDIOP0	DIB	DIBN	I/O									O, PU
P11	VDDIOP0	DIB	DIBP	I/O									O, PU
A7	VDDBU	SYSC	WKUP	I									I, ST
D8	VDDBU	SYSC	SHDN	O									O
P9	VDDIOP0	RSTJTAG	BMS	I									I, PD, ST
D7	VDDBU	SYSC	JTAGSEL	I									I, PD
B7	VDDBU	SYSC	TST	I									I, PD, ST
U10	VDDIOP0	RSTJTAG	TCK	I									I, ST
T9	VDDIOP0	RSTJTAG	TDI	I									I, ST
T10	VDDIOP0	RSTJTAG	TDO	O									O
U11	VDDIOP0	RSTJTAG	TMS	I									I, ST
R10	VDDIOP0	RSTJTAG	RTCK	O									O
P10	VDDIOP0	RSTJTAG	NRST	I/O									I, PU, ST
T11	VDDIOP0	RSTJTAG	NTRST	I									I, PU, ST
A6	VDDBU	CLOCK	XIN32	I									I
A5	VDDBU	CLOCK	XOUT32	O									O
T12	VDDOSC	CLOCK	XIN	I									I
U12	VDDOSC	CLOCK	XOUT	O									O

4. Power Considerations

4.1 Power Supplies

The SAM9G15 has several types of power supply pins. For complete details about power-up and power-down sequences, please refer to Section 45.15 “Power Sequence Requirements”.

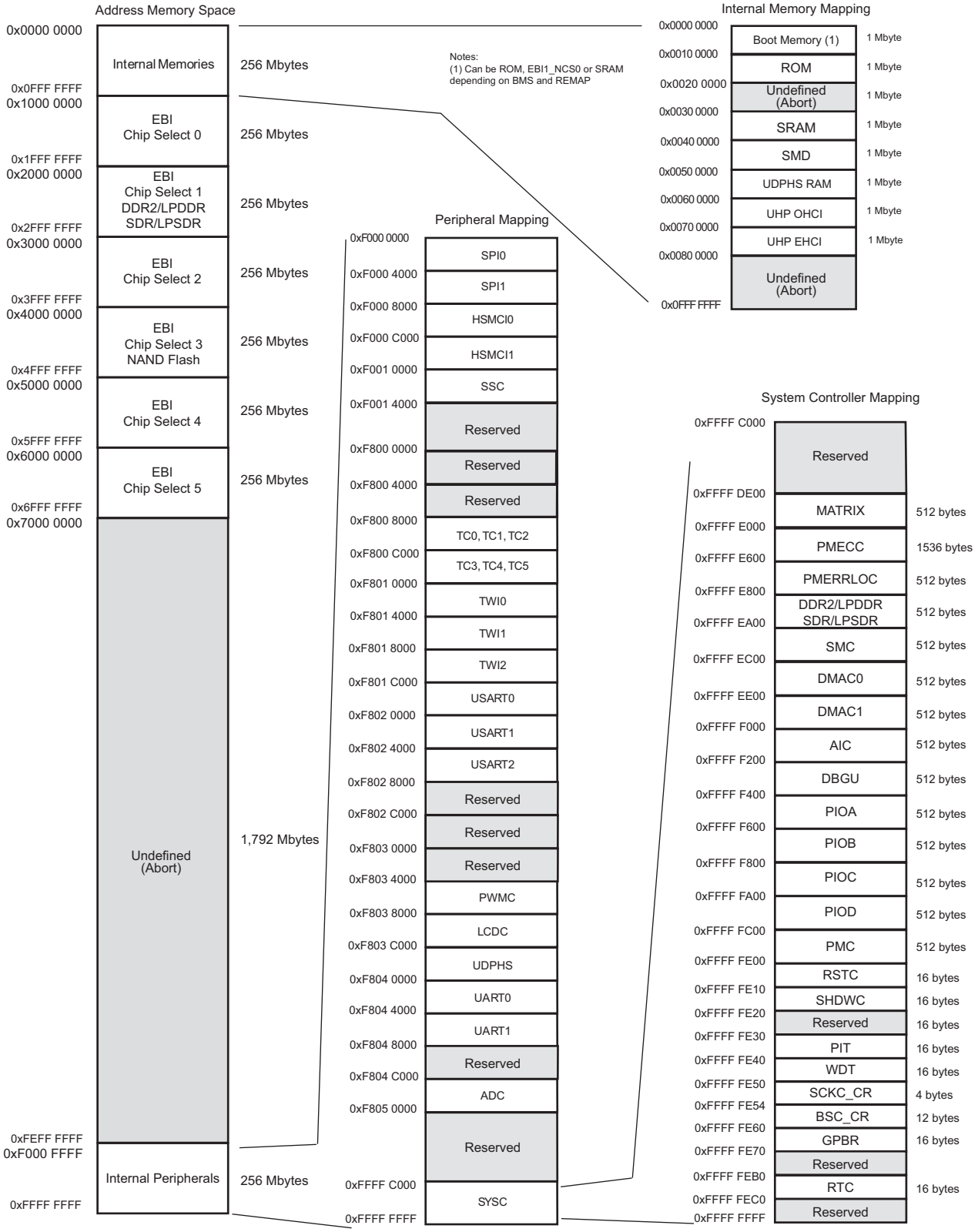
Table 4-1. Power Supplies

Name	Voltage Range, nominal	Powers	Associated Ground
VDDANA	3.0–3.6V, 3.3V	Analog-to-Digital Converter	GNDANA
VDDBU	1.65–3.6V	Slow Clock oscillator, internal 32 kHz RC oscillator and backup part of the System Controller	GNDBU
VDDCORE	0.9–1.1V, 1.0V	ARM core, internal memories, internal peripherals and part of the system controller	GNDCORE
VDDIOM	1.65–1.95V, 1.8V 3.0–3.6V, 3.3V	External Memory Interface I/O lines	GNDIOM
VDDIOP0	1.65–3.6V	Part of peripheral I/O lines (1)	GNDIOP
VDDIOP1	1.65–3.6V	Part of peripheral I/O lines (1)	GNDIOP
VDDNF	1.65–1.95V, 1.8V 3.0–3.6V, 3.3V	NAND Flash I/O and control, D16–D31 and multiplexed SMC lines	GNDIOM
VDDOSC	1.65–3.6V	Main Oscillator cells	GNDOSC
VDDPLLA	0.9–1.1V, 1.0V	PLLA and PLLUTMI cells	GNDOSC
VDDUTMIC	0.9–1.1V, 1.0V	USB transceiver core logic	GNDUTMI
VDDUTMII	3.0–3.6V, 3.3V	USB transceiver interface	GNDUTMI

Note: 1. Refer to Table 3-2 for more details.

5. Memories

Figure 5-1. SAM9G15 Memory Mapping



5.1 Memory Mapping

A first level of address decoding is performed by the AHB Bus Matrix, i.e., the implementation of the Advanced High performance Bus (AHB) for its Master and Slave interfaces with additional features.

Decoding breaks up the 4 Gbytes of address space into 16 banks of 256 Mbytes. Banks 1 to 6 are directed to the EBI that associates these banks to the external chip selects, EBI_NCS0 to EBI_NCS5. Bank 0 is reserved for the addressing of the internal memories, and a second level of decoding provides 1 Mbyte of internal memory area. Bank 15 is reserved for the peripherals and provides access to the Advanced Peripheral Bus (APB).

Other areas are unused and performing an access within them provides an abort to the master requesting such an access.

5.2 Embedded Memories

5.2.1 Internal SRAM

The SAM9G15 embeds a total of 32 Kbytes of high-speed SRAM.

After reset and until the Remap Command is performed, the SRAM is only accessible at address 0x0030 0000.

After Remap, the SRAM also becomes available at address 0x0.

5.2.2 Internal ROM

The SAM9G15 embeds an Internal ROM, which contains the SAM-BA® program.

At any time, the ROM is mapped at address 0x0010 0000. It is also accessible at address 0x0 (BMS = 1) after the reset and before the Remap Command.

5.3 External Memories

5.3.1 External Bus Interface

- Integrates three External Memory Controllers:
  - Static Memory Controller
  - DDR2/SDRAM Controller
  - MLC NAND Flash ECC Controller
- Additional logic for NAND Flash and CompactFlash®
- Up to 26-bit Address Bus (up to 64 Mbytes linear per chip select)
- Up to 6 chip selects, Configurable Assignment:
  - Static Memory Controller on NCS0, NCS1, NCS2, NCS3, NCS4, NCS5
  - DDR2/SDRAM Controller (SDCS) or Static Memory Controller on NCS1
  - Optional NAND Flash support on NCS3

5.3.2 Static Memory Controller

- 8-bit, 16-bit, or 32-bit Data Bus
- Multiple Access Modes supported
  - Byte Write or Byte Select Lines
  - Asynchronous read in Page Mode supported (4- up to 16-byte page size)
- Multiple device adaptability
  - Control signals programmable setup, pulse and hold time for each Memory Bank
- Multiple Wait State Management
  - Programmable Wait State Generation

- External Wait Request
- Programmable Data Float Time

- Slow Clock mode supported

5.3.3 DDR2SDR Controller

- Supports 4-bank and 8-bank DDR2, LPDDR, SDR and LPSDR
- Numerous Configurations Supported
  - 2K, 4K, 8K, 16K Row Address Memory Parts
  - SDRAM with 8 Internal Banks
  - SDR-SDRAM with 32-bit Data Path
  - DDR2/LPDDR with 16-bit Data Path
  - One Chip Select for SDRAM Device (256 Mbyte Address Space)
- Programming Facilities
  - Multibank Ping-pong Access (Up to 8 Banks Opened at Same Time = Reduces Average Latency of Transactions)
  - Timing Parameters Specified by Software
  - Automatic Refresh Operation, Refresh Rate is Programmable
  - Automatic Update of DS, TCR and PASR Parameters (LPSDR)
- Energy-saving Capabilities
  - Self-refresh, Power-down and Deep Power Modes Supported
- SDRAM Power-up Initialization by Software
- CAS Latency of 2, 3 Supported
- Auto Precharge Command Not Used
- SDR-SDRAM with 16-bit Datapath and Eight Columns Not Supported
  - Clock Frequency Change in Precharge Power-down Mode Not Supported

6. System Controller

The System Controller is a set of peripherals that allows handling of key elements of the system, such as power, resets, clocks, time, interrupts, watchdog, etc.

The System Controller User Interface also embeds the registers that configure the Matrix and a set of registers for the chip configuration. The chip configuration registers configure the EBI chip select assignment and voltage range for external memories.

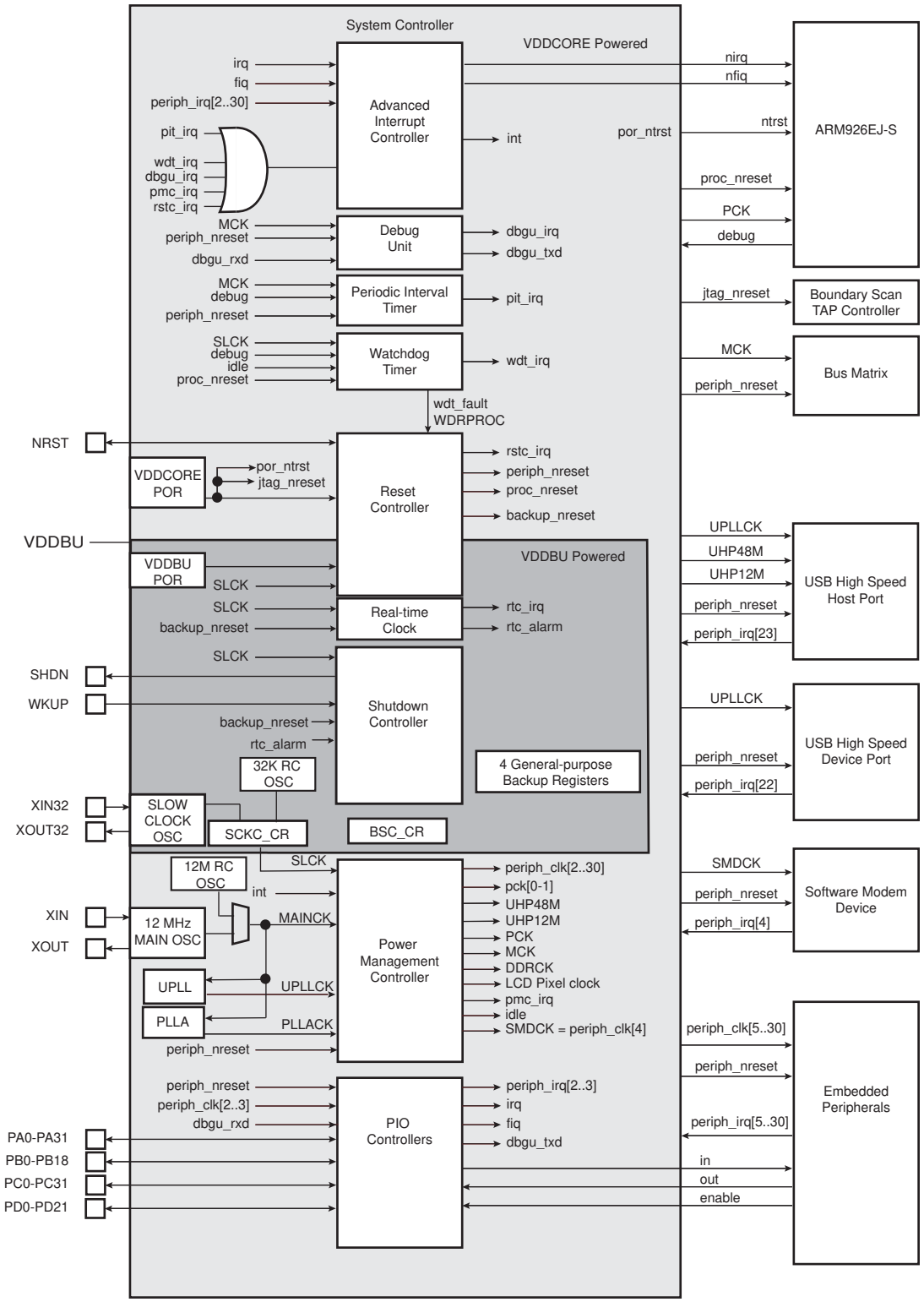
The System Controller's peripherals are all mapped within the highest 16 Kbytes of address space, between addresses 0xFFFF_C000 and 0xFFFF_FFFF.

However, all the registers of System Controller are mapped on the top of the address space. All the registers of the System Controller can be addressed from a single pointer by using the standard ARM instruction set, as the Load/Store instruction have an indexing mode of ±4 Kbytes.

Figure 6-1 on page 21 shows the System Controller block diagram.

Figure 5-1 on page 17 shows the mapping of the User Interface of the System Controller peripherals.

Figure 6-1. SAM9G15 System Controller Block Diagram



6.1 Chip Identification

- Chip ID: 0x819A_05A1
- Chip ID Extension: 0
- JTAG ID: 0x05B2_F03F
- ARM926 TAP ID: 0x0792_603F

6.2 Backup Area

The SAM9G15 features a Backup Area that embeds:

- RC Oscillator
- Slow Clock Oscillator
- Real Time Counter (RTC)
- Shutdown Controller (SHDWC)
- 4 Backup Registers (GPBR)
- Slow Clock Controller Configuration Register (SCKC_CR)
- Boot Sequence Configuration Register (BSC_CR)
- A part of the Reset Controller (RSTC)

This section is powered by the VDDBU rail.

7. Peripherals

7.1 Peripheral Mapping

As shown in Figure 5-1 on page 17, the Peripherals are mapped in the upper 256 Mbytes of the address space between the addresses 0xF000_0000 and 0xFFFF_C000.

Each user peripheral is allocated 16 Kbytes of address space.

7.2 Peripheral Identifiers

Table 7-1 defines the Peripheral Identifiers of the SAM9G15. A peripheral identifier is required for the control of the peripheral interrupt with the Advanced Interrupt Controller and for the control of the peripheral clock with the Power Management Controller.

Table 7-1. Peripheral Identifiers

Instance ID	Instance Name	Instance Description	External interrupt	Wired-OR interrupt
0	AIC	Advanced Interrupt Controller	FIQ	
1	SYS	System Controller		DBGU, PMC, SYSC, PMECC, PMERRLOC, RTSC, SHDWC, PIT, WDT, RTC
2	PIOA, PIOB	Parallel I/O Controller A and B		
3	PIOC, PIOD	Parallel I/O Controller C and D		
4	SMD	Soft Modem Device		
5	USART0	Universal Synchronous Asynchronous Receiver Transmitter 0		
6	USART1	Universal Synchronous Asynchronous Receiver Transmitter 1		
7	USART2	Universal Synchronous Asynchronous Receiver Transmitter 2		
9	TWI0	Two-Wire Interface 0		
10	TWI1	Two-Wire Interface 1		
11	TWI2	Two-Wire Interface 2		
12	HSMCI0	High Speed Multimedia Card Interface 0		
13	SPI0	Serial Peripheral Interface 0		
14	SPI1	Serial Peripheral Interface 1		
15	UART0	Universal Asynchronous Receiver Transmitter 0		
16	UART1	Universal Asynchronous Receiver Transmitter 1		
17	TC0, TC1	Timer Counter Channel 0, 1, 2, 3, 4, 5		
18	PWM	Pulse Width Modulation Controller		
19	ADC	ADC Controller		
20	DMAC0	DMA Controller 0		
21	DMAC1	DMA Controller 1		
22	UHPHS	USB Host Port High Speed		

Table 7-1. Peripheral Identifiers (Continued)

Instance ID	Instance Name	Instance Description	External interrupt	Wired-OR interrupt
23	UDPHS	USB Device Port High Speed		
25	LCDC	LCD Controller		
26	HSMCI1	High Speed Multimedia Card Interface 1		
28	SSC	Synchronous Serial Controller		
31	AIC	Advanced Interrupt Controller	IRQ	

7.3 Peripheral Signal Multiplexing on I/O Lines

The SAM9G15 features four PIO controllers (PIOA, PIOB, PIOC, and PIOD) which multiplex the I/O lines of the peripheral set.

Each PIO controller controls a number of lines:

32 lines for PIOA

19 lines for PIOB

32 lines for PIOC

22 lines for PIOD

Each line can be assigned to one of three peripheral functions, A, B or C. Refer to Table 3-3, “Pin Description BGA217,” on page 10 to see the PIO assignments.

8. ARM926EJ-S™

8.1 Description

The ARM926EJ-S processor is a member of the ARM9™ family of general-purpose microprocessors. The ARM926EJ-S implements ARM architecture version 5TEJ and is targeted at multi-tasking applications where full memory management, high performance, low die size and low power are all important features.

The ARM926EJ-S processor supports the 32-bit ARM and 16-bit THUMB instruction sets, enabling the user to trade off between high performance and high code density. It also supports 8-bit Java instruction set and includes features for efficient execution of Java bytecode, providing a Java performance similar to a JIT (Just-In-Time compilers), for the next generation of Java-powered wireless and embedded devices. It includes an enhanced multiplier design for improved DSP performance.

The ARM926EJ-S processor supports the ARM debug architecture and includes logic to assist in both hardware and software debug.

The ARM926EJ-S provides a complete high performance processor subsystem, including:

- An ARM9EJ-S™ integer core
- A Memory Management Unit (MMU)
- Separate instruction and data AMBA AHB bus interfaces

8.2 Embedded Characteristics

- ARM9EJ-S™ Based on ARM® Architecture v5TEJ with Jazelle Technology
- Three Instruction Sets
  - ARM® High-performance 32-bit Instruction Set
  - Thumb® High Code Density 16-bit Instruction Set
  - Jazelle® 8-bit Instruction Set
- 5-Stage Pipeline Architecture when Jazelle is not Used
  - Fetch (F)
  - Decode (D)
  - Execute (E)
  - Memory (M)
  - Writeback (W)
- 6-Stage Pipeline when Jazelle is Used
  - Fetch
  - Jazelle/Decode (Two Cycles)
  - Execute
  - Memory
  - Writeback
- ICache and DCache
  - Virtually-addressed 4-way Set Associative Caches
  - 8 Words per Line
  - Critical-word First Cache Refilling
  - Write-though and Write-back Operation for DCache Only
  - Pseudo-random or Round-robin Replacement
  - Cache Lockdown Registers
  - Cache Maintenance