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32-BIT ARM-BASED MICROPROCESSORS

SAM9G20

Description

The SAM9G20 embedded microprocessor unit is based on the integration of an Arm926EJ-S™ processor with fast ROM and RAM memories and a wide range of peripherals.

The SAM9G20 embeds an Ethernet MAC, one USB Device Port, and a dual port USB Host controller with on-chip USB transceivers. It also integrates several standard peripherals, such as the USART, SPI, TWI, Timer Counters, Synchronous Serial Controller, ADC and MultiMedia Card Interface.

The SAM9G20 is architectured on a 6-layer matrix, allowing a maximum internal bandwidth of six 32-bit buses. It also features an External Bus Interface capable of interfacing with a wide range of memory devices.

The SAM9G20 is an enhancement of the SAM9260 with the same peripheral features. It is pin-to-pin compatible with the exception of power supply pins. Speed is increased to reach 400 MHz on the Arm core and 133 MHz on the system bus and EBI.

Features

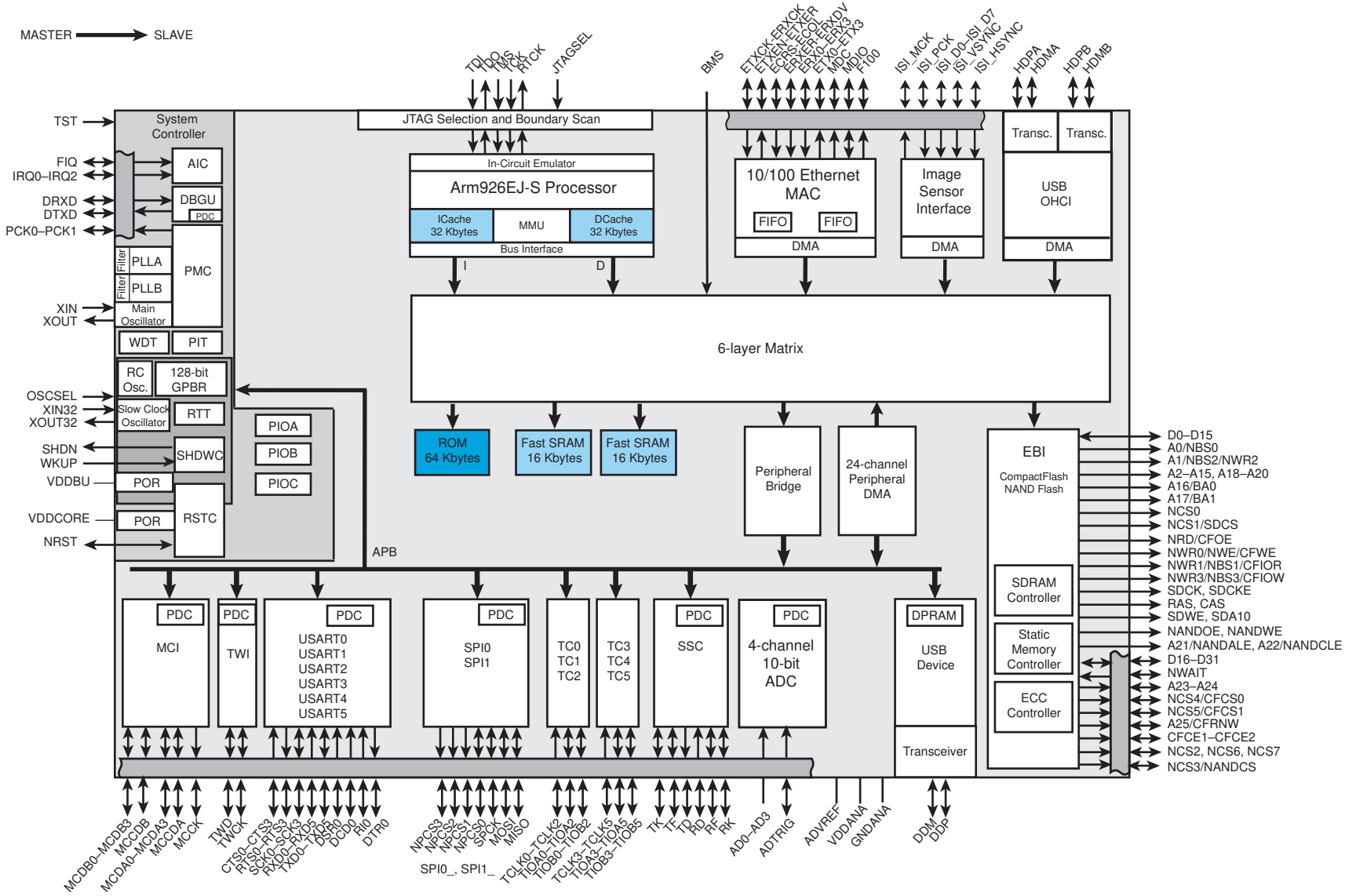
- Incorporates the Arm926EJ-S Arm® Thumb® Processor
  - DSP Instruction Extensions, Arm Jazelle® Technology for Java® Acceleration
  - 32-Kbyte Data Cache, 32-Kbyte Instruction Cache, Write Buffer
  - CPU Frequency 400 MHz
  - Memory Management Unit
  - EmbeddedICE, Debug Communication Channel Support
- Additional Embedded Memories
  - One 64-Kbyte Internal ROM, Single-cycle Access at Maximum Matrix Speed
  - Two 16-Kbyte Internal SRAM, Single-cycle Access at Maximum Matrix Speed
- External Bus Interface (EBI)
  - Supports SDRAM, Static Memory, ECC-enabled SLC NAND Flash and CompactFlash®
- USB 2.0 Full Speed (12 Mbit/s) Device Port
  - On-chip Transceiver, 2,432-byte Configurable Integrated DPRAM
- USB 2.0 Full Speed (12 Mbit/s) Host and Dual Port
  - Single or Dual On-chip Transceivers
  - Integrated FIFOs and Dedicated DMA Channels
- Ethernet MAC 10/100 Base T
  - Media Independent Interface or Reduced Media Independent Interface
  - 128-byte FIFOs and Dedicated DMA Channels for Receive and Transmit
- Image Sensor Interface
  - ITU-R BT. 601/656 External Interface, Programmable Frame Capture Rate
  - 12-bit Data Interface for Support of High Sensibility Sensors
  - SAV and EAV Synchronization, Preview Path with Scaler, YCbCr Format
- Bus Matrix
  - Six 32-bit-layer Matrix
  - Boot Mode Select Option, Remap Command
- Fully-featured System Controller, including
  - Reset Controller, Shutdown Controller
  - 128-bit (4 x 32-bit) General Purpose Backup Registers
  - Clock Generator and Power Management Controller
  - Advanced Interrupt Controller and Debug Unit

  - Periodic Interval Timer, Watchdog Timer and Real-time Timer
- Reset Controller (RSTC)
  - Based on a Power-on Reset Cell, Reset Source Identification and Reset Output Control
- Clock Generator (CKGR)
  - Selectable 32768 Hz Low-power Oscillator or Internal Low Power RC Oscillator on Battery Backup Power Supply, Providing a Permanent Slow Clock
  - 3 to 20 MHz On-chip Oscillator, One up to 800 MHz PLL and One up to 100 MHz PLL
- Power Management Controller (PMC)
  - Very Slow Clock Operating Mode, Software Programmable Power Optimization Capabilities
  - Two Programmable External Clock Signals
- Advanced Interrupt Controller (AIC)
  - Individually Maskable, Eight-level Priority, Vectored Interrupt Sources
  - Three External Interrupt Sources and One Fast Interrupt Source, Spurious Interrupt Protected
- Debug Unit (DBGU)
  - 2-wire UART and Support for Debug Communication Channel, Programmable ICE Access Prevention
  - Mode for General Purpose 2-wire UART Serial Communication
- Periodic Interval Timer (PIT)
  - 20-bit Interval Timer plus 12-bit Interval Counter
- Watchdog Timer (WDT)
  - Key-protected, Programmable Only Once, Windowed 16-bit Counter Running at Slow Clock
- Real-time Timer (RTT)
  - 32-bit Free-running Backup Counter Running at Slow Clock with 16-bit Prescaler
- One 4-channel 10-bit Analog-to-Digital Converter
- Three 32-bit Parallel Input/Output Controllers (PIOA, PIOB, PIOC)
  - 96 Programmable I/O Lines Multiplexed with up to Two Peripheral I/Os
  - Input Change Interrupt Capability on Each I/O Line
  - Individually Programmable Open-drain, Pull-up Resistor and Synchronous Output
  - All I/O Lines are Schmitt Trigger Inputs
- Peripheral DMA Controller Channels (PDC)
- One Two-slot MultiMedia Card Interface (MCI)
  - SDCard/SDIO and MultiMediaCard™ Compliant
  - Automatic Protocol Control and Fast Automatic Data Transfers with PDC
- One Synchronous Serial Controller (SSC)
  - Independent Clock and Frame Sync Signals for Each Receiver and Transmitter
  - I²S Analog Interface Support, Time Division Multiplex Support
  - High-speed Continuous Data Stream Capabilities with 32-bit Data Transfer
- Four Universal Synchronous/Asynchronous Receiver Transmitters (USART)
  - Individual Baud Rate Generator, IrDA® Infrared Modulation/Demodulation, Manchester Encoding/Decoding
  - Support for ISO7816 T0/T1 Smart Card, Hardware Handshaking, RS485 Support
  - Full Modem Signal Control on USART0
- Two 2-wire UARTs
- Two Master/Slave Serial Peripheral Interfaces (SPI)
  - 8- to 16-bit Programmable Data Length, Four External Peripheral Chip Selects
  - Synchronous Communications
- Two Three-channel 16-bit Timer/Counters (TC)
  - Three External Clock Inputs, Two Multi-purpose I/O Pins per Channel
  - Double PWM Generation, Capture/Waveform Mode, Up/Down Capability
  - High-Drive Capability on Outputs TIOA0, TIOA1, TIOA2
- One Two-wire Interface (TWI)
  - Compatible with Standard Two-wire Serial Memories
  - One, Two or Three Bytes for Slave Address
  - Sequential Read/Write Operations
  - Master, Multi-master and Slave Mode Operation
  - Bit Rate: Up to 400 Kbit/s
  - General Call Supported in Slave Mode

  - Connection to Peripheral DMA Controller (PDC) Channel Capabilities Optimizes Data Transfers in Master Mode
- IEEE® 1149.1 JTAG Boundary Scan on All Digital Pins
- Required Power Supplies
  - 0.9V to 1.1V for VDDBU, VDDCORE, VDDPLL
  - 1.65 to 3.6V for VDDOSC
  - 1.65V to 3.6V for VDDIOP (Peripheral I/Os)
  - 3.0V to 3.6V for VDDUSB
  - 3.0V to 3.6V VDDANA (Analog-to-Digital Converter)
  - Programmable 1.65V to 1.95V or 3.0V to 3.6V for VDDIOM (Memory I/Os)
- Available in 217-ball LFBGA and 247-ball TFBGA Green-compliant Packages

1. Block Diagram

Figure 1-1: SAM9G20 Block Diagram



2. Signal Description

Table 2-1: Signal Description List

Signal Name	Function	Type	Active Level	Comments
Power Supplies				
VDDIOM	EBI I/O Lines Power Supply	Power	–	1.65–1.95 V or 3.0–3.6 V
VDDIOP	Peripherals I/O Lines Power Supply	Power	–	1.65–3.6 V
VDDBU	Backup I/O Lines Power Supply	Power	–	0.9–1.1 V
VDDANA	Analog Power Supply	Power	–	3.0–3.6 V
VDDPLL	PLL Power Supply	Power	–	0.9–1.1 V
VDDOSC	Oscillator Power Supply	Power	–	1.65–3.6 V
VDDCORE	Core Chip Power Supply	Power	–	0.9–1.1 V
VDDUSB	USB Power Supply	Power	–	1.65–3.6 V
GND	Ground	Ground	–	
GNDANA	Analog Ground	Ground	–	
GNDBU	Backup Ground	Ground	–	
GNDUSB	USB Ground	Ground	–	
GNDPLL	PLL Ground	Ground	–	
Clocks, Oscillators and PLLs				
XIN	Main Oscillator Input	Input	–	
XOUT	Main Oscillator Output	Output	–	
XIN32	Slow Clock Oscillator Input	Input	–	
XOUT32	Slow Clock Oscillator Output	Output	–	
OSCSEL	Slow Clock Oscillator Selection	Input	–	Accepts between 0V and VDDBU
PCK0–PCK1	Programmable Clock Output	Output	–	
Shutdown, Wakeup Logic				
SHDN	Shutdown Control	Output	–	
WKUP	Wake-up Input	Input	–	Accepts between 0V and VDDBU
ICE and JTAG				
NTRST	Test Reset Signal	Input	Low	Pull-up resistor
TCK	Test Clock	Input	–	No pull-up resistor
TDI	Test Data In	Input	–	No pull-up resistor
TDO	Test Data Out	Output	–	
TMS	Test Mode Select	Input	–	No pull-up resistor
JTAGSEL	JTAG Selection	Input	–	Pull-down resistor. Accepts between 0V and VDDBU.
RTCK	Return Test Clock	Output	–	

Table 2-1: Signal Description List

Signal Name	Function	Type	Active Level	Comments
Reset/Test				
NRST	Microprocessor Reset	I/O	Low	Pull-up resistor
TST	Test Mode Select	Input	–	Pull-down resistor. Accepts between 0V and VDDBU.
BMS	Boot Mode Select	Input	–	No pull-up resistor BMS = 0 when tied to GND BMS = 1 when tied to VDDIOP
Debug Unit - DBGU				
DRXD	Debug Receive Data	Input	–	
DTXD	Debug Transmit Data	Output	–	
Advanced Interrupt Controller - AIC				
IRQ0–IRQ2	External Interrupt Inputs	Input	–	
FIQ	Fast Interrupt Input	Input	–	
PIO Controller - PIOA / PIOB / PIOC				
PA0–PA31	Parallel IO Controller A	I/O	–	Pulled-up input at reset
PB0–PB31	Parallel IO Controller B	I/O	–	Pulled-up input at reset
PC0–PC31	Parallel IO Controller C	I/O	–	Pulled-up input at reset
External Bus Interface - EBI				
D0–D31	Data Bus	I/O	–	Pulled-up input at reset
A0–A25	Address Bus	Output	–	0 at reset
NWAIT	External Wait Signal	Input	Low	
Static Memory Controller - SMC				
NCS0–NCS7	Chip Select Lines	Output	Low	
NWR0–NWR3	Write Signal	Output	Low	
NRD	Read Signal	Output	Low	
NWE	Write Enable	Output	Low	
NBS0–NBS3	Byte Mask Signal	Output	Low	
CompactFlash Support				
CFCE1–CFCE2	CompactFlash Chip Enable	Output	Low	
CFOE	CompactFlash Output Enable	Output	Low	
CFWE	CompactFlash Write Enable	Output	Low	
CFIOR	CompactFlash IO Read	Output	Low	
CFIOW	CompactFlash IO Write	Output	Low	
CFRNW	CompactFlash Read Not Write	Output	–	
CFCS0–CFCS1	CompactFlash Chip Select Lines	Output	Low	

Table 2-1: Signal Description List

Signal Name	Function	Type	Active Level	Comments
NAND Flash Support				
NANDCS	NAND Flash Chip Select	Output	Low	
NANDOE	NAND Flash Output Enable	Output	Low	
NANDWE	NAND Flash Write Enable	Output	Low	
NANDALE	NAND Flash Address Latch Enable	Output	Low	
NANDCLE	NAND Flash Command Latch Enable	Output	Low	
SDRAM Controller - SDRAMC				
SDCK	SDRAM Clock	Output	–	
SDCKE	SDRAM Clock Enable	Output	High	
SDCS	SDRAM Controller Chip Select	Output	Low	
BA0–BA1	Bank Select	Output	–	
SDWE	SDRAM Write Enable	Output	Low	
RAS - CAS	Row and Column Signal	Output	Low	
SDA10	SDRAM Address 10 Line	Output	–	
Multimedia Card Interface - MCI				
MCCK	Multimedia Card Clock	Output	–	
MCCDA	Multimedia Card Slot A Command	I/O	–	
MCDA0–MCDA3	Multimedia Card Slot A Data	I/O	–	
MCCDB	Multimedia Card Slot B Command	I/O	–	
MCDB0–MCDB3	Multimedia Card Slot B Data	I/O	–	
Universal Synchronous Asynchronous Receiver Transmitter - USARTx				
SCKx	USARTx Serial Clock	I/O	–	
TXDx	USARTx Transmit Data	I/O	–	
RXDx	USARTx Receive Data	Input	–	
RTSx	USARTx Request To Send	Output	–	
CTSx	USARTx Clear To Send	Input	–	
DTR0	USART0 Data Terminal Ready	Output	–	
DSR0	USART0 Data Set Ready	Input	–	
DCD0	USART0 Data Carrier Detect	Input	–	
RI0	USART0 Ring Indicator	Input	–	
Synchronous Serial Controller - SSC				
TD	SSC Transmit Data	Output	–	
RD	SSC Receive Data	Input	–	
TK	SSC Transmit Clock	I/O	–	
RK	SSC Receive Clock	I/O	–	
TF	SSC Transmit Frame Sync	I/O	–	

Table 2-1: Signal Description List

Signal Name	Function	Type	Active Level	Comments
RF	SSC Receive Frame Sync	I/O	–	
Timer/Counter - TCx				
TCLKx	TC Channel x External Clock Input	Input	–	
TIOAx	TC Channel x I/O Line A	I/O	–	
TIOBx	TC Channel x I/O Line B	I/O	–	
Serial Peripheral Interface - SPIx				
SPIx_MISO	Master In Slave Out	I/O	–	
SPIx_MOSI	Master Out Slave In	I/O	–	
SPIx_SPCK	SPI Serial Clock	I/O	–	
SPIx_NPCS0	SPI Peripheral Chip Select 0	I/O	Low	
SPIx_NPCS1–SPIx_NPCS3	SPI Peripheral Chip Select	Output	Low	
Two-Wire Interface - TWI				
TWD	Two-wire Serial Data	I/O	–	
TWCK	Two-wire Serial Clock	I/O	–	
USB Host Port - UHP				
HDPA	USB Host Port A Data +	Analog	–	
HDMA	USB Host Port A Data -	Analog	–	
HDPB	USB Host Port B Data +	Analog	–	
HDMB	USB Host Port B Data -	Analog	–	
USB Device Port - UDP				
DDM	USB Device Port Data -	Analog	–	
DDP	USB Device Port Data +	Analog	–	
Ethernet MAC 10/100 - EMAC				
ETXCK	Transmit Clock or Reference Clock	Input	–	MII only, REFCK in RMII
ERXCK	Receive Clock	Input	–	MII only
ETXEN	Transmit Enable	Output	–	
ETX0–ETX3	Transmit Data	Output	–	ETX0–ETX1 only in RMII
ETXER	Transmit Coding Error	Output	–	MII only
ERXDV	Receive Data Valid	Input	–	RXDV in MII, CRSDV in RMII
ERX0–ERX3	Receive Data	Input	–	ERX0–ERX1 only in RMII
ERXER	Receive Error	Input	–	
ECRS	Carrier Sense and Data Valid	Input	–	MII only
ECOL	Collision Detect	Input	–	MII only
EMDC	Management Data Clock	Output	–	
EMDIO	Management Data Input/Output	I/O	–	

Table 2-1: Signal Description List

Signal Name	Function	Type	Active Level	Comments
Image Sensor Interface - ISI				
ISI_D0-ISI_D11	Image Sensor Data	Input	–	
ISI_MCK	Image Sensor Reference Clock	Output	–	
ISI_HSYNC	Image Sensor Horizontal Synchro	Input	–	
ISI_VSYNC	Image Sensor Vertical Synchro	Input	–	
ISI_PCK	Image Sensor Data clock	Input	–	
Analog-to-Digital Converter - ADC				
AD0-AD3	Analog Inputs	Analog	–	Digital pulled-up inputs at reset
ADVREF	Analog Positive Reference	Analog	–	
ADTRG	ADC Trigger	Input	–	

3. Package and Pinout

The SAM9G20 is available in the following Green-compliant packages:

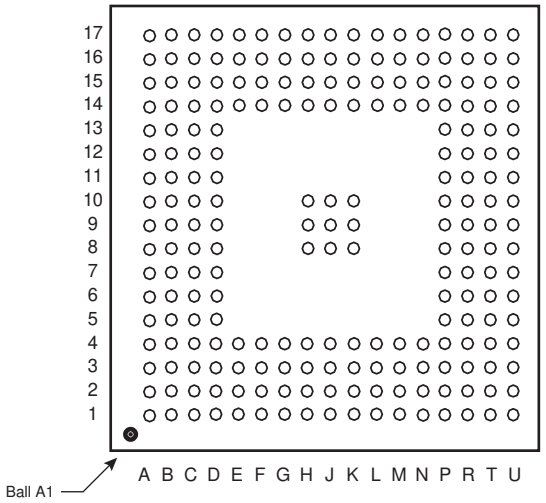
- 217-ball LFBGA, 15 x 15 mm x 1.4 mm (0.8 mm pitch)
- 247-ball TFBGA, 10 x 10 x 1.1 mm (0.5 mm pitch)

3.1 217-ball LFBGA Package Outline

Figure 3-1 shows the orientation of the 217-ball LFBGA package.

A detailed mechanical description is given in Section 41.1 “217-ball LFBGA Package Drawing”.

Figure 3-1: 217-ball LFBGA Package (Top View)



3.2 217-ball LFBGA Pinout

Table 3-1: Pinout for 217-ball LFBGA Package

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	CFIOW/NBS3/NWR3	D5	A5	J14	TDO	P17	PB5
A2	NBS0/A0	D6	GND	J15	PB19	R1	NC
A3	NWR2/NBS2/A1	D7	A10	J16	TDI	R2	GNDANA
A4	A6	D8	GND	J17	PB16	R3	PC29
A5	A8	D9	VDDCORE	K1	PC24	R4	VDDANA
A6	A11	D10	GNDUSB	K2	PC20	R5	PB12
A7	A13	D11	VDDIOM	K3	D15	R6	PB23
A8	BA0/A16	D12	GNDUSB	K4	PC21	R7	GND
A9	A18	D13	DDM	K8	GND	R8	PB26
A10	A21	D14	HDPB	K9	GND	R9	PB28
A11	A22	D15	NC	K10	GND	R10	PA0
A12	CFWE/NWE/NWR0	D16	VDDBU	K14	PB4	R11	PA4
A13	CFOE/NRD	D17	XIN32	K15	PB17	R12	PA5
A14	NCS0	E1	D10	K16	GND	R13	PA10

Table 3-1: Pinout for 217-ball LFBGA Package (Continued)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A15	PC5	E2	D5	K17	PB15	R14	PA21
A16	PC6	E3	D3	L1	GND	R15	PA23
A17	PC4	E4	D4	L2	PC26	R16	PA24
B1	SDCK	E14	HDPA	L3	PC25	R17	PA29
B2	CFIOR/NBS1/NWR1	E15	HDMA	L4	VDDOSC	T1	NC
B3	SDCS/NCS1	E16	GNDBU	L14	PA28	T2	GNDPLL
B4	SDA10	E17	XOUT32	L15	PB9	T3	PC0
B5	A3	F1	D13	L16	PB8	T4	PC1
B6	A7	F2	SDWE	L17	PB14	T5	PB10
B7	A12	F3	D6	M1	VDDCORE	T6	PB22
B8	A15	F4	GND	M2	PC31	T7	GND
B9	A20	F14	OSCSEL	M3	GND	T8	PB29
B10	NANDWE	F15	BMS	M4	PC22	T9	PA2
B11	PC7	F16	JTAGSEL	M14	PB1	T10	PA6
B12	PC10	F17	TST	M15	PB2	T11	PA8
B13	PC13	G1	PC15	M16	PB3	T12	PA11
B14	PC11	G2	D7	M17	PB7	T13	VDDCORE
B15	PC14	G3	SDCKE	N1	XIN	T14	PA20
B16	PC8	G4	VDDIOM	N2	VDDPLL	T15	GND
B17	WKUP	G14	GND	N3	PC23	T16	PA22
C1	D8	G15	NRST	N4	PC27	T17	PA27
C2	D1	G16	RTCK	N14	PA31	U1	GNDPLL
C3	CAS	G17	TMS	N15	PA30	U2	ADVREF
C4	A2	H1	PC18	N16	PB0	U3	PC2
C5	A4	H2	D14	N17	PB6	U4	PC3
C6	A9	H3	D12	P1	XOUT	U5	PB20
C7	A14	H4	D11	P2	VDDPLL	U6	PB21
C8	BA1/A17	H8	GND	P3	PC30	U7	PB25
C9	A19	H9	GND	P4	PC28	U8	PB27
C10	NANDOE	H10	GND	P5	PB11	U9	PA12
C11	PC9	H14	VDDCORE	P6	PB13	U10	PA13
C12	PC12	H15	TCK	P7	PB24	U11	PA14
C13	DDP	H16	NTRST	P8	VDDIOP	U12	PA15
C14	HDMB	H17	PB18	P9	PB30	U13	PA19
C15	NC	J1	PC19	P10	PB31	U14	PA17
C16	VDDUSB	J2	PC17	P11	PA1	U15	PA16

Table 3-1: Pinout for 217-ball LFBGA Package (Continued)

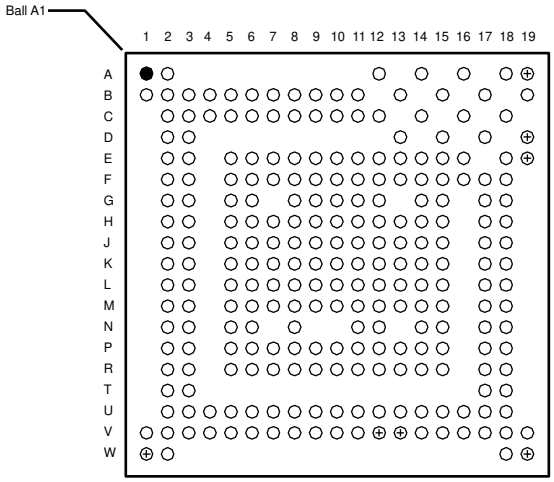
Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
C17	SHDN	J3	VDDIOM	P12	PA3	U16	PA18
D1	D9	J4	PC16	P13	PA7	U17	VDDIOP
D2	D2	J8	GND	P14	PA9		
D3	RAS	J9	GND	P15	PA26		
D4	D0	J10	GND	P16	PA25		

3.3 247-ball TFBGA Package Outline

Figure 3-2 shows the orientation of the 247-ball TFBGA package.

A detailed mechanical description is given in Section 41.2 “247-ball TFBGA Package Drawing”.

Figure 3-2: 247-ball TFBGA Package (Top View)



3.4 247-ball TFBGA Package Pinout

Table 3-2: Pinout for 247-ball TFBGA Package

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	D13	F7	CFIOR/NBS1/NWR1	K10	GND	P17	RTCK
A2	D12	F8	SDA10	K11	VDDIOM	P18	PB16
A12	A9	F9	NBS0/A0	K12	GND	R2	GND
A14	A13	F10	A6	K13	GND	R3	PB29
A16	A20	F11	A12	K14	XOUT32	R5	PB26
A18	A22	F12	A15	K15	XIN32	R6	PB27
A19	NANDOE	F13	BA1/A17	K17	HDPA	R7	PA5
B1	D15	F14	PC10	K18	HDMA	R8	GND
B2	D14	F15	PC14	L2	NC	R9	PA12
B3	D10	F16	VDDUSB	L3	NC	R10	GND

Table 3-2: Pinout for 247-ball TFBGA Package (Continued)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
B4	D9	F17	PC9	L5	ADVREF	R11	PA19
B5	D7	F18	PC12	L6	PC2	R12	PA26
B6	D3	G2	PC26	L7	GND	R13	PB1
B7	D2	G3	PC25	L8	GND	R14	GND
B8	RAS	G5	PC24	L9	GND	R15	PB7
B9	CAS	G6	PC21	L10	GND	R17	PB14
B10	NWR2/NBS2/A1	G8	VDDCORE	L11	VDDCORE	R18	PB9
B11	A3	G9	A5	L12	GND	T2	PA1
B13	A10	G10	VDDCORE	L13	OSCSEL	T3	PB10
B15	A18	G11	VDDCORE	L14	GNDBU	T17	PB19
B17	A21	G12	VDDCORE	L15	GND	T18	PB17
B19	VDDUSB	G14	PC13	L17	NRST	U2	GNDANA
C2	PC15	G15	GND	L18	TCK	U3	PB21
C3	D11	G17	GNDUSB	M2	PC0	U4	PB28
C4	D8	G18	PC11	M3	PC1	U5	PB31
C5	SDCKE	H2	PC31	M5	PC3	U6	PA4
C6	SDWE	H3	PC30	M6	NTRST	U7	PA3
C7	SDCK	H5	PC28	M7	GND	U8	PA9
C8	D1	H6	PC27	M8	GND	U9	GND
C9	SDCS/NCS1	H7	PC29	M9	GND	U10	PA15
C10	A2	H8	GND	M10	PA16	U11	PA21
C11	A7	H9	GND	M11	VDDCORE	U12	PA25
C12	A11	H10	VDDIOM	M12	GND	U13	PA29
C14	A19	H11	VDDIOM	M13	VDDIOP	U14	PA27
C16	GNDUSB	H12	GND	M14	TST	U15	PA31
C18	CFWE/NWE/NWR0	H13	VDDCORE	M15	JTAGSEL	U16	GND
D2	PC17	H14	SHDW	M17	PB18	U17	PB2
D3	PC16	H15	VDDBU	M18	TMS	U18	GND
D13	A14	H17	HDPB	N2	PB20	V1	PB12
D15	NANDWE	H18	HDMB	N3	PB13	V2	PB23
D17	CFOE/NRD	J2	VDDOSC	N5	PB11	V3	PB30
D19	NCS0	J3	VDDPLL	N6	BMS	V4	PA2
E2	PC18	J5	XOUT	N8	GND	V5	PA8
E3	PC19	J6	XIN	N11	PA17	V6	PA10
E5	D6	J7	VDDPLL	N12	PA23	V7	PA13
E6	D5	J8	GND	N14	GND	V8	VDDIOP

Table 3-2: Pinout for 247-ball TFBGA Package (Continued)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
E7	D0	J9	VDDIOM	N15	VDDIOP	V9	PA14
E8	CFIOW/NBS3/NWR3	J10	VDDIOM	N17	TDO	V10	VDDIOP
E9	GND	J11	VDDIOM	N18	TDI	V11	PA20
E10	A4	J12	GND	P2	PB24	V12	PA22
E11	A8	J13	GND	P3	PB22	V13	VDDIOP
E12	VDDIOM	J14	WKUP	P5	GND	V14	PA30
E13	BA0/A16	J15	DDP	P6	GND	V15	PB0
E14	PC8	J17	DDM	P7	PA6	V16	GND
E15	PC4	J18	VDDIOP	P8	PA7	V17	PB4
E16	PC5	K2	GNDPLL	P9	PA11	V18	GND
E18	PC7	K3	GND	P10	GND	V19	PB6
E19	PC6	K5	NC	P11	PA18	W1	PB25
F2	PC22	K6	GNDPLL	P12	PA24	W2	PA0
F3	PC23	K7	VDDANA	P13	PA28	W18	PB8
F5	PC20	K8	GND	P14	PB3	W19	PB15
F6	D4	K9	GND	P15	PB5		

4. Power Considerations

4.1 Power Supplies

The SAM9G20 has several types of power supply pins. Some supply pins share common ground (GND) pins whereas others have separate grounds. See Table 4-1.

Table 4-1: SAM9G20 Power Supply Pins

Pin(s)	Item(s) powered	Range	Nominal	Ground
VDDCORE	Core, including the processor Embedded memories Peripherals	0.9–1.1 V	1.0V	GND
VDDIOM	External Bus Interface I/O lines	1.65–1.95 V	1.8V	
		3.0–3.6 V	3.3V	
VDDOSC	Main Oscillator cells	1.65–3.6 V	–	
VDDIOP	Peripherals I/O lines	1.65–1.95 V	1.8V	
		3.0–3.6 V	3.3V	
VDDBU	Slow Clock oscillator Internal RC oscillator Part of the System Controller	0.9–1.1 V	1.0V	GNDBU
VDDPLL	PLL cells	0.9–1.1 V	1.0V	GNDPLL
VDDUSB	USB transceiver	3.0–3.6 V	3.3V	GNDUSB
VDDANA	Analog-to-Digital Converter	3.0–3.6 V	3.3V	GNDANA

4.2 Programmable I/O Lines

The power supply pins VDDIOM accept two voltage ranges. This allows the device to reach its maximum speed either out of 1.8V or 3.3V external memories.

The maximum speed is 133 MHz on the pin SDCK (SDRAM Clock) loaded with 10 pF. The other signals (control, address and data signals) do not go over 66 MHz, loaded with 30 pF for power supply at 1.8V and 50 pF for power supply at 3.3V.

The EBI I/Os accept two slew rate modes, Fast and Slow. This allows to adapt the rising and falling time on SDRAM clock, control and data to the bus load.

The voltage ranges and the slew rates are determined by programming VDDIOMSEL and IOSR bits in the Chip Configuration registers located in the Matrix User Interface.

At reset, the selected voltage defaults to 3.3V nominal and power supply pins can accept either 1.8V or 3.3V. The user must make sure to program the EBI voltage range before getting the device out of its Slow Clock mode.

At reset, the selected slew rates defaults are Fast.

4.3 Power Sequence Requirements

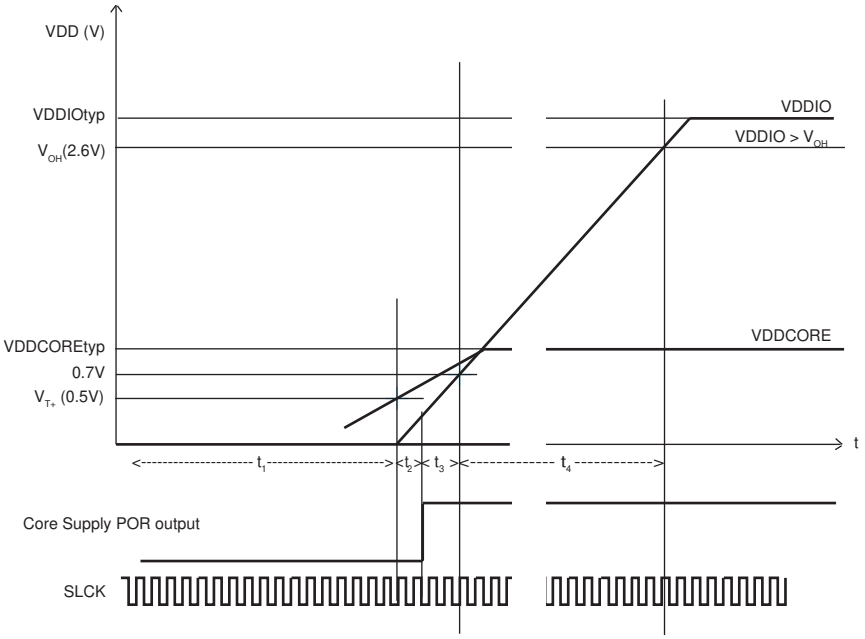
The SAM9G20 board design must comply with the power-up and power-down sequence guidelines described in the following sections to guarantee reliable operation of the device. Any deviation from these sequences may lead to the following situations:

- Excessive current consumption during the power-up phase which, in the worst case, can result in irreversible damage to the device.
- Prevent the device from booting.

4.3.1 Power-up Sequence

The power sequence described below is applicable to all the SAM9G20 revisions. However, the power sequence can be simplified for the revision B device. In this revision, the over consumption during the power-up phase has been limited to less than 200 mA. This current can not damage the device and if it is acceptable for the final application, the power sequence becomes VDDIO followed by VDDCORE. VDDIO must be established first (> 0.7V) to ensure a correct sampling of the BMS signal and also to guarantee the correct voltage level when accessing an external memory.

Figure 4-1: VDDCORE and VDDIO Constraints at Startup



VDDCORE and VDDBU are controlled by Power-on-Reset (POR) to guarantee that these power sources reach their target values prior to the release of POR. (See Figure 4-1.)

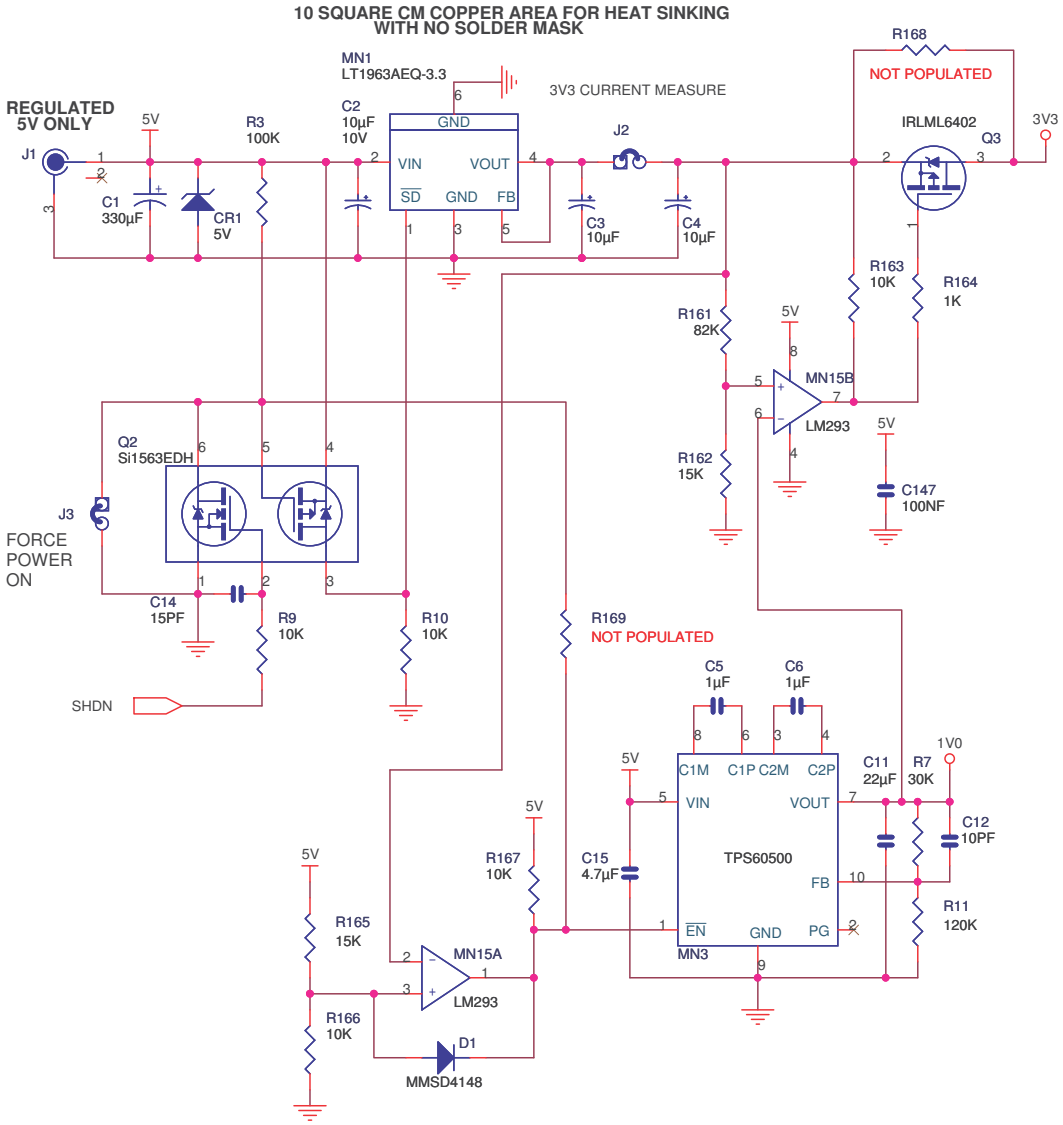
- VDDIOM and VDDIOP must NOT be powered until VDDCORE has reached a level superior or equal to V_{T+} (0.5V).
- VDDIOP must be ≥ V_{IH} (refer to Table 40-2 ”DC Characteristics” for more details), (t_{RST} + t_1) at the latest, after VDDCORE has reached V_{T+}.
- VDDIOM must reach V_{OH} (refer to Table 40-2 ”DC Characteristics” for more details), (t_{RST} + t_1 + t_2) at the latest, after VDDCORE has reached V_{T+}.
- t_2 = t_{RST} = 30 µs
- t_3 = 3 × t_{SLCK}
- t_4 = 14 × t_{SLCK}

The t_{SLCK} min (22 µs) is obtained for the maximum frequency of the internal RC oscillator (44 kHz). This gives:

- t_2 = t_{RST} = 30 µs
- t_3 = 66 µs
- t_4 = 308 µs

Figure 4-2 shows an example of the implementation on the evaluation kit AT91SAM9G20-EK Rev.C.

Figure 4-2: Power-up Sequence Implementation Example on AT91SAM9G20-EK Rev.C



4.3.2 Power-down Sequence

Switch off the VDDIOM and VDDIOP power supplies prior to, or at the same time, as VDDCORE. No power-up or power-down restrictions apply to VDDBU, VDDPL, VDDANA and VDDUSB.

5. I/O Line Considerations

5.1 JTAG Port Pins

TMS, TDI and TCK are schmitt trigger inputs and have no pull-up resistors.

TDO and RTCK are outputs, driven at up to VDDIOP, and have no pull-up resistor.

The JTAGSEL pin is used to select the JTAG boundary scan when asserted at a high level. It integrates a permanent pull-down resistor of about 15 kΩ to GND, so that it can be left unconnected for normal operations.

The NTRST signal is described in Section 5.3 “Reset Pins”.

All the JTAG signals are supplied with VDDIOP.

5.2 Test Pin

The TST pin is used for manufacturing test purposes when asserted high. It integrates a permanent pull-down resistor of about 15 kΩ to GNDBU, so that it can be left unconnected for normal operations. Driving this line at a high level leads to unpredictable results.

This pin is supplied with VDDBU.

5.3 Reset Pins

NRST is an open-drain output integrating a non-programmable pull-up resistor. It can be driven with voltage at up to VDDIOP.

NTRST is an input which allows reset of the JTAG Test Access port. It has no action on the processor.

As the product integrates power-on reset cells, which manages the processor and the JTAG reset, the NRST and NTRST pins can be left unconnected.

The NRST and NTRST pins both integrate a permanent pull-up resistor of 100 kΩ minimum to VDDIOP.

The NRST signal is inserted in the Boundary Scan.

5.4 PIO Controllers

All the I/O lines are Schmitt trigger inputs and all the lines managed by the PIO Controllers integrate a programmable pull-up resistor of 75 kΩ typical with the exception of P4–P31. For details, refer to Section 40. “Electrical Characteristics”. Programming of this pull-up resistor is performed independently for each I/O line through the PIO Controllers.

5.5 I/O Line Drive Levels

The PIO lines drive current capability is described in Section 40.2 “DC Characteristics”.

5.6 Shutdown Logic Pins

The SHDN pin is a tri-state output only pin, which is driven by the Shutdown Controller. There is no internal pull-up. An external pull-up to VDDBU is needed and its value must be higher than 1 MΩ.. The resistor value is calculated according to the regulator enable implementation and the SHDN level.

The pin WKUP is an input-only. It can accept voltages only between 0V and VDDBU.

6. Processor and Architecture

6.1 Arm926EJ-S Processor

- RISC Processor Based on Arm v5TEJ Architecture with Jazelle technology for Java acceleration
- Two Instruction Sets
  - Arm High-performance 32-bit Instruction Set
  - Thumb High Code Density 16-bit Instruction Set
- DSP Instruction Extensions
- 5-Stage Pipeline Architecture:
  - Instruction Fetch (F)
  - Instruction Decode (D)
  - Execute (E)
  - Data Memory (M)
  - Register Write (W)
- 32-Kbyte Data Cache, 32-Kbyte Instruction Cache
  - Virtually-addressed 4-way Associative Cache
  - Eight words per line
  - Write-through and Write-back Operation
  - Pseudo-random or Round-robin Replacement
- Write Buffer
  - Main Write Buffer with 16-word Data Buffer and 4-address Buffer
  - DCache Write-back Buffer with 8-word Entries and a Single Address Entry
  - Software Control Drain
- Standard Arm v4 and v5 Memory Management Unit (MMU)
  - Access Permission for Sections
  - Access Permission for large pages and small pages can be specified separately for each quarter of the page
  - 16 embedded domains
- Bus Interface Unit (BIU)
  - Arbitrates and Schedules AHB Requests
  - Separate Masters for both instruction and data access providing complete Matrix system flexibility
  - Separate Address and Data Buses for both the 32-bit instruction interface and the 32-bit data interface
  - On Address and Data Buses, data can be 8-bit (Bytes), 16-bit (Half-words) or 32-bit (Words)

6.2 Bus Matrix

- 6-layer Matrix, handling requests from 6 masters
- Programmable Arbitration strategy
  - Fixed-priority Arbitration
  - Round-Robin Arbitration, either with no default master, last accessed default master or fixed default master
- Burst Management
  - Breaking with Slot Cycle Limit Support
  - Undefined Burst Length Support
- One Address Decoder provided per Master
  - Three different slaves may be assigned to each decoded memory area: one for internal boot, one for external boot, one after remap
- Boot Mode Select
  - Non-volatile Boot Memory can be internal or external
  - Selection is made by BMS pin sampled at reset
- Remap Command
  - Allows Remapping of an Internal SRAM in Place of the Boot Non-Volatile Memory
- Allows Handling of Dynamic Exception Vectors

6.2.1 Matrix Masters

The Bus Matrix of the SAM9G20 manages six Masters, which means that each master can perform an access concurrently with others, according the slave it accesses is available.

Each Master has its own decoder that can be defined specifically for each master. In order to simplify the addressing, all the masters have the same decodings.

Table 6-1: List of Bus Matrix Masters

Master 0	Arm926™ Instruction
Master 1	Arm926 Data
Master 2	PDC
Master 3	ISI Controller
Master 4	Ethernet MAC
Master 5	USB Host DMA

6.2.2 Matrix Slaves

Each Slave has its own arbiter, thus allowing to program a different arbitration per Slave.

Table 6-2: List of Bus Matrix Slaves

Slave 0	Internal SRAM0 16 Kbytes
Slave 1	Internal SRAM1 16 Kbytes
Slave 2	Internal ROM
	USB Host User Interface
Slave 3	External Bus Interface
Slave 4	Internal Peripherals

6.2.3 Masters to Slaves Access

All the Masters can normally access all the Slaves. However, some paths do not make sense, like as example allowing access from the Ethernet MAC to the Internal Peripherals. Thus, these paths are forbidden or simply not wired, and shown "–" in Table 6-3.

Table 6-3: SAM9G20 Masters to Slaves Access

Master		0 & 1	2	3	4	5
Slave		Arm926 Instruction & Data	Peripheral DMA Controller	ISI Controller	Ethernet MAC	USB Host Controller
0	Internal SRAM 16 Kbytes	X	X	X	X	X
1	Internal SRAM 16 Kbytes	X	X	X	X	X
2	Internal ROM	X	X	–	–	–
	UHP User Interface	X	X	–	–	–
3	External Bus Interface	X	X	X	X	X
4	Internal Peripherals	X	X	–	–	–

6.3 Peripheral DMA Controller

- Acting as one Matrix Master
- Allows data transfers from/to peripheral to/from any memory space without any intervention of the processor.
- Next Pointer Support, forbids strong real-time constraints on buffer management.
- Twenty-four channels
  - Two for each USART
  - Two for the Debug Unit
  - Two for the Serial Synchronous Controller
  - Two for each Serial Peripheral Interface
  - One for Multimedia Card Interface
  - One for Analog-to-Digital Converter
  - Two for the Two-wire Interface

The Peripheral DMA Controller handles transfer requests from the channel according to the following priorities (Low to High priorities):

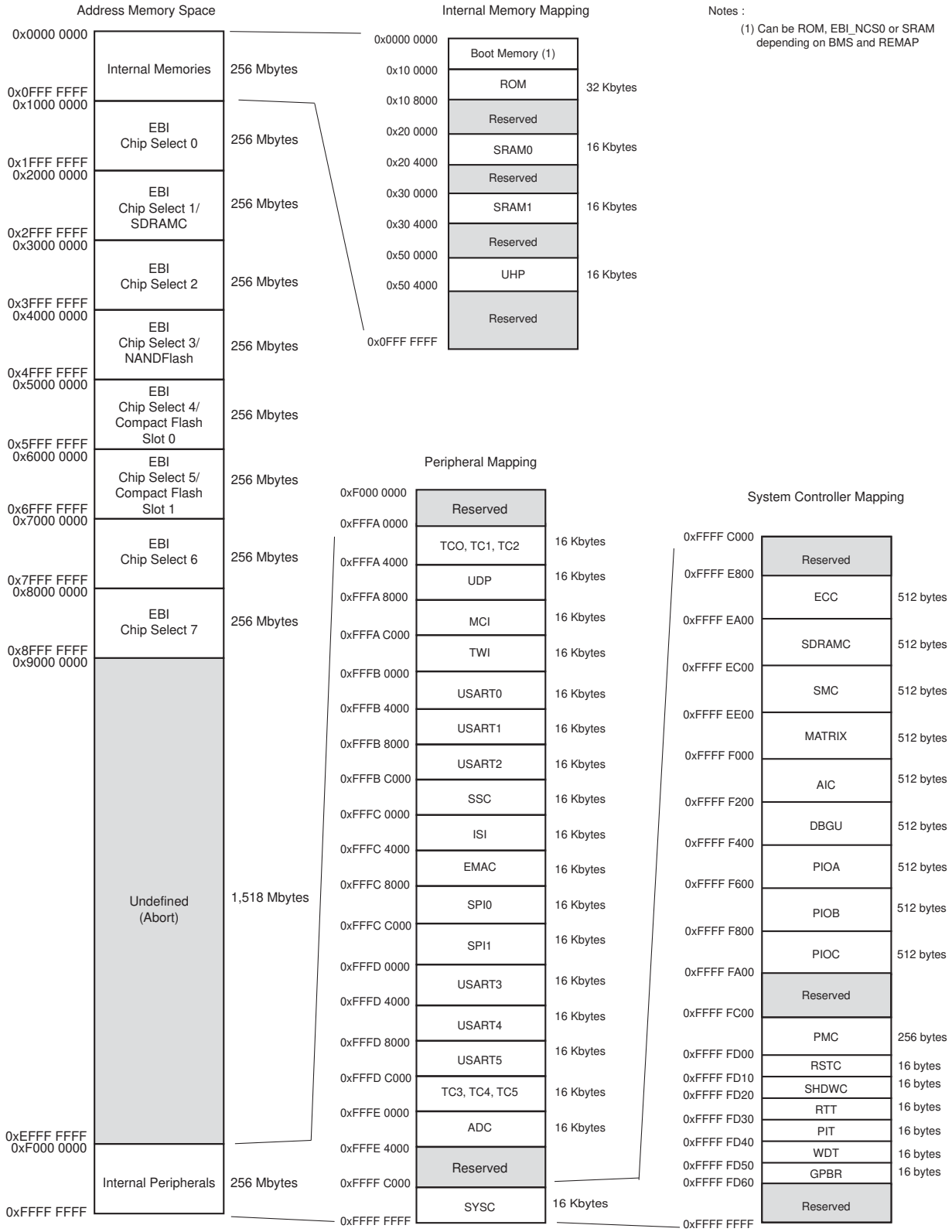
- TWI Transmit Channel
- DBGU Transmit Channel
- USART5 Transmit Channel
- USART4 Transmit Channel
- USART3 Transmit Channel
- USART2 Transmit Channel
- USART1 Transmit Channel
- USART0 Transmit Channel
- SPI1 Transmit Channel
- SPI0 Transmit Channel
- SSC Transmit Channel
- TWI Receive Channel
- DBGU Receive Channel
- USART5 Receive Channel
- USART4 Receive Channel
- USART3 Receive Channel
- USART2 Receive Channel
- USART1 Receive Channel
- USART0 Receive Channel
- ADC Receive Channel
- SPI1 Receive Channel
- SPI0 Receive Channel
- SSC Receive Channel
- MCI Transmit/Receive Channel

6.4 Debug and Test Features

- Arm926 Real-time In-circuit Emulator
  - Two real-time Watchpoint Units
  - Two Independent Registers: Debug Control Register and Debug Status Register
  - Test Access Port Accessible through JTAG Protocol
  - Debug Communications Channel
- Debug Unit
  - Two-pin UART
  - Debug Communication Channel Interrupt Handling
  - Chip ID Register
- IEEE1149.1 JTAG Boundary-scan on All Digital Pins

7. Memories

Figure 7-1: SAM9G20 Memory Mapping



A first level of address decoding is performed by the Bus Matrix, i.e., the implementation of the Advanced High Performance Bus (AHB) for its Master and Slave interfaces with additional features.

Decoding breaks up the 4 Gbytes of address space into 16 banks of 256 Mbytes. Banks 1 to 7 are directed to the EBI that associates these banks to the external chip selects EBI_NCS0 to EBI_NCS7. Bank 0 is reserved for the addressing of the internal memories, and a second level of decoding provides 1 Mbyte of internal memory area. Bank 15 is reserved for the peripherals and provides access to the Advanced Peripheral Bus (APB).

Other areas are unused and performing an access within them provides an abort to the master requesting such an access.

Each Master has its own bus and its own decoder, thus allowing a different memory mapping per Master. However, in order to simplify the mappings, all the masters have a similar address decoding.

Regarding Master 0 and Master 1 (Arm926 Instruction and Data), three different Slaves are assigned to the memory space decoded at address 0x0: one for internal boot, one for external boot, one after remap. Refer to Table 7-1 ”Internal Memory Mapping” for details.

7.1 Embedded Memories

- 64 Kbyte ROM
  - Single Cycle Access at full matrix speed
- Two 16 Kbyte Fast SRAM
  - Single Cycle Access at full matrix speed

7.1.1 Boot Strategies

Table 7-1 summarizes the Internal Memory Mapping for each Master, depending on the Remap status and the BMS state at reset.

Table 7-1: Internal Memory Mapping

Address	REMAP = 0		REMAP = 1
	BMS = 1	BMS = 0	
0x0000 0000	ROM	EBI_NCS0	SRAM0 16 KB
0x0010 0000	ROM		
0x0020 0000	SRAM0 16 KB		
0x0030 0000	SRAM1 16 KB		
0x0050 0000	USB Host User Interface		

The system always boots at address 0x0. To ensure a maximum number of possibilities for boot, the memory layout can be configured with two parameters.

REMAP allows the user to lay out the first internal SRAM bank to 0x0 to ease development. This is done by software once the system has booted. When REMAP = 1, BMS is ignored. Refer to Section 18. “SAM9G20 Bus Matrix” for more details.

When REMAP = 0, BMS allows the user to lay out to 0x0, at his convenience, the ROM or an external memory. This is done via hardware at reset.

Note: Memory blocks not affected by these parameters can always be seen at their specified base addresses. See the complete memory map presented in Figure 7-1.

The SAM9G20 matrix manages a boot memory that depends on the level on the BMS pin at reset. The internal memory area mapped between address 0x0 and 0x000F FFFF is reserved for this purpose.

If BMS is detected at 1, the boot memory is the embedded ROM.

If BMS is detected at 0, the boot memory is the memory connected on the Chip Select 0 of the External Bus Interface.

7.1.1.1 BMS = 1, Boot on Embedded ROM

The system boots using the Boot Program.

- Boot on slow clock (On-chip RC or 32768 Hz)
- Auto baudrate detection
- Downloads and runs an application from external storage media into internal SRAM
- Downloaded code size depends on embedded SRAM size

- Automatic detection of valid application
- Bootloader on a non-volatile memory
  - SDCard (boot ROM does not support high capacity SDCards.)
  - NAND Flash
  - SPI DataFlash and Serial Flash connected on NPCS0 and NPCS1 of the SPI0
  - EEPROM on TWI
- SAM-BA® Boot in case no valid program is detected in external NVM, supporting
  - Serial communication on a DBGU
  - USB Device HS Port

7.1.1.2 BMS = 0, Boot on External Memory

- Boot on slow clock (On-chip RC or 32768 Hz)
- Boot with the default configuration for the Static Memory Controller, byte select mode, 16-bit data bus, Read/Write controlled by Chip Select, allows boot on 16-bit non-volatile memory.

The customer-programmed software must perform a complete configuration.

To speed up the boot sequence when booting at 32 kHz EBI CS0 (BMS = 0), the user must take the following steps:

1. Program the PMC (main oscillator enable or bypass mode).
2. Program and start the PLL.
3. Reprogram the SMC setup, cycle, hold, mode timings registers for CS0 to adapt them to the new clock.
4. Switch the main clock to the new value.

7.2 External Memories

The external memories are accessed through the External Bus Interface. Each Chip Select line has a 256-Mbyte memory area assigned.

Refer to the memory map in Figure 7-1.

7.2.1 External Bus Interface

- Integrates three External Memory Controllers
  - Static Memory Controller
  - SDRAM Controller
  - ECC Controller
- Additional logic for NAND Flash
- Full 32-bit External Data Bus
- Up to 26-bit Address Bus (up to 64 Mbytes linear)
- Up to 8 chip selects, Configurable Assignment:
  - Static Memory Controller on NCS0
  - SDRAM Controller or Static Memory Controller on NCS1
  - Static Memory Controller on NCS2
  - Static Memory Controller on NCS3, Optional NAND Flash support
  - Static Memory Controller on NCS4–NCS5, Optional CompactFlash support
  - Static Memory Controller on NCS6–NCS7

7.2.2 Static Memory Controller

- 8-, 16- or 32-bit Data Bus
- Multiple Access Modes supported
  - Byte Write or Byte Select Lines
  - Asynchronous read in Page Mode supported (4- up to 32-byte page size)
- Multiple device adaptability
  - Compliant with LCD Module
  - Control signals programmable setup, pulse and hold time for each Memory Bank

- Multiple Wait State Management
  - Programmable Wait State Generation
  - External Wait Request
  - Programmable Data Float Time
- Slow Clock mode supported

7.2.3 SDRAM Controller

- Supported devices
  - Standard and Low-power SDRAM (Mobile SDRAM)
- Numerous configurations supported
  - 2K, 4K, 8K Row Address Memory Parts
  - SDRAM with two or four Internal Banks
  - SDRAM with 16- or 32-bit Datapath
- Programming facilities
  - Word, half-word, byte access
  - Automatic page break when Memory Boundary has been reached
  - Multibank Ping-pong Access
  - Timing parameters specified by software
  - Automatic refresh operation, refresh rate is programmable
- Energy-saving capabilities
  - Self-refresh, power down and deep power down modes supported
- Error detection
  - Refresh Error Interrupt
- SDRAM Power-up Initialization by software
- CAS Latency of 1, 2 and 3 supported
- Auto Precharge Command not used

7.2.4 Error Correction Code Controller

- Hardware Error Correction Code (ECC) Generation
  - Detection and Correction by Software
- Supports NAND Flash and SmartMedia™ Devices with 8- or 16-bit Data Path.
- Supports NAND Flash/SmartMedia with Page Sizes of 528, 1056, 2112 and 4224 Bytes, Specified by Software
- Supports 1 bit correction for a page of 512,1024,2048 and 4096 Bytes with 8- or 16-bit Data Path
- Supports 1 bit correction per 512 bytes of data for a page size of 512, 2048 and 4096 Bytes with 8-bit Data Path
- Supports 1 bit correction per 256 bytes of data for a page size of 512, 2048 and 4096 Bytes with 8-bit Data Path