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AT91SAM ARM-based Embedded MPU

SAM9G45

SUMMARY

Description

The ARM926EJ-S based SAM9G45 features the frequently demanded combination of user interface functionality and high data rate connectivity, including LCD Controller, resistive touch-screen, camera interface, audio, Ethernet 10/100 and high speed USB and SDIO. With the processor running at 400 MHz and multiple 100+ Mbps data rate peripherals, the SAM9G45 has the performance and bandwidth to the network or local storage media to provide an adequate user experience.

The SAM9G45 supports DDR2 and NAND Flash memory interfaces for program and data storage. An internal 133 MHz multi-layer bus architecture associated with 37 DMA channels, a dual external bus interface and distributed memory including a 64-Kbyte SRAM which can be configured as a tightly coupled memory (TCM) sustains the high bandwidth required by the processor and the high speed peripherals.

The I/Os support 1.8V or 3.3V operation, which are independently configurable for the memory interface and peripheral I/Os. This feature completely eliminates the need for any external level shifters. In addition it supports 0.8 ball pitch package for low cost PCB manufacturing.

The SAM9G45 power management controller features efficient clock gating and a battery backup section minimizing power consumption in active and standby modes.

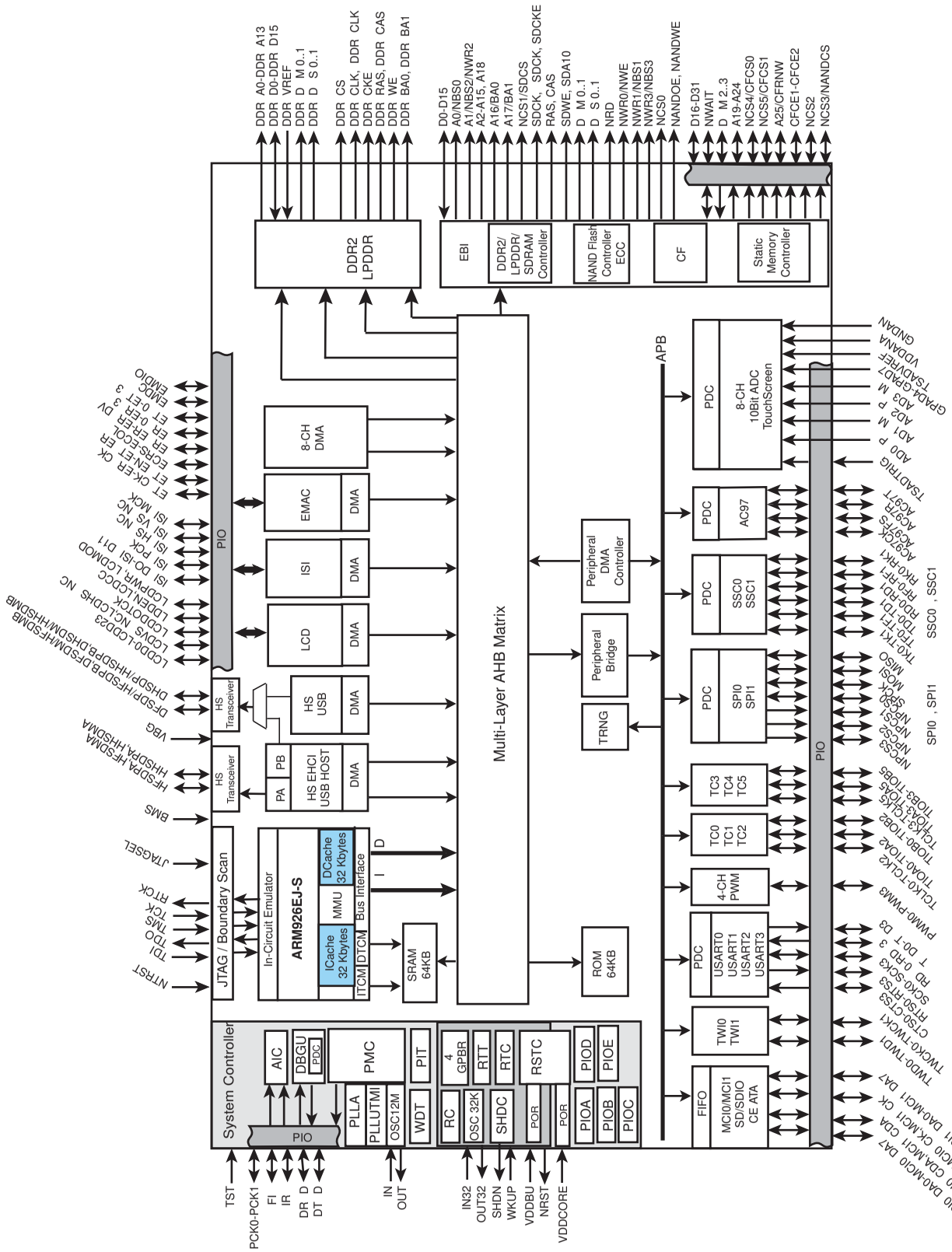
This is a summary document. The complete document is available on the Atmel website at www.atmel.com.

1. Features

- 400 MHz ARM926EJ-S™ ARM® Thumb® Processor
  - 32 Kbytes Data Cache, 32 Kbytes Instruction Cache, MMU
- Memories
  - DDR2 Controller 4-bank DDR2/LPDDR, SDRAM/LPSDR
  - External Bus Interface supporting 4-bank DDR2/LPDDR, SDRAM/LPSDR, Static Memories, CompactFlash, SLC NAND Flash with ECC
  - One 64-Kbyte internal SRAM, single-cycle access at system speed or processor speed through TCM interface
  - One 64-Kbyte internal ROM, embedding bootstrap routine
- Peripherals
  - LCD Controller supporting STN and TFT displays up to 1280*860
  - ITU-R BT. 601/656 Image Sensor Interface
  - USB Device High Speed, USB Host High Speed and USB Host Full Speed with On-Chip Transceiver
  - 10/100 Mbps Ethernet MAC Controller
  - Two High Speed Memory Card Hosts (SDIO, SDCard, MMC)
  - AC'97 controller
  - Two Master/Slave Serial Peripheral Interfaces
  - Two Three-channel 16-bit Timer/Counters
  - Two Synchronous Serial Controllers (I2S mode)
  - Four-channel 16-bit PWM Controller
  - Two Two-wire Interfaces
  - Four USARTs with ISO7816, IrDA, Manchester and SPI modes
  - 8-channel 10-bit ADC with 4-wire Touch Screen support
  - Write Protected Registers
- System
  - 133 MHz twelve 32-bit layer AHB Bus Matrix
  - 37 DMA Channels
  - Boot from NAND Flash, SDCard, DataFlash® or serial DataFlash
  - Reset Controller with on-chip Power-on Reset
  - Selectable 32768 Hz Low-power and 12 MHz Crystal Oscillators
  - Internal Low-power 32 kHz RC Oscillator
  - One PLL for the system and one 480 MHz PLL optimized for USB High Speed
  - Two Programmable External Clock Signals
  - Advanced Interrupt Controller and Debug Unit
  - Periodic Interval Timer, Watchdog Timer, Real Time Timer and Real Time Clock
- I/O
  - Five 32-bit Parallel Input/Output Controllers
  - 160 Programmable I/O Lines Multiplexed with up to Two Peripheral I/Os with Schmitt trigger input
- Package
  - 324-ball TFBGA, pitch 0.8 mm

2. Block Diagram

Figure 2-1. SAM9G45 Block Diagram



3. Signal Description

Table 3-1 gives details on the signal names classified by peripheral.

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level	Reference Voltage	Comments
Power Supplies					
VDDIOM0	DDR2 I/O Lines Power Supply	Power			1.65V to 1.95V
VDDIOM1	EBI I/O Lines Power Supply	Power			1.65V to 1.95V or 3.0V to3.6V
VDDIOP0	Peripherals I/O Lines Power Supply	Power			1.65V to 3.6V
VDDIOP1	Peripherals I/O Lines Power Supply	Power			1.65V to 3.6V
VDDIOP2	ISI I/O Lines Power Supply	Power			1.65V to 3.6V
VDDBU	Backup I/O Lines Power Supply	Power			1.8V to 3.6V
VDDANA	Analog Power Supply	Power			3.0V to 3.6V
VDDPLLA	PLLA Power Supply	Power			0.9V to 1.1V
VDDPLLUTMI	PLLUTMI Power Supply	Power			0.9V to 1.1V
VDDOSC	Oscillator Power Supply	Power			1.65V to 3.6V
VDDCORE	Core Chip Power Supply	Power			0.9V to 1.1V
VDDUTMIC	UDPHS and UHPHS UTMI+ Core Power Supply	Power			0.9V to 1.1V
VDDUTMII	UDPHS and UHPHS UTMI+ interface Power Supply	Power			3.0V to 3.6V
GNDIOM	DDR2 and EBI I/O Lines Ground	Ground			
GNDIOP	Peripherals and ISI I/O lines Ground	Ground			
GNDCORE	Core Chip Ground	Ground			
GNDOSC	PLLA, PLLUTMI and Oscillator Ground	Ground			
GNDBU	Backup Ground	Ground			
GNDUTMI	UDPHS and UHPHS UTMI+ Core and interface Ground	Ground			
GNDANA	Analog Ground	Ground			
Clocks, Oscillators and PLLs					
XIN	Main Oscillator Input	Input			
XOUT	Main Oscillator Output	Output			
XIN32	Slow Clock Oscillator Input	Input			
XOUT32	Slow Clock Oscillator Output	Output			
VBG	Bias Voltage Reference for USB	Analog			
PCK0 - PCK1	Programmable Clock Output	Output		(1)	

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Reference Voltage	Comments
Shutdown, Wakeup Logic					
SHDN	Shut-Down Control	Output		VDDBU	Driven at 0V only. 0: The device is in backup mode 1: The device is running (not in backup mode).
WKUP	Wake-Up Input	Input		VDDBU	Accept between 0V and VDDBU.
ICE and JTAG					
TCK	Test Clock	Input		VDDIOP0	No pull-up resistor, Schmitt trigger
TDI	Test Data In	Input		VDDIOP0	No pull-up resistor, Schmitt trigger
TDO	Test Data Out	Output		VDDIOP0	
TMS	Test Mode Select	Input		VDDIOP0	No pull-up resistor, Schmitt trigger
JTAGSEL	JTAG Selection	Input		VDDBU	Pull-down resistor (15 kΩ).
RTCK	Return Test Clock	Output		VDDIOP0	
Reset/Test					
NRST	Microcontroller Reset[2]	I/O	Low	VDDIOP0	Open-drain output, Pull-Up resistor (100 kΩ), Schmitt trigger
TST	Test Mode Select	Input		VDDBU	Pull-down resistor (15 kΩ), Schmitt trigger
NTRST	Test Reset Signal	Input		VDDIOP0	Pull-Up resistor (100 kΩ), Schmitt trigger
BMS	Boot Mode Select	**Input**		VDDIOP0	must be connected to GND or VDDIOP.
Debug Unit - DBGU					
DRXD	Debug Receive Data	Input		[1]	
DTXD	Debug Transmit Data	Output		[1]	
Advanced Interrupt Controller - AIC					
IRQ	External Interrupt Input	Input		[1]	
FIQ	Fast Interrupt Input	Input		[1]	
PIO Controller - PIOA- PIOB - PIOC - PIOD - PIOE					
PA0 - PA31	Parallel IO Controller A	I/O		[1]	Pulled-up input at reset (100kΩ)[3], Schmitt trigger
PB0 - PB31	Parallel IO Controller B	I/O		[1]	Pulled-up input at reset (100kΩ)[3], Schmitt trigger
PC0 - PC31	Parallel IO Controller C	I/O		[1]	Pulled-up input at reset (100kΩ)[3], Schmitt trigger

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Reference Voltage	Comments
PD0 - PD31	Parallel IO Controller D	I/O		(1)	Pulled-up input at reset (100kΩ)(3), Schmitt trigger
PE0 - PE31	Parallel IO Controller E	I/O		(1)	Pulled-up input at reset (100kΩ)(3), Schmitt trigger
DDR Memory Interface- DDR2/SDRAM/LPDDR Controller					
DDR_D0 - DDR_D15	Data Bus	I/O		VDDIOM0	Pulled-up input at reset
DDR_A0 - DDR_A13	Address Bus	Output		VDDIOM0	0 at reset
DDR_CLK-#DDR_CLK	DDR differential clock input	Output		VDDIOM0	
DDR_CKE	DDR Clock Enable	Output	High	VDDIOM0	
DDR_CS	DDR Chip Select	Output	Low	VDDIOM0	
DDR_WE	DDR Write Enable	Output	Low	VDDIOM0	
DDR_RAS-DDR_CAS	Row and Column Signal	Output	Low	VDDIOM0	
DDR_DQM[0..1]	Write Data Mask	Output		VDDIOM0	
DDR_DQS[0..1]	Data Strobe	Output		VDDIOM0	
DDR_BA0 - DDR_BA1	Bank Select	Output		VDDIOM0	
DDR_VREF	Reference Voltage	Input		VDDIOM0	
External Bus Interface - EBI					
D0 -D31	Data Bus	I/O		VDDIOM1	Pulled-up input at reset
A0 - A25	Address Bus	Output		VDDIOM1	0 at reset
NWAIT	External Wait Signal	Input	Low	VDDIOM1	
Static Memory Controller - SMC					
NCS0 - NCS5	Chip Select Lines	Output	Low	VDDIOM1	
NWR0 - NWR3	Write Signal	Output	Low	VDDIOM1	
NRD	Read Signal	Output	Low	VDDIOM1	
NWE	Write Enable	Output	Low	VDDIOM1	
NBS0 - NBS3	Byte Mask Signal	Output	Low	VDDIOM1	
CompactFlash Support					
CFCE1 - CFCE2	CompactFlash Chip Enable	Output	Low	VDDIOM1	
CFOE	CompactFlash Output Enable	Output	Low	VDDIOM1	
CFWE	CompactFlash Write Enable	Output	Low	VDDIOM1	
CFIOR	CompactFlash IO Read	Output	Low	VDDIOM1	
CFIOW	CompactFlash IO Write	Output	Low	VDDIOM1	
CFRNW	CompactFlash Read Not Write	Output		VDDIOM1	
CFCS0 -CFCS1	CompactFlash Chip Select Lines	Output	Low	VDDIOM1	

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Reference Voltage	Comments
NAND Flash Support					
NANDCS	NAND Flash Chip Select	Output	Low	VDDIOM1	
NANDOE	NAND Flash Output Enable	Output	Low	VDDIOM1	
NANDWE	NAND Flash Write Enable	Output	Low	VDDIOM1	
DDR2/SDRAM/LPDDR Controller					
SDCK,#SDCK	DDR2/SDRAM differential clock	Output		VDDIOM1	
SDCKE	DDR2/SDRAM Clock Enable	Output	High	VDDIOM1	
SDCS	DDR2/SDRAM Controller Chip Select	Output	Low	VDDIOM1	
BA0 - BA1	Bank Select	Output		VDDIOM1	
SDWE	DDR2/SDRAM Write Enable	Output	Low	VDDIOM1	
RAS - CAS	Row and Column Signal	Output	Low	VDDIOM1	
SDA10	SDRAM Address 10 Line	Output		VDDIOM1	
DQS[0..1]	Data Strobe	Output		VDDIOM1	
DQM[0..3]	Write Data Mask	Output		VDDIOM1	
High Speed Multimedia Card Interface - HSMCIx					
MCIx_CK	Multimedia Card Clock	I/O		(1)	
MCIx_CDA	Multimedia Card Slot A Command	I/O		(1)	
MCIx_DA0 - MCIx_DA7	Multimedia Card Slot A Data	I/O		(1)	
Universal Synchronous Asynchronous Receiver Transmitter - USARTx					
SCKx	USARTx Serial Clock	I/O		(1)	
TXDx	USARTx Transmit Data	Output		(1)	
RXDx	USARTx Receive Data	Input		(1)	
RTSx	USARTx Request To Send	Output		(1)	
CTSx	USARTx Clear To Send	Input		(1)	
Synchronous Serial Controller - SSCx					
TDx	SSC Transmit Data	Output		(1)	
RDx	SSC Receive Data	Input		(1)	
TKx	SSC Transmit Clock	I/O		(1)	
RKx	SSC Receive Clock	I/O		(1)	
TFx	SSC Transmit Frame Sync	I/O		(1)	
RFx	SSC Receive Frame Sync	I/O		(1)	

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Reference Voltage	Comments
AC97 Controller - AC97C					
AC97RX	AC97 Receive Signal	Input		(1)	
AC97TX	AC97 Transmit Signal	Output		(1)	
AC97FS	AC97 Frame Synchronization Signal	Output		(1)	
AC97CK	AC97 Clock signal	Input		(1)	
Time Counter - TCx					
TCLKx	TC Channel x External Clock Input	Input		(1)	
TIOAx	TC Channel x I/O Line A	I/O		(1)	
TIOBx	TC Channel x I/O Line B	I/O		(1)	
Pulse Width Modulation Controller - PWM					
PWMx	Pulse Width Modulation Output	Output		(1)	
Serial Peripheral Interface - SPIx_					
SPIx_MISO	Master In Slave Out	I/O		(1)	
SPIx_MOSI	Master Out Slave In	I/O		(1)	
SPIx_SPCK	SPI Serial Clock	I/O		(1)	
SPIx_NPCS0	SPI Peripheral Chip Select 0	I/O	Low	(1)	
SPIx_NPCS1-SPIx_NPCS3	SPI Peripheral Chip Select	Output	Low	(1)	
Two-Wire Interface					
TWDx	Two-wire Serial Data	I/O		(1)	
TWCKx	Two-wire Serial Clock	I/O		(1)	
USB Host High Speed Port - UHPHS					
HFSDPA	USB Host Port A Full Speed Data +	Analog		VDDUTMII	
HFSDMA	USB Host Port A Full Speed Data -	Analog		VDDUTMII	
HHSDPA	USB Host Port A High Speed Data +	Analog		VDDUTMII	
HHSDMA	USB Host Port A High Speed Data -	Analog		VDDUTMII	
HFSDPB	USB Host Port B Full Speed Data +	Analog		VDDUTMII	Multiplexed with DFSDP
HFSDMB	USB Host Port B Full Speed Data -	Analog		VDDUTMII	Multiplexed with DFSDM
HHSDPB	USB Host Port B High Speed Data +	Analog		VDDUTMII	Multiplexed with DHSDP
HHSDMB	USB Host Port B High Speed Data -	Analog		VDDUTMII	Multiplexed with DHSDM
USB Device High Speed Port - UDPHS					
DFSDM	USB Device Full Speed Data -	Analog		VDDUTMII	
DFSDP	USB Device Full Speed Data +	Analog		VDDUTMII	
DHSDM	USB Device High Speed Data -	Analog		VDDUTMII	
DHSDP	USB Device High Speed Data +	Analog		VDDUTMII	

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Reference Voltage	Comments
Ethernet 10/100					
ETXCK	Transmit Clock or Reference Clock	Input		(1)	MII only, REFCK in RMII
ERXCK	Receive Clock	Input		(1)	MII only
ETXEN	Transmit Enable	Output		(1)	
ETX0-ETX3	Transmit Data	Output		(1)	ETX0-ETX1 only in RMII
ETXER	Transmit Coding Error	Output		(1)	MII only
ERXDV	Receive Data Valid	Input		(1)	RXDV in MII, CRSDV in RMII
ERX0-ERX3	Receive Data	Input		(1)	ERX0-ERX1 only in RMII
ERXER	Receive Error	Input		(1)	
ECRS	Carrier Sense and Data Valid	Input		(1)	MII only
ECOL	Collision Detect	Input		(1)	MII only
EMDC	Management Data Clock	Output		(1)	
EMDIO	Management Data Input/Output	I/O		(1)	
Image Sensor Interface					
ISI_D0-ISI_D11	Image Sensor Data	Input		VDDIOP2	
ISI_MCK	Image sensor Reference clock	output		VDDIOP2	
ISI_HSYNC	Image Sensor Horizontal Synchro	input		VDDIOP2	
ISI_VSYNC	Image Sensor Vertical Synchro	input		VDDIOP2	
ISI_PCK	Image Sensor Data clock	input		VDDIOP2	
LCD Controller - LCDC					
LCDD0 - LCDD23	LCD Data Bus	Output		VDDIOP1	
LCDVSYNC	LCD Vertical Synchronization	Output		VDDIOP1	
LCDHSYNC	LCD Horizontal Synchronization	Output		VDDIOP1	
LCDDOTCK	LCD Dot Clock	Output		VDDIOP1	
LCDDEN	LCD Data Enable	Output		VDDIOP1	
LCDCC	LCD Contrast Control	Output		VDDIOP1	
LCDPWR	LCD panel Power enable control	Output		VDDIOP1	
LCDMOD	LCD Modulation signal	Output		VDDIOP1	
Touch Screen Analog-to-Digital Converter					
$AD0X_P$	Analog input channel 0 or Touch Screen Top channel	Analog		VDDANA	Multiplexed with AD0
$AD1X_M$	Analog input channel 1 or Touch Screen Bottom channel	Analog		VDDANA	Multiplexed with AD1
$AD2Y_P$	Analog input channel 2 or Touch Screen Right channel	Analog		VDDANA	Multiplexed with AD2
$AD3Y_M$	Analog input channel 3 or Touch Screen Left channel	Analog		VDDANA	Multiplexed with AD3

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Reference Voltage	Comments
GPAD4-GPAD7	Analog Inputs	Analog		VDDANA	
TSADTRG	ADC Trigger	Input		VDDANA	
TSADVREF	ADC Reference	Analog		VDDANA	

Notes:
1. Refer to peripheral multiplexing tables in Section 9.4 “Peripheral Signals Multiplexing on I/O Lines” for these signals.
2. When configured as an input, the NRST pin enables asynchronous reset of the device when asserted low. This allows connection of a simple push button on the NRST pin as a system-user reset.
3. Programming of this pull-up resistor is performed independently for each I/O line through the PIO Controllers. After reset, all the I/O lines default as inputs with pull-up resistors enabled, except those which are multiplexed with the External Bus Interface signals that require to be enabled as Peripheral at reset. This is explicitly indicated in the column “Reset State” of the peripheral multiplexing tables.

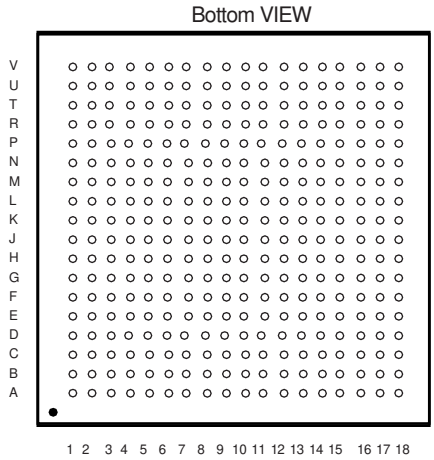
4. Package and Pinout

The SAM9G45 is delivered in a 324-ball TFBGA package.

4.1 Mechanical Overview of the 324-ball TFBGA Package

Figure 4-1 shows the orientation of the 324-ball TFBGA Package

Figure 4-1. Orientation of the 324-ball TFBGA Package



4.2 324-ball TFBGA Package Pinout

Table 4-1. SAM9G45 Pinout for 324-ball BGA Package

Pin	Signal Name
A1	PC27
A2	PC28
A3	PC25
A4	PC20
A5	PC12
A6	PC7
A7	PC5
A8	PC0
A9	NWR3/NBS3
A10	NCS0
A11	DQS0
A12	RAS
A13	SDCK
A14	NSDCK
A15	D7
A16	DDR_VREF
A17	D0
A18	A14
B1	PC31
B2	PC29
B3	PC30
B4	PC22
B5	PC17
B6	PC10
B7	PC11
B8	PC2
B9	SDA10
B10	A17/BA1
B11	DQM0
B12	SDCKE
B13	D12
B14	D8
B15	D4
B16	D3
B17	A15
B18	A13
C1	XIN32
C2	GNDANA
C3	WKUP
C4	PC26
C5	PC21
C6	PC15
C7	PC9
C8	PC3
C9	NWR0/NWE
C10	A16/BA0
C11	CAS
C12	D15
C13	D10
C14	D6

Pin	Signal Name
E10	NANDWE
E11	DQS1
E12	D13
E13	D11
E14	A4
E15	A8
E16	A9
E17	A7
E18	VDDCORE
F1	PD22
F2	PD24
F3	SHDN
F4	PE1
F5	PE3
F6	VDDIOM1
F7	PC19
F8	PC14
F9	PC4
F10	NCS1/SDCS
F11	NRD
F12	SDWE
F13	A0/NBS0
F14	A1/NBS2/NWR2
F15	A3
F16	A6
F17	A5
F18	A2
G1	PD25
G2	PD23
G3	PE6
G4	PE0
G5	PE2
G6	PE8
G7	PE4
G8	PE11
G9	GNDCORE
G10	VDDIOM1
G11	VDDIOM1
G12	VDDCORE
G13	VDDCORE
G14	DDR_DQM0
G15	DDR_DQS1
G16	DDR_BA1
G17	DDR_BA0
G18	DDR_DQS0
H1	PD26
H2	PD27
H3	VDDIOP1
H4	PE13
H5	PE5

Pin	Signal Name
K1	PE21
K2	PE23
K3	PE26
K4	PE22
K5	PE24
K6	PE25
K7	PE27
K8	PE28
K9	VDDIOP0
K10	VDDIOP0
K11	GNDIOM
K12	GNDIOM
K13	VDDIOM0
K14	DDR_A7
K15	DDR_A8
K16	DDR_A9
K17	DDR_A11
K18	DDR_A10
L1	PA0
L2	PE30
L3	PE29
L4	PE31
L5	PA2
L6	PA4
L7	PA8
L8	PD2
L9	PD13
L10	PD29
L11	PD31
L12	VDDIOM0
L13	VDDIOM0
L14	DDR_A1
L15	DDR_A3
L16	DDR_A4
L17	DDR_A6
L18	DDR_A5
M1	PA1
M2	PA5
M3	PA6
M4	PA7
M5	PA10
M6	PA14
M7	PB14
M8	PD4
M9	PD15
M10	NRST
M11	PB11
M12	PB25
M13	PB27
M14	VDDIOM0

Pin	Signal Name
P10	TMS
P11	VDDPLLA
P12	PB20
P13	PB31
P14	DDR_D7
P15	DDR_D3
P16	DDR_D4
P17	DDR_D5
P18	DDR_D10
R1	PA18
R2	PA20
R3	PA24
R4	PA30
R5	PB4
R6	PB13
R7	PD0
R8	PD9
R9	PD18
R10	TDI
R11	RTCK
R12	PB22
R13	PB29
R14	DDR_D6
R15	DDR_D1
R16	DDR_D0
R17	HHSDMA
R18	HFSDMA
T1	PA22
T2	PA25
T3	PA26
T4	PB0
T5	PB6
T6	PB16
T7	PD1
T8	PD11
T9	PD19
T10	PD30
T11	BMS
T12	PB8
T13	PB30
T14	DDR_D2
T15	PB21
T16	PB23
T17	HHSDPA
T18	HFSDPA
U1	PA27
U2	PA29
U3	PA28
U4	PB3
U5	PB7

Table 4-1. SAM9G45 Pinout for 324-ball BGA Package (Continued)

Pin	Signal Name
C15	D2
C16	GNDIOM
C17	A18
C18	A12
D1	XOUT32
D2	PD20
D3	GNDBU
D4	VDDBU
D5	PC24
D6	PC18
D7	PC13
D8	PC6
D9	NWR1/NBS1
D10	NANDOE
D11	DQM1
D12	D14
D13	D9
D14	D5
D15	D1
D16	VDDIOM1
D17	A11
D18	A10
E1	PD21
E2	TSADVREF
E3	VDDANA
E4	JTAGSEL
E5	TST
E6	PC23
E7	PC16
E8	PC8
E9	PC1

Pin	Signal Name
H6	PE7
H7	PE9
H8	PE10
H9	GNDCORE
H10	GNDIOP
H11	VDDCORE
H12	GNDIOM
H13	GNDIOM
H14	DDR_CS
H15	DDR_WE
H16	DDR_DQM1
H17	DDR_CAS
H18	DDR_NCLK
J1	PE19
J2	PE16
J3	PE14
J4	PE15
J5	PE12
J6	PE17
J7	PE18
J8	PE20
J9	GNDCORE
J10	GNDCORE
J11	GNDIOP
J12	GNDIOM
J13	GNDIOM
J14	DDR_A12
J15	DDR_A13
J16	DDR_CKE
J17	DDR_RAS
J18	DDR_CLK

Pin	Signal Name
M15	DDR_D14
M16	DDR_D15
M17	DDR_A0
M18	DDR_A2
N1	PA3
N2	PA9
N3	PA12
N4	PA15
N5	PA16
N6	PA17
N7	PB18
N8	PD6
N9	PD16
N10	NTRST
N11	PB9
N12	PB24
N13	PB28
N14	DDR_D13
N15	DDR_D8
N16	DDR_D9
N17	DDR_D11
N18	DDR_D12
P1	PA11
P2	PA13
P3	PA19
P4	PA21
P5	PA23
P6	PB12
P7	PB19
P8	PD8
P9	PD28

Pin	Signal Name
U6	PB17
U7	PD7
U8	PD10
U9	PD14
U10	TCK
U11	VDDOSC
U12	GNDOSC
U13	PB10
U14	PB26
U15	HHSDPB/DHSDP
U16	HHSDMB/DHSDM
U17	GNDUTMI
U18	VDDUTMIC
V1	PA31
V2	PB1
V3	PB2
V4	PB5
V5	PB15
V6	PD3
V7	PD5
V8	PD12
V9	PD17
V10	TDO
V11	XOUT
V12	XIN
V13	VDDPLLUTMI
V14	VDDIOP2
V15	HFSDPB/DFSDP
V16	HFSDMB/DFSDM
V17	VDDUTMII
V18	VBG

5. Power Considerations

5.1 Power Supplies

The SAM9G45 has several types of power supply pins:

- VDDCORE pins: Power the core, including the processor, the embedded memories and the peripherals; voltage ranges from 0.9V to 1.1V, 1.0V typical.
- VDDIOM0 pins: Power the DDR2/LPDDR I/O lines; voltage ranges between 1.65V and 1.95V (1.8V typical).
- VDDIOM1 pins: Power the External Bus Interface 1 I/O lines; voltage ranges between 1.65V and 1.95V (1.8V typical) or between 3.0V and 3.6V (3.3V typical).
- VDDIOP0, VDDIOP1, VDDIOP2 pins: Power the Peripherals I/O lines; voltage ranges from 1.65V to 3.6V.
- VDDBU pin: Powers the Slow Clock oscillator, the internal RC oscillator and a part of the System Controller; voltage ranges from 1.8V to 3.6V.
- VDDPLLUTMI pin: Powers the PLLUTMI cell; voltage range from 0.9V to 1.1V.
- VDDUTMIC pin: Powers the USB device and host UTMI+ core; voltage range from 0.9V to 1.1V, 1.0V typical.
- VDDUTMII pin: Powers the USB device and host UTMI+ interface; voltage range from 3.0V to 3.6V, 3.3V typical.
- VDDPLLA pin: Powers the PLLA cell; voltage ranges from 0.9V to 1.1V.
- VDDOSC pin: Powers the Main Oscillator cells; voltage ranges from 1.65V to 3.6V
- VDDANA pin: Powers the Analog to Digital Converter; voltage ranges from 3.0V to 3.6V, 3.3V typical.

Some supply pins share common ground (GND) pins whereas others have separate grounds.

The respective power/ground pin assignments are as follows:

VDDCORE	GNDCORE
VDDIOM0, VDDIOM1	GNDIOM
VDDIOP0, VDDIOP1, VDDIOP2	GNDIOP
VDDBU	GNDBU
VDDUTMIC, VDDUTMII	GNDUTMI
VDDPLLUTMI, VDDPLLA, VDDOSC,	GNDOSC
VDDANA	GNDANA

6. Processor and Architecture

6.1 ARM926EJ-S Processor

- RISC Processor Based on ARM v5TEJ Architecture with Jazelle technology for Java acceleration
- Two Instruction Sets
  - ARM High-performance 32-bit Instruction Set
  - Thumb High Code Density 16-bit Instruction Set
- DSP Instruction Extensions
- 5-Stage Pipeline Architecture:
  - Instruction Fetch (F)
  - Instruction Decode (D)
  - Execute (E)
  - Data Memory (M)
  - Register Write (W)
- 32-KByte Data Cache, 32-KByte Instruction Cache
  - Virtually-addressed 4-way Associative Cache
  - Eight words per line
  - Write-through and Write-back Operation
  - Pseudo-random or Round-robin Replacement
- Write Buffer
  - Main Write Buffer with 16-word Data Buffer and 4-address Buffer
  - DCache Write-back Buffer with 8-word Entries and a Single Address Entry
  - Software Control Drain
- Standard ARM v4 and v5 Memory Management Unit (MMU)
  - Access Permission for Sections
  - Access Permission for large pages and small pages can be specified separately for each quarter of the page
  - 16 embedded domains
- Bus Interface Unit (BIU)
  - Arbitrates and Schedules AHB Requests
  - Separate Masters for both instruction and data access providing complete Matrix system flexibility
  - Separate Address and Data Buses for both the 32-bit instruction interface and the 32-bit data interface
  - On Address and Data Buses, data can be 8-bit (Bytes), 16-bit (Half-words) or 32-bit (Words)
- TCM Interface

6.2 Bus Matrix

- 12-layer Matrix, handling requests from 11 masters
- Programmable Arbitration strategy
  - Fixed-priority Arbitration
  - Round-Robin Arbitration, either with no default master, last accessed default master or fixed default master
- Burst Management
  - Breaking with Slot Cycle Limit Support
  - Undefined Burst Length Support
- One Address Decoder provided per Master
  - Three different slaves may be assigned to each decoded memory area: one for internal ROM boot, one for internal flash boot, one after remap
- Boot Mode Select
  - Non-volatile Boot Memory can be internal ROM or external memory on EBI_NCS0
  - Selection is made by General purpose NVM bit sampled at reset
- Remap Command
  - Allows Remapping of an Internal SRAM in Place of the Boot Non-Volatile Memory (ROM or External Flash)
  - Allows Handling of Dynamic Exception Vectors

6.2.1 Matrix Masters

The Bus Matrix of the SAM9G45 manages Masters, thus each master can perform an access concurrently with others, depending on whether the slave it accesses is available.

Each Master has its own decoder, which can be defined specifically for each master. In order to simplify the addressing, all the masters have the same decodings.

Table 6-1. List of Bus Matrix Masters

Master 0	ARM926™ Instruction
Master 1	ARM926 Data
Master 2	Peripheral DMA Controller (PDC)
Master 3	USB HOST OHCI
Master 4	DMA
Master 5	DMA
Master 6	ISI Controller DMA
Master 7	LCD DMA
Master 8	Ethernet MAC DMA
Master 9	USB Device High Speed DMA
Master 10	USB Host High Speed EHCI DMA

6.2.2 Matrix Slaves

Each Slave has its own arbiter, thus allowing a different arbitration per Slave to be programmed.

Table 6-2. List of Bus Matrix Slaves

Slave 0	Internal SRAM
Slave 1	Internal ROM
	USB OHCI
	USB EHCI
	UDP High Speed RAM
	LCD User Interface
Slave 2	DDR Port 0
Slave 3	DDR Port 1
Slave 4	DDR Port 2
Slave 5	DDR Port 3
Slave 6	External Bus Interface
Slave 7	Internal Peripherals

6.2.3 Masters to Slaves Access

All the Masters can normally access all the Slaves. However, some paths do not make sense, such as allowing access from the Ethernet MAC to the internal peripherals. Thus, these paths are forbidden or simply not wired, and shown “-” in the following tables.

The four DDR ports are connected differently according to the application device.

The user can disable the DDR multi-port in the DDR multi-port Register (bit DDRMP_DIS) in the Chip Configuration User Interface.

- When the DDR multi-port is enabled (DDRMP_DIS=0), the ARM instruction and data are respectively connected to DDR Port 0 and DDR Port 1. The other masters share DDR Port 2 and DDR Port 3.
- When the DDR multi-port is disabled (DDRMP_DIS=1), DDR Port 1 is dedicated to the LCD controller. The remaining masters share DDR Port 2 and DDR Port 3.

Figure 6-1. DDR Multi-port

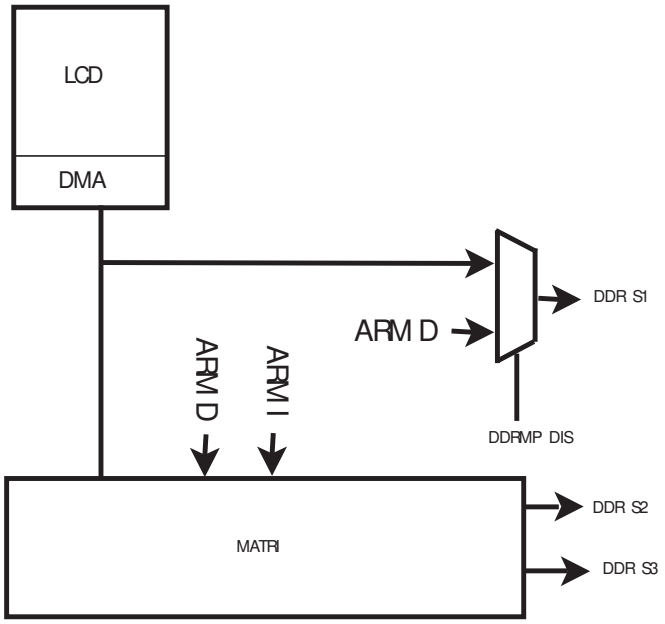


Table 6-3. SAM9G45 Masters to Slaves Access DDRMP_DIS = 0

Master		0	1	2	3	4 & 5	6	7	8	9	10	11
Slave		ARM 926 Instr.	ARM 926 Data	PDC	USB Host OHCI	DMA	ISI DMA	LCD DMA	Ethernet MAC	USB Device HS	USB Host EHCI	Reserved
0	Internal SRAM 0	X	X	X	X	X	X	-	X	X	X	-
1	Internal ROM	X	X	X	-	-	-	-	-	X	-	-
	UHP OHCI	X	X	-	-	-	-	-	-	-	-	-
	UHP EHCI	X	X	-	-	-	-	-	-	-	-	-
	LCD User Int.	X	X	-	-	-	-	-	-	-	-	-
	UDPHS RAM	X	X	-	-	-	-	-	-	-	-	-
	Reserved	X	X	-	-	-	-	-	-	-	-	-
2	DDR Port 0	X	-	-	-	-	-	-	-	-	-	-
3	DDR Port 1	-	X	-	-	-	-	-	-	-	-	-
4	DDR Port 2	-	-	X	X	X	X	-	X	X	X	X
5	DDR Port 3	-	-	X	X	X	X	X	X	X	X	-
6	EBI	X	X	X	X	X	X	X	X	X	X	X
7	Internal Periph.	X	X	X	-	X	-	-	-	-	-	-

Table 6-4. SAM9G45 Masters to Slaves Access with DDRMP_DIS = 1 (default)

Master		0	1	2	3	4 & 5	6	7	8	9	10	11
Slave		ARM 926 Instr.	ARM 926 Data	PDC	USB HOST OHCI	DMA	ISI DMA	LCD DMA	Ethernet MAC	USB Device HS	USB Host EHCI	Reserved
0	Internal SRAM 0	X	X	X	X	X	X	-	X	X	X	-
1	Internal ROM	X	X	X	-	-	-	-	-	X	-	-
	UHP OHCI	X	X	-	-	-	-	-	-	-	-	-
	UHP EHCI	X	X	-	-	-	-	-	-	-	-	-
	LCD User Int.	X	X	-	-	-	-	-	-	-	-	-
	UDPHS RAM	X	X	-	-	-	-	-	-	-	-	-
	Reserved	X	X	-	-	-	-	-	-	-	-	-
2	DDR Port 0	-	-	-	-	-	-	-	-	-	-	X
3	DDR Port 1	-	-	-	-	-	-	X	-	-	-	-
4	DDR Port 2	X	-	X	X	X	X	-	X	X	X	-
5	DDR Port 3	-	X	X	X	X	X	-	X	X	X	-
6	EBI	X	X	X	X	X	X	X	X	X	X	X
7	Internal Periph.	X	X	X	-	X	-	-	-	-	-	-

Table 6-5 summarizes the Slave Memory Mapping for each connected Master, depending on the Remap status (RCBx bit in Bus Matrix Master Remap Control Register MATRIX_MRCR) and the BMS state at reset.

Table 6-5. Internal Memory Mapping

	Master		
Slave Base Address	RCBx = 0		RCBx = 1
	BMS = 1	BMS = 0	
0x0000 0000	Internal ROM	EBI NCS0	Internal SRAM

6.3 Peripheral DMA Controller (PDC)

- Acting as one AHB Bus Matrix Master
- Allows data transfers from/to peripheral to/from any memory space without any intervention of the processor.
- Next Pointer support, prevents strong real-time constraints on buffer management.

The Peripheral DMA Controller handles transfer requests from the channel according to the following priorities (Low to High priorities):

Table 6-6. Peripheral DMA Controller

Instance name	Channel T/R
DBGU	Transmit
USART3	Transmit
USART2	Transmit
USART1	Transmit
USART0	Transmit
AC97C	Transmit
SPI1	Transmit
SPI0	Transmit
SSC1	Transmit
SSC0	Transmit
TSADCC	Receive
DBGU	Receive
USART3	Receive
USART2	Receive
USART1	Receive
USART0	Receive
AC97C	Receive
SPI1	Receive
SPI0	Receive
SSC1	Receive
SSC0	Receive

6.4 USB

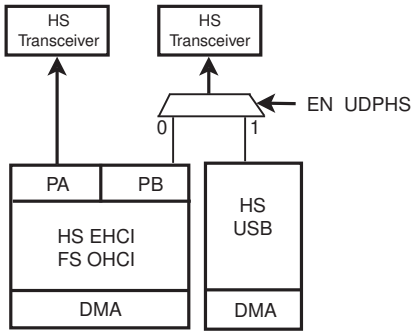
The SAM9G45 features USB communication ports as follows:

- 2 Ports USB Host full speed OHCI and High speed EHCI
- 1 Device High speed

USB Host Port A is directly connected to the first UTMI transceiver.

The Host Port B is multiplexed with the USB device High speed and connected to the second UTMI port. The selection between Host Port B and USB device high speed is controlled by a the bit UDPHS enable bit located in the UDPHS_CTRL control register.

Figure 6-2. USB Selection



6.5 DMA Controller

- Two Masters
- Embeds 8 channels
- 64 bytes/FIFO for Channel Buffering
- Linked List support with Status Write Back operation at End of Transfer
- Word, HalfWord, Byte transfer support.
- memory to memory transfer
- Peripheral to memory
- Memory to peripheral

The DMA controller can handle the transfer between peripherals and memory and so receives the triggers from the peripherals below. The hardware interface numbers are also given below in Table 6-7.

Table 6-7. DMA Channel Definition

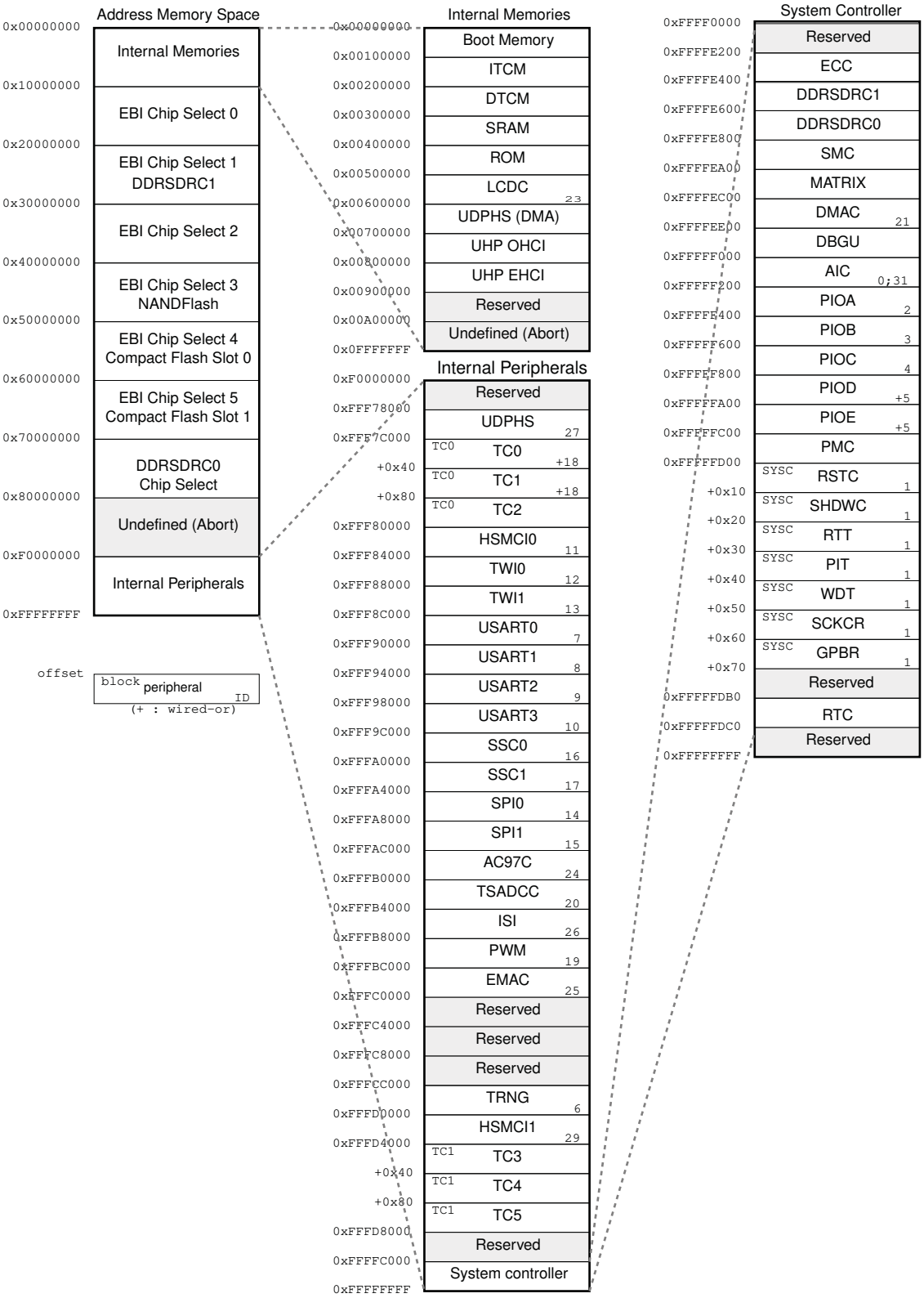
Instance Name	T/R	DMA Channel HW interface Number
MCI0	TX/RX	0
SPI0	TX	1
SPI0	RX	2
SPI1	TX	3
SPI1	RX	4
SSC0	TX	5
SSC0	RX	6
SSC1	TX	7
SSC1	RX	8
AC97C	TX	9
AC97C	RX	10
MCI1	TX/RX	13

6.6 Debug and Test Features

- ARM926 Real-time In-circuit Emulator
  - Two real-time Watchpoint Units
  - Two Independent Registers: Debug Control Register and Debug Status Register
  - Test Access Port Accessible through JTAG Protocol
  - Debug Communications Channel
- Debug Unit
  - Two-pin UART
  - Debug Communication Channel Interrupt Handling
  - Chip ID Register
- IEEE1149.1 JTAG Boundary-scan on All Digital Pins.

7. Memories

Figure 7-1. SAM9G45 Memory Mapping



7.1 Memory Mapping

A first level of address decoding is performed by the AHB Bus Matrix, i.e., the implementation of the Advanced High performance Bus (AHB) for its Master and Slave interfaces with additional features.

Decoding breaks up the 4 Gbytes of address space into 16 banks of 256 Mbytes. The banks 1 to 6 are directed to the EBI that associates these banks to the external chip selects NCS0 to NCS5.

The bank 7 is directed to the DDRSDRC0 that associates this bank to DDR_NCS chip select and so dedicated to the 4-port DDR2/LPDDR controller.

The bank 0 is reserved for the addressing of the internal memories, and a second level of decoding provides 1 Mbyte of internal memory area. The bank 15 is reserved for the peripherals and provides access to the Advanced Peripheral Bus (APB).

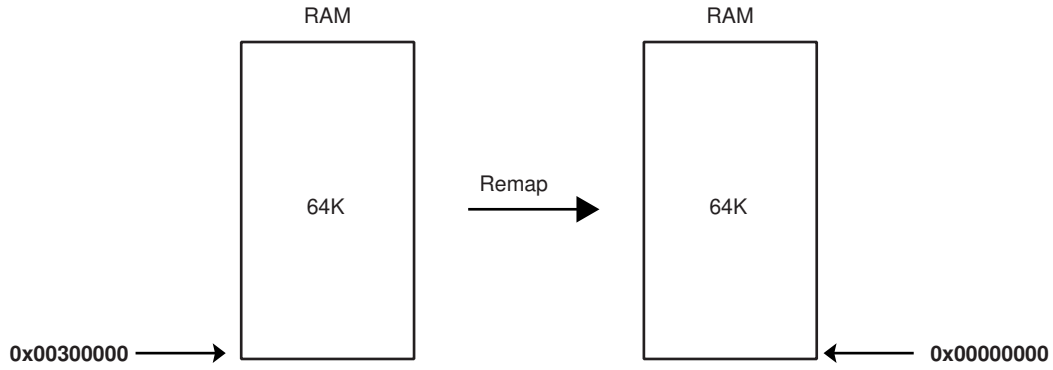
Other areas are unused and performing an access within them provides an abort to the master requesting such an access.

7.2 Embedded Memories

7.2.1 Internal SRAM

The SAM9G45 product embeds a total of 64 Kbytes high-speed SRAM split in 4 blocks of 16 KBytes connected to one slave of the matrix. After reset and until the Remap Command is performed, the four SRAM blocks are contiguous and only accessible at address 0x00300000. After Remap, the SRAM also becomes available at address 0x0.

Figure 7-2. Internal SRAM Reset



The SAM9G45 device embeds two memory features. The processor Tightly Coupled Memory Interface (TCM) that allows the processor to access the memory up to processor speed (PCK) and the interface on the AHB side allowing masters to access the memory at AHB speed (MCK).

A wait state is necessary to access the TCM at 400 MHz. Setting the bit NWS_TCM in the bus Matrix TCM Configuration Register of the matrix inserts a wait state on the ITCM and DTCM accesses.

7.2.2 TCM Interface

On the processor side, this Internal SRAM can be allocated to two areas.

- Internal SRAM A is the ARM926EJ-S Instruction TCM. The user can map this SRAM block anywhere in the ARM926 instruction memory space using CP15 instructions and the TCR configuration register located in the Chip Configuration User Interface. This SRAM block is also accessible by the ARM926 Masters and by the AHB Masters through the AHB bus

- Internal SRAM B is the ARM926EJ-S Data TCM. The user can map this SRAM block anywhere in the ARM926 data memory space using CP15 instructions. This SRAM block is also accessible by the ARM926 Data Master and by the AHB Masters through the AHB bus.
- Internal SRAM C is only accessible by all the AHB Masters. After reset and until the Remap Command is performed, this SRAM block is accessible through the AHB bus at address 0x0030 0000 by all the AHB Masters. After Remap, this SRAM block also becomes accessible through the AHB bus at address 0x0 by the ARM926 Instruction and the ARM926 Data Masters.

Within the 64 Kbyte SRAM size available, the amount of memory assigned to each block is software programmable according to Table 7-1.

Table 7-1. ITCM and DTCM Memory Configuration

SRAM A ITCM size (KBytes) seen at 0x100000 through AHB	SRAM B DTCM size (KBytes) seen at 0x200000 through AHB	SRAM C (KBytes) seen at 0x300000 through AHB
0	0	64
0	64	0
32	32	0

7.2.3 Internal ROM

The SAM9G45 embeds an Internal ROM, which contains the Boot ROM and SAM-BA program.

At any time, the ROM is mapped at address 0x0040 0000. It is also accessible at address 0x0 (BMS =1) after the reset and before the Remap Command.

7.2.4 Boot Strategies

The system always boots at address 0x0. To ensure maximum boot possibilities the memory layout can be changed with two parameters.

REMAP allows the user to layout the internal SRAM bank to 0x0 to ease the development. This is done by software once the system has boot.

BMS allows the user to lay out to 0x0, when convenient, the ROM or an external memory. This is done by a hardware way at reset.

Note: All the memory blocks can always be seen at their specified base addresses that are not concerned by these parameters.

The SAM9G45 Bus Matrix manages a boot memory that depends on the level on the pin BMS at reset. The internal memory area mapped between address 0x0 and 0x000F FFFF is reserved to this effect.

If BMS is detected at 1, the boot memory is the embedded ROM.

If BMS is detected at 0, the boot memory is the memory connected on the Chip Select 0 of the External Bus Interface.

7.2.4.1 BMS = 1, boot on embedded ROM

The system boots on Boot Program.

- Boot on on-chip RC
- Enable the 32768 Hz oscillator
- Auto baudrate detection
- Downloads and runs an application from external storage media into internal SRAM
- Downloaded code size depends on embedded SRAM size
- Automatic detection of valid application