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SAM9M10

Atmel | SMART ARM-based Embedded MPU

DATASHEET

Description

The Atmel® | SMART SAM9M10 is a multimedia-enabled mid-range ARM926-based embedded MPU running at 400 MHz, combining user interfaces, video playback and connectivity. It includes hardware video decoder, LCD Controller, resistive touchscreen, camera interface, audio, Ethernet 10/100 and high speed USB and SDIO.

The hardware video decoder supports the standards H.264, MPEG-4, MPEG-2, VC-1, and H.263. The SAM9M10 also provides hardware image post-processing, such as image scaling, color conversion and image rotation.

The SAM9M10 supports DDR2 and NAND Flash memory interfaces for program and data storage. An internal 133 MHz multi-layer bus architecture associated with 37 DMA channels, a dual external bus interface and distributed memory including a 64-Kbyte SRAM which can be configured as a tightly coupled memory (TCM) sustains the high bandwidth required by the processor and the high speed peripherals.

A True Random Number Generator is embedded for key generation and exchange protocols.

The I/Os support 1.8V or 3.3V operation, which are independently configurable for the memory interface and peripheral I/Os. This feature completely eliminates the need for any external level shifters. In addition it supports a 0.8 mm ball pitch package for low cost PCB manufacturing.

The SAM9M10 devices have three software-selectable low-power modes: Idle, Ultra Low-power and Backup. In Idle mode, the processor is stopped while all other functions can be kept running at normal operating bus frequency. In Ultra Low-power mode, the processor is stopped while all other functions can be kept running at minimum operating bus frequency. In Backup mode, only the real-time clock, real-time timer, 128-bit general purpose backup registers, and wake-up logic are running.

The SAM9M10 power management controller features efficient clock gating and a battery backup section minimizing power consumption in active and standby modes.

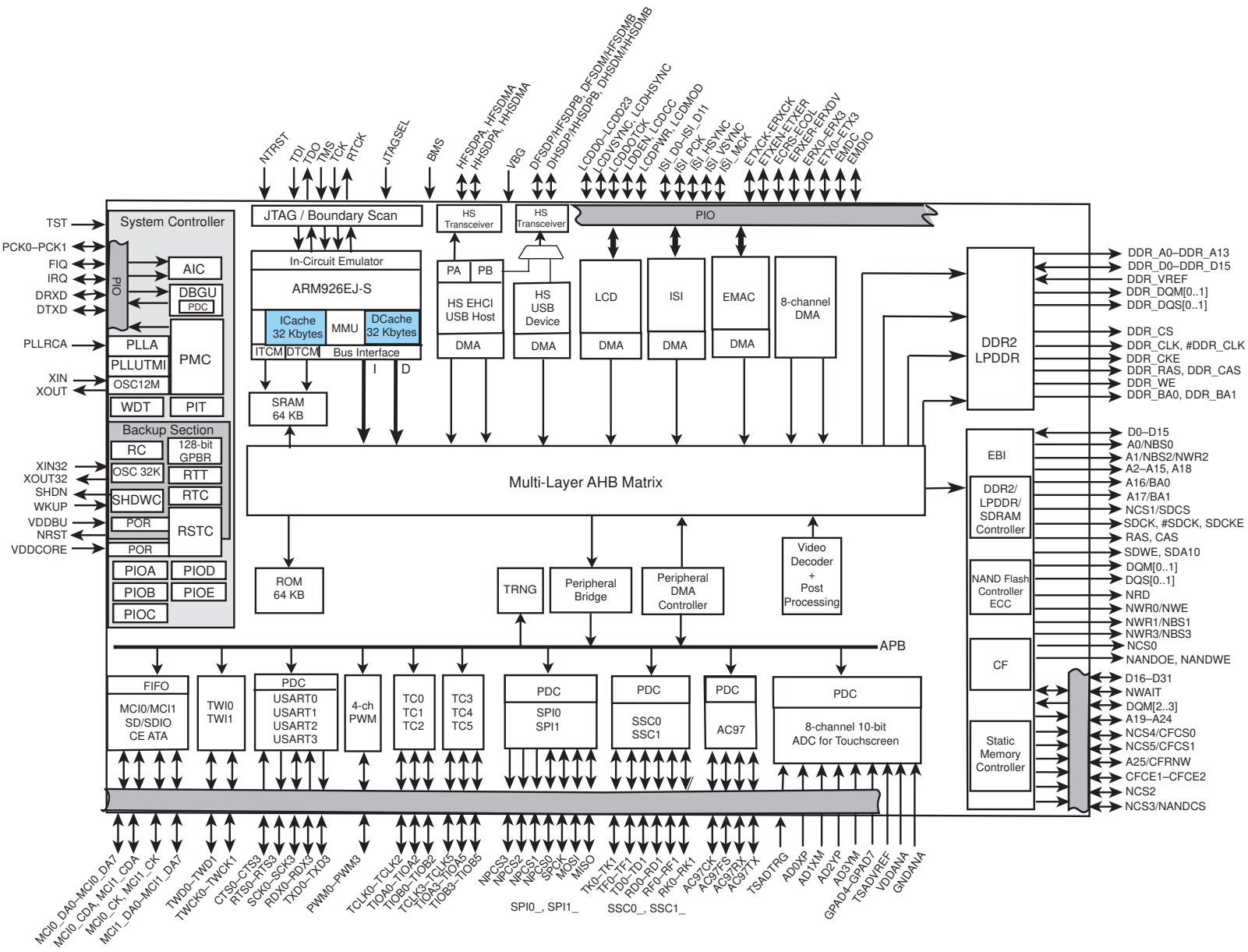
The SAM9M10 device is particularly well suited for media-rich displays and control panels in home and commercial buildings, POS terminals, entertainment systems, internet appliances and medical.

Features

- 400 MHz ARM926EJ-S™ ARM® Thumb® Processor
  - 32 Kbytes Data Cache, 32 Kbytes Instruction Cache, MMU
- Memories
  - 4-port, 4-bank DDR2/LPDDR Controller
  - External Bus Interface supporting 4-bank DDR2/LPDDR, SDR/LPSDR, Static Memories, CompactFlash®, SLC NAND Flash with ECC
  - 64 Kbyte internal SRAM, single-cycle access at system speed or processor speed through TCM interface
  - 64 Kbyte internal ROM, embedding bootstrap routine
- System
  - 133 MHz twelve 32-bit layer AHB Bus Matrix
  - 37 DMA Channels
  - Boot from NAND Flash, SDCard, DataFlash or serial DataFlash
  - Reset Controller (RSTC) with on-chip Power-on Reset
  - Selectable 32768 Hz Low-power and 12 MHz Crystal Oscillators
  - Internal Low-power 32 kHz RC Oscillator
  - One PLL for the system and one 480 MHz PLL optimized for USB High Speed
  - Two Programmable External Clock Signals
  - Advanced Interrupt Controller (AIC)
  - Periodic Interval Timer (PIT), Watchdog Timer (WDT), Real-time Timer (RTT) and Real-time Clock (RTC)
- Three Low-power Modes: Idle, Ultra Low-power, and Backup
- Peripherals
  - Universal Video Decoder (VDEC) – decoding at up to 30 fps at D1 (720 x 576 pixels) or WVGA (800 x 480) resolution
  - LCD Controller (LCDC) supporting STN and TFT displays up to 1280*860
  - ITU-R BT. 601/656 Image Sensor Interface (ISI)
  - Dual High Speed USB Host and a High Speed USB Device with On-Chip Transceivers
  - 10/100 Mbps Ethernet MAC Controller (EMAC)
  - Two High Speed Memory Card Hosts (SDIO, SDCard, MMC and CE-ATA)
  - AC'97 Controller (AC97C)
  - Two Master/Slave Serial Peripheral Interfaces (SPI)
  - 2 Three-channel 16-bit Timer Counters (TC)
  - Two Synchronous Serial Controllers (I2S mode)
  - Four-channel 16-bit PWM Controller
  - 2 Two-wire Interfaces (TWI)
  - Four USARTs with ISO7816, IrDA, Manchester and SPI modes, one DBGU
  - 8-channel 10-bit ADC controller with 4-wire Touchscreen support (TSADCC)
- Cryptography
  - True Random Number Generator (TRNG)
- I/O
  - Five 32-bit Parallel Input/Output Controllers
  - 160 Programmable I/O Lines Multiplexed with up to Two Peripheral I/Os with Schmitt trigger input
- Package
  - 324-ball TFBGA – 15 x 15 x 1.2 mm, 0.8 mm pitch

1. Block Diagram

Figure 1-1. SAM9M10 Block Diagram



2. Signal Description

Table 2-1 gives details on the signal names classified by peripheral.

Table 2-1. Signal Description List

Signal Name	Function	Type	Active Level	Reference Voltage	Comments
Power Supplies					
VDDIOM0	DDR2 I/O Lines Power Supply	Power	–	–	1.65V to 1.95V
VDDIOM1	EBI I/O Lines Power Supply	Power	–	–	1.65V to 1.95V or 3.0V to 3.6V
VDDIOP0	Peripherals I/O Lines Power Supply	Power	–	–	1.65V to 3.6V
VDDIOP1	Peripherals I/O Lines Power Supply	Power	–	–	1.65V to 3.6V
VDDIOP2	ISI I/O Lines Power Supply	Power	–	–	1.65V to 3.6V
VDDBU	Backup I/O Lines Power Supply	Power	–	–	1.8V to 3.6V
VDDANA	Analog Power Supply	Power	–	–	3.0V to 3.6V
VDDPLLA	PLLA Power Supply	Power	–	–	0.9V to 1.1V
VDDPLLUTMI	PLLUTMI Power Supply	Power	–	–	0.9V to 1.1V
VDDOSC	Oscillator Power Supply	Power	–	–	1.65V to 3.6V
VDDCORE	Core Chip Power Supply	Power	–	–	0.9V to 1.1V
VDDUTMIC	UDPHS and UHPHS UTMI+ Core Power Supply	Power	–	–	0.9V to 1.1V
VDDUTMII	UDPHS and UHPHS UTMI+ Interface Power Supply	Power	–	–	3.0V to 3.6V
GNDIOM	DDR2 and EBI I/O Lines Ground	Ground	–	–	–
GNDIOP	Peripherals and ISI I/O Lines Ground	Ground	–	–	–
GNDCORE	Core Chip Ground	Ground	–	–	–
GNDOSC	PLLA, PLLUTMI and Oscillator Ground	Ground	–	–	–
GNDBU	Backup Ground	Ground	–	–	–
GNDUTMI	UDPHS and UHPHS UTMI+ Core and Interface Ground	Ground	–	–	–
GNDANA	Analog Ground	Ground	–	–	–
Clocks, Oscillators and PLLs					
XIN	Main Oscillator Input	Input	–	–	–
XOUT	Main Oscillator Output	Output	–	–	–
XIN32	Slow Clock Oscillator Input	Input	–	–	–
XOUT32	Slow Clock Oscillator Output	Output	–	–	–
VBG	Bias Voltage Reference for USB	Analog	–	–	–
PCK0–PCK1	Programmable Clock Output	Output	–	(1)	–

Table 2-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Reference Voltage	Comments
Shutdown, Wakeup Logic					
SHDN	Shutdown Control	Output	–	VDDBU	Driven at 0V only. 0: The device is in backup mode 1: The device is running (not in backup mode).
WKUP	Wake-Up Input	Input	–	VDDBU	Accepts between 0V and VDDBU
ICE and JTAG					
TCK	Test Clock	Input	–	VDDIOP0	No pull-up resistor, Schmitt trigger
TDI	Test Data In	Input	–	VDDIOP0	No pull-up resistor, Schmitt trigger
TDO	Test Data Out	Output	–	VDDIOP0	
TMS	Test Mode Select	Input	–	VDDIOP0	No pull-up resistor, Schmitt trigger
JTAGSEL	JTAG Selection	Input	–	VDDBU	Pull-down resistor (15 kΩ)
RTCK	Return Test Clock	Output	–	VDDIOP0	
Reset/Test					
NRST	Microcontroller Reset [2]	I/O	Low	VDDIOP0	Open drain output Pull-up resistor (100 kΩ), Schmitt trigger
TST	Test Mode Select	Input	–	VDDBU	Pull-down resistor (15 kΩ), Schmitt trigger
NTRST	Test Reset Signal	Input	–	VDDIOP0	Pull-up resistor (100 kΩ), Schmitt trigger
BMS	Boot Mode Select	Input	–	VDDIOP0	Must be connected to GND or VDDIOP0
Debug Unit - DBGU					
DRXD	Debug Receive Data	Input	–	[1]	–
DTXD	Debug Transmit Data	Output	–	[1]	–
Advanced Interrupt Controller - AIC					
IRQ	External Interrupt Input	Input	–	[1]	–
FIQ	Fast Interrupt Input	Input	–	[1]	–
PIO Controller - PIOA / PIOB / PIOC / PIOD / PIOE					
PA0–PA31	Parallel IO Controller A	I/O	–	[1]	Pulled-up input at reset (100 kΩ)[3], Schmitt trigger
PB0–PB31	Parallel IO Controller B	I/O	–	[1]	
PC0–PC31	Parallel IO Controller C	I/O	–	[1]	
PD0–PD31	Parallel IO Controller D	I/O	–	[1]	
PE0–PE31	Parallel IO Controller E	I/O	–	[1]	

Table 2-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Reference Voltage	Comments
DDR Memory Interface - DDR2/LPDDR Controller - DDRSDRC0					
DDR_D0–DDR_D15	Data Bus	I/O	–	VDDIOM0	Pulled-up input at reset
DDR_A0–DDR_A13	Address Bus	Output	–	VDDIOM0	0 at reset
DDR_CLK-#DDR_CLK	DDR differential clock input	Output	–	VDDIOM0	–
DDR_CKE	DDR Clock Enable	Output	High	VDDIOM0	–
DDR_CS	DDR Chip Select	Output	Low	VDDIOM0	–
DDR_WE	DDR Write Enable	Output	Low	VDDIOM0	–
DDR_RAS-DDR_CAS	Row and Column Signal	Output	Low	VDDIOM0	–
DDR_DQM[0..1]	Write Data Mask	Output	–	VDDIOM0	–
DDR_DQS[0..1]	Data Strobe	Output	–	VDDIOM0	–
DDR_BA0–DDR_BA1	Bank Select	Output	–	VDDIOM0	–
DDR_VREF	Reference Voltage	Input	–	VDDIOM0	–
External Bus Interface - EBI					
D0 -D31	Data Bus	I/O	–	VDDIOM1	Pulled-up input at reset
A0–A25	Address Bus	Output	–	VDDIOM1	0 at reset
NWAIT	External Wait Signal	Input	Low	VDDIOM1	–
Static Memory Controller - SMC					
NCS0–NCS5	Chip Select Lines	Output	Low	VDDIOM1	–
NWR0–NWR3	Write Signal	Output	Low	VDDIOM1	–
NRD	Read Signal	Output	Low	VDDIOM1	–
NWE	Write Enable	Output	Low	VDDIOM1	–
NBS0–NBS3	Byte Mask Signal	Output	Low	VDDIOM1	–
CompactFlash Support					
CFCE1–CFCE2	CompactFlash Chip Enable	Output	Low	VDDIOM1	–
CFOE	CompactFlash Output Enable	Output	Low	VDDIOM1	–
CFWE	CompactFlash Write Enable	Output	Low	VDDIOM1	–
CFIOR	CompactFlash IO Read	Output	Low	VDDIOM1	–
CFIOW	CompactFlash IO Write	Output	Low	VDDIOM1	–
CFRNW	CompactFlash Read Not Write	Output	–	VDDIOM1	–
CFCS0–CFCS1	CompactFlash Chip Select Lines	Output	Low	VDDIOM1	–
NAND Flash Support					
NANDCS	NAND Flash Chip Select	Output	Low	VDDIOM1	–
NANDOE	NAND Flash Output Enable	Output	Low	VDDIOM1	–
NANDWE	NAND Flash Write Enable	Output	Low	VDDIOM1	–

Table 2-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Reference Voltage	Comments
EBI - DDR2/SDRAM/LPDDR Controller - DDRSDRC1					
SDCK, #SDCK	DDR2/SDRAM differential clock	Output	–	VDDIOM1	–
SDCKE	DDR2/SDRAM Clock Enable	Output	High	VDDIOM1	–
SDCS	DDR2/SDRAM Controller Chip Select	Output	Low	VDDIOM1	–
BA0–BA1	Bank Select	Output	–	VDDIOM1	–
SDWE	DDR2/SDRAM Write Enable	Output	Low	VDDIOM1	–
RAS - CAS	Row and Column Signal	Output	Low	VDDIOM1	–
SDA10	SDRAM Address 10 Line	Output	–	VDDIOM1	–
DQS[0..1]	Data Strobe	Output	–	VDDIOM1	–
DQM[0..3]	Write Data Mask	Output	–	VDDIOM1	–
High Speed Multimedia Card Interface - HSMCIx					
MCIx_CK	Multimedia Card Clock	I/O	–	(1)	–
MCIx_CDA	Multimedia Card Slot A Command	I/O	–	(1)	–
MCIx_DA0–MCIx_DA7	Multimedia Card Slot A Data	I/O	–	(1)	–
Universal Synchronous Asynchronous Receiver Transmitter - USARTx					
SCKx	USARTx Serial Clock	I/O	–	(1)	–
TXDx	USARTx Transmit Data	Output	–	(1)	–
RXDx	USARTx Receive Data	Input	–	(1)	–
RTSx	USARTx Request To Send	Output	–	(1)	–
CTSx	USARTx Clear To Send	Input	–	(1)	–
Synchronous Serial Controller - SSCx					
TDx	SSC Transmit Data	Output	–	(1)	–
RDx	SSC Receive Data	Input	–	(1)	–
TKx	SSC Transmit Clock	I/O	–	(1)	–
RKx	SSC Receive Clock	I/O	–	(1)	–
TFx	SSC Transmit Frame Sync	I/O	–	(1)	–
RFx	SSC Receive Frame Sync	I/O	–	(1)	–
AC97 Controller - AC97C					
AC97RX	AC97 Receive Signal	Input	–	(1)	–
AC97TX	AC97 Transmit Signal	Output	–	(1)	–
AC97FS	AC97 Frame Synchronization Signal	Output	–	(1)	–
AC97CK	AC97 Clock signal	Input	–	(1)	–
Time Counter - TCx					
TCLKx	TC Channel x External Clock Input	Input	–	(1)	–
TIOAx	TC Channel x I/O Line A	I/O	–	(1)	–
TIOBx	TC Channel x I/O Line B	I/O	–	(1)	–

Table 2-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Reference Voltage	Comments
Pulse Width Modulation Controller - PWM					
PWMx	Pulse Width Modulation Output	Output	–	(1)	–
Serial Peripheral Interface - SPIx_					
SPIx_MISO	Master In Slave Out	I/O	–	(1)	–
SPIx_MOSI	Master Out Slave In	I/O	–	(1)	–
SPIx_SPCK	SPI Serial Clock	I/O	–	(1)	–
SPIx_NPCS0	SPI Peripheral Chip Select 0	I/O	Low	(1)	–
SPIx_NPCS1–SPIx_NPCS3	SPI Peripheral Chip Select	Output	Low	(1)	–
Two-Wire Interface - TWI					
TWDx	Two-wire Serial Data	I/O	–	(1)	–
TWCKx	Two-wire Serial Clock	I/O	–	(1)	–
USB Host High Speed Port - UHPHS					
HFSDPA	USB Host Port A Full Speed Data +	Analog	–	VDDUTMII	–
HFSDMA	USB Host Port A Full Speed Data -	Analog	–	VDDUTMII	–
HHSDPA	USB Host Port A High Speed Data +	Analog	–	VDDUTMII	–
HHSDMA	USB Host Port A High Speed Data -	Analog	–	VDDUTMII	–
HFSDPB	USB Host Port B Full Speed Data +	Analog	–	VDDUTMII	Multiplexed with DFSDP
HFSDMB	USB Host Port B Full Speed Data -	Analog	–	VDDUTMII	Multiplexed with DFSDM
HHSDPB	USB Host Port B High Speed Data +	Analog	–	VDDUTMII	Multiplexed with DHSDP
HHSDMB	USB Host Port B High Speed Data -	Analog	–	VDDUTMII	Multiplexed with DHSDM
USB Device High Speed Port - UDPHS					
DFSDM	USB Device Full Speed Data -	Analog	–	VDDUTMII	–
DFSDP	USB Device Full Speed Data +	Analog	–	VDDUTMII	–
DHSDM	USB Device High Speed Data -	Analog	–	VDDUTMII	–
DHSDP	USB Device High Speed Data +	Analog	–	VDDUTMII	–

Table 2-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Reference Voltage	Comments
Ethernet 10/100 - EMAC					
ETXCK	Transmit Clock or Reference Clock	Input	–	(1)	MII only, REFCK in RMII
ERXCK	Receive Clock	Input	–	(1)	MII only
ETXEN	Transmit Enable	Output	–	(1)	–
ETX0–ETX3	Transmit Data	Output	–	(1)	ETX0–ETX1 only in RMII
ETXER	Transmit Coding Error	Output	–	(1)	MII only
ERXDV	Receive Data Valid	Input	–	(1)	RXDV in MII, CRSDV in RMII
ERX0–ERX3	Receive Data	Input	–	(1)	ERX0–ERX1 only in RMII
ERXER	Receive Error	Input	–	(1)	–
ECRS	Carrier Sense and Data Valid	Input	–	(1)	MII only
ECOL	Collision Detect	Input	–	(1)	MII only
EMDC	Management Data Clock	Output	–	(1)	–
EMDIO	Management Data Input/Output	I/O	–	(1)	–
Image Sensor Interface - ISI					
ISI_D0–ISI_D11	Image Sensor Data	Input	–	VDDIOP2	–
ISI_MCK	Image sensor Reference clock	output	–	VDDIOP2	–
ISI_HSYNC	Image Sensor Horizontal Synchro	input	–	VDDIOP2	–
ISI_VSYNC	Image Sensor Vertical Synchro	input	–	VDDIOP2	–
ISI_PCK	Image Sensor Data clock	input	–	VDDIOP2	–
LCD Controller - LCDC					
LCDD0–LCDD23	LCD Data Bus	Output	–	VDDIOP1	–
LCDVSYNC	LCD Vertical Synchronization	Output	–	VDDIOP1	–
LCDHSYNC	LCD Horizontal Synchronization	Output	–	VDDIOP1	–
LCDDOTCK	LCD Dot Clock	Output	–	VDDIOP1	–
LCDDEN	LCD Data Enable	Output	–	VDDIOP1	–
LCDCC	LCD Contrast Control	Output	–	VDDIOP1	–
LCDPWR	LCD panel Power enable control	Output	–	VDDIOP1	–
LCDMOD	LCD Modulation signal	Output	–	VDDIOP1	–

Table 2-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Reference Voltage	Comments
Touchscreen Analog-to-Digital Converter Controller - TSADCC					
$AD0X_P$	Analog input channel 0 or Touch Screen Top channel	Analog	–	VDDANA	Multiplexed with AD0
$AD1X_M$	Analog input channel 1 or Touch Screen Bottom channel	Analog	–	VDDANA	Multiplexed with AD1
$AD2Y_P$	Analog input channel 2 or Touch Screen Right channel	Analog	–	VDDANA	Multiplexed with AD2
$AD3Y_M$	Analog input channel 3 or Touch Screen Left channel	Analog	–	VDDANA	Multiplexed with AD3
GPAD4–GPAD7	Analog Inputs	Analog	–	VDDANA	–
TSADTRG	ADC Trigger	Input	–	VDDANA	–
TSADVREF	ADC Reference	Analog	–	VDDANA	–

Notes:
1. Refer to peripheral multiplexing tables in Section 7.4 “Peripheral Signals Multiplexing on I/O Lines” for these signals.
2. When configured as an input, the NRST pin enables asynchronous reset of the device when asserted low. This allows connection of a simple push button on the NRST pin as a system-user reset.
3. Programming of this pull-up resistor is performed independently for each I/O line through the PIO Controllers. After reset, all the I/O lines default as inputs with pull-up resistors enabled, except those which are multiplexed with the External Bus Interface signals that require to be enabled as Peripheral at reset. This is explicitly indicated in the column “Reset State” of the peripheral multiplexing tables.

3. Package and Pinout

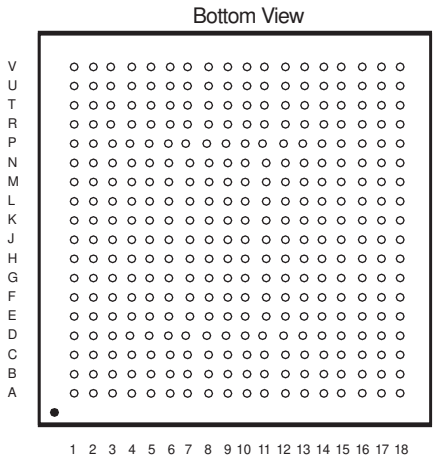
The SAM9M10 is delivered in a 324-ball TFBGA Green-compliant package.

3.1 Mechanical Overview of the 324-ball TFBGA Package

Figure 3-1 shows the orientation of the 324-ball TFBGA package.

A detailed mechanical description is given in Section 47. “Mechanical Characteristics”.

Figure 3-1. Orientation of the 324-ball TFBGA Package



3.2 324-ball TFBGA Package Pinout

Table 3-1. SAM9M10 Pinout for 324-ball TFBGA Package

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	PC27	E10	NANDWE	K1	PE21	P10	TMS
A2	PC28	E11	DQS1	K2	PE23	P11	VDDPLLA
A3	PC25	E12	D13	K3	PE26	P12	PB20
A4	PC20	E13	D11	K4	PE22	P13	PB31
A5	PC12	E14	A4	K5	PE24	P14	DDR_D7
A6	PC7	E15	A8	K6	PE25	P15	DDR_D3
A7	PC5	E16	A9	K7	PE27	P16	DDR_D4
A8	PC0	E17	A7	K8	PE28	P17	DDR_D5
A9	NWR3/NBS3	E18	VDDCORE	K9	VDDIOP0	P18	DDR_D10
A10	NCS0	F1	PD22	K10	VDDIOP0	R1	PA18
A11	DQS0	F2	PD24	K11	GNDIOM	R2	PA20
A12	RAS	F3	SHDN	K12	GNDIOM	R3	PA24
A13	SDCK	F4	PE1	K13	VDDIOM0	R4	PA30
A14	NSDCK	F5	PE3	K14	DDR_A7	R5	PB4
A15	D7	F6	VDDIOM1	K15	DDR_A8	R6	PB13
A16	DDR_VREF	F7	PC19	K16	DDR_A9	R7	PD0

Table 3-1. SAM9M10 Pinout for 324-ball TFBGA Package (Continued)

Pin	Signal Name
A17	D0
A18	A14
B1	PC31
B2	PC29
B3	PC30
B4	PC22
B5	PC17
B6	PC10
B7	PC11
B8	PC2
B9	SDA10
B10	A17/BA1
B11	DQM0
B12	SDCKE
B13	D12
B14	D8
B15	D4
B16	D3
B17	A15
B18	A13
C1	XIN32
C2	GNDANA
C3	WKUP
C4	PC26
C5	PC21
C6	PC15
C7	PC9
C8	PC3
C9	NWR0/NWE
C10	A16/BA0
C11	CAS
C12	D15
C13	D10
C14	D6
C15	D2
C16	GNDIOM
C17	A18

Pin	Signal Name
F8	PC14
F9	PC4
F10	NCS1/SDCS
F11	NRD
F12	SDWE
F13	A0/NBS0
F14	A1/NBS2/NWR2
F15	A3
F16	A6
F17	A5
F18	A2
G1	PD25
G2	PD23
G3	PE6
G4	PE0
G5	PE2
G6	PE8
G7	PE4
G8	PE11
G9	GNDCORE
G10	VDDIOM1
G11	VDDIOM1
G12	VDDCORE
G13	VDDCORE
G14	DDR_DQM0
G15	DDR_DQS1
G16	DDR_BA1
G17	DDR_BA0
G18	DDR_DQS0
H1	PD26
H2	PD27
H3	VDDIOP1
H4	PE13
H5	PE5
H6	PE7
H7	PE9
H8	PE10

Pin	Signal Name
K17	DDR_A11
K18	DDR_A10
L1	PA0
L2	PE30
L3	PE29
L4	PE31
L5	PA2
L6	PA4
L7	PA8
L8	PD2
L9	PD13
L10	PD29
L11	PD31
L12	VDDIOM0
L13	VDDIOM0
L14	DDR_A1
L15	DDR_A3
L16	DDR_A4
L17	DDR_A6
L18	DDR_A5
M1	PA1
M2	PA5
M3	PA6
M4	PA7
M5	PA10
M6	PA14
M7	PB14
M8	PD4
M9	PD15
M10	NRST
M11	PB11
M12	PB25
M13	PB27
M14	VDDIOM0
M15	DDR_D14
M16	DDR_D15
M17	DDR_A0

Pin	Signal Name
R8	PD9
R9	PD18
R10	TDI
R11	RTCK
R12	PB22
R13	PB29
R14	DDR_D6
R15	DDR_D1
R16	DDR_D0
R17	HHSDMA
R18	HFSDMA
T1	PA22
T2	PA25
T3	PA26
T4	PB0
T5	PB6
T6	PB16
T7	PD1
T8	PD11
T9	PD19
T10	PD30
T11	BMS
T12	PB8
T13	PB30
T14	DDR_D2
T15	PB21
T16	PB23
T17	HHSDPA
T18	HFSDPA
U1	PA27
U2	PA29
U3	PA28
U4	PB3
U5	PB7
U6	PB17
U7	PD7
U8	PD10

Table 3-1. SAM9M10 Pinout for 324-ball TFBGA Package (Continued)

Pin	Signal Name
C18	A12
D1	XOUT32
D2	PD20
D3	GNDBU
D4	VDDBU
D5	PC24
D6	PC18
D7	PC13
D8	PC6
D9	NWR1/NBS1
D10	NANDOE
D11	DQM1
D12	D14
D13	D9
D14	D5
D15	D1
D16	VDDIOM1
D17	A11
D18	A10
E1	PD21
E2	TSADVREF
E3	VDDANA
E4	JTAGSEL
E5	TST
E6	PC23
E7	PC16
E8	PC8
E9	PC1

Pin	Signal Name
H9	GNDCORE
H10	GNDIOP
H11	VDDCORE
H12	GNDIOM
H13	GNDIOM
H14	DDR_CS
H15	DDR_WE
H16	DDR_DQM1
H17	DDR_CAS
H18	DDR_NCLK
J1	PE19
J2	PE16
J3	PE14
J4	PE15
J5	PE12
J6	PE17
J7	PE18
J8	PE20
J9	GNDCORE
J10	GNDCORE
J11	GNDIOP
J12	GNDIOM
J13	GNDIOM
J14	DDR_A12
J15	DDR_A13
J16	DDR_CKE
J17	DDR_RAS
J18	DDR_CLK

Pin	Signal Name
M18	DDR_A2
N1	PA3
N2	PA9
N3	PA12
N4	PA15
N5	PA16
N6	PA17
N7	PB18
N8	PD6
N9	PD16
N10	NTRST
N11	PB9
N12	PB24
N13	PB28
N14	DDR_D13
N15	DDR_D8
N16	DDR_D9
N17	DDR_D11
N18	DDR_D12
P1	PA11
P2	PA13
P3	PA19
P4	PA21
P5	PA23
P6	PB12
P7	PB19
P8	PD8
P9	PD28

Pin	Signal Name
U9	PD14
U10	TCK
U11	VDDOSC
U12	GNDOSC
U13	PB10
U14	PB26
U15	HHSDPB/DHSDP
U16	HHSDMB/DHSDM
U17	GNDUTMI
U18	VDDUTMIC
V1	PA31
V2	PB1
V3	PB2
V4	PB5
V5	PB15
V6	PD3
V7	PD5
V8	PD12
V9	PD17
V10	TDO
V11	XOUT
V12	XIN
V13	VDDPLLUTMI
V14	VDDIOP2
V15	HFSDPB/DFSDP
V16	HFSDMB/DFSDM
V17	VDDUTMII
V18	VBG

4. Power Considerations

4.1 Power Supplies

The SAM9M10 has several types of power supply pins. Some supply pins share common ground (GND) pins whereas others have separate grounds. See Table 4-1.

Table 4-1. SAM9M10 Power Supply Pins

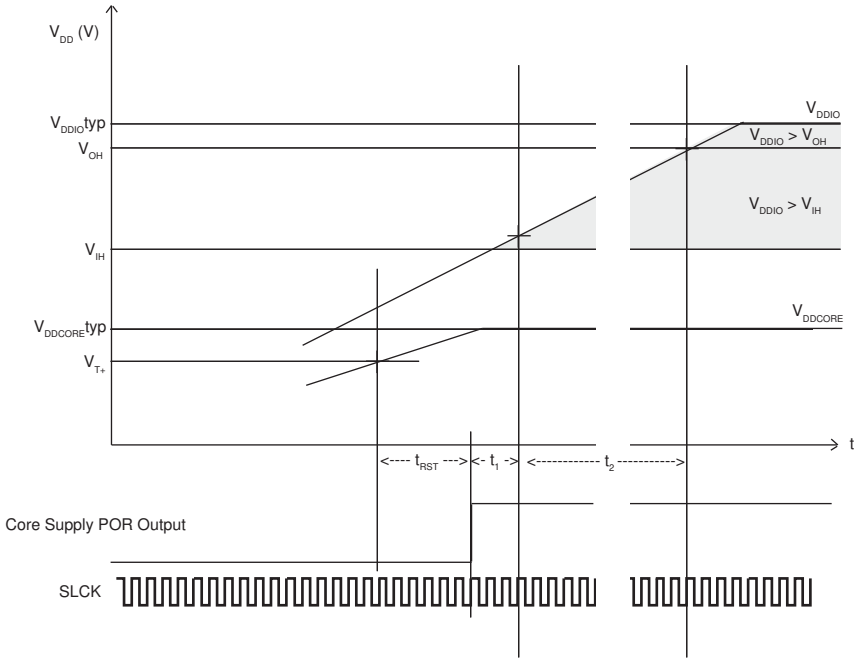
Pin(s)	Item(s) powered	Range	Typical	Ground
VDDCORE	Core, including the processor Embedded memories Peripherals	0.9–1.1 V	1.0V	GNDCORE
VDDIOM0	DDR2/LPDDR I/O lines	1.65–1.95 V	1.8V	GNDIOM
VDDIOM1	External Bus Interface 1 I/O lines	1.65–1.95 V	1.8V	
		3.0–3.6 V	3.3V	
VDDIOP0, VDDIOP1, VDDIOP2	Peripherals I/O lines	1.65–1.95 V	1.8V	GNDIOP
		3.0–3.6 V	3.3V	
VDDBU	Slow Clock oscillator Internal RC oscillator Part of the System Controller	1.8–3.6 V	–	GNDBU
VDDPLLUTMI	PLLUTMI cell	0.9–1.1 V	1.0V	GNDOSC
VDDPLLA	PLLA cell	0.9–1.1 V	1.0V	
VDDOSC	Main Oscillator cells	1.65–3.6 V	–	
VDDUTMIC	USB device Host UTMI+ core	0.9–1.1 V	1.0V	GNDUTMI
VDDUTMII	USB device Host UTMI+ interface	3.0–3.6 V	3.3V	
VDDANA	Analog-to-Digital Converter	3.0–3.6 V	3.3V	GNDANA

4.2 Power Sequence Requirements

The SAM9M10 board design must comply with the guidelines described in Section 4.2.1 “Power-up Sequence” and Section 4.2.2 “Power-down Sequence” to guarantee reliable operation of the device. Any deviation from these sequences may lead to unpredictable results.

4.2.1 Power-up Sequence

Figure 4-1. VDDCORE and VDDIO Constraints at Startup



V_{DDCORE} and V_{DDBU} are controlled by the internal PORs (Power-on Reset) to guarantee that these power sources reach their target values prior to the release of POR.

- V_{DDIOP} must be ≥ V_{IH} (refer to Table 48-2 “DC Characteristics” for more details) within (t_{RST} + t_1) after V_{DDCORE} has reached V_{T+}
- V_{DDIOM} must reach V_{OH} (refer to Table 48-2 “DC Characteristics” for more details) within (t_{RST} + t_1 + t_2) after V_{DDCORE} has reached V_{T+}
  - t_{RST} is a POR characteristic
  - t_1 = 3 × t_{SLCK}
  - t_2 = 16 × t_{SLCK}

The t_{SLCK} min (22 µs) is obtained for the maximum frequency of the internal RC oscillator (44 kHz).

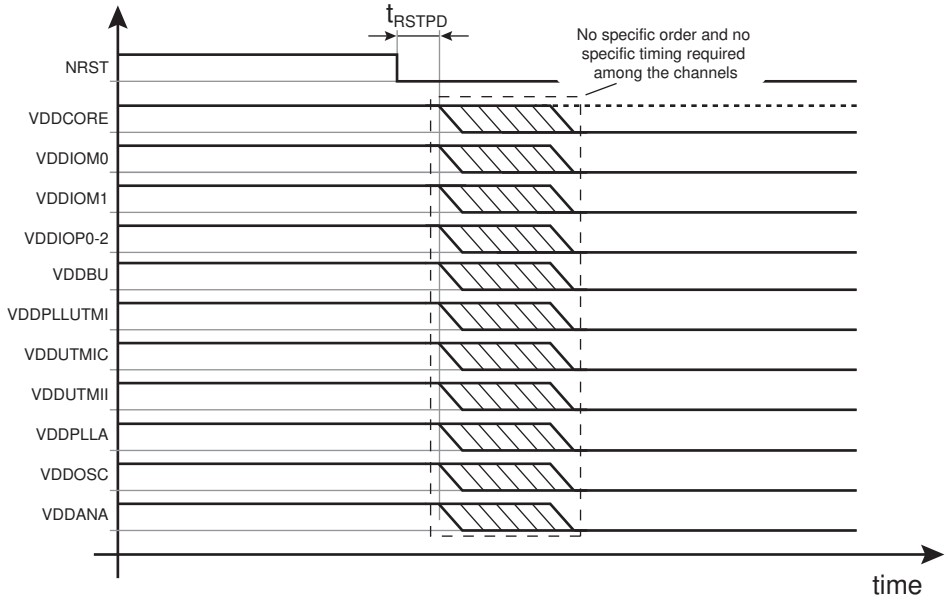
- t_{RST} = 30 µs
- t_1 = 66 µs
- t_2 = 352 µs

In conclusion, V_{DDIOP} and V_{DDIOM} must be established first, then V_{DDCORE} to ensure a reliable operation of the device. V_{DDOSC}, V_{DDPLL}, $V_{DDUTMII}$ and $V_{DDUTMIC}$ must be started at any time prior to V_{DDCORE} to ensure correct behavior of the ROM code.

4.2.2 Power-down Sequence

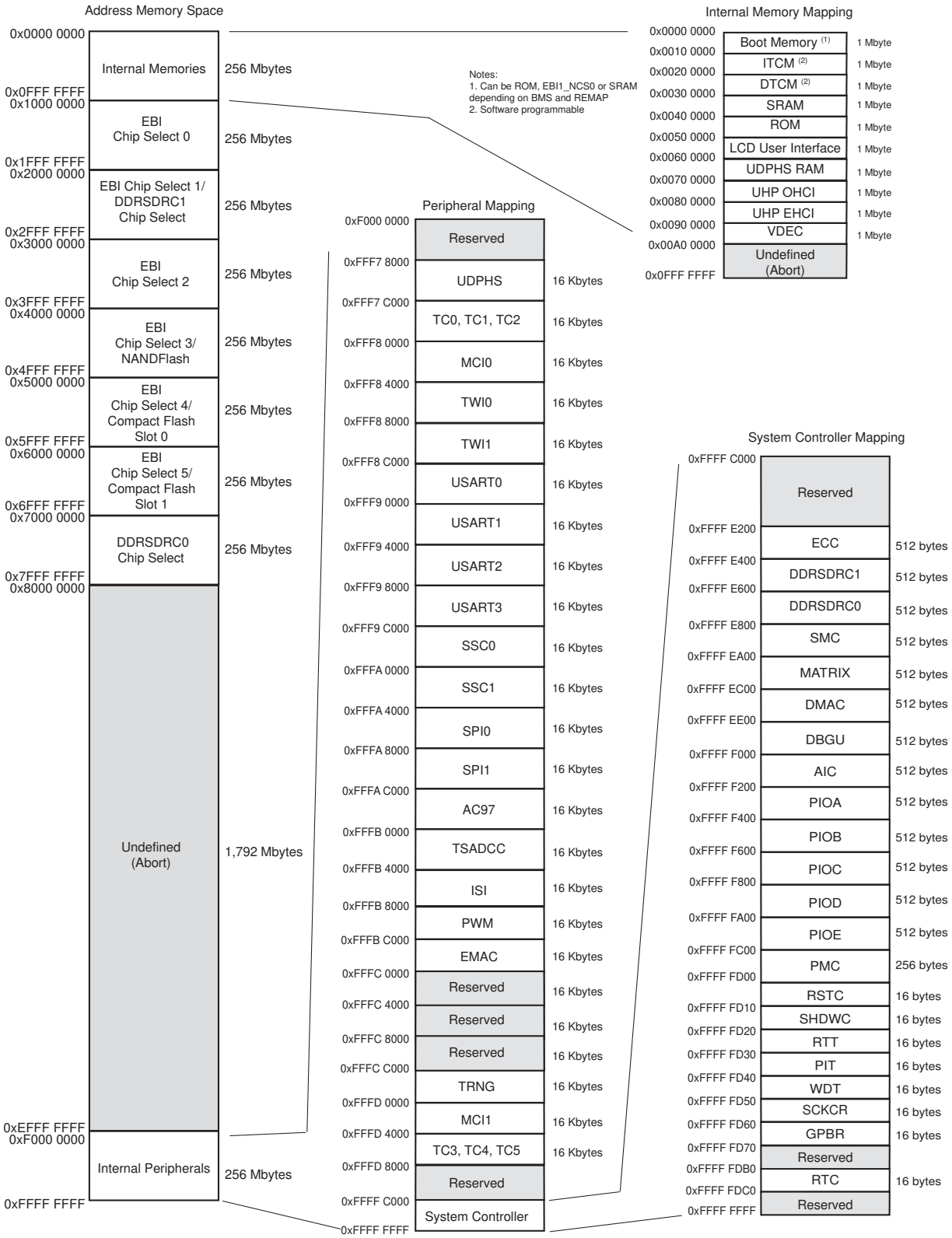
To ensure that the device does not operate outside the operating conditions defined in Section 4.1 “Power Supplies”, it is good practice to first place the device in reset state before removing its power supplies. No specific sequencing is required with respect to its supply channels as long as the NRST line is held active during the power-down phase.

Figure 4-2. Recommended Power-down Sequence



5. Memories

Figure 5-1. SAM9M10 Memory Mapping



5.1 Memory Mapping

A first level of address decoding is performed by the AHB Bus Matrix, i.e., the implementation of the Advanced High performance Bus (AHB) for its Master and Slave interfaces with additional features.

Decoding breaks up the 4 Gbytes of address space into 16 banks of 256 Mbytes. The banks 1 to 6 are directed to the EBI that associates these banks to the external chip selects NCS0 to NCS5.

The bank 7 is directed to the DDRSDRC0 that associates this bank to DDR_NCS chip select and so dedicated to the 4-port DDR2/ LPDDR controller.

The bank 0 is reserved for the addressing of the internal memories, and a second level of decoding provides 1 Mbyte of internal memory area. The bank 15 is reserved for the peripherals and provides access to the Advanced Peripheral Bus (APB).

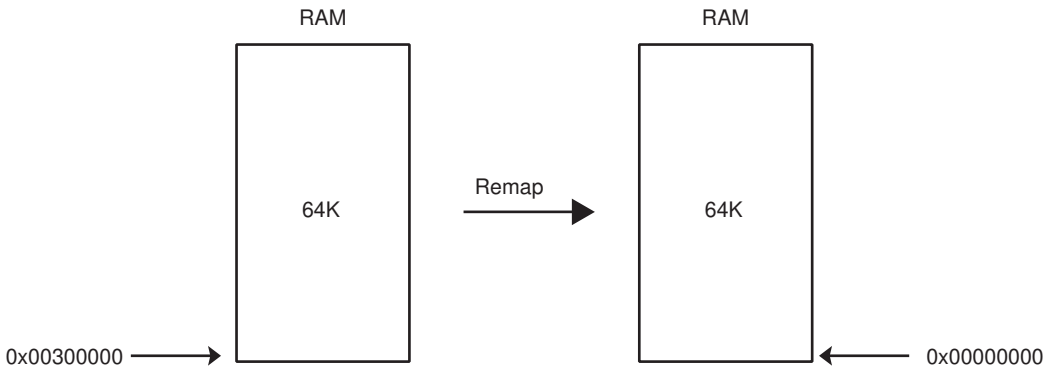
Other areas are unused and performing an access within them provides an abort to the master requesting such an access.

5.2 Embedded Memories

5.2.1 Internal SRAM

The SAM9M10 product embeds a total of 64 Kbytes high-speed SRAM split in 4 blocks of 16 Kbytes connected to one slave of the matrix. After reset and until the Remap Command is performed, the four SRAM blocks are contiguous and only accessible at address 0x00300000. After Remap, the SRAM also becomes available at address 0x0.

Figure 5-2. Internal SRAM Reset



The SAM9M10 device embeds two memory features. The processor Tightly Coupled Memory Interface (TCM) that allows the processor to access the memory up to processor speed (PCK) and the interface on the AHB side allowing masters to access the memory at AHB speed (MCK).

A wait state is necessary to access the TCM at 400 MHz. Setting the bit NWS_TCM in the bus Matrix TCM Configuration Register of the matrix inserts a wait state on the ITCM and DTCM accesses.

5.2.2 TCM Interface

On the processor side, this Internal SRAM can be allocated to three areas:

- Internal SRAM A is the ARM926EJ-S Instruction TCM. The user can map this SRAM block anywhere in the ARM926 instruction memory space using CP15 instructions and the TCR configuration register located in the Chip Configuration User Interface. This SRAM block is also accessible by the ARM926 Masters and by the AHB Masters through the AHB bus

- Internal SRAM B is the ARM926EJ-S Data TCM. The user can map this SRAM block anywhere in the ARM926 data memory space using CP15 instructions. This SRAM block is also accessible by the ARM926 Data Master and by the AHB Masters through the AHB bus.
- Internal SRAM C is only accessible by all the AHB Masters. After reset and until the Remap Command is performed, this SRAM block is accessible through the AHB bus at address 0x0030 0000 by all the AHB Masters. After Remap, this SRAM block also becomes accessible through the AHB bus at address 0x0 by the ARM926 Instruction and the ARM926 Data Masters.

Within the 64 Kbyte SRAM size available, the amount of memory assigned to each block is software programmable according to Table 5-1.

Table 5-1. ITCM and DTCM Memory Configuration

SRAM A ITCM size (Kbytes) seen at 0x100000 through AHB	SRAM B DTCM size (Kbytes) seen at 0x200000 through AHB	SRAM C (Kbytes) seen at 0x300000 through AHB
0	0	64
0	64	0
32	32	0

5.2.3 Internal ROM

The SAM9M10 embeds an Internal ROM, which contains the boot ROM and SAM-BA® program.

At any time, the ROM is mapped at address 0x0040 0000. It is also accessible at address 0x0 (BMS =1) after the reset and before the Remap Command.

5.3 I/O Drive Selection and Delay Control

5.3.1 I/O Drive Selection

The aim of this control is to adapt the signal drive to the frequency. Two bits allow the user to select High or Low drive for memories data/address/ctrl signals.

- Setting the bit [17], EBI_DRIVE, in the CCFG_EBICSA register of the matrix allows to control the drive of the EBI.
- Setting the bit [18], DDR_DRIVE, in the CCFG_EBICSA register of the matrix allows to control the drive of the DDR.

5.3.2 Delay Control

To avoid the simultaneous switching of all the I/Os, a delay can be inserted on the different EBI, DDR2 and PIO lines.

The control of these delays is the following:

- DDRSDRC

DDR_D[15:0] controlled by two registers, DELAY1 and DELAY2, located in the DDRSDRC user interface

  - DDR_D[0] <=> DELAY1[3:0],
  - DDR_D[1] <=> DELAY1[7:4],...
  - DDR_D[6] <=> DELAY1[27:24],
  - DDR_D[7] <=> DELAY1[31:28]
  - DDR_D[8] <=> DELAY2[3:0],
  - DDR_D[9] <=> DELAY2[7:4],...,
  - DDR_D[14] <=> DELAY2[27:24],
  - DDR_D[15] <=> DELAY2[31:28]

DDR_A[13:0] controlled by two registers, DELAY3 and DELAY4, located in the DDRSDRC user interface

- DDR_A[0] <=> DELAY3[3:0],
- DDR_A[1] <=> DELAY3[7:4], ...,
- DDR_A[6] <=> DELAY3[27:24],
- DDR_A[7] <=> DELAY3[31:28]
- DDR_A[8] <=> DELAY4[3:0],
- DDR_A[9] <=> DELAY4[7:4], ...,
- DDR_A[12] <=> DELAY4[19:16],
- DDR_A[13] <=> DELAY4[23:20]

- EBI (DDRSDRC\HSMC3\Nandflash)

D[15:0] controlled by two registers, DELAY1 and DELAY2, located in the HSMC3 user interface

- D[0] <=> DELAY1[3:0],
- D[1] <=> DELAY1[7:4],...,
- D[6] <=> DELAY1[27:24],
- D[7] <=> DELAY1[31:28]
- D[8] <=> DELAY2[3:0],
- D[9] <=> DELAY2[7:4],...,
- D[14] <=> DELAY2[27:24],
- D[15] <=> DELAY2[31:28]

D[31,16]on PIOC[31:16] controlled by two registers, DELAY3 and DELAY4, located in the HSMC3 user interface

- D[16] <=> DELAY3[3:0],
- D[17] <=> DELAY3[7:4],...,
- D[22] <=> DELAY3[27:24],
- PC[23] <=> DELAY3[31:28]
- D[24] <=> DELAY4[3:0],
- D[25] <=> DELAY4[7:4],...,
- D[30] <=> DELAY4[27:24],
- D[31] <=> DELAY4[31:28]

A[25:0], controlled by four registers, DELAY5, DELAY6, DELAY7and DELAY8, located in the HSMC3 user interface

- A[0] <=> DELAY5[3:0],
- A[1] <=> DELAY5[7:4],...,
- A[6] <=> DELAY5[27:24],
- A[7] <=> DELAY5[31:28]
- A[8] <=> DELAY6[3:0],
- A[9] <=> DELAY6[7:4],...,
- A[14] <=> DELAY6[27:24],
- A[15] <=> DELAY6[31:28]
- A[16] <=> DELAY7[3:0],
- A[17] <=> DELAY7[7:4],
- A[18] <=> DELAY7[11:8]

A25 on PC[12] and A[24:19] on PC[7:2]

- A19 <=> DELAY7[15:12],
- A20 <=> DELAY7[19:16],...,
- A23 <=> DELAY7[31:28],
- A24 <=> DELAY8[3:0],
- A25 <=> DELAY8[7:4]

- PIOA User interface

The delay can only be inserted on the HSMCI0 and HSMCI1 I/O lines, so on PA[9:2] and PA[30:23]. The delay is controlled by two registers, DELAY1 and DELAY2, located in the PIOA user interface.

- PA[2] <=> DELAY1[3:0],
- PA[3] <=> DELAY1[7:4],...,
- PA[8] <=> DELAY1[27:24],
- PA[9] <=> DELAY1[31:28]
- PA[23] <=> DELAY2[3:0],
- PA[24] <=> DELAY2[7:4],...,
- PA[29] <=> DELAY2[27:24],
- PA[30] <=> DELAY2[31:28]

6. System Controller

The System Controller is a set of peripherals that allows handling of key elements of the system, such as power, resets, clocks, time, interrupts, watchdog, etc.

The System Controller User Interface also embeds the registers that configure the Matrix and a set of registers for the chip configuration. The chip configuration registers configure the EBI chip select assignment and voltage range for external memories.

6.1 System Controller Mapping

The System Controller's peripherals are all mapped within the highest 16 Kbytes of address space, between addresses 0xFFFF E800 and 0xFFFF FFFF.

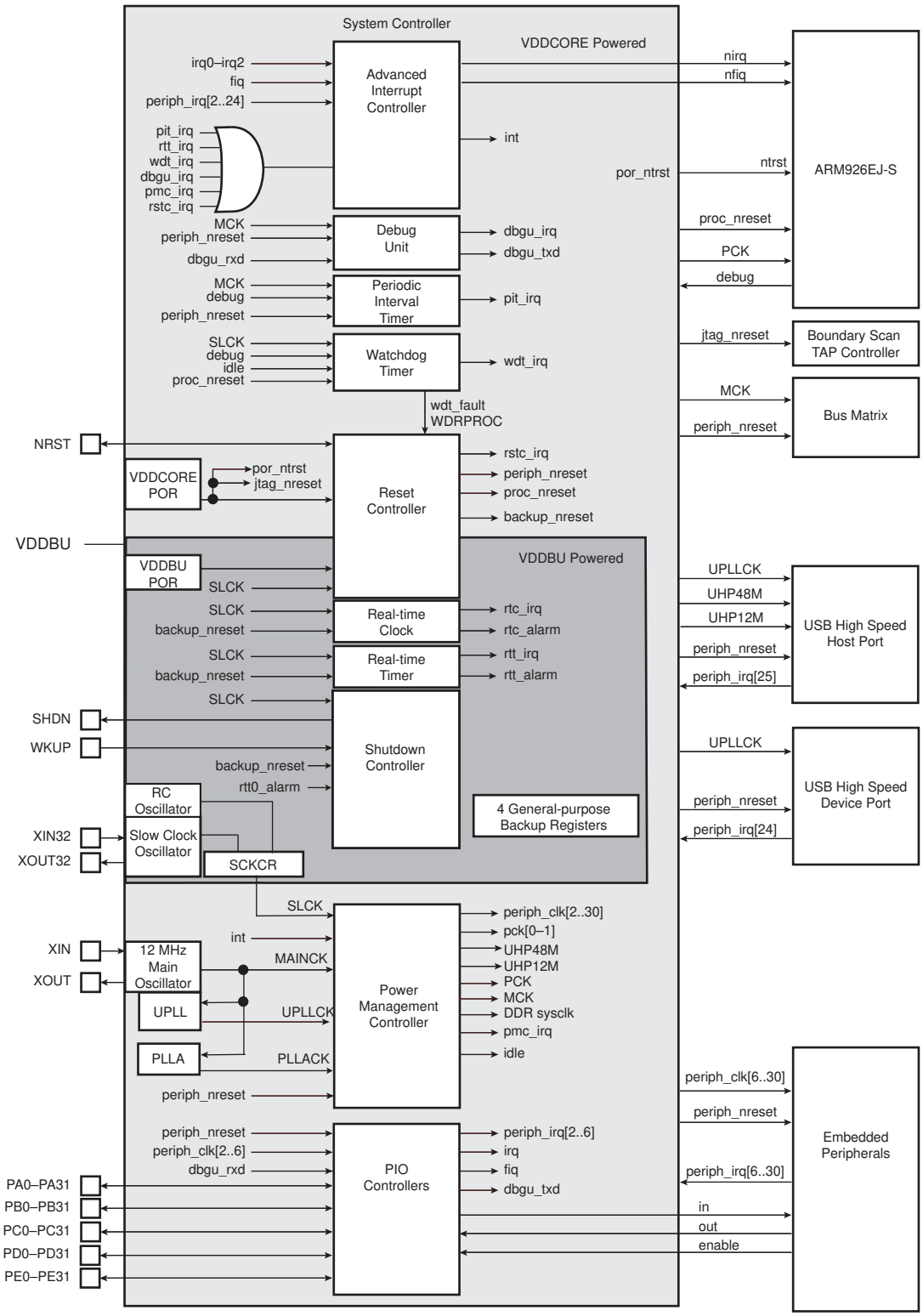
However, all the registers of the System Controller are mapped on the top of the address space. All the registers of the System Controller can be addressed from a single pointer by using the standard ARM instruction set, as the Load/Store instruction have an indexing mode of ±4 KB.

Figure 6-1 on page 23 shows the System Controller block diagram.

Figure 5.1 on page 18 shows the mapping of the User Interfaces of the System Controller peripherals.

6.2 System Controller Block Diagram

Figure 6-1. SAM9M10 System Controller Block Diagram



6.3 Chip Identification

The SAM9M10 Chip ID is defined in the Debug Unit Chip ID Register and Debug Unit Chip ID Extension Register.

- Chip ID: 0x819B05A2
- Ext ID: 0x00000002
- JTAG ID: 05B2_703F
- ARM926 TAP ID: 0x0792603F

6.4 Backup Section

The SAM9M10 features a Backup Section that embeds:

- RC Oscillator
- Slow Clock Oscillator
- Slow Clock Controller Configuration Register (SCKCR)
- RTT
- RTC
- Shutdown Controller
- 128-bit backup registers
- A part of RSTC

This section is powered by the VDDBU rail.

7. Peripherals

7.1 Peripheral Mapping

As shown in Figure 5.1 “Memory Mapping”, the peripherals are mapped in the upper 256 Mbytes of the address space between the addresses 0xFFF7 8000 and 0xFFFC FFFF.

Each User Peripheral is allocated 16 Kbytes of address space.

7.2 Peripheral Identifiers

Table 7-1 defines the Peripheral Identifiers of the SAM9M10. A peripheral identifier is required for the control of the peripheral interrupt with the Advanced Interrupt Controller and for the control of the peripheral clock with the Power Management Controller.

Table 7-1. SAM9M10 Peripheral Identifiers

Peripheral ID	Peripheral Mnemonic	Peripheral Name	External Interrupt
0	AIC	Advanced Interrupt Controller	FIQ
1	SYSC	System Controller	
2	PIOA	Parallel I/O Controller A	
3	PIOB	Parallel I/O Controller B	
4	PIOC	Parallel I/O Controller C	
5	PIOD/PIOE	Parallel I/O Controller D/E	
6	TRNG	True Random Number Generator	
7	US0	Universal Synchronous Asynchronous Receiver Transmitter 0	
8	US1	Universal Synchronous Asynchronous Receiver Transmitter 1	
9	US2	Universal Synchronous Asynchronous Receiver Transmitter 2	
10	US3	Universal Synchronous Asynchronous Receiver Transmitter 3	
11	MCI0	High Speed Multimedia Card Interface 0	
12	TWI0	Two-wire Interface 0	
13	TWI1	Two-wire Interface 1	
14	SPI0	Serial Peripheral Interface 0	
15	SPI1	Serial Peripheral Interface 1	
16	SSC0	Synchronous Serial Controller 0	
17	SSC1	Synchronous Serial Controller 1	
18	TC0 .. TC5	Timer Counter 0 .. Timer Counter 5	
19	PWM	Pulse Width Modulation Controller	
20	TSADCC	Touchscreen ADC Controller	
21	DMA	DMA Controller	
22	UHPHS	USB High Speed Host Port	
23	LCDC	LCD Controller	
24	AC97C	AC97 Controller	
25	EMAC	Ethernet MAC	