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SAM9XE Series

Atmel | SMART ARM-based Embedded MCU

DATASHEET

Description

The Atmel® | SMART SAM9XE microcontroller series is based on the integration of an ARM926EJ-S™ processor with fast ROM, RAM and Flash, and a wide range of peripherals.

The embedded Flash memory can be programmed in-system via the JTAG-ICE interface or via a parallel interface on a production programmer prior to mounting. Built-in lock bits, a security bit and MMU protect the firmware from accidental overwrite and preserve its confidentiality.

The SAM9XE series embeds an Ethernet MAC, one USB Device Port, and a USB Host Controller. It also integrates several standard peripherals, including six UARTs, SPI, TWI, Timer Counters, Synchronous Serial Controller, ADC and a MultiMedia/SD Card Interface.

The SAM9XE system controller includes a reset controller capable of managing the power-on sequence of the microcontroller and the complete system. Correct device operation can be monitored by a built-in brownout detector and a watchdog running off an integrated RC oscillator.

The SAM9XE series architecture includes a 6-layer matrix, allowing a maximum internal bandwidth of six 32-bit buses. It also features an External Bus Interface capable of interfacing with a wide range of memory devices.

The pinout and ball-out are fully compatible with the Atmel | SMART SAM9260 eMPU with the exception that the pin BMS is replaced by the pin ERASE.

SAM9XE Embedded Internal Memories Configuration

Device	ROM	SRAM	High-speed Flash
SAM9XE128	32 KB	16 KB	128 KB
SAM9XE256	32 KB	32 KB	256 KB
SAM9XE512	32 KB	32 KB	512 KB

Features

- Incorporates the ARM926EJ-S ARM® Thumb® Processor
  - DSP instruction Extensions, ARM Jazelle® Technology for Java® Acceleration
  - 8 KB Data Cache, 16 KB Instruction Cache, Write Buffer
  - 200 MIPS at 180 MHz
  - Memory Management Unit
  - EmbeddedICE, Debug Communication Channel Support
- Additional Embedded Memories
  - One 32 KB Internal ROM, Single-cycle Access at Maximum Matrix Speed
  - One 32 KB (SAM9XE256 and SAM9XE512) or 16 KB (SAM9XE128) Internal SRAM, Single-cycle Access at Maximum Matrix Speed
  - Internal High-speed Flash: 128 KB (SAM9XE128), 256 KB (SAM9XE256) or 512 KB (SAM9XE512) organized in 256, 512 or 1024 pages of 512 bytes respectively
    - 128-bit Wide Access
    - Fast Read Time: 45 ns
    - Page Programming Time: 4 ms, Including Page Auto-erase
      Full Erase Time: 10 ms
    - 10,000 Write Cycles, 10 Years Data Retention, Page Lock Capabilities, Flash Security Bit
- Enhanced Embedded Flash Controller (EEFC)
  - Interface of the Flash Block with the 32-bit Internal Bus
  - Increases Performance in ARM and Thumb Mode with 128-bit Wide Memory Interface
- External Bus Interface (EBI)
  - Supports SDRAM, Static Memory, ECC-enabled NAND Flash and CompactFlash®
- USB 2.0 Full Speed (12 Mbit/s) Device Port
  - On-chip Transceiver, 2688-byte Configurable Integrated DPRAM
- USB 2.0 Full Speed (12 Mbit/s) Host Single Port in 208-pin PQFP Device and Double Port in 217-ball LFBGA Device
  - Single or Dual On-chip Transceivers
  - Integrated FIFOs and Dedicated DMA Channels
- Ethernet MAC 10/100 Base-T
  - Media Independent Interface (MII) or Reduced Media Independent Interface (RMII)
  - 128-byte FIFOs and Dedicated DMA Channels for Receive and Transmit
- Image Sensor Interface (ISI)
  - ITU-R BT. 601/656 External Interface, Programmable Frame Capture Rate
  - 12-bit Data Interface for Support of High Sensibility Sensors
  - SAV and EAV Synchronization, Preview Path with Scaler, YCbCr Format
- Bus Matrix
  - Six 32-bit-layer Matrix
  - Remap Command
- Fully-featured System Controller, including
  - Reset Controller (RSTC), Shutdown Controller (SHDWC)
  - 128-bit (4 x 32-bit) General Purpose Backup Registers
  - Clock Generator and Power Management Controller
  - Advanced Interrupt Controller (AIC) and Debug Unit (DBGU)
  - Periodic Interval Timer (PIT), Watchdog Timer (WDT) and Real-time Timer (RTT)
- Reset Controller (RSTC)
  - Based on a Power-on Reset Cell, Reset Source Identification and Reset Output Control

- Clock Generator (CKGR)
  - Selectable 32768 Hz Low-power Oscillator or Internal Low Power RC Oscillator on Battery Backup Power Supply, Providing a Permanent Slow Clock
  - 3 to 20 MHz On-chip Oscillator, One Up to 240 MHz PLL and One Up to 100 MHz PLL
- Power Management Controller (PMC)
  - Very Slow Clock Operating Mode, Software Programmable Power Optimization Capabilities
  - Two Programmable External Clock Signals
- Advanced Interrupt Controller (AIC)
  - Individually Maskable, Eight-level Priority, Vectored Interrupt Sources
  - Three External Interrupt Sources and One Fast Interrupt Source, Spurious Interrupt Protected
- Debug Unit (DBGU)
  - 2-wire UART and support for Debug Communication Channel, Programmable ICE Access Prevention
  - Mode for General Purpose Two-wire UART Serial Communication
- Periodic Interval Timer (PIT)
  - 20-bit Interval Timer Plus 12-bit Interval Counter
- Watchdog Timer (WDT)
  - Key-protected, Programmable Only Once, Windowed 16-bit Counter Running at Slow Clock
- Real-time Timer (RTT)
  - 32-bit Free-running Backup Counter Running at Slow Clock with 16-bit Prescaler
- One 4-channel 10-bit Analog-to-Digital Converter
- Three 32-bit Parallel Input/Output Controllers (PIOA, PIOB, PIOC)
  - 96 Programmable I/O Lines Multiplexed with up to Two Peripheral I/Os
  - Input Change Interrupt Capability on Each I/O Line
  - Individually Programmable Open-drain, Pull-up Resistor and Synchronous Output
- Peripheral DMA Controller (PDC) Channels
- Two-slot Multimedia Card Interface (MCI)
  - SDCard/SDIO and MultiMediaCard™ Compliant
  - Automatic Protocol Control and Fast Automatic Data Transfers with PDC
- One Synchronous Serial Controllers (SSC)
  - Independent Clock and Frame Sync Signals for Each Receiver and Transmitter
  - I²S Analog Interface Support, Time Division Multiplex Support
  - High-speed Continuous Data Stream Capabilities with 32-bit Data Transfer
- Four Universal Synchronous/Asynchronous Receiver Transmitters (USART)
  - Individual Baud Rate Generator, IrDA® Infrared Modulation/Demodulation, Manchester Encoding/Decoding
  - Support for ISO7816 T0/T1 Smart Card, Hardware Handshaking, RS485 Support
  - Full Modem Signal Control on USART0
- One 2-wire UART
- Two Master/Slave Serial Peripheral Interface (SPI)
  - 8- to 16-bit Programmable Data Length, Four External Peripheral Chip Selects
  - Synchronous Communications
- Two 3-channel 16-bit Timer/Counters (TC)
  - Three External Clock Inputs, Two Multi-purpose I/O Pins per Channel
  - Double PWM Generation, Capture/Waveform Mode, Up/Down Capability
  - High-Drive Capability on Outputs TIOA0, TIOA1, TIOA2

- 2 Two-wire Interfaces (TWI)
  - Master, Multi-master and Slave Mode Operation
  - General Call Supported in Slave Mode
  - Connection to PDC Channel to Optimize Data Transfers in Master Mode Only
- IEEE® 1149.1 JTAG Boundary Scan on All Digital Pins
- Required Power Supplies:
  - 1.65V to 1.95V for VDDBU, VDDCORE and VDDPLL
  - 1.65V to 3.6V for VDDIOP1 (Peripheral I/Os)
  - 3.0V to 3.6V for VDDIOP0 and VDDANA (Analog-to-Digital Converter)
  - Programmable 1.65V to 1.95V or 3.0V to 3.6V for VDDIOM (Memory I/Os)
- Available in 208-pin PQFP and 217-ball LFBGA Green-compliant Packages

1. Block Diagram

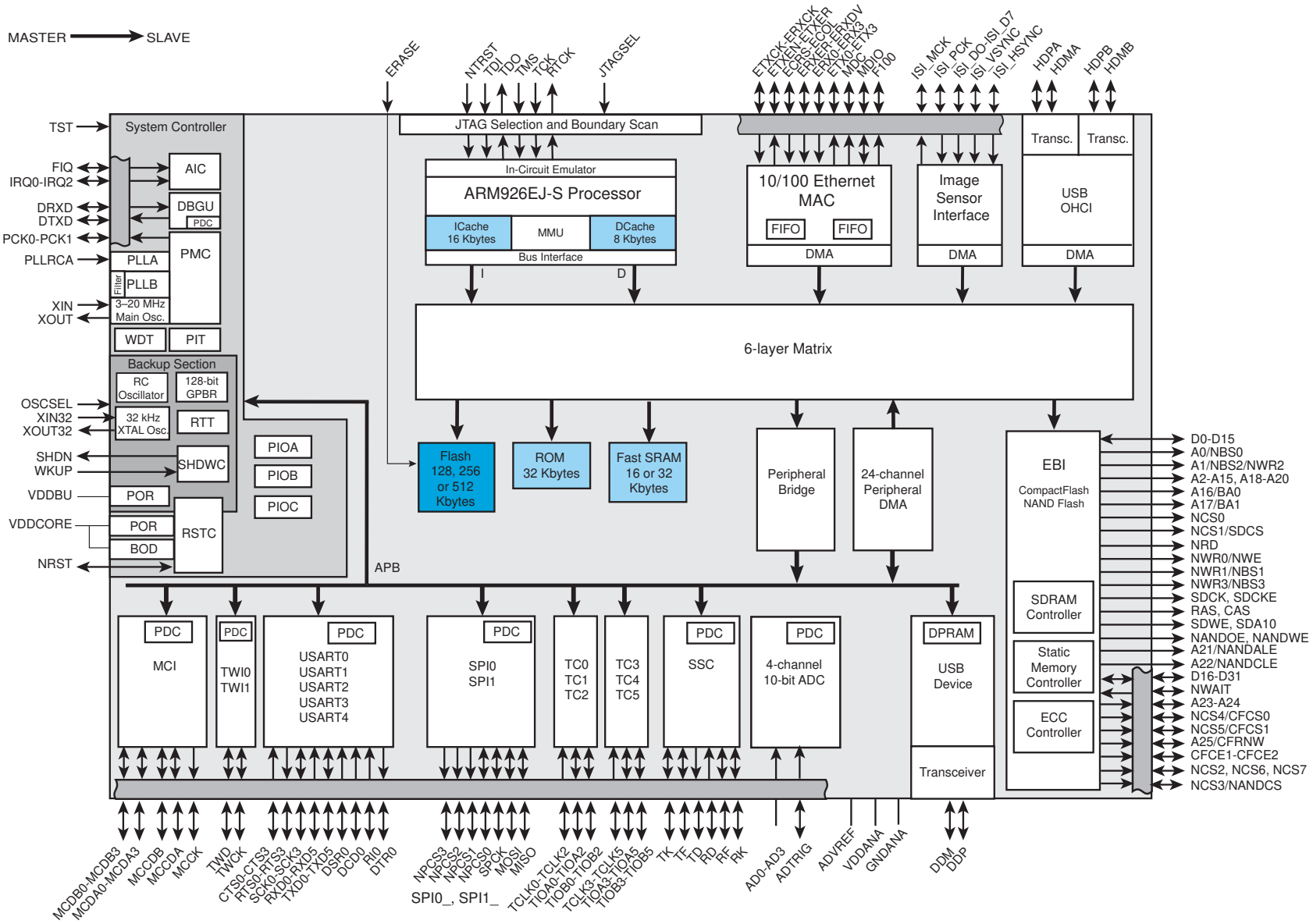
Figure 1-1, “SAM9XE Series Block Diagram,” on page 6 shows all the features for the 217-LFBGA package. Some functions are not accessible in the 208-PQFP package and the unavailable pins are highlighted in “Multiplexing on PIO Controller A” on page 40, “Multiplexing on PIO Controller B” on page 41, “Multiplexing on PIO Controller C” on page 42. The USB Host Port B is also not available.

Table 1-1 defines all the multiplexed and not multiplexed pins not available in the 208-PQFP package.

Table 1-1. Unavailable Signals in 208-pin PQFP Device

PIO	Peripheral A	Peripheral B
–	HDPB	–
–	HDMB	–
PA30	SCK2	RXD4
PA31	SCK0	TXD4
PB12	TWD1	ISI_D10
PB13	TWCK1	ISI_D11
PC2	AD2	PCK1
PC3	AD3	SPI1_NPCS3
PC12	IRQ0	NCS7

Figure 1-1. SAM9XE Series Block Diagram



2. Signal Description

Table 2-1 gives details on the signal name classified by peripheral.

Table 2-1. Signal Description List

Signal Name	Function	Type	Active Level	Reference Voltage	Comments
Power Supplies					
VDDIOM	EBI I/O Lines Power Supply	Power			1.65V to 1.95V or 3.0V to 3.6V
VDDIOP0	Peripherals I/O Lines Power Supply	Power			3.0V to 3.6V
VDDIOP1	Peripherals I/O Lines Power Supply	Power			1.65V to 3.6V
VDDBU	Backup I/O Lines Power Supply	Power			1.65V to 1.95V
VDDANA	Analog Power Supply	Power			3.0V to 3.6V
VDDPLL	PLL Power Supply	Power			1.65V to 1.95V
VDDCORE	Core Chip and Embedded Memories Power Supply	Power			1.65V to 1.95V
GND	Ground	Ground			
GNDPLL	PLL Ground	Ground			
GNDANA	Analog Ground	Ground			
GNDBU	Backup Ground	Ground			
Clocks, Oscillators and PLLs					
XIN	Main Oscillator Input	Input			
XOUT	Main Oscillator Output	Output			
XIN32	Slow Clock Oscillator Input	Input			
XOUT32	Slow Clock Oscillator Output	Output			
OSCSEL	Slow Clock Oscillator Selection	Input		VDDBU	Accepts between 0V and VDDBU
PLLRCA	PLL A Filter	Input			
PCK0–PCK1	Programmable Clock Output	Output		(2)	
Shutdown, Wakeup Logic					
SHDN	Shutdown Control	Output	Low	VDDBU	Driven at 0V only
WKUP	Wake-up Input	Input		VDDBU	Accepts between 0V and VDDBU
ICE and JTAG					
NTRST	Test Reset Signal	Input	Low	VDDIOP0	Pull-up resistor (100 kΩ)
TCK	Test Clock	Input		VDDIOP0	No pull-up resistor, Schmitt trigger
TDI	Test Data In	Input		VDDIOP0	No pull-up resistor, Schmitt trigger
TDO	Test Data Out	Output		VDDIOP0	
TMS	Test Mode Select	Input		VDDIOP0	No pull-up resistor, Schmitt trigger
JTAGSEL	JTAG Selection	Input		VDDBU	Pull-down resistor (15 kΩ)
RTCK	Return Test Clock	Output		VDDIOP0	
Flash Memory					
ERASE	Flash and NVM Configuration Bits Erase Command	Input	High	VDDIOP0	Pull-down resistor (15 kΩ)

Table 2-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Reference Voltage	Comments
Reset/Test					
NRST	Microcontroller Reset	I/O	Low	VDDIOP0	Open-drain output, Pull-up resistor (100 kΩ) Inserted in the Boundary Scan
TST	Test Mode Select	Input		VDDBU	Pull-down resistor (15 kΩ)
Debug Unit - DBGU					
DRXD	Debug Receive Data	Input		(2)	
DTXD	Debug Transmit Data	Output		(2)	
Advanced Interrupt Controller - AIC					
IRQ0–IRQ2	External Interrupt Inputs	Input		(2)	
FIQ	Fast Interrupt Input	Input		(2)	
PIO Controller - PIOA / PIOB / PIOC					
PA0–PA31	Parallel IO Controller A	I/O		VDDIOP0	Pulled-up input at reset (100 kΩ)(1)
PB0–PB31	Parallel IO Controller B	I/O		VDDIOP0	Pulled-up input at reset (100 kΩ)(1)
PC0–PC31	Parallel IO Controller C	I/O		(2)	Pulled-up input at reset (100 kΩ)(1)
External Bus Interface - EBI					
D0–D31	Data Bus	I/O		VDDIOM	Pulled-up input at reset
A0–A25	Address Bus	Output		VDDIOM	0 at reset
NWAIT	External Wait Signal	Input	Low	VDDIOM	
Static Memory Controller - SMC					
NCS0–NCS7	Chip Select Lines	Output	Low	VDDIOM	
NWR0–NWR3	Write Signal	Output	Low	VDDIOM	
NRD	Read Signal	Output	Low	VDDIOM	
NWE	Write Enable	Output	Low	VDDIOM	
NBS0–NBS3	Byte Mask Signal	Output	Low	VDDIOM	
CompactFlash Support					
CFCE1–CFCE2	CompactFlash Chip Enable	Output	Low	VDDIOM	
CFOE	CompactFlash Output Enable	Output	Low	VDDIOM	
CFWE	CompactFlash Write Enable	Output	Low	VDDIOM	
CFIOR	CompactFlash IO Read	Output	Low	VDDIOM	
CFIOW	CompactFlash IO Write	Output	Low	VDDIOM	
CFRNW	CompactFlash Read Not Write	Output		VDDIOM	
CFCS0–CFCS1	CompactFlash Chip Select Lines	Output	Low	VDDIOM	
NAND Flash Support					
NANDCS	NAND Flash Chip Select	Output	Low	VDDIOM	
NANDOE	NAND Flash Output Enable	Output	Low	VDDIOM	
NANDWE	NAND Flash Write Enable	Output	Low	VDDIOM	

Table 2-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Reference Voltage	Comments
SDRAM Controller - SDRAMC					
SDCK	SDRAM Clock	Output		VDDIOM	
SDCKE	SDRAM Clock Enable	Output	High	VDDIOM	
SDCS	SDRAM Controller Chip Select	Output	Low	VDDIOM	
BA0–BA1	Bank Select	Output		VDDIOM	
SDWE	SDRAM Write Enable	Output	Low	VDDIOM	
RAS - CAS	Row and Column Signal	Output	Low	VDDIOM	
SDA10	SDRAM Address 10 Line	Output		VDDIOM	
Multimedia Card Interface - MCI					
MCCK	Multimedia Card Clock	Output		VDDIOP0	
MCCDA	Multimedia Card Slot A Command	I/O		VDDIOP0	
MCDA0–MCDA3	Multimedia Card Slot A Data	I/O		VDDIOP0	
MCCDB	Multimedia Card Slot B Command	I/O		VDDIOP0	
MCDB0–MCDB3	Multimedia Card Slot B Data	I/O		VDDIOP0	
Universal Synchronous Asynchronous Receiver Transmitter - USARTx					
SCKx	USARTx Serial Clock	I/O		(2)	
TXDx	USARTx Transmit Data	I/O		(2)	
RXDx	USARTx Receive Data	Input		(2)	
RTSx	USARTx Request To Send	Output		(2)	
CTSx	USARTx Clear To Send	Input		(2)	
DTR0	USART0 Data Terminal Ready	Output		(2)	
DSR0	USART0 Data Set Ready	Input		(2)	
DCD0	USART0 Data Carrier Detect	Input		(2)	
RI0	USART0 Ring Indicator	Input		(2)	
Synchronous Serial Controller - SSC					
TD	SSC Transmit Data	Output		(2)	
RD	SSC Receive Data	Input		(2)	
TK	SSC Transmit Clock	I/O		(2)	
RK	SSC Receive Clock	I/O		(2)	
TF	SSC Transmit Frame Sync	I/O		(2)	
RF	SSC Receive Frame Sync	I/O		(2)	
Timer/Counter - TCx					
TCLKx	TC Channel x External Clock Input	Input		(2)	
TIOAx	TC Channel x I/O Line A	I/O		(2)	
TIOBx	TC Channel x I/O Line B	I/O		(2)	
Serial Peripheral Interface - SPIx					
SPIx_MISO	Master In Slave Out	I/O		(2)	
SPIx_MOSI	Master Out Slave In	I/O		(2)	
SPIx_SPCK	SPI Serial Clock	I/O		(2)	
SPIx_NPCS0	SPI Peripheral Chip Select 0	I/O	Low	(2)	
SPIx_NPCS1–SPIx_NPCS3	SPI Peripheral Chip Select	Output	Low	(2)	

Table 2-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Reference Voltage	Comments
Two-wire Interface - TWI					
TWDx	Two-wire Serial Data	I/O		(2)	
TWCKx	Two-wire Serial Clock	I/O		(2)	
USB Host Port - UHP					
HDPA	USB Host Port A Data +	Analog		VDDIOP0	
HDMA	USB Host Port A Data -	Analog		VDDIOP0	
HDPB	USB Host Port B Data +	Analog		VDDIOP0	
HDMB	USB Host Port B Data +	Analog		VDDIOP0	
USB Device Port - UDP					
DDM	USB Device Port Data -	Analog		VDDIOP0	
DDP	USB Device Port Data +	Analog		VDDIOP0	
Ethernet MAC 10/100 - EMAC					
ETXCK	Transmit Clock or Reference Clock	Input		VDDIOP0	MII only, REFCK in RMII
ERXCK	Receive Clock	Input		VDDIOP0	MII only
ETXEN	Transmit Enable	Output		VDDIOP0	
ETX0–ETX3	Transmit Data	Output		VDDIOP0	ETX0–ETX1 only in RMII
ETXER	Transmit Coding Error	Output		VDDIOP0	MII only
ERXDV	Receive Data Valid	Input		VDDIOP0	RXDV in MII, CRSDV in RMII
ERX0–ERX3	Receive Data	Input		VDDIOP0	ERX0–ERX1 only in RMII
ERXER	Receive Error	Input		VDDIOP0	
ECRS	Carrier Sense and Data Valid	Input		VDDIOP0	MII only
ECOL	Collision Detect	Input		VDDIOP0	MII only
EMDC	Management Data Clock	Output		VDDIOP0	
EMDIO	Management Data Input/Output	I/O		VDDIOP0	
EF100	Force 100Mbit/sec.	Output	High	VDDIOP0	
Image Sensor Interface - ISI					
ISI_D0–ISI_D11	Image Sensor Data	Input		VDDIOP1	
ISI_MCK	Image sensor Reference clock	output		VDDIOP1	
ISI_HSYNC	Image Sensor Horizontal Synchro	input		VDDIOP1	
ISI_VSYNC	Image Sensor Vertical Synchro	input		VDDIOP1	
ISI_PCK	Image Sensor Data clock	input		VDDIOP1	
Analog-to-Digital Converter - ADC					
AD0–AD3	Analog Inputs	Analog		VDDANA	Digital pulled-up inputs at reset
ADVREF	Analog Positive Reference	Analog		VDDANA	
ADTRG	ADC Trigger	Input		VDDANA	

Table 2-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Reference Voltage	Comments
Fast Flash Programming Interface - FFPI					
PGMEN[3:0]	Programming Enabling	Input		VDDIOP0	
PGMNCMD	Programming Command	Input	Low	VDDIOP0	
PGMRDY	Programming Ready	Output	High	VDDIOP0	
PGMNOE	Programming Read	Input	Low	VDDIOP0	
PGMNVALID	Data Direction	Output	Low	VDDIOP0	
PGMM[3:0]	Programming Mode	Input		VDDIOP0	
PGMD[15:0]	Programming Data	I/O		VDDIOP0	

Notes:
1. Programming of this pull-up resistor is performed independently for each I/O line through the PIO Controllers. After reset, all the I/O lines default as inputs with pull-up resistors enabled, except those which are multiplexed with the External Bus Interface signals that require to be enabled as Peripheral at reset. This is explicitly indicated in the column “Reset State” of the peripheral multiplexing tables.
2. Refer to PIO Multiplexing (see Section 9.3 “Peripheral Signals Multiplexing on I/O Lines”).

3. Package and Pinout

The SAM9XE devices are available in the following Green-compliant packages:

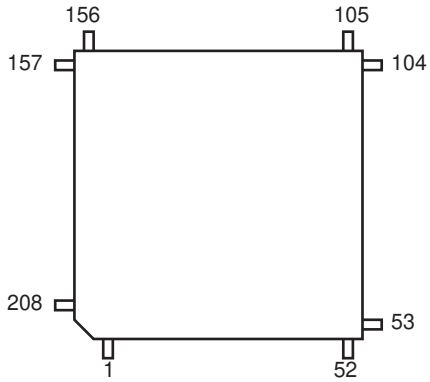
- 208-pin PQFP (0.5 mm pitch)
- 217-ball LFBGA (0.8 mm ball pitch)

3.1 208-pin PQFP Package Outline

Figure 3-1 shows the orientation of the 208-pin PQFP package.

A detailed mechanical description is given in Section 43. “Mechanical Characteristics”.

Figure 3-1. 208-pin PQFP Package Outline (Top View)



3.2 208-pin PQFP Package Pinout

Table 3-1. Pinout for 208-pin PQFP Package

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
1	PA24	53	GND	105	RAS	157	ADVREF
2	PA25	54	DDM	106	D0	158	PC0
3	PA26	55	DDP	107	D1	159	PC1
4	PA27	56	PC13	108	D2	160	VDDANA
5	VDDIOP0	57	PC11	109	D3	161	PB10
6	GND	58	PC10	110	D4	162	PB11
7	PA28	59	PC14	111	D5	163	PB20
8	PA29	60	PC9	112	D6	164	PB21
9	PB0	61	PC8	113	GND	165	PB22
10	PB1	62	PC4	114	VDDIOM	166	PB23
11	PB2	63	PC6	115	SDCK	167	PB24
12	PB3	64	PC7	116	SDWE	168	PB25
13	VDDIOP0	65	VDDIOM	117	SDCKE	169	VDDIOP1
14	GND	66	GND	118	D7	170	GND
15	PB4	67	PC5	119	D8	171	PB26
16	PB5	68	NCS0	120	D9	172	PB27

Table 3-1. Pinout for 208-pin PQFP Package (Continued)

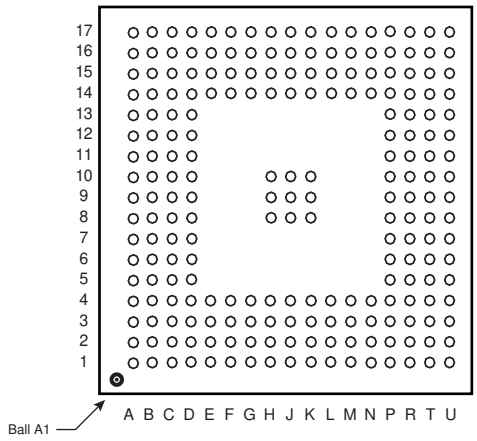
Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
17	PB6	69	CFOE/NRD	121	D10	173	GND
18	PB7	70	CFWE/NWE/NWR0	122	D11	174	VDDCORE
19	PB8	71	NANDOE	123	D12	175	PB28
20	PB9	72	NANDWE	124	D13	176	PB29
21	PB14	73	A22	125	D14	177	PB30
22	PB15	74	A21	126	D15	178	PB31
23	PB16	75	A20	127	PC15	179	PA0
24	VDDIOP0	76	A19	128	PC16	180	PA1
25	GND	77	VDDCORE	129	PC17	181	PA2
26	PB17	78	GND	130	PC18	182	PA3
27	PB18	79	A18	131	PC19	183	PA4
28	PB19	80	BA1/A17	132	VDDIOM	184	PA5
29	TDO	81	BA0/A16	133	GND	185	PA6
30	TDI	82	A15	134	PC20	186	PA7
31	TMS	83	A14	135	PC21	187	VDDIOP0
32	VDDIOP0	84	A13	136	PC22	188	GND
33	GND	85	A12	137	PC23	189	PA8
34	TCK	86	A11	138	PC24	190	PA9
35	NTRST	87	A10	139	PC25	191	PA10
36	NRST	88	A9	140	PC26	192	PA11
37	RTCK	89	A8	141	PC27	193	PA12
38	VDDCORE	90	VDDIOM	142	PC28	194	PA13
39	GND	91	GND	143	PC29	195	PA14
40	ERASE	92	A7	144	PC30	196	PA15
41	OSCSEL	93	A6	145	PC31	197	PA16
42	TST	94	A5	146	GND	198	PA17
43	JTAGSEL	95	A4	147	VDDCORE	199	VDDIOP0
44	GNDBU	96	A3	148	VDDPLL	200	GND
45	XOUT32	97	A2	149	XIN	201	PA18
46	XIN32	98	NWR2/NBS2/A1	150	XOUT	202	PA19
47	VDDBU	99	NBS0/A0	151	GNDPLL	203	VDDCORE
48	WKUP	100	SDA10	152	NC	204	GND
49	SHDN	101	CFIOW/NBS3/NWR3	153	GNDPLL	205	PA20
50	HDMA	102	CFIOR/NBS1/NWR1	154	PLLRCA	206	PA21
51	HDPA	103	SDCS/NCS1	155	VDDPLL	207	PA22
52	VDDIOP0	104	CAS	156	GNDANA	208	PA23

3.3 217-ball LFBGA Package Outline

Figure 3-2 shows the orientation of the 217-ball LFBGA package.

A detailed mechanical description is given in Section 43. “Mechanical Characteristics”.

Figure 3-2. 217-ball LFBGA Package Outline (Top View)



3.4 217-ball LFBGA Package Pinout

Table 3-2. Pinout for 217-ball LFBGA Package

Pin	Signal Name
A1	CFIOW/NBS3/NWR3
A2	NBS0/A0
A3	NWR2/NBS2/A1
A4	A6
A5	A8
A6	A11
A7	A13
A8	BA0/A16
A9	A18
A10	A21
A11	A22
A12	CFWE/NWE/NWR0
A13	CFOE/NRD
A14	NCS0
A15	PC5
A16	PC6
A17	PC4
B1	SDCK
B2	CFIOR/NBS1/NWR1
B3	SDCS/NCS1

Pin	Signal Name
D5	A5
D6	GND
D7	A10
D8	GND
D9	VDDCORE
D10	GND
D11	VDDIOM
D12	GND
D13	DDM
D14	HDPB
D15	NC
D16	VDDBU
D17	XIN32
E1	D10
E2	D5
E3	D3
E4	D4
E14	HDPA
E15	HDMA
E16	GNDBU

Pin	Signal Name
J14	TDO
J15	PB19
J16	TDI
J17	PB16
K1	PC24
K2	PC20
K3	D15
K4	PC21
K8	GND
K9	GND
K10	GND
K14	PB4
K15	PB17
K16	GND
K17	PB15
L1	GND
L2	PC26
L3	PC25
L4	VDDIOP0
L14	PA28

Pin	Signal Name
P17	PB5
R1	NC
R2	GNDANA
R3	PC29
R4	VDDANA
R5	PB12
R6	PB23
R7	GND
R8	PB26
R9	PB28
R10	PA0
R11	PA4
R12	PA5
R13	PA10
R14	PA21
R15	PA23
R16	PA24
R17	PA29
T1	PLLRCA
T2	GNDPLL

Table 3-2. Pinout for 217-ball LFBGA Package (Continued)

Pin	Signal Name
B4	SDA10
B5	A3
B6	A7
B7	A12
B8	A15
B9	A20
B10	NANDWE
B11	PC7
B12	PC10
B13	PC13
B14	PC11
B15	PC14
B16	PC8
B17	WKUP
C1	D8
C2	D1
C3	CAS
C4	A2
C5	A4
C6	A9
C7	A14
C8	BA1/A17
C9	A19
C10	NANDOE
C11	PC9
C12	PC12
C13	DDP
C14	HDMB
C15	NC
C16	VDDIOP0
C17	SHDN
D1	D9
D2	D2
D3	RAS
D4	D0

Pin	Signal Name
E17	XOUT32
F1	D13
F2	SDWE
F3	D6
F4	GND
F14	OSCSEL
F15	ERASE
F16	JTAGSEL
F17	TST
G1	PC15
G2	D7
G3	SDCKE
G4	VDDIOM
G14	GND
G15	NRST
G16	RTCK
G17	TMS
H1	PC18
H2	D14
H3	D12
H4	D11
H8	GND
H9	GND
H10	GND
H14	VDDCORE
H15	TCK
H16	NTRST
H17	PB18
J1	PC19
J2	PC17
J3	VDDIOM
J4	PC16
J8	GND
J9	GND
J10	GND

Pin	Signal Name
L15	PB9
L16	PB8
L17	PB14
M1	VDDCORE
M2	PC31
M3	GND
M4	PC22
M14	PB1
M15	PB2
M16	PB3
M17	PB7
N1	XIN
N2	VDDPLL
N3	PC23
N4	PC27
N14	PA31
N15	PA30
N16	PB0
N17	PB6
P1	XOUT
P2	VDDPLL
P3	PC30
P4	PC28
P5	PB11
P6	PB13
P7	PB24
P8	VDDIOP1
P9	PB30
P10	PB31
P11	PA1
P12	PA3
P13	PA7
P14	PA9
P15	PA26
P16	PA25

Pin	Signal Name
T3	PC0
T4	PC1
T5	PB10
T6	PB22
T7	GND
T8	PB29
T9	PA2
T10	PA6
T11	PA8
T12	PA11
T13	VDDCORE
T14	PA20
T15	GND
T16	PA22
T17	PA27
U1	GNDPLL
U2	ADVREF
U3	PC2
U4	PC3
U5	PB20
U6	PB21
U7	PB25
U8	PB27
U9	PA12
U10	PA13
U11	PA14
U12	PA15
U13	PA19
U14	PA17
U15	PA16
U16	PA18
U17	VDDIOP0

4. Power Considerations

4.1 Power Supplies

The SAM9XE devices have several types of power supply pins. Some supply pins share common ground (GND) pins whereas others have separate grounds. See Table 4-1.

Table 4-1. SAM9XE Power Supply Pins

Pin(s)	Item(s) powered	Range	Typical	Ground
VDDCORE	Core, including the processor Embedded memories Peripherals	1.65–1.95 V	1.8V	GND
VDDIOM	External Bus Interface I/O lines	1.65–1.95 V(1)	1.8V	
		3.0–3.6 V(1)	3.3V	
VDDIOP0	Peripheral I/O lines and the USB transceivers	3.0–3.6 V	3.3V	
VDDIOP1	Peripherals I/O lines involving the Image Sensor Interface	1.65–3.6 V	1.8V 2.5V 3.3V	
VDDBU	Slow Clock oscillator Part of the System Controller	1.65–1.95 V	1.8V	GNDBU
VDDPLL	PLL cells main oscillator	1.65–1.95 V	1.8V	GNDPLL
VDDANA	Analog-to-Digital Converter	3.0–3.6 V	3.3V	GNDANA

Note: 1. Desired voltage range selectable by software

The power supplies VDDIOM, VDDIOP0 and VDDIOP1 are identified in the pinout table and their associated I/O lines in the multiplexing tables. These supplies enable the user to power the device differently for interfacing with memories and for interfacing with peripherals.

4.2 Power Sequence Requirements

The board design must comply with the power-up guidelines below to guarantee reliable operation of the device. Any deviation from these sequences may prevent the device from booting.

4.2.1 Power-up Sequence

VDDCORE and VDDBU are controlled by internal POR (Power-On-Reset) to guarantee that these power sources reach their target values prior to the release of POR.

To ensure a working system, VDDIOP0, VDDIOP1, and VDDIOM should be established to power external memories and I/Os before the first access. This can be achieved if VDDIOP0, VDDIOP1, and VDDIOM are powered before VDDCORE.

4.2.2 Power-down Sequence

To ensure external memories and I/Os are powered until the last access, switch off VDDIOM, VDDIOP0 and VDDIOP1 power supplies after or at the same time as switching off VDDCORE.

No power-up or power-down restrictions apply to VDDBU, VDDPLL and VDDANA.

5. I/O Line Considerations

5.1 ERASE Pin

The ERASE pin is used to re-initialize the Flash content and the NVM bits. It integrates a permanent pull-down resistor of about 15 kΩ, so that it can be left unconnected for normal operations. The ERASE pin is powered by VDDIOP0 rail.

This pin is debounced on the RC oscillator or 32768 Hz low-power oscillator to improve the glitch tolerance. Minimum debouncing time is 200 ms.

5.2 I/O Line Drive Levels

The PIO lines PA0 to PA31 and PB0 to PB31 and PC0 to PC3 are high-drive current capable. Each of these I/O lines can drive up to 16 mA permanently with a total of 350 mA on all I/O lines.

Refer to Section 42.2 “DC Characteristics”.

5.3 Shutdown Logic Pins

The SHDN pin is a tri-state output only pin, which is driven by the Shutdown Controller. There is no internal pull-up. An external pull-up to VDDBU is needed and its value must be higher than 1 MΩ. The resistor value is calculated according to the regulator enable implementation and the SHDN level.

The WKUP pin is an input-only. It can accept voltages only between 0V and VDDBU.

6. Processor and Architecture

6.1 ARM926EJ-S Processor

- RISC Processor Based on ARM v5TEJ Architecture with Jazelle technology for Java acceleration
- Two Instruction Sets
  - ARM High-performance 32-bit Instruction Set
  - Thumb High Code Density 16-bit Instruction Set
- DSP Instruction Extensions
- 5-Stage Pipeline Architecture:
  - Instruction Fetch (F)
  - Instruction Decode (D)
  - Execute (E)
  - Data Memory (M)
  - Register Write (W)
- 8 KB Data Cache, 16 KB Instruction Cache
  - Virtually-addressed 4-way Associative Cache
  - Eight words per line
  - Write-through and Write-back Operation
  - Pseudo-random or Round-robin Replacement
- Write Buffer
  - Main Write Buffer with 16-word Data Buffer and 4-address Buffer
  - DCache Write-back Buffer with 8-word Entries and a Single Address Entry
  - Software Control Drain
- Standard ARM v4 and v5 Memory Management Unit (MMU)
  - Access Permission for Sections
  - Access Permission for large pages and small pages can be specified separately for each quarter of the page
  - 16 embedded domains
- Bus Interface Unit (BIU)
  - Arbitrates and Schedules AHB Requests
  - Separate Masters for both instruction and data access providing complete Matrix system flexibility
  - Separate Address and Data Buses for both the 32-bit instruction interface and the 32-bit data interface
  - On Address and Data Buses, data can be 8-bit (Bytes), 16-bit (Half-words) or 32-bit (Words)

6.2 Bus Matrix

- 6-layer Matrix, handling requests from 6 masters
- Programmable Arbitration strategy
  - Fixed-priority Arbitration
  - Round-Robin Arbitration, either with no default master, last accessed default master or fixed default master
- Burst Management
  - Breaking with Slot Cycle Limit Support
  - Undefined Burst Length Support
- One Address Decoder provided per Master
  - Three different slaves may be assigned to each decoded memory area: one for internal ROM boot, one for internal flash boot, one after remap
- Boot Mode Select
  - Non-volatile Boot Memory can be internal ROM or internal Flash
  - Selection is made by General purpose NVM bit sampled at reset
- Remap Command
  - Allows Remapping of an Internal SRAM in Place of the Boot Non-Volatile Memory (ROM or Flash)
  - Allows Handling of Dynamic Exception Vectors

6.2.1 Matrix Masters

The Bus Matrix manages six Masters, thus each master can perform an access concurrently with others, depending on whether the slave it accesses is available.

Each Master has its own decoder, which can be defined specifically for each master. In order to simplify the addressing, all the masters have the same decodings.

Table 6-1. List of Bus Matrix Masters

Master 0	ARM926™ Instruction
Master 1	ARM926 Data
Master 2	Peripheral DMA Controller
Master 3	USB Host Controller
Master 4	Image Sensor Controller
Master 5	Ethernet MAC

6.2.2 Matrix Slaves

Each Slave has its own arbiter, thus allowing a different arbitration per Slave to be programmed.

Table 6-2. List of Bus Matrix Slaves

Slave 0	Internal SRAM
Slave 1	Internal ROM
	USB Host User Interface
Slave 2	External Bus Interface
Slave 3	Internal Flash
Slave 4	Internal Peripherals
Slave 5	Reserved

6.2.3 Masters to Slaves Access

All the Masters can normally access all the Slaves. However, some paths do not make sense, such as allowing access from the Ethernet MAC to the internal peripherals.

Thus, these paths are forbidden or simply not wired, and shown as “–” in the following table.

Table 6-3. Masters to Slaves Access

Slave	Master	0 and 1	2	3	4	5
		ARM926 Instruction and Data	Peripheral DMA Controller	ISI Controller	Ethernet MAC	USB Host Controller
0	Internal SRAM	X	X	X	X	X
1	Internal ROM	X	X	–	–	–
	UHP User Interface	X	–	–	–	–
2	External Bus Interface	X	X	X	X	X
3	Internal Flash	X	–	–	X	–
4	Internal Peripherals	X	X	–	–	–
–	Reserved	–	–	–	–	–

6.3 Peripheral DMA Controller

- Acting as one Matrix Master
- Allows data transfers from/to peripheral to/from any memory space without any intervention of the processor.
- Next Pointer Support, forbids strong real-time constraints on buffer management.
- Twenty-four channels
  - Two for each USART
  - Two for the Debug Unit
  - Two for each Serial Synchronous Controller
  - Two for each Serial Peripheral Interface
  - Two for the Two Wire Interface
  - One for Multimedia Card Interface
  - One for Analog-to-Digital Converter

The Peripheral DMA Controller handles transfer requests from the channel according to the following priorities (Low to High priorities):

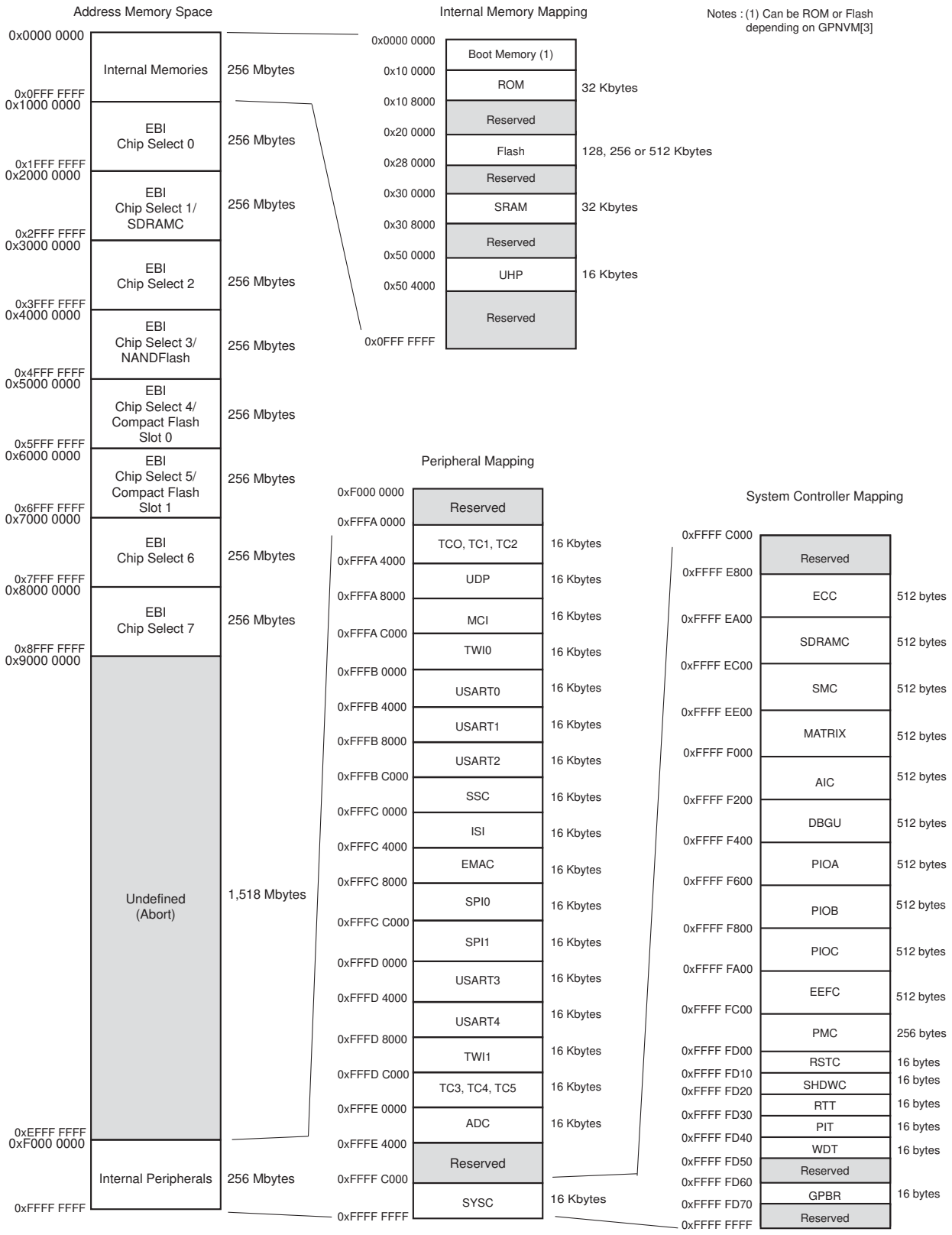
- TWI0 Transmit Channel
- TWI1 Transmit Channel
- DBGU Transmit Channel
- USART4 Transmit Channel
- USART3 Transmit Channel
- USART2 Transmit Channel
- USART1 Transmit Channel
- USART0 Transmit Channel
- SPI1 Transmit Channel
- SPI0 Transmit Channel
- SSC Transmit Channel
- TWI0 Receive Channel
- TWI1 Receive Channel
- DBGU Receive Channel
- USART4 Receive Channel
- USART3 Receive Channel
- USART2 Receive Channel
- USART1 Receive Channel
- USART0 Receive Channel
- ADC Receive Channel
- SPI1 Receive Channel
- SPI0 Receive Channel
- SSC Receive Channel
- MCI Transmit/Receive Channel

6.4 Debug and Test Features

- ARM926 Real-time In-circuit Emulator
  - Two real-time Watchpoint Units
  - Two Independent Registers: Debug Control Register and Debug Status Register
  - Test Access Port Accessible through JTAG Protocol
  - Debug Communications Channel
- Debug Unit
  - Two-pin UART
  - Debug Communication Channel Interrupt Handling
  - Chip ID Register
- IEEE1149.1 JTAG Boundary-scan on All Digital Pins

7. Memories

Figure 7-1. Memory Mapping



A first level of address decoding is performed by the Bus Matrix, i.e., the implementation of the Advanced High performance Bus (AHB) for its Master and Slave interfaces with additional features.

Decoding breaks up the 4 Gbytes of address space into 16 banks of 256 MB. Banks 1 to 7 are directed to the EBI that associates these banks to the external chip selects EBI_NCS0 to EBI_NCS7. Bank 0 is reserved for the addressing of the internal memories, and a second level of decoding provides 1 MB of internal memory area. Bank 15 is reserved for the peripherals and provides access to the Advanced Peripheral Bus (APB).

Other areas are unused and performing an access within them provides an abort to the master requesting such an access.

Each Master has its own bus and its own decoder, thus allowing a different memory mapping per Master. However, in order to simplify the mappings, all the masters have a similar address decoding.

Regarding Master 0 and Master 1 (ARM926 Instruction and Data), three different Slaves are assigned to the memory space decoded at address 0x0: one for internal boot, one for external boot, one after remap, refer to Table 7-3, “Internal Memory Mapping,” on page 28 for details.

7.1 Embedded Memories

7.1.1 SAM9XE128

- 32 KB ROM
  - Single Cycle Access at full matrix speed
- 16 KB Fast SRAM
  - Single Cycle Access at full matrix speed
- 128 KB Embedded Flash

7.1.2 SAM9XE256

- 32 KB ROM
  - Single Cycle Access at full matrix speed
- 32 KB Fast SRAM
  - Single Cycle Access at full matrix speed
- 256 KB Embedded Flash

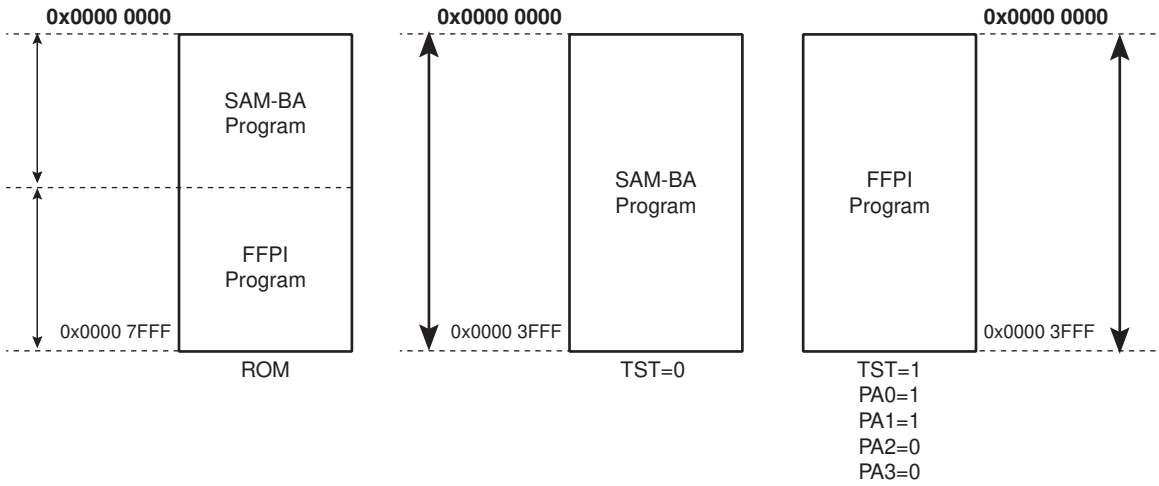
7.1.3 SAM9XE512

- 32 KB ROM
  - Single Cycle Access at full matrix speed
- 32 KB Fast SRAM
  - Single Cycle Access at full matrix speed
- 512 KB Embedded Flash

7.1.4 ROM Topology

The embedded ROM contains the Fast Flash Programming and the SAM-BA® boot programs. Each of these two programs is stored on 16 KB Boundary of FFPI and the program executed at address zero depends on the combination of the TST pin and PA0 to PA3 pins. Figure 7-2 shows the contents of the ROM and the program available at address zero.

Figure 7-2. ROM Boot Memory Map



7.1.4.1 Fast Flash Programming Interface

The Fast Flash Programming Interface programs the device through a serial JTAG interface or a multiplexed fully-handshaked parallel port. It allows gang-programming with market-standard industrial programmers.

The FFPI supports read, page program, page erase, full erase, lock, unlock and protect commands.

The Fast Flash Programming Interface is enabled and the Fast Programming Mode is entered when the TST pin and the PA0 and PA1 pins are all tied high, while PA2 and PA3 are tied low.

Table 7-1. Signal Description

Signal Name	PIO	Type	Active Level	Comments
PGMEN0	PA0	Input	High	Must be connected to VDDIO
PGMEN1	PA1	Input	High	Must be connected to VDDIO
PGMEN2	PA2	Input	Low	Must be connected to GND
PGMEN3	PA3	Input	Low	Must be connected to GND
PGMNCMD	PA4	Input	Low	Pulled-up input at reset
PGMRDY	PA5	Output	High	Pulled-up input at reset
PGMNOE	PA6	Input	Low	Pulled-up input at reset
PGMNVALID	PA7	Output	Low	Pulled-up input at reset
PGMM[3:0]	PA8..PA10	Input		Pulled-up input at reset
PGMD[15:0]	PA12..PA27	Input/Output		Pulled-up input at reset

7.1.4.2 SAM-BA Boot Assistant

The SAM-BA Boot Assistant is a default Boot Program that provides an easy way to program in situ the on-chip Flash memory.

The SAM-BA Boot Assistant supports serial communication through the DBGU or through the USB Device Port.

- Communication through the DBGU supports a wide range of crystals from 3 to 20 MHz via software auto-detection.
- Communication through the USB Device Port is depends on crystal selected:
  - limited to an 18432 Hz crystal if the internal RC oscillator is selected
  - supports a wide range of crystals from 3 to 20 MHz if the 32768 Hz crystal is selected

The SAM-BA Boot provides an interface with SAM-BA Graphic User Interface (GUI).