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Automotive LED Driver IC with High Current Accuracy

Features

- Switch mode controller for boost, SEPIC & buck converters
- Closed loop control of output current
- High PWM dimming ratio
- Internal 40V linear regulator
- Internal 3% voltage reference
- Constant frequency operation with programmable slope compensation
- Linear and PWM dimming
- Programmable jitter to reduce EMI
- +/-1.0A MOSFET gate driver
- Output short circuit protection
- Output over voltage protection
- Programmable hiccup timer
- Temperature fold-back with external NTC resistor
- Soft start
- Meets AEC-Q100 requirements

Applications

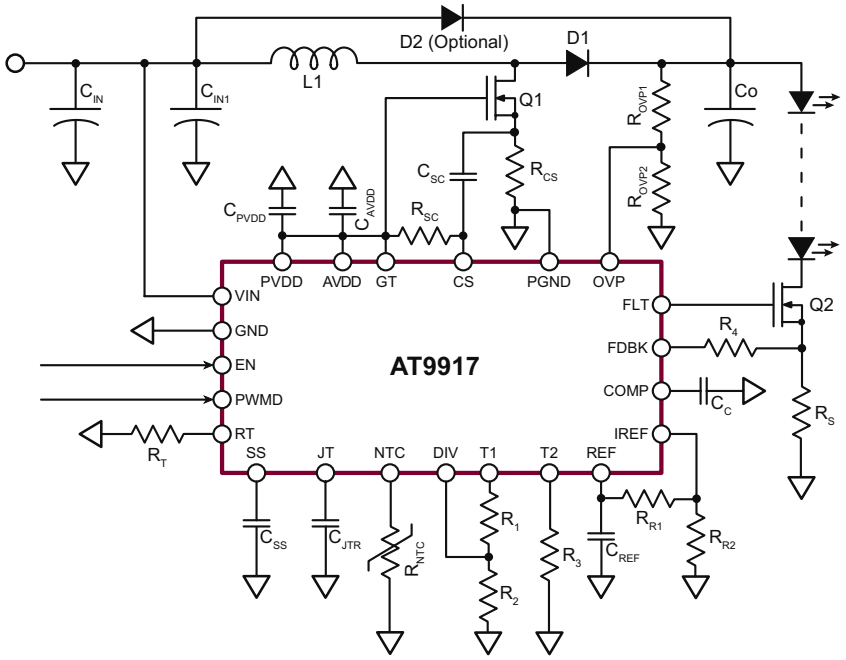
- Automotive LED driver applications

General Description

The AT9917 is an advanced fixed frequency PWM IC designed to control single-switch, boost, SEPIC, and buck LED drivers in a constant current mode. The controller uses a peak current-mode control scheme (with programmable slope compensation) and includes an internal transconductance amplifier to control the output current with high accuracy. The IC includes a +/-1A gate driver that makes the AT9917 suitable for high power applications. An internal 40V linear regulator powers the IC eliminating the need for a separate power supply for the IC. The IC provides a FAULT output, which can be used to disconnect the LEDs in case of a fault condition (such as an alternator load dump in automobiles) using an external disconnect FET. AT9917 also provides a TTL compatible, low-frequency PWM dimming input that can accept an external control signal with a duty ratio of 0-100% and a frequency of up to several kilohertz. Temperature foldback of the output current is possible, using an external NTC resistor.

The AT9917-based LED driver is suited for automotive LED driver applications. The AT9917 based LED lamp drivers can achieve efficiencies in excess of 90% when buck or boost topologies are used.

Typical Boost Application Circuit



Ordering Information

Device	24-Lead TSSOP *7.80x4.40mm body* *1.20mm height (max)* *0.65mm pitch*
AT9917	AT9917TS-G

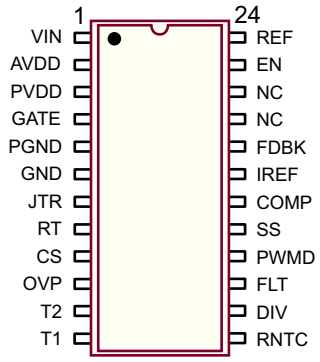
-G indicates package is RoHS compliant ('Green')

Absolute Maximum Ratings

Parameter	Value
V_{IN} to GND	-0.5V to +45V
PV_{DD}, AV_{DD} to GND	-0.3V to +6.0V
GATE to GND	-0.3V to (PV_{DD} +0.3V)
All other pins to GND	-0.3V to (AV_{DD} +0.3V)
Continuous power dissipation (T_A = +25°C)	1000mW
Junction temperature	-40°C to +150°C
Storage temperature range	-65°C to +150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Configuration



24-Lead TSSOP (TS)
(top view)

Product Marking

YY = Year Sealed
WW = Week Sealed
L = Lot Number
C = Country of Origin*
A = Assembler ID
——— = "Green" Packaging
**May be part of ejector pin*

Package may or may not include the following marks: Si or

24-Lead TSSOP (TS)

Electrical Characteristics

(Specifications are at T_A = 25°C. V_{IN} = 12V, PV_{DD} = AV_{DD}, EN = PWMD = AV_{DD}, GATE = OPEN, C_{REF} = 0.1µF, C_{AVDD} = C_{PVDD} = 1.0µF, R_T = 200kΩ, I_{T1} = I_{T2} = 100µA unless otherwise noted.)

Sym	Parameter		Min	Typ	Max	Units	Conditions
Input							
V_{INDC}	Input DC supply voltage range	-	5.3	-	40	V	DC input voltage
I_{INDIS}	Shut-down mode supply current	*	-	-	100	µA	EN = 0.8V, PWMD = GND
I_{INEN}	Input current when enabled	*	-	-	2.0	mA	EN = 2.0V, GATE OPEN, PWMD = GND
Internal Regulator							
AV_{DD}	Internally regulated voltage	*	4.65	5.0	5.35	V	V_{IN} = 6.0 - 40V, GATE OPEN, PWMD = GND, I_{DD} = 0 - 20mA
UVLO	AV_{DD} undervoltage lockout threshold	*	4.25	-	4.85	V	AV_{DD} rising
ΔUVLO	AV_{DD} undervoltage lockout hysteresis	-	-	250	-	mV	AV_{DD} falling

Notes:

* *Specifications apply over the full operating ambient temperature range of -40°C < T_A < +125°C. Guaranteed by design and characterization.*

Electrical Characteristics *(Specifications are at T_A = 25°C. V_{IN} = 12V, PV_{DD} = AV_{DD}, EN = PWMD = AV_{DD}, GATE = OPEN, C_{REF} = 0.1µF, C_{AVDD} = C_{PVDD} = 1.0µF, R_T = 200kΩ, I_{T1} = I_{T2} = 100µA unless otherwise noted.)*

Sym	Description		Min	Typ	Max	Units	Conditions
EN Input							
$V_{EN(LO)}$	EN input low voltage	*	-	-	0.8	V	---
$V_{EN(HI)}$	EN input high voltage	*	2.0	-	-	V	---
R_{EN}	Pull down resistor at EN	-	-	100	-	kΩ	---
Reference							
V_{REF}	REF pin voltage	*	1.210	1.250	1.290	V	I_{REF} = 0
$V_{REF,DIS}$	REF pin voltage when disabled	-	-	0	-	mV	I_{REF} = 0, EN = GND
$V_{REFLOAD}$	Load regulation of reference voltage	-	0	-	2.0	mV	I_{REF} = 0 - 1.0mA
GATE							
T_{RISE}	GATE output rise time	-	-	20	35	ns	C_{GATE} = 4.0nF, V_{IN} = AV_{DD} = PV_{DD} = 5.0V
T_{FALL}	GATE output fall time	-	-	20	35	ns	C_{GATE} = 4.0nF, V_{IN} = AV_{DD} = PV_{DD} = 5.0V
D_{MAX}	Maximum duty cycle	*	87	-	93	%	---
PWM Dimming							
$V_{PWMD(lo)}$	PWMD input low voltage	*	-	-	0.8	V	---
$V_{PWMD(hi)}$	PWMD input high voltage	*	2.0	-	-	V	---
R_{PWMD}	PWMD pull-down resistance	-	-	200	-	kΩ	---
Over Voltage Protection							
$V_{OVP,rising}$	Over voltage rising trip point	*	1.15	1.25	1.35	V	OVP rising
$V_{OVP,HYST}$	Over voltage hysteresis	-	-	0.125	-	V	OVP falling
Current Sense							
T_{BLANK}	Leading edge blanking	*	100	-	250	ns	---
T_{DELAY1}	Delay to output of comparator	-	-	-	150	ns	COMP = AV_{DD} = PV_{DD} = 5.0V, V_{CS} = 0 - 400mV step
V_{OFFSET}	Comparator offset voltage	#	-10	-	10	mV	---
Internal Transconductance Opamp							
G_B	Gainbandwidth product	#	1.0	-	-	MHz	150pF capacitance at COMP pin
A_V	Open loop DC gain	-	65	-	-	dB	Output OPEN
V_{CM}	Input common-mode range	#	-0.3	-	3.0	V	---
V_O	Output voltage range	#	0.7	-	AV_{DD}	-	---
G_M	Transconductance	-	-	950	-	µA/V	---
V_{OFFSET}	Input offset voltage	*	-9.0	-	9.0	mV	---

Notes:

* *Specifications apply over the full operating ambient temperature range of -40ºC < T_A < +125ºC. Guaranteed by design and characterization.*

\# *Specifications guaranteed by design and not tested in production*

Electrical Characteristics *(Specifications are at T_A = 25°C. V_{IN} = 12V, PV_{DD} = AV_{DD}, EN = PWMD = AV_{DD}, GATE = OPEN, C_{REF} = 0.1µF, C_{AVDD} = C_{PVDD} = 1.0µF, R_T = 200kΩ, I_{T1} = I_{T2} = 100µA unless otherwise noted.)*

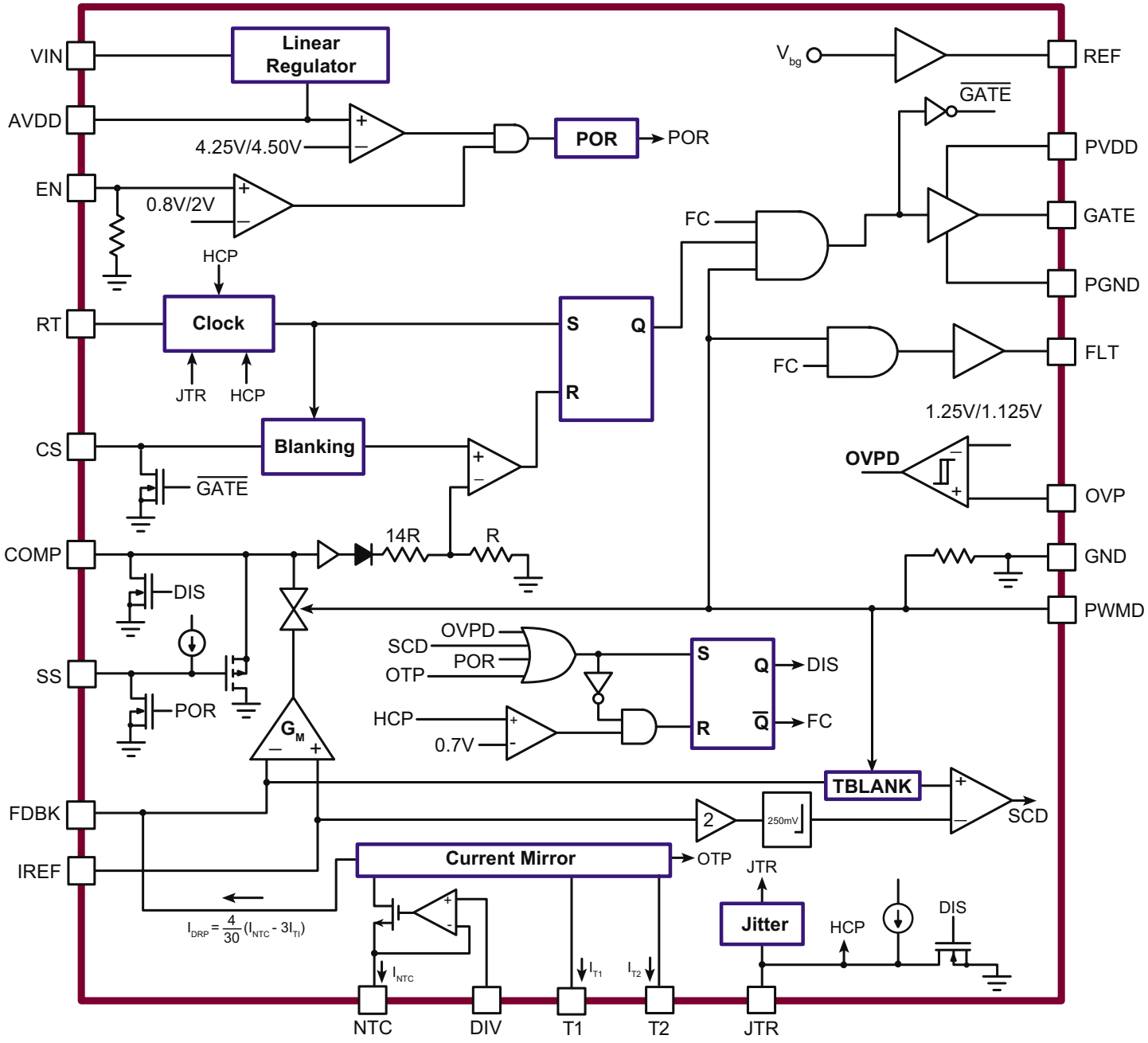
Sym	Parameter		Min	Typ	Max	Units	Conditions
I_{COMP}	COMP sink current	#	0.2	-	-	mA	V_{FB} = 0.1V, V_{COMP} = 0
I_{COMP}	COMP source current	#	-0.2	-	-	mA	V_{FB} = -0.1V, V_{COMP} = AV_{DD}
I_{BIAS}	Input bias current	#	-	0.5	1.0	nA	---
Oscillator							
f_{OSC1}	Oscillator frequency	*	90	105	120	kHz	RT = 1.0MΩ
f_{OSC2}	Oscillator frequency	*	427	505	583	kHz	RT = 200kΩ
f_{OSC}	Output frequency range	#	100	-	800	kHz	---
Jitter							
F_{JTR}	Jitter frequency	-	-	50	-	Hz	C_{JTR} = 100nF
		-	-	500	-	Hz	C_{JTR} = 10nF
ΔF	Change in the switching frequency	-	±4.5	-	-	kHz	---
Hiccup Timer							
I_{hiccup}	Charging current	-	-	10	-	µA	---
ΔV	Voltage swing for hiccup timer	-	-	0.6	-	V	---
Temperature Foldback Circuit							
I_{NTC}	NTC current range	#	-	-	1.0	mA	---
N_{NTC}	I_{FDBK} / I_{NTC} current gain	-	-	0.13	-	-	I_{NTC} = 0.5mA
N_{T1}	I_{NTC} / I_{T1} current gain	-	-	3.0	-	-	I_{NTC} = 0.5mA
N_{T2}	I_{NTC} / I_{T2} current gain	-	-	6.0	-	-	I_{NTC} = 0.5mA
$V_{T1,}$ V_{T2}	T1 and T2 reference voltage	-	-	3.5	-	V	---
Output Short Circuit							
G_{FAULT}	Amplifier gain at IREF pin	-	1.8	2.0	2.2	-	V_{IREF} = 400mV
T_{OFF}	Propagation time for short circuit detection	-	-	-	250	ns	V_{IREF} = 400mV, FDBK steps from 0 - 1.0V; FLT goes from high to low
$T_{RISE,FAULT}$	Fault output rise time	-	-	-	300	ns	330pF capacitor at FLT pin
$T_{FALL,FAULT}$	Fault output fall time	-	-	-	200	ns	330pF capacitor at FLT pin
V_{MIN}	Minimum voltage at the output of the amplifier	#	250	-	-	mV	V_{IREF} = 0
T_{PWMD}	PWMD Blanking time	*	200	-	900	ns	---
Soft Start							
I_{SS}	Charging current	-	10	-	25	µA	---
I_{SS}	Discharging current	-	1.0	-	-	mA	V_{SS} = 5.0V
V_{SS}	Reset voltage	-	-	-	100	mV	---
Slope Compensation							
R_{SLOPE}	On-resistance of FET at CS pin	*	-	-	200	Ω	---

Notes:

* *Specifications apply over the full operating ambient temperature range of -40°C < T_A < +125°C. Guaranteed by design and characterization.*

\# *Specifications guaranteed by design and not tested in production*

Functional Block Diagram



Power Topology

The AT9917 is a closed-loop, switch-mode LED driver designed to control a buck, boost or SEPIC converter in a constant frequency mode. The IC includes an internal linear regulator, which operates from input voltages from 6.0 to 40V. The IC includes features typically required in LED drivers like open LED protection, output short circuit protection, linear and PWM dimming, and accurate control of the LED current. It also includes a thermal derating circuit which can be used to reduce the LED current at high temperatures to prevent a thermal runaway. A high current gate drive output enables the controller to be used in high power converters.

Power Supply to the IC (VIN, AVDD, PVDD)

The AT9917 can be powered directly from its VIN pin that takes a voltage up to 40V. When a voltage is applied at the VIN pin, the AT9917 tries to maintain a constant 5.0V(typ) at the AVDD pin. The regulator also has a built in under-voltage lockout which shuts off the IC if the voltage at the AVDD pin falls below the UVLO threshold. This linear regulator also provides the power supply to the built-in gate driver.

The AVDD pin must by bypassed by a low ESR capacitor (≥0.1µF) to provide a low impedance path for the high frequency current of the output gate driver. The PVDD pin is used to provide power to the gate driver. It should be bypassed with a low ESR capacitor (≥0.1µF), and should be shorted to the AVDD pin.

The input current drawn from the external power supply (or VIN pin) is a sum of the 2.0mA (max) current drawn by the all the internal circuitry and the current drawn by the gate driver (which, in turn, depends on the switching frequency and the gate charge of the external FET).

$$I_{IN} = 2mA + Q_G \bullet f_S$$

In the above equation, f_S is the switching frequency of the converter and Q_G is the gate charge of the external FET (which can be obtained from the FET datasheet).

The EN pin is a TTL compatible input used to disable the IC. Pulling the EN pin to GND will shut down the IC and reduce the quiescent current drawn by the IC to be less than 100µA. If the enable function is not required, the EN pin can be connected to AVDD.

Reference Voltage (REF)

The AT9917 provides a 1.25V reference voltage at the REF pin. This voltage is used to derive the various internal voltages required by the IC, and is also used to set the LED current externally. It should be bypassed with a low impedance (≥0.1µF) capacitor (0.01 -0.1µF).

Timing Resistor (RT)

The switching frequency of the converter is set by connecting a resistor between RT and GND. The resistor value can be determined as:

$$R_T = \frac{1.0}{f_S \bullet 9.5pF}$$

Current Sense (CS)

The current sense input is used to sense the source current of the switching FET. The CS input of the AT9917 includes a built in 100ns (minimum) blanking time to prevent spurious turn off due to the initial current spike when the FET turns on.

The IC includes an internal resistor divider network, which steps down the voltage at the COMP pins by a factor of 15. This voltage is used as the reference for the current sense comparators. Since the maximum voltage of the COMP pin is AV_{DD}, this voltage determines the maximum reference current for the current sense comparator and thus the maximum inductor current.

The current sense resistor R_{CS} should be chosen so that the input inductor current is limited to below the saturation current level of the input inductor. For discontinuous conduction mode of operation, no slope compensation is necessary. In this case, the current sense resistor is chosen as:

$$R_{CS} = \frac{AV_{DD} - 0.8V}{15 \bullet I_{SAT}}$$

where I_{SAT} is the maximum desired peak inductor current.

For continuous conduction mode converters operating in the constant frequency mode, slope compensation becomes necessary to ensure stability of the peak current mode controller, if the operating duty cycle is greater than 0.5. This factor must also be accounted for when determining R_{CS} (see Slope Compensation section).

Slope Compensation

Choosing a slope compensation, which is one half of the down slope of the inductor current, ensures that the converter will be stable for all duty cycles.

Slope compensation in the AT9917 can be programmed by two external components (see Fig. 1). A resistor from AVDD

sets a current (which is almost constant since the AVDD voltage is much larger than the voltage at the CS pin). This current flows into the capacitor and produces a ramp voltage across the capacitor. The voltage at the CS pin is then the sum of the voltage across the capacitor and the voltage across the current sense resistor, with the voltage across the capacitor providing the required slope compensation. When the GATE turns off, an internal pull down FET discharges the capacitor. The 200Ω(max) resistance of the internal FET will prevent the voltage at the CS pin from going all the way to zero. The minimum value of the voltage will instead be:

$$V_{CS,MIN} = \frac{AV_{DD}}{R_{SC}} \bullet 200\Omega$$

The slope compensation capacitor is chosen so that it can be completely discharged by the internal 200Ω(max) FET at the CS pin during the time the FET is off. Assuming the worst case switch duty cycle of 93%,

$$C_{SC} = \frac{0.07}{3 \bullet 200\Omega \bullet f_S}$$

Assuming a down slope of DS (A/µs) for the inductor current, the current sense resistor and the slope compensation resistor can be computed as:

$$R_{CS} = \frac{AV_{DD} - 0.8V}{15} \bullet \frac{1}{\left\{\frac{DS \bullet 10^6 \bullet 0.93}{2 \bullet f_S}\right\} + I_{SAT}}$$

$$R_{CS} = \frac{2 \bullet AV_{DD}}{DS \bullet 10^6 \bullet C_{SC} \bullet R_{CS}}$$

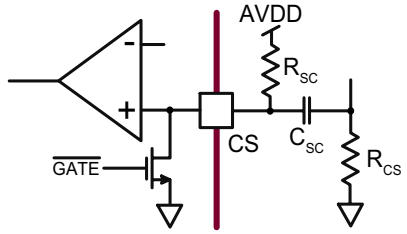


Figure 1: Slope Compensation

Gate Driver Output (GATE, PGND)

The GATE output of the AT9917 is used to drive the gate of the switching FET. The PGND pin should be connected to the GND connection of the current sense resistor and the two grounds of the IC (PGND and GND) should be connected together at the input GND connection to minimize noise.

FLT Output

The FLT pin is used to drive a disconnect FET while driving boost and SEPIC converters. In the case of boost converters, when there is a short circuit fault at the output, there is a direct path from the input source to ground which can cause high currents to flow. The disconnect switch is used to interrupt this path and prevent damage to the converter.

The disconnect switch also helps to disconnect the output filter capacitors for the boost and SEPIC converters from the LED load during PWM dimming and enables a very high PWM dimming ratio.

Control of the LED Current (IREF, FDBK and COMP)

The LED current in the AT9917 is controlled in a closed-loop manner. The current reference which sets the LED current at the IREF pin is set by using a resistor divider from the REF pin (or can be set externally with a low voltage source). This reference voltage is compared to the voltage at the FDBK pin, which senses the LED current in the current sense resistor. The AT9917 includes a 1.0MHz transconductance amplifier with a tri-state output, which is used to close the feedback loops and provide accurate current control. The compensation network is connected at the COMP pin.

The output of the op-amp is buffered and connected to the current sense comparator using a 14R:1R resistor divider.

The output of the op-amp is also controlled by the signal applied to the PWMD pin. When PWMD is high, the output of the op-amp is connected to the COMP pin. When PWMD is low, the output is left open. This enables the integrating capacitor to hold the charge when the PWMD signal has turned off the gate drive. When the IC is enabled, the voltage on the integrating capacitor will almost instantaneously force the converter into a steady state.

Linear Dimming

Linear dimming can be accomplished in the AT9917 by varying the voltages at the IREF pin. Note that since the AT9917 is a peak current mode controller, it has a minimum on-time for the GATE output. This minimum on-time will prevent the converter from completely turning off even when the IREF pin is pulled to GND. Thus, linear dimming cannot accomplish true zero LED current. To get zero LED current, PWM dimming has to be used.

Due to the offset voltage of the short circuit comparator, as well as the non-linearity of the X2 gain stage, pulling the IREF pin very close to GND might cause the internal short circuit comparator to trigger and shut down the IC. To overcome this, the output of the gain stage is limited to 250mV

(minimum), allowing the IREF pin to be pulled all the way to 0V without triggering the short circuit comparator. Therefore, the minimum voltage for a short circuit detection is 250mV.

PWM Dimming (PWMD)

PWM dimming in the AT9917 can be accomplished using a TTL-compatible square wave source at the PWMD pin.

When the PWM signal is high, the GATE and FLT pins are enabled and the output of the transconductance op-amp is connected to the external compensation network. Thus, the internal amplifier controls the output current. When the PWMD signal goes low, the output of the transconductance amplifier is disconnected from the compensation network. Thus, the integrating capacitor maintains the voltage across it. The GATE is disabled, so the converter stops switching and the FLT pin goes low, turning off the disconnect switch.

Note that disconnecting the LED load during PWM dimming causes the energy stored in the inductor to be dumped into the output capacitor. The filter capacitor that is chosen should be large enough so that it can absorb the inductor energy without significant change of the voltage across it. If the capacitor voltage change is significant, it would cause a turn-on spike in the inductor current when PWMD goes high.

Jitter and Hiccup Timer (JTR)

The JTR pin is a multipurpose pin in the AT9917. It is used to set the jitter frequency (frequency at which the switching frequency swings between its limits). It is also used to set the hiccup time for fault conditions.

The value of the capacitor required for the jitter frequency is given by:

$$C_{JTR} = \frac{5.0\mu F}{F_{JTR}(Hz)}$$

Note that the jitter frequency must be chosen to be significantly lower than the cross over frequency of the closed loop control. If not, the controller will not be able to reject the jitter frequency and the LED current will have a current ripple at the jitter frequency.

The same capacitor is used to determine the hiccup time. The hiccup time is computed as:

$$t_{HICCUP} = \frac{C_{JTR} \bullet 0.6V}{10\mu A}$$

If the hiccup time is lower than desired, the capacitor at the pin can be increased at the cost of a lower jitter frequency.

Fault Conditions

The AT9917 is a robust controller which can protect the LEDs and the LED driver in case of fault conditions. The AT9917 includes both open LED protection and output short circuit protection. In both cases, the AT9917 shuts down and attempts a restart. The hiccup time is programmed by the capacitor at the JTR pin.

When a fault condition is detected, both GATE and FLT outputs are disabled, the COMP pins and JTR pins are pulled to GND. Once the voltage at the JTR pin falls below 0.1V and the fault condition(s) have disappeared, the capacitor at the JTR pin is released and is charged slowly by a 10µA current source. Once the capacitor is charged to 0.7V, the COMP pins are released and GATE and FLT pins are allowed to turn on. If the hiccup time is long enough, it will ensure that the compensation networks are all completely discharged and that the converters start at minimum duty cycle.

Short Circuit Protection

When a short circuit condition is detected (output current becomes higher than twice the steady state current), the GATE and FLT outputs are pulled low. As soon as the disconnect FET is turned off, the output current goes to zero and the short circuit condition disappears. At this time, the hiccup timer is started. Once the timing is complete, the converter attempts to restart. If the fault condition still persists, the converter shuts down and goes through the cycle again. If the fault condition is cleared (due to a momentary output short) the converter will start regulating the output current normally. This allows the LED driver to recover from accidental shorts without having to reset the IC.

During short circuit conditions, there are two conditions that determine the hiccup time.

The first is the time required to discharge the compensation capacitors. Assuming a pole-zero R-C network at the COMP pin (series combination of R_Z and C_Z in parallel with C_C),

$$t_{COMP} = 3 \bullet R_Z \bullet C_Z$$

In case the compensation networks are only type 1 (single capacitor), then:

$$t_{COMP} = 3 \bullet 300\Omega \bullet C_C$$

The second is the time required for the inductors to completely discharge following a short circuit. This time can be computed as:

$$t_{IND} = \frac{\pi}{4} \sqrt{L \bullet C_O}$$

where L and Co are the input inductor and output capacitor of the power stage.

The hiccup time is then chosen as:

$$t_{HICCUP} > max\ (t_{COMP},\ t_{IND})$$

Note that the power rating of the LED sense inductor has to be chosen properly if it has to survive a persistent fault condition. The power rating can be determined using:

$$P_{RS} \geq \frac{I^2_{SAT} \bullet R_S \bullet (t_{fall,fault} + t_{OFF})}{t_{HICCUP}}$$

Where I_{SAT} is the saturation current of the disconnect FET. In case of the AT9917, ($t_{fall,fault}$ + t_{OFF}) is 450ns (max).

False Triggering of the Short Circuit Comparator During PWM Dimming

During PWM dimming, the parasitic capacitance of the LED string might cause a spike in the output current when the disconnect FET is turned on. If this spike is detected by the short circuit comparator, it will cause the IC to falsely detect an over current condition and shut down.

In the AT9917, to prevent these false triggerings, there is a built in 500ns blanking network for the short circuit comparator. This blanking network is activated when the PWMD input goes high. Thus, the short circuit comparator will not see the spike in the LED current during the PWM dimming turn-on transition. Once the blanking timer has completed its task, the short circuit comparator will start monitoring the output current. Thus, the total delay time for detecting a short circuit will depend on the condition of the PWMD input.

If the output short circuit exists before the PWM dimming signal goes high, the total detection time will be:

$$t_{DETECT1} = t_{PWMD} + t_{fall,\ fault} + t_{OFF} \approx 950ns(max)$$

If the short circuit occurs when the PWM dimming signal is already high, the time to detect will be:

$$t_{DETECT1} = t_{fall,\ fault} + t_{OFF} \approx 450ns(max)$$

Over Voltage Protection

The AT9917 provides hysteretic over voltage protection. allowing the IC to recover in case the LED load is momentarily disconnected.

When the load is disconnected in a boost converter, the output voltage rises as the output capacitor starts charging. When the output voltage reaches the OVP rising threshold, the AT9917 detects an over voltage condition and turns off the converter. The converter is turned back on only when the output voltage falls below the falling OVP threshold (which is 10% lower than the rising threshold). This time is mostly dictated by the R-C time constant of the output capacitor C_O and the resistor network used to sense over voltage (R_{OVP1} + R_{OVP2}). In case of a persistent open circuit condition, this cycle maintains the output voltage within a 10% band.

In most designs, the lower threshold voltage of the over voltage protection (V_{OVP} -10%) at which point the AT9917 attempts to restart will be more than the LED string voltage. Thus, when the LED load is reconnected to the output of the converter, the voltage differential between the actual output voltage and the LED string voltage will cause a spike in the output current. This causes a short circuit to be detected and the AT9917 will trigger short circuit protection. This behavior continues until the output voltage becomes lower than the LED string voltage, at which point no fault will be detected and normal operation of the circuit will commence.

Thermal Derating

The reference voltage used to set the LED current is programmed using two resistors - R_{r1} and R_{r2} connected as shown in Figure 2.

$$I_O \bullet R_S = V_{REF} \bullet \frac{R_{r2}}{R_{r1} + R_{r2}}$$

where I_O is the output LED current and R_S is the current sense resistor.

Thermal derating is programmed using 4 pins - NTC, DIV, T1 and T2. When no temperature foldback is required, NTC and T1 should be connected to AVDD, and DIV should be connected to GND. T2 still requires a resistor to GND (10~100kΩ). No pins should be left floating (Figure 2).

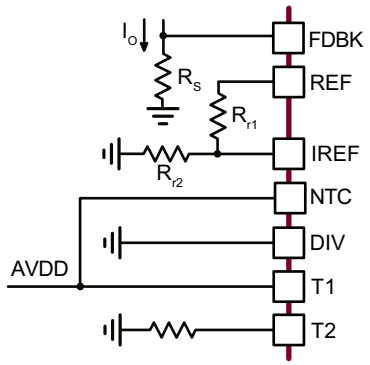


Figure 2: No Thermal Derating

When thermal derating needs to be implemented, four resistors are used to set the various points to obtain the thermal derating curve shown in Figure 3.

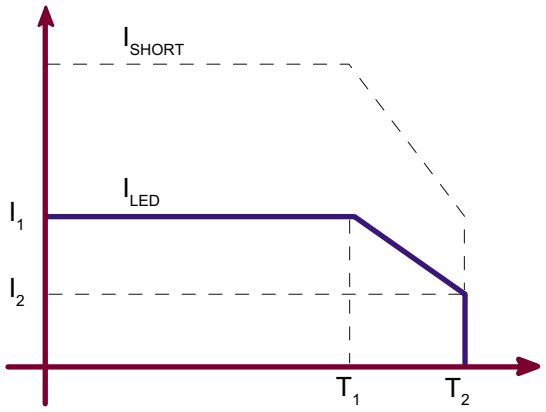


Figure 3: Thermal Derating Curve

When an external NTC resistor is connected (Figure 4), both temperatures T_1 and T_2, as well as the current I_2 can be accurately programmed to maximize the light output of the LED lamp.

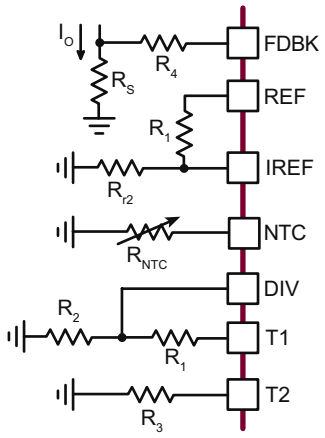


Figure 4: With Thermal Derating

The ratio of the resistor divider $R_2/(R_1 + R_2)$ programs the voltage at the NTC pin. The voltage V_{T1} at T1 is approximately 3.5V. The current sourced by NTC and T1 is mirrored out of FDBK in accordance with the following equation:

$$I_{FDBK} = \frac{4}{30}(I_{NTC} - 3I_{T1})$$

when:

$$I_{NTC} > 3 \bullet I_{T1}.$$

I_{NTC}, I_{T1}, and I_{T2} are the currents sourced from pins NTC, T1, and T2 respectively.

Temperature T_1 is programmed by selecting R_2 such that:

$$R_2 = 3 \bullet R_{NTC}(T_1)$$

where $R_{NTC}(T_1)$ is resistance of the NTC resistor at the temperature T_1.

R_1 can be computed using the maximum current (≤1.0mA) that will flow through the NTC resistor at temperature T_2.

$$R_1 = \frac{V_{T1}}{I_{NTC,MAX}} \bullet \left\{ \frac{R_2}{R_{NTC(T2)}} \right\} - R_2$$

Further reduction of the NTC resistance R_{NTC} will create a proportional offset of the current feedback reference at FDBK, and hence will cause decrease of the LED current. To program the desired current I_2 at the temperature T_2, resistor R_4 at FDBK can be calculated as:

$$R_4 = \frac{(I_1 - I_2) \bullet R_S \bullet (R_1 + R_2)}{V_{T1} \bullet \frac{4}{30} \left\{ \frac{R_2}{R_{NTC(T2)}} - 3.0 \right\}}$$

The turn off of the converter at the maximum temperature is programmed using R_3.

$$R_3 = \frac{6 \bullet (R_1 + R_2)}{\left\{ \frac{R_2}{R_{NTC(T2)}} - 3.0 \right\}}$$

The over-temperature recovery threshold is independent of the current in T_2. AT9917 recovers from thermal shutdown at the break temperature T_1, where:

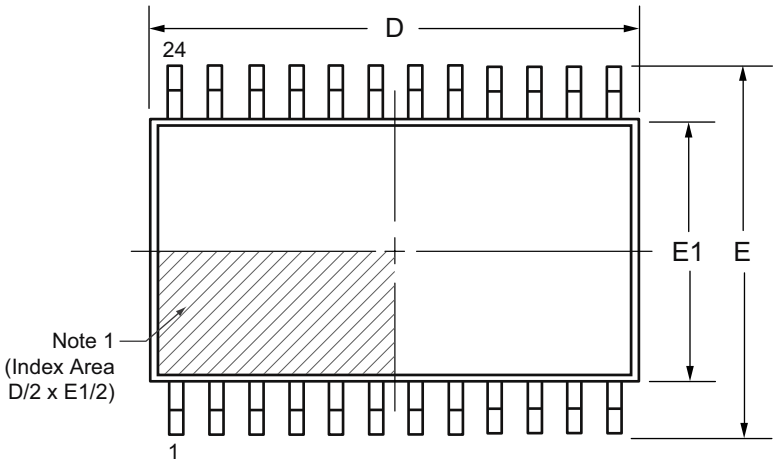
$$I_{NTC} < 3 \bullet I_{T1}.$$

Pin Description

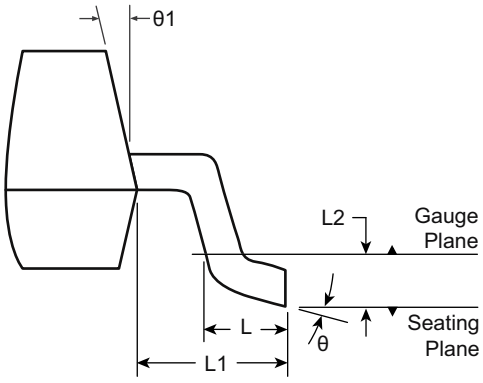
Pin #	Name	Description
1	VIN	This pin is the input of a 40V high voltage regulator.
2	AVDD	This is a power supply pin for all internal circuits. It must be bypassed with a low ESR capacitor to GND (at least 0.1µF).
3	PVDD	This is the power supply pin for the gate driver. It should be connected externally to AVDD and bypassed with a low ESR capacitor to PGND (at least 0.1µF).
4	GATE	This pin is the output gate driver for an external logic level N-channel power MOSFET.
5	PGND	Ground return for the gate drive circuitry.
6	GND	Ground return for all the low power analog internal circuitry. This pin must be connected to the return path from the input.
7	JTR	This pin controls the jitter of the clock programmed by a capacitor connected at this pin. This capacitor also determines the hiccup time.
8	RT	This pin sets the frequency of the power circuit. A resistor between RT and GND will program the circuit in constant frequency mode.
9	CS	This pin is used to sense the source current of the external power FET. It includes a built-in 100ns (min) blanking time. Slope compensation is implemented by connecting an RC network to this pin as shown in the Typical Application.
10	OVP	This pin provides the over voltage protection for the converter. When the voltage at this pin exceeds 1.25V, the gate output of the AT9917 is turned off and FLT goes low. Switching is enabled when the voltage at this pin goes below 1.125V.
11	T2	This current programs the temperature at which the driver is shut off due to over temperature conditions for the LED.
12	T1	This current input programs the break temperature threshold which determines the start of the current derating when using the external NTC resistor.
13	RNTC	Connect an external NTC resistor to this pin for temperature fold-back of the output current.
14	DIV	Programs the voltage input for the transconductance at NTC pin.
15	FLT	This pin is pulled to ground when there is an output short circuit condition or output over voltage condition. This pin can be used to drive an external MOSFET in the case of boost converters to disconnect the load from the source. It is also controlled by the PWM dimming input to provide excellent PWM dimming response.
16	PWMD	When this pin is pulled to GND (or left open), switching of the AT9917 is disabled. When an external TTL high level is applied to it, switching will resume.
17	SS	Connecting a capacitor from this pin to GND programs the soft start time of the LED driver.
18	COMP	Stable closed loop control can be accomplished by connecting a compensation network between COMP and GND. This pin is discharged upon detection of a fault condition and on startup.
19	IREF	The voltage at this pin sets the output current level. The current reference can be set using a resistor divider from the REF pin.
20	FDBK	This pin provides output current feedback to the AT9917 by using a current sense resistor. A resistor in series with the FDBK pin can be used to reduce the current at elevated temperatures.
21	NC	No connection.
22	NC	
23	EN	Pulling EN to GND causes the AT9917 to go into a low current standby mode. A voltage greater than 2.0V will cause the IC to start up.
24	REF	This pin provides accurate reference voltage. It must be bypassed with a 0.01µF -0.1µF capacitor to GND.

24-Lead TSSOP Package Outline (TS)

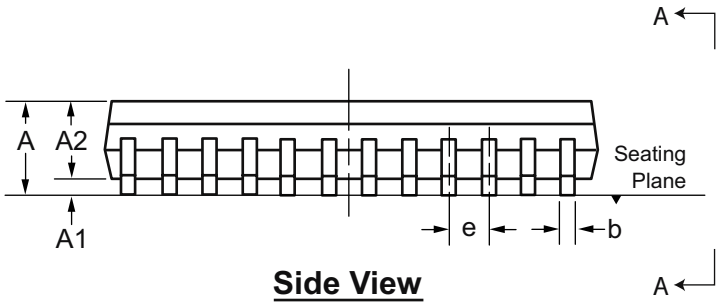
7.80x4.40mm body, 1.20mm height (max), 0.65mm pitch



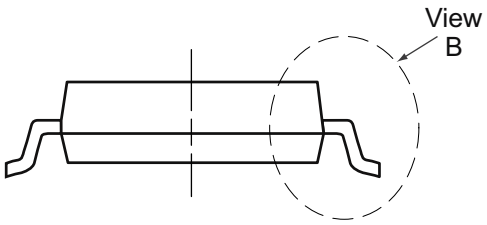
Top View



View B



Side View



View A-A

Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	L	L1	L2	θ	θ1
Dimension (mm)	MIN	0.85*	0.05	0.80	0.19	7.70	6.20*	4.30	0.65 BSC	0.45	1.00 REF	0.25 BSC	0°	12° REF
	NOM	-	-	1.00	-	7.80	6.40	4.40		0.60			-	
	MAX	1.20	0.15	1.15†	0.30	7.90	6.60*	4.50		0.75			8°	

JEDEC Registration MS-153, Variation AD, Issue F, May 2001.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings are not to scale.
***Supertex** Doc. #: DSPD-24TSSOPTS, Version B041309.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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