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Automotive Boost-Buck LED Lamp Driver IC

Features

- Constant output current
- Steps output voltage up or down
- Very low susceptibility to Input voltage transients
- Frequency jitter
- Externally programmable fixed switching frequency
- Temperature foldback with external NTC resistor
- Internal 40V voltage regulator
- +/-1A MOSFET gate driver
- Short LED protection
- Open LED protection
- Input undervoltage protection
- Enable & PWM dimming
- Trimmed reference (±3% accurate)
- AEC-Q100 compliant

Applications

- Automobile lighting
- Battery powered LED lamps
- Other low voltage AC/DC or DC/DC LED drivers

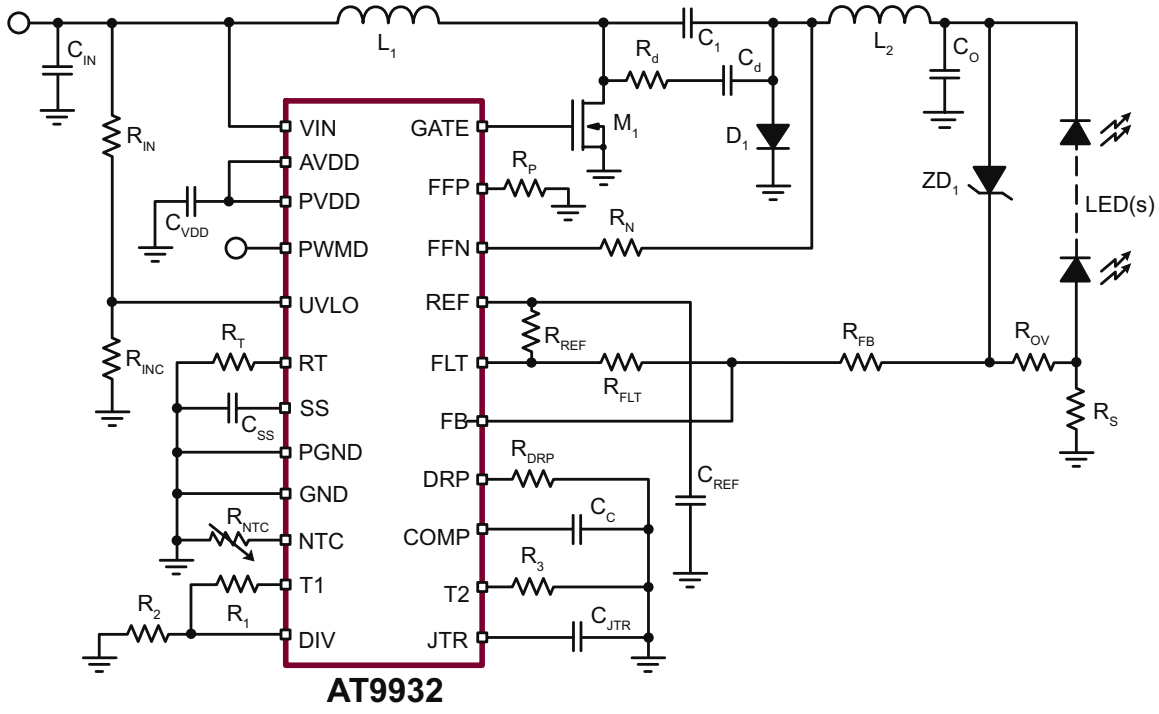
General Description

The AT9932 is an advanced fixed frequency PWM controller IC designed to control an LED lamp driver using a boost-buck topology that can step the input voltage up or down automatically. The IC provides fast output current transient response and very low susceptibility to input voltage transients, which allows the lamp driver to pass the rigorous electrical transient requirements of SAE J1455 or ISO 7637-2, making the AT9932 an ultimate solution for automobile lighting. Capacitive isolation protects the LED Lamp from failure of the switching MOSFET.

The AT9932 features a unique feed-forward current control scheme, differential output current sensing, soft start, protection from short or open LED load. Switching frequency can be programmed with a single external resistor.

The AT9932 includes a temperature fold-back of the output current using an external NTC resistor. This feature allows maximizing the light output of the LED load over the entire operating temperature range.

Typical Application Circuit



Ordering Information

Device	24-Lead TSSOP *7.80x4.40mm body* *1.20mm height (max)* *0.65mm pitch*
AT9932	AT9932TS-G

-G indicates package is RoHS compliant ('Green')

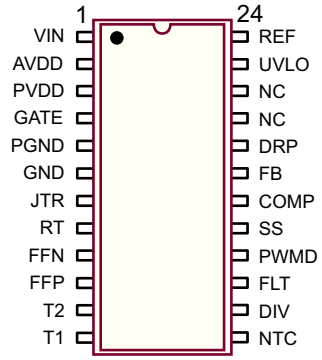
Absolute Maximum Ratings

Parameter	Value
VIN to GND	-0.5V to +45V
PVDD, AVDD to GND voltage	-0.3V to +6.0V
GATE to GND voltage	-0.3V to (PVDD+0.3V)
All other pins to GND voltage	-0.3V to (AVDD+0.3V)
FFN, FFP current	+2.0mA
REF current	+5.0mA
Continuous Power Dissipation (T_A = +25°C)	1000mW*
Junction temperature	-40°C to +150°C
Storage temperature range	-65°C to +150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* $R_{\theta JA}$ = 125°C/W (max.)

Pin Configuration



24-Lead TSSOP (TS)
(top view)

Product Marking

YY = Year Sealed
WW = Week Sealed
L = Lot Number
C = Country of Origin*
A = Assembler ID
_____ = "Green" Packaging
**May be part of ejector pin*

Package may or may not include the following marks: Si or

24-Lead TSSOP (TS)

Electrical Characteristics

(Specifications are at T_A = 25°C, V_{IN} = 12V, V_{PWMD} = UVLO = AVDD = PVDD, GATE open, R_T = 200KΩ, C_{REF} = 0.1µF, C_{AVDD} = C_{PVDD} = 1.0µF, I_{T1} = I_{T2} = 100µA unless otherwise noted.)

Sym	Parameter		Min	Typ	Max	Units	Conditions
Input							
V_{IN}	Input DC supply voltage range	-	5.3	-	40	V	---
I_{INEN}	Input supply current	*	-	-	2.0	mA	PWMD = GND
I_{INDIS}	Input current, UVLO mode	*	-	-	100	µA	UVLO = GND, PWMD = GND
Internal Regulator							
V_{DD}	Regulated output voltage	*	4.65	5.00	5.35	V	I_{DD} = 0 - 20mA, V_{IN} = 6.0 - 40V, PWMD = GND
$\Delta V_{DD,OFF}$	Hysteresis	-	-	250	-	mV	V_{DD} falling
$V_{DD,ON}$	Start voltage	*	4.25	-	4.85	V	V_{DD} rising

Notes:

* *Specifications apply over the full operating ambient temperature range of -40°C < T_A < +125°C. Guaranteed by design and characterization.*

Electrical Characteristics *(Specifications are at T_A = 25°C, V_{IN} = 12V, V_{PWMD} = UVLO = AVDD = PVDD, GATE open, R_T = 200KΩ, C_{REF} = 0.1µF, C_{AVDD} = C_{PVDD} = 1.0µF, I_{T1} = I_{T2} = 100µA unless otherwise noted.)*

Sym	Description		Min	Typ	Max	Units	Conditions
Reference							
V_{REF}	Reference output voltage	*	1.210	1.250	1.290	V	I_{REF} = 0
$V_{REF,DIS}$	Reference output voltage, UVLO mode	-	-	0	-	mV	UVLO = GND
ΔV_{REF}	Load regulation	-	0	-	2.0	mV	I_{REF} = 0 - 1.0mA
GATE Output							
t_R	Gate output rise time	-	-	20	35	ns	C_{GATE} = 4.0nF, V_{IN} = AVDD = PVDD = 5.0V
t_F	Gate output fall time	-	-	20	35	ns	
D_{MAX}	Maximum duty cycle	*	87	-	93	%	---
Feed-Forward Ramp Generator							
$t_{ON(MIN)}$	Minimum GATE ON time	*	250	-	400	ns	I_{FFN} = 500µA, I_{FFP} = 0, V_{COMP} = 3.5V
$t_{ON(MAX)}$	Maximum GATE ON time	*	6.0	-	13	µs	I_{FFN} = 10µA, I_{FFP} = 0, V_{COMP} = 3.5V
t_{ON}	GATE ON time	*	1.0	-	2.0	µs	I_{FFN} = 110µA, I_{FFP} = 10µA, V_{COMP} = 3.5V
$\Delta t_{ON}/t_{ON}$	FFN/FFP current balancing	#	-3.0	-	3.0	%	I_{FFN} = 100µA, I_{FFP} = 0, V_{COMP} = 3.5V
Transconductance Operation Amplifier							
V_{FB}, V_{DRP}	Input common-mode range	#	-0.3	-	3.0	V	---
V_{OS}	Input offset voltage	*	-9.0	-	9.0	mV	---
Gm	Transconductance	-	-	0.95	-	mA/V	---
A_V	Open loop voltage gain	-	65	-	-	dB	COMP open
G_B	Gain bandwidth product	#	1.0	-	-	MHz	C_{COMP} = 150pF
I_{COMP}	COMP sink current	#	0.2	-	-	mA	V_{FB} = 0.1V, COMP = GND
	COMP source current	#	-0.2	-	-	mA	V_{FB} = -0.1V, COMP = VDD
I_{BIAS}	Input bias current	#	-	0.5	1.0	nA	---
V_{COMP}	Output voltage range	#	0.7	-	V_{DD}	V	---
	Hiccup threshold	-	-	700	-	mV	---
I_{LEAK}	Output leakage current	#	-	0.5	1.0	nA	PWMD = GND
Oscillator							
f_{OSC1}	Output frequency	*	90	105	120	kHz	R_T = 1.0MΩ
f_{OSC2}		*	427	505	583	kHz	R_T = 200kΩ
f_{OSC}	Output frequency range	#	100	-	800	kHz	---

Notes:

* *Specifications apply over the full operating ambient temperature range of -40ºC < T_A < +125ºC. Guaranteed by design and characterization.*

\# *Specifications guaranteed by design and not tested in production*

Electrical Characteristics

(Specifications are at T_A = 25°C, V_{IN} = 12V, V_{PWMD} = UVLO = AVDD = PVDD, GATE open, R_T = 200KΩ, C_{REF} = 0.1µF, C_{AVDD} = C_{PVDD} = 1.0µF, I_{T1} = I_{T2} = 100µA unless otherwise noted.)

Sym	Description		Min	Typ	Max	Units	Conditions
Jitter							
F_{JTR}	Jitter frequency	-	-	50	-	Hz	C_{JTR} = 0.1µF
		-	-	500	-	Hz	C_{JTR} = 0.01µF
ΔF	Change in switching frequency	-	±4.5	-	-	kHz	---
Temperature Foldback Circuit							
I_{NTC}	NTC current range	#	-	-	1.0	mA	---
N_{NTC}	NTC to DRP current gain	-	-	0.13	-	-	I_{NTC} = 0.5mA
N_{T1}	NTC to T1 current gain	-	-	3.0	-	-	I_{NTC} = 0.5mA
N_{T2}	NTC to T2 current gain	-	-	6.0	-	-	I_{NTC} = 0.5mA
$V_{T1,}$ V_{T2}	T1 and T2 reference voltage	-	-	3.5	-	V	---
Soft Start							
$I_{SS,CHG}$	Charging current	-	10	-	25	µA	---
$I_{SS,DIS}$	Discharging current	-	1.0	-	-	mA	V_{SS} = 5.0V
$V_{SS,RST}$	Reset voltage	-	-	-	100	mV	---
Fault Detect Comparator							
V_{FLT}	Trip voltage	-	-20	-	20	mV	---
I_{BIAS}	Input bias current	#	-	0.5	1.0	nA	---
Input Under Voltage Lockout							
ΔV_{UVLO}	Under voltage threshold hysteresis	-	-	200	-	mV	UVLO falling
$V_{UVLO,ON}$	Under voltage threshold	*	1.15	1.25	1.40	V	UVLO rising
I_{BIAS}	Input bias current	#	-	0.5	1.0	nA	---
PWM Dimming							
V_{EN}, V_{PWM}	Enable voltage level	*	2.0	-	-	V	---
	Disable voltage level	*	-	-	0.8	V	---
R_{PWMD}	Pull-down resistor	-	120	-	280	kΩ	---

Notes:

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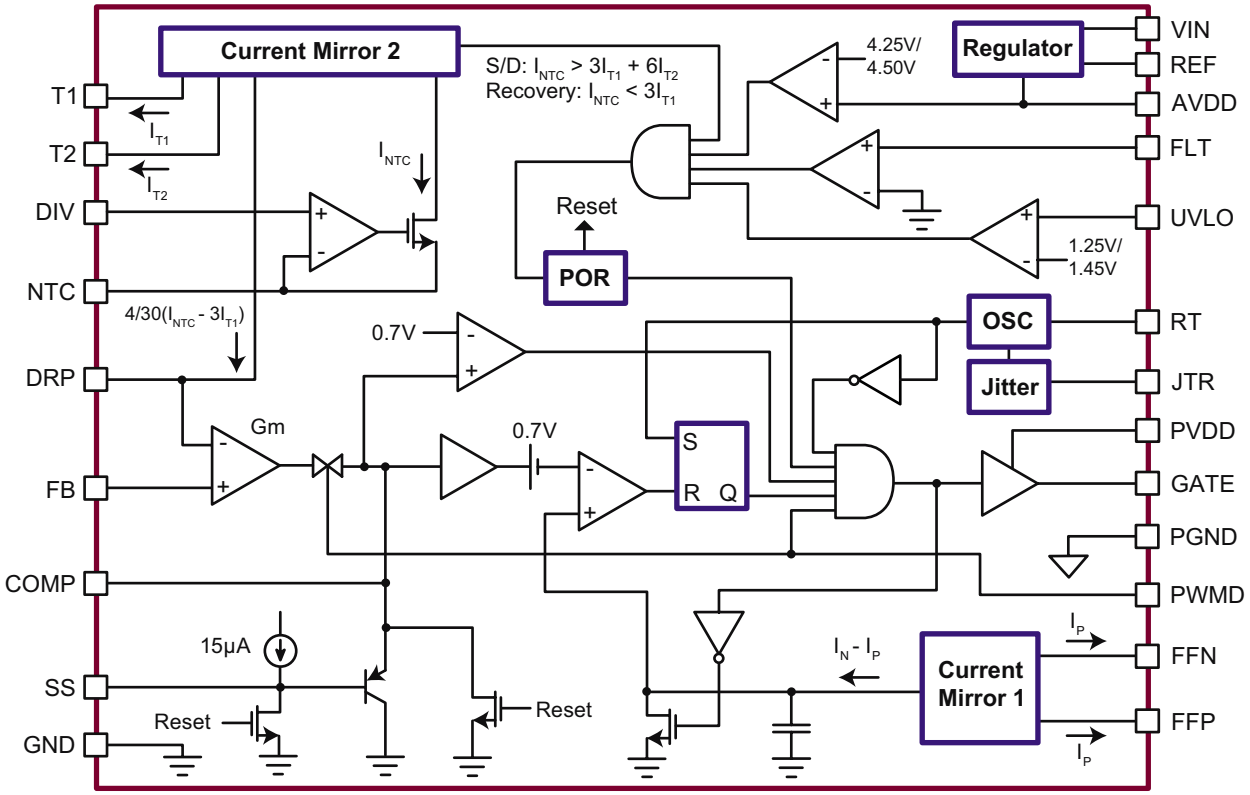
\# *Specifications guaranteed by design and not tested in production*

Functional Block Diagram



Functional Description

Power Topology

The AT9932 is optimized to drive a continuous conduction mode (CCM) boost-buck DC/DC converter topology commonly referred to as "Čuk converter". (See the circuit diagram on page 1.) This power converter topology offers numerous advantages useful for driving high-brightness light emitting diodes (HB LEDs). These advantages include step-up or step-down voltage conversion ratio and low input and output current ripple. The output load is decoupled from the input voltage with a capacitor, making the driver inherently failure-safe for the output load.

The AT9932 features an optimal control method for use with a boost-buck LED driver. This method achieves very low susceptibility to input voltage transients, which makes it indispensable for automotive LED lighting applications. The AT9932 can maintain constant output current even under vigorous input transient conditions. Its output current control loop is inherently stable and can be compensated using a single capacitor with the appropriate damping at the coupling capacitor.

Regulator (VIN, AVDD) and Gate Driver (GATE, PVDD)

The AT9932 can be powered directly from its VIN pin that takes a voltage up to 40V. When V_{IN} voltage is applied, AT9932 seeks to maintain constant voltage at the AVDD pin. When the under-voltage threshold is exceeded at AVDD, the gate driver is enabled after a 100µs power-on reset (POR) delay. The output of the gate driver (GATE) controls the gate of an external N-channel power MOSFET. The maximum duty cycle of the GATE signal is limited to 0.9(typ). The under voltage protection comparator disables it when the voltage falls below the under voltage threshold.

A separate PVDD input is provided to power the GATE output to decouple the high switching currents of the gate driver from AVDD. Both pins (AVDD, PVDD) must be wired together on the printed circuit board (PCB). AVDD needs to be bypassed to GND by a low ESR capacitor (≥0.1µF). PVDD needs to be bypassed to PGND by a low ESR capacitor (≥0.1µF).

The input current drawn from the external power supply (or VIN pin) is a sum of the 2.0mA (max) current drawn by the all the internal circuitry and the current drawn by the gate driver (which in turn depends on the switching frequency and the gate charge of the external FET).

$$I_{IN} = 2.0mA + Q_G \bullet f_S$$

In the previous equation, f_S is the switching frequency of the converter and Q_G is the gate charge of the external FET (which can be obtained from the FET datasheet).

Timing Resistor (RT)

The switching frequency f_S is programmed by selecting an external sense resistor R_T. The resistance value can be computed as:

$$R_T = \frac{1}{f_S \bullet C_T}$$

where C_T = 9.5pF.

Jitter (JTR)

Clock frequency can be modulated by an externally programmed saw-tooth wave shape to reduce conducted electro-magnetic emission (EMI) from the LED driver. The deviation of the oscillator frequency is set internally to ±5.0kHz. The modulation frequency is programmed by connecting a capacitor at JTR. The value of the capacitor required for the jitter frequency is given by:

$$C_{JTR} = \frac{5\mu F}{F_{JTR}(Hz)}$$

Note that the jitter frequency must be chosen to be significantly lower than the cross over frequency of the closed loop control. If not, the controller will not be able to reject the jitter frequency and the LED current will have a current ripple at the jitter frequency.

Reference Voltage (REF)

The AT9932 provides a 1.25V reference voltage at the REF pin. This voltage is used to derive the various internal voltages required by the IC and is also used to set the LED current externally. It should be bypassed with a low impedance capacitor (0.01 -0.1µF).

Internal 1.0MHz Transconductance Amplifier

The AT9932 includes a 1.0MHz transconductance amplifier, which can be used to close the LED current feedback loop. The output state of the amplifier is controlled by the signal applied to the PWMD pin. When PWMD is high, the output of the amplifier is connected to the COMP pin. When PWMD is low, COMP is left open. This enables the integrating capacitor at the COMP pin to hold its charge when the PWMD signal has turned off the gate drive. When the IC is enabled, the voltage at COMP will be positioned for the converter to return to its steady state condition.

When the voltage at COMP falls below 700mV, the GATE output is disabled. This feature reduces power dissipation in the Zener diode ZD_1 during open circuit condition.

Soft Start (SS)

The soft start feature can determine the initial ramp-up of the error voltage at the COMP pin. Connecting a single capacitor between SS to GND can program the soft-start time. Upon the first applying voltage to the VDD pin, a current of 15µA is supplied from the SS pin gradually charging the soft start capacitor. The COMP voltage is tracking the voltage at the SS pin until regulation of the output current is reached. When V_{DD} falls below the under-voltage threshold, the soft start capacitor is discharged rapidly.

Feed-Forward Ramp Generator (FFP, FFN) and PWM Comparator

The heart of the AT9932 is the feed-forward circuit having two inputs: FFN and FFP. This circuit generates a voltage ramp proportional to the difference between the FFN and FFP currents.

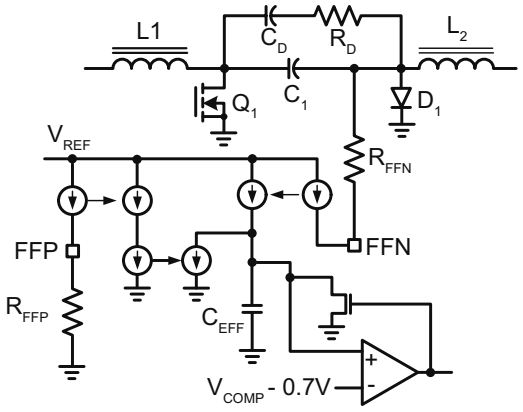


Figure 1. Feed-Forward Ramp Generator

As shown in Fig. 1, the resistor R_{FFN} is connected between FFN and the negative terminal of the coupling capacitor C1. A resistor of the same value (R_{FFP} = R_{FFN}) is connected between FFP and GND. The on-time of the GATE output can be computed as:

$$t_{ON} = \frac{R_{FFN} \bullet C_{EFF} \bullet (V_{COMP} - 0.7V)}{V_{C1}}$$

where C_{EFF} = 50pF±40%, V_{COMP} is the COMP voltage, and V_{C1} is the voltage across the coupling capacitor C_1.

The duty cycle of a continuous conduction mode boost-buck converter is given as:

$$D = t_{ON} \bullet f_S = \frac{V_{OUT}}{V_{C1}} = \frac{V_{OUT}}{V_{OUT} + V_{IN}}$$

where V_{IN} is the input supply voltage, and V_{OUT} is the forward voltage of the LED string. Since the output voltage at COMP is limited to $V_{COMP} = V_{DD}$, the feed-forward resistors must be selected in accordance with:

$$R_{FFN} = R_{FFP} \geq \frac{V_{OUT}}{C_{EFF} \bullet f_S \bullet (V_{DD} - 0.7V)}$$

Otherwise, the steady-state duty cycle D will not be reached, and the LED driver will be unable to develop the desired current.

The feed-forward loop provides instantaneous response to any transient at C_1, and therefore achieves excellent rejection of the input voltage transients along the supply line. It is inherently stable with proper selection of the damping network R_d and C_d. Optimal selection of R_d and C_d is complex. However, the worst case design of the damping circuit can be performed under the assumption that $V_{OUT(MAX)} >> V_{IN(MIN)}$ for most automotive applications of the AT9932. The simplified equations given below produce very good results under this assumption.

$$C_d = \frac{9D_{MAX}}{(1 - D_{MAX})} \bullet \frac{L_1 \bullet I_O^2}{V_{IN(MIN)}}$$

$$R_d = \frac{V_{IN(MIN)}}{3D_{MAX} I_O}$$

In the cases where the above assumption is not valid, the equations for R_d and C_d could still be used. However, they may produce somewhat too conservative results. Power dissipation in the damping resistor R_d can be computed as:

$$P_{Rd} = \frac{\Delta V_{C1}^2}{12 \bullet R_d}$$

where:

$$\Delta V_{C1} = \frac{I_{OUT} \bullet D}{f_S \bullet C_1}$$

is the peak-to-peak voltage ripple at the coupling capacitor C_1.

Output Over Voltage Protection

The AT9932 LED lamp driver supplies constant current to the load. Therefore, an output circuit protection is needed to prevent dramatic failures when the output load fails open. A simple addition of a Zener diode (ZD_1 in the Typical Application Circuit on page 1) will limit the output voltage when the output LED connection is lost.

Programming LED Current and Temperature Foldback

The AT9932 offers a temperature foldback feature that allows programming the output current in accordance with the temperature derating characteristics provided by the LED manufacturers. A typical derating curve is shown in Figure 2.

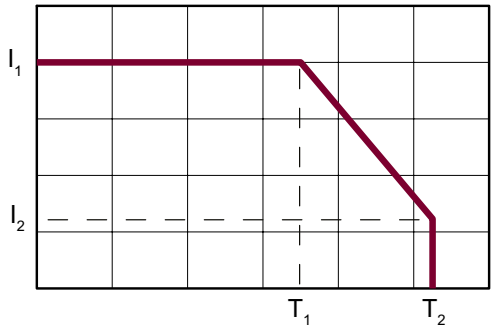


Figure 2. Temperature Derating Curve of LED Current

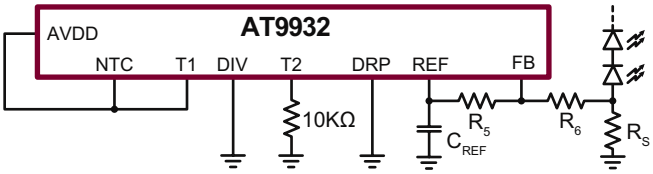


Figure 3. Output Current Feedback without Temperature Foldback

When no temperature foldback is required, NTC and T1 should be connected to AVDD, DIV and DRP should be connected to GND. T2 still requires a resistor to GND (10~100kΩ). No pins should be left floating. The DRP pin can be connected to GND (Figure 3). In this case, the output current of the AT9932 LED driver is programmed using the following equation:

$$I_1 = \frac{V_{REF}}{R_S} \bullet \frac{R_6}{R_5}$$

where V_{REF} is voltage at the REF pin (V_{REF} = 1.25V).

The same equation for calculating I_1 is used when temperature fold-back is required, to calculate the current below T_1.

When an external NTC resistor is connected (Figure 4), both temperatures T_1 and T_2, as well as the current I_2 can be accurately programmed to maximize the light output of the LED lamp.

The ratio of the resistor divider $R_2/(R_1 + R_2)$ programs the voltage at the NTC pin. The voltage at T1 is approximately 3.5V. The currents sourced by NTC and T1 are mirrored into DRP in accordance with the following equation:

$$I_{DRP} = \frac{I_{NTC}}{3} - I_{T1} > 0$$

No current is sourced from DRP when $I_{NTC} < 3 \cdot I_{T1}$.

Temperature T_1 is programmed by selecting R_2 such that:

$$R_2 = 3R_{NTC}(T_1)$$

where $R_{NTC}(T_1)$ is the resistance of the NTC resistor at the temperature T_1.

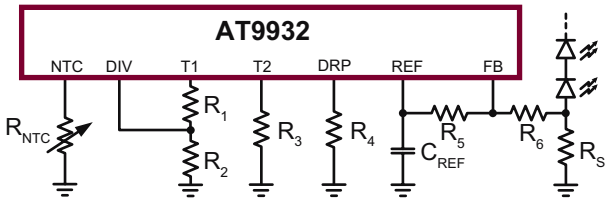


Figure 4. Output Current Feedback with Temperature Foldback

Further reduction of the NTC resistance R_{NTC} will create a proportional offset of the current feedback reference at DRP, and hence will cause decrease of the LED current. To program the desired current I_2 at the temperature T_2, the resistor R_4 at DRP can be calculated as:

$$R_4 = \frac{30}{4} \cdot \frac{V_{REF}}{V_{T1}} \cdot \frac{R_{NTC}(T_2)(R_1 + R_2)}{R_2 - 3R_{NTC}(T_2)} \cdot \frac{R_6 - \frac{I_2 \cdot R_S}{V_{REF}} \cdot R_5}{R_5 + R_6}$$

where $R_{NTC}(T2)$ is resistance of the NTC resistor at the temperature T_2, and V_{T1} is voltage at the T1 pin ($V_{T1} \approx 3.5V$).

When the current from the NTC pin exceeds ($3 \cdot I_{T1} + 6 \cdot I_{T2}$), over-temperature shutdown is triggered. The voltage at T2 is approximately equal to the voltage at T1. Selecting resistance of R_3 at the T2 pin programs the desired shutdown temperature T_2.

$$R_3 = \frac{6R_{NTC}(T_2) \cdot (R_1 + R_2)}{R_2 - 3R_{NTC}(T_2)}$$

The over-temperature recovery threshold is independent of the current in T2. The AT9932 recovers from thermal shutdown at the break temperature T_1, where:

$$I_{NTC} < 3 \cdot I_{T1}$$

Input Under Voltage Protection (UVLO)

To protect the AT9932 against excessive input current at low input supply voltage, the under-voltage lockout (UVLO) protection comparator input is provided. Connecting a resistor divider between VIN and GND programs the UVLO thresholds as follows:

$$V_{IN(START)} = \frac{(R_{IN1} + R_{IN2}) \cdot 1.25V}{R_{IN2}}$$

$$V_{IN(STOP)} = 0.84 \cdot V_{IN(START)}$$

The hysteresis is provided to prevent oscillation.

The AT9932 becomes disabled and draws less than 100µA of current from VIN or VDD when the UVLO pin voltage falls below the threshold. The 1.25V reference at the REF pin becomes 0V at this condition. Hence, the UVLO input can be also used as a low stand-by power disable input.

Fault Comparator (FLT)

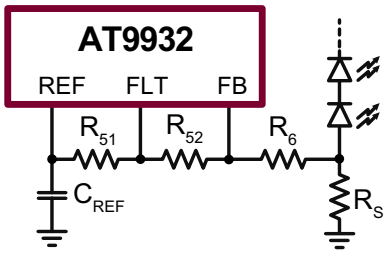


Figure 5. Output Short Circuit Protection

The AT9932 also provides an internal protection comparator that can be used for protection against short and open LED string conditions. When the voltage at the FLT input falls below the GND potential, the AT9932 shuts down. The soft-start capacitor at SS is discharged. Switching resumes automatically after a POR delay.

Configuring the FLT input to protect against a short LED string is illustrated by Figure 5. The short circuit current can be calculated as:

$$I_{SHORT} = \frac{V_{REF}}{R_S} \cdot \frac{R_6 + R_{52}}{R_{51}}$$

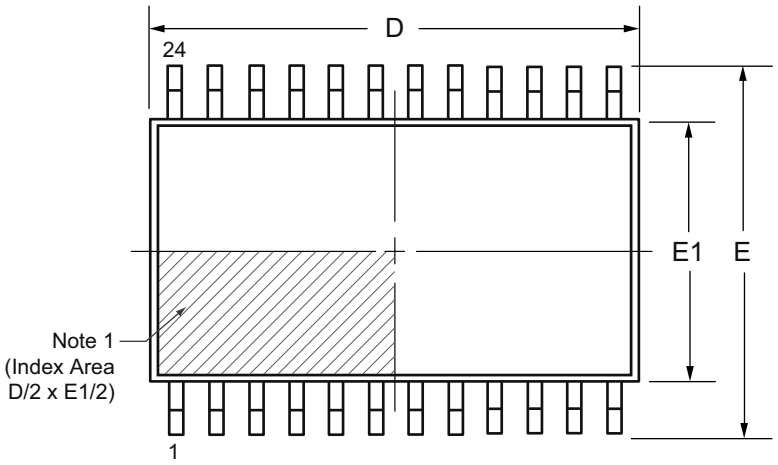
The same resistor divider can be used to protect the LED driver from the open LED condition, as shown in the schematic diagram on Page 1. The addition of a Zener diode ZD_1 causes the FLT comparator to trip when $V_{OUT} > V_Z$.

Pin Description

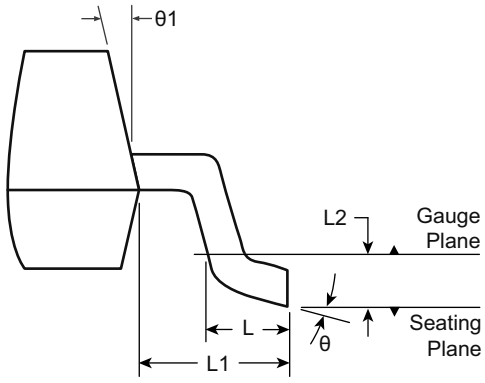
Pin	Name	Description
1	VIN	This pin is the input of a 40V high voltage regulator.
2	AVDD	This is a power supply pin for all internal circuits. It must be bypassed with a low ESR capacitor to GND (at least 0.1µF).
3	PVDD	This is the power supply pin for the gate driver. It should be connected externally to AVDD and bypassed with a low ESR capacitor to PGND (at least 0.1µF).
4	GATE	This pin is the output gate driver for an external logic level N-channel power MOSFET.
5	PGND	Ground return for the gate drive circuitry.
6	GND	Ground return for all the low power analog internal circuitry. This pin must be connected to the return path from the input.
7	JTR	This pin controls the jitter of the clock programmed by a capacitor connected at this pin.
8	RT	Connecting an external resistor from this pin to GND sets the frequency of the oscillator circuit.
9	FFN	Connecting a resistor between this pin and a negative terminal of the coupling capacitor in the boost-buck converter programs positive PWM ramp signal. The slew rate is proportional to the current sunk from this pin. When the ramp voltage exceeds the voltage at COMP, the GATE signal terminates.
10	FFP	Connecting a resistor between this pin and GND cancels the FFN current error due to non-zero voltage at FFN. The FFN and FFP current mirrors are internally matched.
11	T2	Connecting a resistor to this current output programs the over-temperature shutdown threshold temperature detected by an external NTC resistor.
12	T1	Connecting a resistor to this current input programs the temperature threshold beyond which the LED current is reduced.
13	NTC	Connect an external NTC resistor to this pin for temperature foldback of the output current and over-temperature shutdown.
14	DIV	This is the reference input that programs the voltage at the NTC pin.
15	FLT	This pin is an input of the fault comparator. This comparator is used for open and short LED protection. The IC shuts down and restarts after a POR delay when this comparator is triggered.
16	PWMD	When this pin is pulled to GND (or left open), the GATE output is disabled. The COMP pin becomes high-impedance and holds its voltage level. When this pin is logic-high, switching of GATE resumes.
17	SS	Connecting a capacitor from this pin to GND programs the soft start time of the LED driver.
18	COMP	This pin is the output of the error amplifier. Stable closed-loop control of the output LED current can be achieved by connecting a compensation network between COMP and GND. This pin is pulled to GND internally upon a start-up or detection of a fault condition.
19	FB	This pin is the high impedance non-inverting input of the error amplifier. The output current reference is programmed by connecting a resistor divider between REF and the negative terminal of the current sense resistor.
20	DRP	This is the output current reference input. Connect this pin to GND when no NTC derating is used. Connect a resistor from this pin to GND to program temperature droop of the LED current.
21	NC	No Connection.
22	NC	
23	UVLO	This pin provides input under voltage protection. When voltage at this pin falls below its threshold, AT9932 halts switching, and the soft start capacitor is discharged rapidly. The voltage at the REF pin becomes 0V, and the entire IC consumes quiescent current less ofthan 100µA. The switching resumes when the input voltage exceeds the start-up threshold. Hysteresis is provided between the two thresholds.
24	REF	This pin provides accurate reference voltage. It must be bypassed with a 0.01-0.1µF capacitor to GND.

24-Lead TSSOP Package Outline (TS)

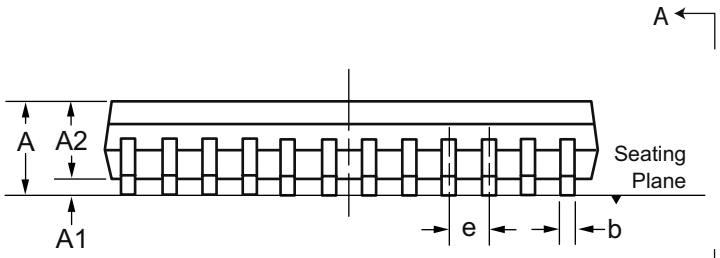
7.80x4.40mm body, 1.20mm height (max), 0.65mm pitch



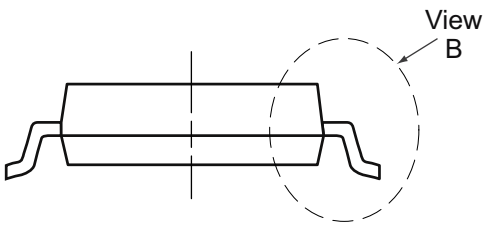
Top View



View B



Side View



View A-A

Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	L	L1	L2	θ	θ1
Dimension (mm)	MIN	0.85*	0.05	0.80	0.19	7.70	6.20*	4.30	0.65 BSC	0.45	1.00 REF	0.25 BSC	0°	12° REF
	NOM	-	-	1.00	-	7.80	6.40	4.40		0.60			-	
	MAX	1.20	0.15	1.15†	0.30	7.90	6.60*	4.50		0.75			8°	

JEDEC Registration MS-153, Variation AD, Issue F, May 2001.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings are not to scale.
***Supertex** Doc. #: DSPD-24TSSOPTS, Version B041309.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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