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## Features

- IC Distinguishes the Signal Strength of Several Transmitters via RSSI (Received Signal Strength Indicator) Output
- Minimal External Circuitry Requirements, No RF Components on the PC Board Except Matching to the Receiver Antenna
- High Sensitivity, Especially at Low Data Rates
- Sensitivity Reduction Possible Even While Receiving
- Fully Integrated VCO
- Low Power Consumption Due to Configurable Self-polling With a Programmable Time Frame Check
- Supply Voltage 4.5V to 5.5V
- Operating Temperature Range  $-40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$
- Single-ended RF Input for Easy Adaptation to  $\lambda / 4$  Antenna or Printed Antenna on PCB
- Low-cost Solution Due to High Integration Level
- ESD Protection According to MIL-STD. 883 (4 KV HBM)
- High Image Frequency Suppression Due to 1 MHz IF in Conjunction With a SAW Front-end Filter (Up to 40 dB Achievable With Newer SAWs)
- Communication to Microcontroller Possible via a Single, Bi-directional Data Line
- Power Management (Polling) is also Possible by Means of a Separate Pin via the Microcontroller

## 1. Description

The ATA3742 is a multi-chip PLL receiver device supplied in an SO20 package. It has been specially developed for the demands of RF low-cost data transmission systems with data rates from 1 kBaud to 10 kBaud (1 kBaud to 3.2 kBaud for FSK) in Manchester or Bi-phase code. The receiver is well-suited to operate with Atmel<sup>®</sup>'s PLL RF transmitter IC U2741B. Its main applications in the area of wireless control are telemetering, security technology, tire-pressure monitoring and keyless-entry systems. It can be used in the frequency receiving range of  $f_0 = 300\text{ MHz}$  to  $450\text{ MHz}$  for ASK or FSK data transmission. All the statements made in this datasheet refer both to 433.92 MHz and 315 MHz applications.

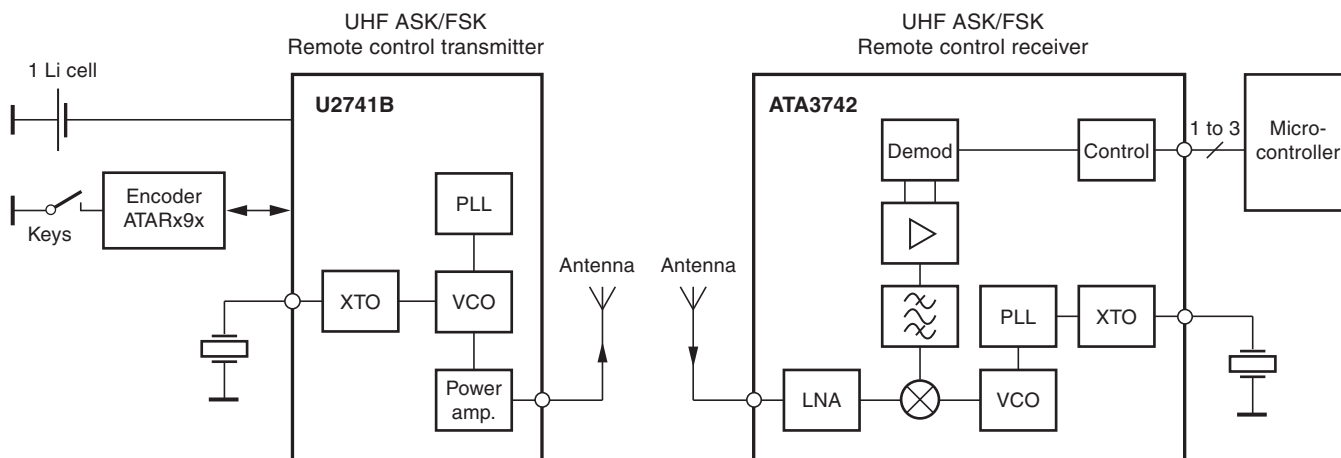


## UHF ASK/FSK Receiver

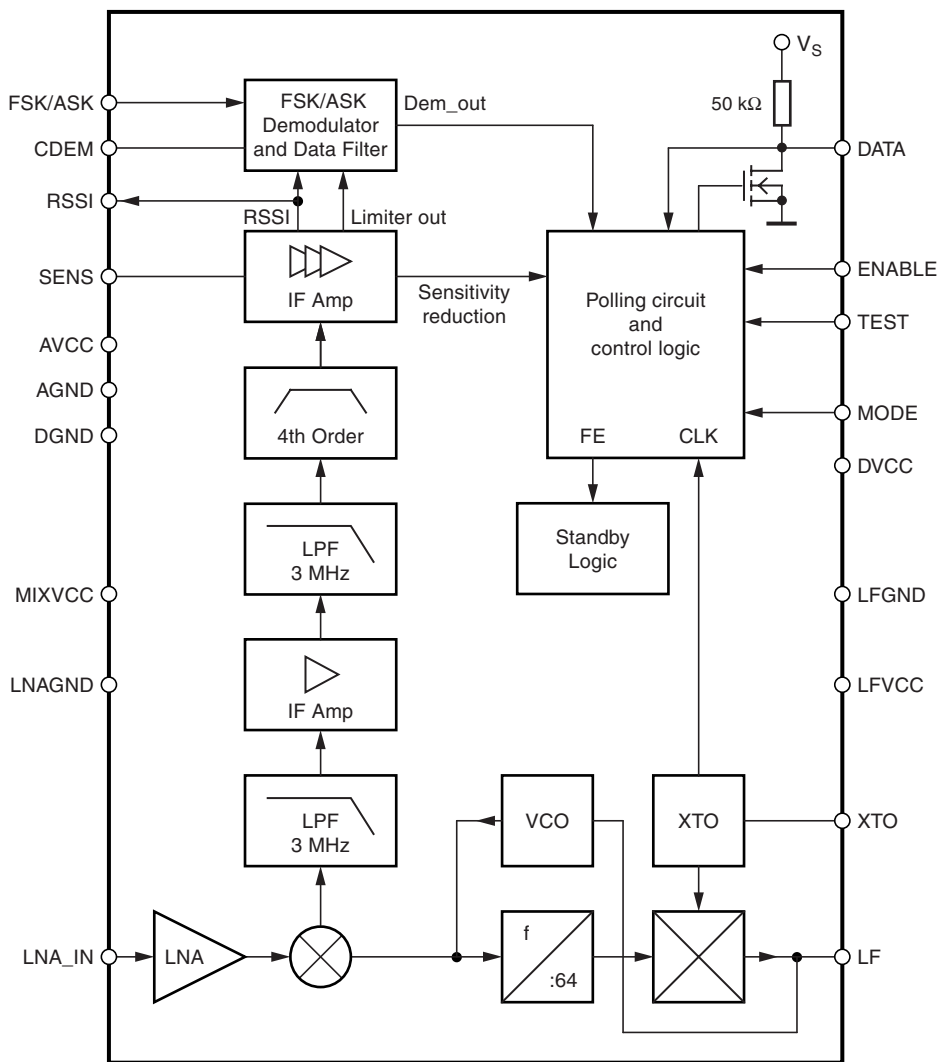
**ATA3742**



**Figure 1-1. System Block Diagram**



**Figure 1-2. Block Diagram**



## 2. Pin Configuration

Figure 2-1. Pinning SO20

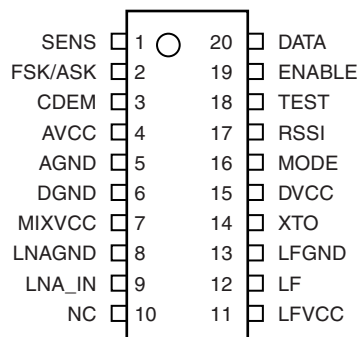


Table 2-1. Pin Description

Pin	Symbol	Function
1	SENS	Sensitivity-control resistor
2	FSK/ASK	Selecting FSK/ASK Low: FSK, High: ASK
3	CDEM	Lower cut-off frequency of the data filter
4	AVCC	Analog power supply
5	AGND	Analog ground
6	DGND	Digital ground
7	MIXVCC	Power supply mixer
8	LNAGND	High-frequency ground LNA and mixer
9	LNA_IN	RF input
10	NC	Not connected
11	LFVCC	Power supply VCO
12	LF	Loop filter
13	LFGND	Ground VCO
14	XTO	Crystal oscillator
15	DVCC	Digital power supply
16	MODE	Selecting 433.92 MHz/315 MHz Low: 4.90625 MHz (USA) High: 6.76438 (Europe)
17	RSSI	Output of the RSSI amplifier
18	TEST	Test pin, during operation at GND
19	ENABLE	Enables the polling mode Low: polling mode off (sleep mode) High: polling mode on (active mode)
20	DATA	Data output/configuration input



### 3. RF Front End

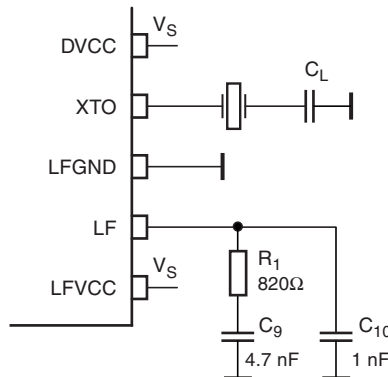
The RF front end of the receiver is a heterodyne configuration that converts the input signal into a 1 MHz IF signal. As seen in [Figure 1-2 on page 2](#), the front end consists of an LNA (low noise amplifier), LO (local oscillator), a mixer and an RF amplifier.

The LO generates the carrier frequency for the mixer via a PLL synthesizer. The XTO (crystal oscillator) generates the reference frequency  $f_{XTO}$ . The VCO (voltage-controlled oscillator) generates the drive voltage frequency  $f_{LO}$  for the mixer.  $f_{LO}$  is dependent on the voltage at pin LF.  $f_{LO}$  is divided by a factor of 64. The divided frequency is compared to  $f_{XTO}$  by the phase frequency detector. The current output of the phase frequency detector is connected to a passive loop filter and thereby generates the control voltage  $V_{LF}$  for the VCO. By means of that configuration,  $V_{LF}$  is controlled in a way that  $f_{LO} / 64$  is equal to  $f_{XTO}$ . If  $f_{LO}$  is determined,  $f_{XTO}$  can be calculated using the following formula:

$$f_{XTO} = f_{LO} / 64$$

The XTO is a one-pin oscillator that operates at the series resonance of the quartz crystal. The crystal should be connected to GND via the capacitor  $C_L$  according to [Figure 3-1](#). The value of that capacitor is recommended by the crystal supplier. The value of  $C_L$  should be optimized for the individual board layout to achieve the exact value of  $f_{XTO}$  and hereby of  $f_{LO}$ . When designing the system in terms of receiving bandwidth, the accuracy of the crystal and the XTO must be considered.

**Figure 3-1.** PLL Peripherals



The passive loop filter connected to pin LF is designed for a loop bandwidth of  $B_{Loop} = 100$  kHz. This value for  $B_{Loop}$  exhibits the best possible noise performance of the LO. [Figure 3-1](#) shows the appropriate loop filter components to achieve the desired loop bandwidth. If the filter components are changed for any reason, please note that the maximum capacitive load at pin LF is limited. If the capacitive load is exceeded, a bit check may no longer be possible since  $f_{LO}$  cannot settle in time before the bit check starts to evaluate the incoming data stream. In that case, self-polling will also not work.

$f_{LO}$  is determined by the RF input frequency  $f_{RF}$  and the IF frequency  $f_{IF}$  using the following formula:

$$f_{LO} = f_{RF} - f_{IF}$$

To determine  $f_{LO}$ , the construction of the IF filter must be considered at this point. The nominal IF frequency is  $f_{IF} = 1$  MHz. To achieve a good accuracy of the filter's corner frequencies, the filter is tuned by the crystal frequency  $f_{XTO}$ . This means that there is a fixed relation between  $f_{IF}$  and  $f_{LO}$  that depends on the logic level at pin MODE. This is described by the following formulas:

$$\text{MODE} = 0 \text{ (USA)} \quad f_{IF} = \frac{f_{LO}}{314}$$

$$\text{MODE} = 1 \text{ (Europe)} \quad f_{IF} = \frac{f_{LO}}{432.92}$$

The relation is designed to achieve the nominal IF frequency of  $f_{IF} = 1$  MHz for most applications. For applications where  $f_{RF} = 315$  MHz, MODE must be set to "0". In the case of  $f_{RF} = 433.92$  MHz, MODE must be set to "1". For other RF frequencies,  $f_{IF}$  is not equal to 1 MHz.  $f_{IF}$  is then dependent on the logical level at pin MODE and on  $f_{RF}$ . [Table 3-1](#) summarizes the different conditions.

The RF input either from an antenna or from a generator must be transformed to the RF input pin LNA\_IN. The input impedance of that pin is provided in the electrical parameters. The parasitic board inductances and capacitances also influence the input matching. The RF receiver ATA3742 exhibits its highest sensitivity at the best signal-to-noise ratio in the LNA. Hence, noise matching is the best choice for designing the transformation network.

A good practice when designing the network is to start with power matching. From that starting point, the values of the components can be varied to some extent to achieve the best sensitivity.

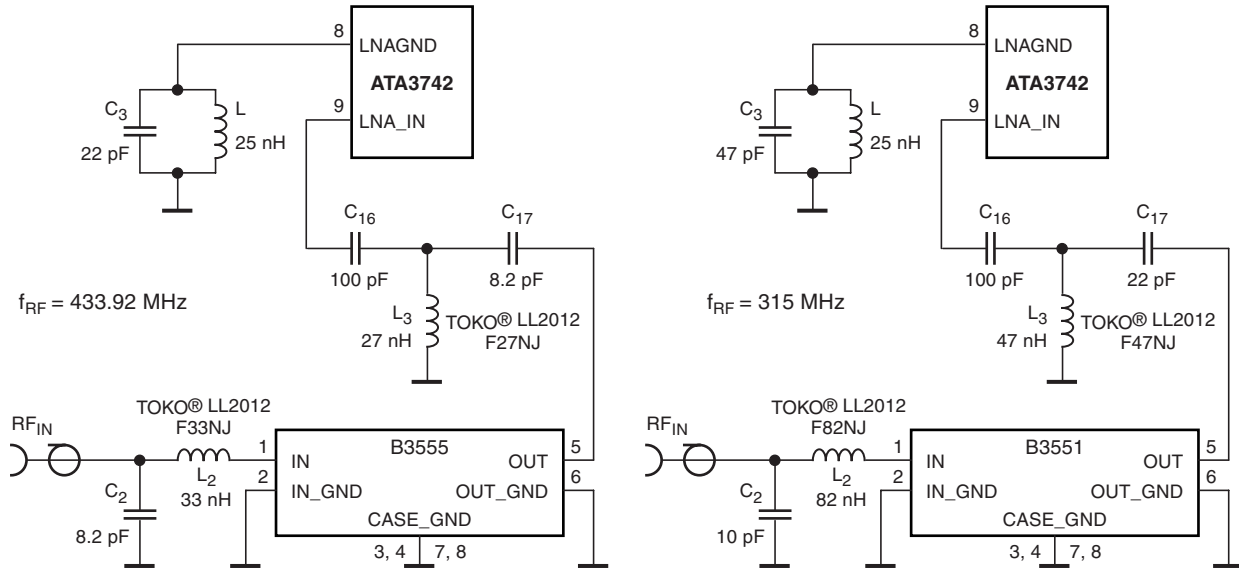
If a SAW is implemented into the input network, a mirror frequency suppression of  $\Delta P_{Ref} = 40$  dB can be achieved. There are SAWs available that exhibit a notch at  $\Delta f = 2$  MHz. These SAWs work best for an intermediate frequency of IF = 1 MHz. The selectivity of the receiver is also improved by using a SAW. In typical automotive applications, a SAW is used.

[Figure 3-2 on page 6](#) shows a typical input matching network for  $f_{RF} = 315$  MHz and  $f_{RF} = 433.92$  MHz using a SAW. [Figure 3-3 on page 6](#) illustrates input matching to  $50\Omega$  without a SAW. The input matching networks shown in [Figure 3-3 on page 6](#) are the reference networks for the parameters given in the "Electrical Characteristics" on page 26.

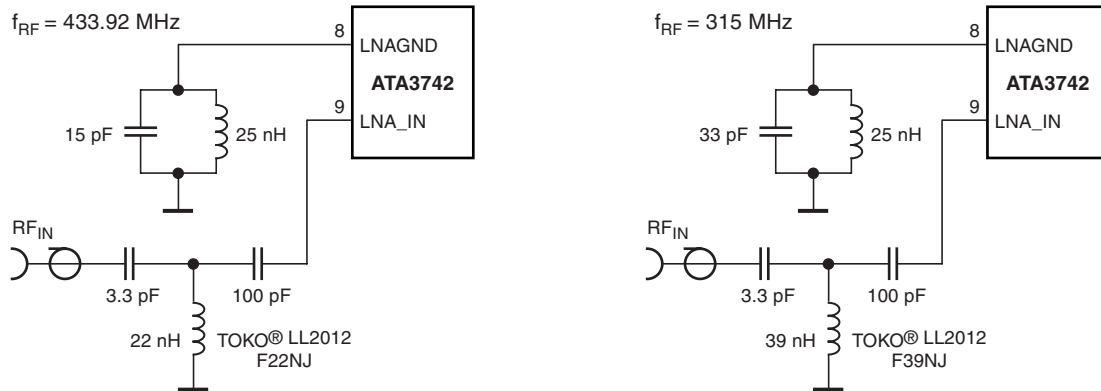
**Table 3-1.** Calculation of LO and IF Frequency

Conditions	Local Oscillator Frequency	Intermediate Frequency
$f_{RF} = 315$ MHz, MODE = 0	$f_{LO} = 314$ MHz	$f_{IF} = 1$ MHz
$f_{RF} = 433.92$ MHz, MODE = 1	$f_{LO} = 432.92$ MHz	$f_{IF} = 1$ MHz
$300 \text{ MHz} < f_{RF} < 365 \text{ MHz}$ , MODE = 0	$f_{LO} = \frac{f_{RF}}{1 + \frac{1}{314}}$	$f_{IF} = \frac{f_{LO}}{314}$
$365 \text{ MHz} < f_{RF} < 450 \text{ MHz}$ , MODE = 1	$f_{LO} = \frac{f_{RF}}{1 + \frac{1}{432.92}}$	$f_{IF} = \frac{f_{LO}}{432.92}$

**Figure 3-2.** Input Matching Network With SAW Filter



**Figure 3-3.** Input Matching Network Without SAW Filter



Please note that for all coupling conditions (see [Figure 3-2](#) and [Figure 3-3](#)), the bond wire inductivity of the LNA ground is compensated.  $C_3$  forms a series resonance circuit together with the bond wire.  $L = 25$  nH is a feed inductor to establish a DC path. Its value is not critical but must be large enough not to detune the series resonance circuit. For cost reduction, this inductor can be easily printed on the PCB. This configuration improves the sensitivity of the receiver by about 1 dB to 2 dB.

## 4. Analog Signal Processing

### 4.1 IF Amplifier

The signals coming from the RF front end are filtered by the fully integrated 4th-order IF filter. The IF center frequency is  $f_{IF} = 1$  MHz for applications where  $f_{RF} = 315$  MHz or  $f_{RF} = 433.92$  MHz is used. For other RF input frequencies, see [Table 3-1 on page 5](#) to determine the center frequency.

The receiver ATA3742-M3 employs an IF bandwidth of  $B_{IF} = 600$  kHz and can be used together with the U2741B in FSK and ASK mode.

### 4.2 RSSI Amplifier

The subsequent RSSI amplifier enhances the output signal of the IF amplifier before it is fed into the demodulator. The dynamic range of this amplifier is  $\Delta R_{RSSI} = 60$  dB. If the RSSI amplifier is operated within its linear range, the best signal-to-noise ratio (SNR) is maintained in ASK mode. If the dynamic range is exceeded by the transmitter signal, the SNR is defined by the ratio of the maximum RSSI output voltage and the RSSI output voltage due to a disturber. The dynamic range of the RSSI amplifier is exceeded if the RF input signal is about 60 dB higher compared to the RF input signal at full sensitivity.

In FSK mode, the SNR is not affected by the dynamic range of the RSSI amplifier.

The output voltage of the RSSI amplifier is internally compared to a threshold voltage  $V_{Th\_red}$ .  $V_{Th\_red}$  is determined by the value of the external resistor  $R_{Sense}$ .  $R_{Sense}$  is connected between pin SENS and GND or  $V_S$ . The output of the comparator is fed into the digital control logic. By this means, it is possible to operate the receiver at a lower sensitivity.

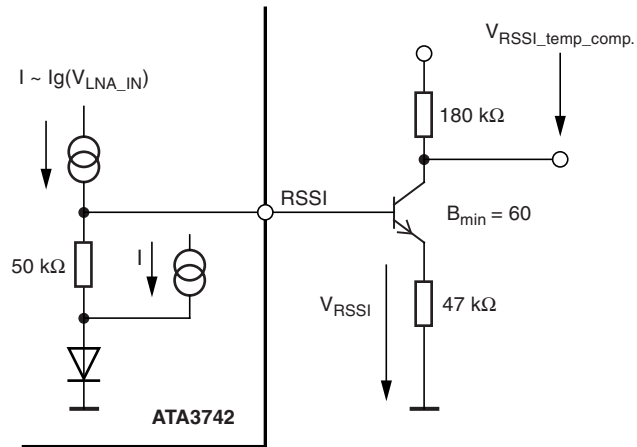
### 4.3 Pin RSSI

The output voltage of the RSSI amplifier ( $V_{RSSI}$ ) is available at pin RSSI. Using the RSSI output signal, the signal strength of different transmitters can be distinguished.

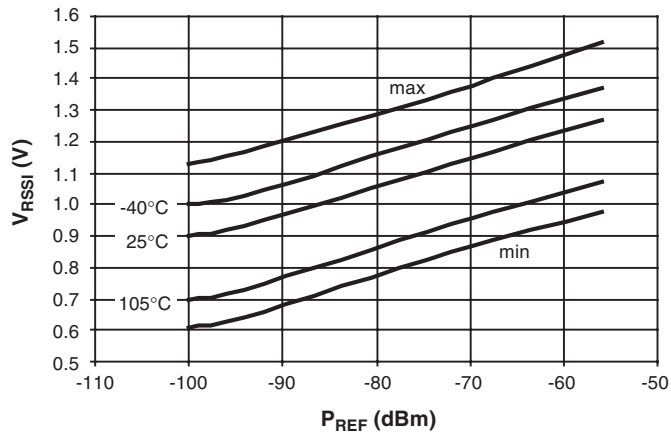
The usable input-power range  $P_{Ref}$  is  $-100$  dBm to  $-55$  dBm. The temperature coefficient TC of  $V_{RSSI}$  is typically  $-2.2$  mV/K. Due to TC and gain tolerance, it is not possible to find out the absolute level of each transmitter, but the level differences can be used to distinguish several transmitters. As illustrated in [Figure 4-2 on page 8](#), the RSSI output voltage is not constant over the temperature range. [Figure 4-1](#) illustrates an application that realizes a temperature compensation of  $V_{RSSI}$ .



**Figure 4-1.** Temperature Compensation of  $V_{RSSI}$



**Figure 4-2.** RSSI Characteristic

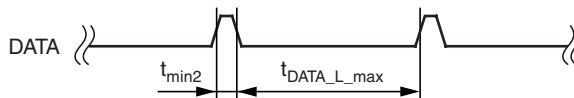


If  $R_{Sense}$  is connected to  $V_S$ , the receiver operates at a lower sensitivity. The reduced sensitivity is defined by the value of  $R_{Sense}$ , the maximum sensitivity by the signal-to-noise ratio of the LNA input. The reduced sensitivity is dependent on the signal strength at the output of the RSSI amplifier.

Since different RF input networks may exhibit slightly different values for the LNA gain, the sensitivity values given in the electrical characteristics refer to a specific input matching. This matching is illustrated in [Figure 3-3 on page 6](#) and exhibits the best possible sensitivity.

$R_{\text{Sense}}$  can be connected to  $V_S$  or GND via a microcontroller. The receiver can be switched from full sensitivity to reduced sensitivity or vice versa at any time. In polling mode, the receiver will not wake up if the RF input signal does not exceed the selected sensitivity. If the receiver is already active, the data stream at pin DATA will disappear when the input signal is lower than defined by the reduced sensitivity. Instead of the data stream, the pattern shown in [Figure 4-3](#) is issued at pin DATA to indicate that the receiver is still active.

**Figure 4-3.** Steady L State Limited DATA Output Pattern



#### 4.4 FSK/ASK Demodulator and Data Filter

The signal coming from the RSSI amplifier is converted into the raw data signal by the ASK/FSK demodulator. The operating mode of the demodulator is set via pin ASK/FSK. Logic “L” sets the demodulator to FSK mode; logic “H” sets it into ASK mode.

In ASK mode, an automatic threshold control circuit (ATC) is employed to set the detection reference voltage to a value where a good signal-to-noise ratio is achieved. This circuit also implies the effective suppression of any kind of inband noise signals or competing transmitters. If the SNR exceeds 10 dB, the data signal can be detected properly.

The FSK demodulator is intended to be used for an FSK deviation of  $\Delta f \geq 20$  kHz. Lower values may be used, but the sensitivity of the receiver will be reduced. The minimum usable deviation is dependent on the selected baud rate. In FSK mode, only BR\_Range0 and BR\_Range1 are available. In FSK mode, the data signal can be detected if the SNR exceeds 2 dB.

The output signal of the demodulator is filtered by the data filter before it is fed into the digital signal processing circuit. The data filter improves the SNR as its pass band can be adopted to the characteristics of the data signal. The data filter consists of a 1st-order high-pass and a 1st-order low-pass filter.

The high-pass filter cut-off frequency is defined by an external capacitor connected to pin CDEM. The cut-off frequency of the high-pass filter is defined by the following formula:

$$f_{\text{cu\_DF}} = \frac{1}{2 \times \pi \times 30 \text{ k}\Omega \times \text{CDEM}}$$

In self-polling mode, the data filter must settle very rapidly to achieve a low current consumption. Therefore, CDEM cannot be increased to very high values if self-polling is used. On the other hand, CDEM must be large enough to meet the data filter requirements according to the data signal. Recommended values for CDEM are given in [“Electrical Characteristics” on page 26](#). The values are slightly different for ASK and FSK mode.

The cut-off frequency of the low-pass filter is defined by the selected baud rate range (BR\_Range). BR\_Range is defined in the OPMODE register (refer to [Section “Configuration of the Receiver” on page 20](#)). BR\_Range must be set in accordance to the used baud rate.

The ATA3742 is designed to operate with data coding where the DC level of the data signal is 50%. This is valid for Manchester and Bi-phase coding. If other modulation schemes are used, the DC level should always remain within the range of  $V_{\text{DC\_min}} = 33\%$  and  $V_{\text{DC\_max}} = 66\%$ . The sensitivity may be reduced by up to 1.5 dB in that condition.

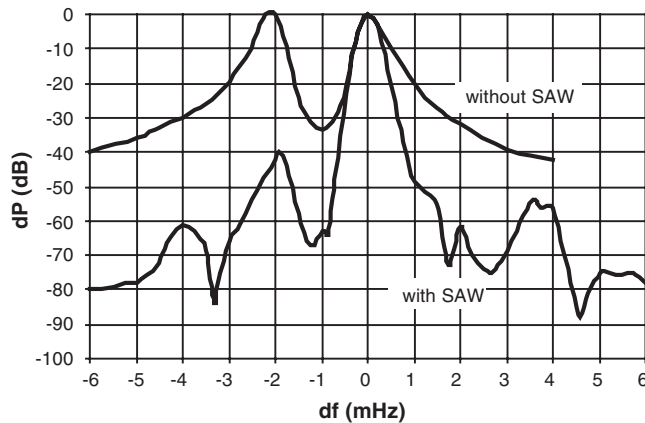
Each BR\_Range is also defined by a minimum and a maximum edge-to-edge time ( $t_{ee\_sig}$ ). These limits are defined in the electrical characteristics. They should not be exceeded to maintain full sensitivity of the receiver.

## 4.5 Receiving Characteristics

The RF receiver ATA3742 can be operated with and without a SAW front-end filter. In a typical automotive application, a SAW filter is used to achieve better selectivity. The selectivity with and without a SAW front-end filter is illustrated in [Figure 4-4 on page 10](#). This example relates to ASK mode. FSK mode exhibits similar behavior. Note that the mirror frequency is reduced by 40 dB. The plots are printed relatively to the maximum sensitivity. If a SAW filter is used, an insertion loss of about 4 dB must be considered.

When designing the system in terms of receiving bandwidth, the LO deviation must be considered as it also determines the IF center frequency. The total LO deviation is calculated to be the sum of the deviation of the crystal and the XTO deviation of the ATA3742. Low-cost crystals are specified to be within  $\pm 100$  ppm. The XTO deviation of the ATA3742 is an additional deviation due to the XTO circuit. This deviation is specified to be  $\pm 30$  ppm. If a crystal of  $\pm 100$  ppm is used, the total deviation is  $\pm 130$  ppm. Note that the receiving bandwidth and the IF-filter bandwidth are equivalent in ASK mode but not in FSK mode.

**Figure 4-4.** Receiving Frequency Response



## 5. Polling Circuit and Control Logic

The receiver is designed to consume less than 1 mA while being sensitive to signals from a corresponding transmitter. This is achieved via the polling circuit. This circuit enables the signal path periodically for a short time. During this time, the bit check logic verifies the presence of a valid transmitter signal. Only if a valid signal is detected does the receiver remain active and transfer the data to the connected microcontroller. If there is no valid signal present, the receiver is in sleep mode most of the time, resulting in low current consumption. This condition is called polling mode. A connected microcontroller is disabled during that time.

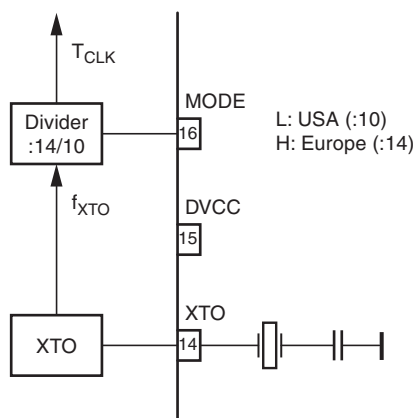
All relevant parameters of the polling logic can be configured by the connected microcontroller. This flexibility enables the user to meet the specifications in terms of current consumption, system response time, data rate, etc.

Regarding the number of connection wires to the microcontroller, the receiver is very flexible. It can be either operated by a single bi-directional line to save ports to the connected microcontroller, or it can be operated by up to three uni-directional ports.

### 5.1 Basic Clock Cycle of the Digital Circuitry

The complete timing of the digital circuitry and the analog filtering is derived from one clock. According to [Figure 5-1 on page 11](#), this clock cycle  $T_{CLK}$  is derived from the crystal oscillator (XTO) in combination with a divider. The division factor is controlled by the logical state at pin MODE. As described in Section “RF Front End” on page 4, the frequency of the crystal oscillator ( $f_{XTO}$ ) is defined by the RF input signal ( $f_{RFIn}$ ), which also defines the operating frequency of the local oscillator ( $f_{LO}$ ).

**Figure 5-1.** Generation of the Basic Clock Cycle



Pin MODE can now be set in accordance with the desired clock cycle  $T_{CLK}$ .  $T_{CLK}$  controls the following application-relevant parameters:

- Timing of the polling circuit including bit check
- Timing of the analog and digital signal processing
- Timing of the register programming
- Frequency of the reset marker
- IF filter center frequency ( $f_{IF0}$ )

Most applications are dominated by two transmission frequencies:  $f_{\text{Send}} = 315 \text{ MHz}$  is mainly used in the USA,  $f_{\text{Send}} = 433.92 \text{ MHz}$  in Europe. In order to ease the usage of all  $T_{\text{Clk}}$ -dependent parameters, the electrical characteristics display three conditions for each parameter.

- Application USA ( $f_{\text{XTO}} = 4.90625 \text{ MHz}$ ,  $\text{MODE} = \text{L}$ ,  $T_{\text{Clk}} = 2.0383 \mu\text{s}$ )
- Application Europe ( $f_{\text{XTO}} = 6.76438 \text{ MHz}$ ,  $\text{MODE} = \text{H}$ ,  $T_{\text{Clk}} = 2.0697 \mu\text{s}$ )
- Other applications ( $T_{\text{Clk}}$  is dependent on  $f_{\text{XTO}}$  and on the logical state of pin  $\text{MODE}$ . The electrical characteristic is given as a function of  $T_{\text{Clk}}$ ).

The clock cycle of some function blocks depends on the selected baud rate range ( $\text{BR\_Range}$ ) which is defined in the  $\text{OPMODE}$  register. This clock cycle  $T_{\text{XClk}}$  is defined by the following formulas for further reference:

$\text{BR\_Range} =$	$\text{BR\_Range0:}$	$T_{\text{XClk}} = 8 \times T_{\text{Clk}}$
	$\text{BR\_Range1:}$	$T_{\text{XClk}} = 4 \times T_{\text{Clk}}$
	$\text{BR\_Range2:}$	$T_{\text{XClk}} = 2 \times T_{\text{Clk}}$
	$\text{BR\_Range3:}$	$T_{\text{XClk}} = 1 \times T_{\text{Clk}}$

## 5.2 Polling Mode

As seen in [Figure 5-3 on page 15](#), the receiver stays in polling mode in a continuous cycle of three different modes. In sleep mode, the signal processing circuitry is disabled for the time period  $T_{\text{Sleep}}$  while consuming low current of  $I_{\text{S}} = I_{\text{Soff}}$ . During the start-up period,  $T_{\text{Startup}}$ , all signal processing circuits are enabled and settled. In the following bit-check mode, the incoming data stream is analyzed bit by bit, looking for a valid transmitter signal. If no valid signal is present, the receiver is set back to sleep mode after the period  $T_{\text{Bitcheck}}$ . This period varies check by check as it is a statistical process. An average value for  $T_{\text{Bitcheck}}$  is given in the electrical characteristics. During  $T_{\text{Startup}}$  and  $T_{\text{Bitcheck}}$  the current consumption is  $I_{\text{S}} = I_{\text{Son}}$ . The average current consumption in polling mode is dependent on the duty cycle of the active mode and can be calculated as:

$$I_{\text{Spoll}} = \frac{I_{\text{Soff}} \times T_{\text{Sleep}} + I_{\text{Son}} \times (T_{\text{Startup}} + T_{\text{Bitcheck}})}{T_{\text{Sleep}} + T_{\text{Startup}} + T_{\text{Bitcheck}}}$$

During  $T_{\text{Sleep}}$  and  $T_{\text{Startup}}$ , the receiver is not sensitive to a transmitter signal. To guarantee the reception of a transmitted command, the transmitter must start the telegram with an adequate preburst. The required length of the preburst is dependent on the polling parameters  $T_{\text{Sleep}}$ ,  $T_{\text{Startup}}$ ,  $T_{\text{Bitcheck}}$  and the startup time of a connected microcontroller ( $T_{\text{Start,microcontroller}}$ ).  $T_{\text{Bitcheck}}$  thus depends on the actual bit rate and the number of bits ( $N_{\text{Bitcheck}}$ ) to be tested.

The following formula indicates how to calculate the preburst length.

$$T_{\text{Purburst}} \geq T_{\text{Sleep}} + T_{\text{Startup}} + T_{\text{Bitcheck}} + T_{\text{Start\_microcontroller}}$$

### 5.2.1 Sleep Mode

The length of period  $T_{\text{Sleep}}$  is defined by the 5-bit word Sleep of the OPMODE register, the extension factor  $X_{\text{Sleep}}$  according to [Table 5-7 on page 22](#), and the basic clock cycle  $T_{\text{Clk}}$ . It is calculated to be:

$$T_{\text{Sleep}} = \text{Sleep} \times X_{\text{Sleep}} \times 1024 \times T_{\text{Clk}}$$

In US and European applications, the maximum value of  $T_{\text{Sleep}}$  is about 60 ms if  $X_{\text{Sleep}}$  is set to “1”. The time resolution is about 2 ms in that case. The sleep time can be extended to almost half a second by setting  $X_{\text{Sleep}}$  to 8.  $X_{\text{Sleep}}$  can be set to 8 by bit  $X_{\text{SleepStd}}$  or by bit  $X_{\text{SleepTemp}}$ , resulting in a different mode of action as described below:

$X_{\text{SleepStd}} = 1$  implies the standard extension factor. The sleep time is always extended.

$X_{\text{SleepTemp}} = 1$  implies the temporary extension factor. The extended sleep time is used as long as every bit check is OK. If the bit check fails once, this bit is set back to “0”, automatically resulting in a regular sleep time. This functionality can be used to save current in the presence of a modulated disturber similar to an expected transmitter signal. The connected microcontroller is rarely activated in that condition. If the disturber disappears, the receiver switches back to regular polling and is again sensitive to appropriate transmitter signals.

The highest register value of Sleep sets the receiver into a permanent sleep condition (see [Table 5-6 on page 22](#)). The receiver remains in that condition until another value for Sleep is programmed into the OPMODE register. This function is desirable where several devices share a single data line.

### 5.2.2 Bit-check Mode

In bit-check mode, the incoming data stream is examined to distinguish between a valid signal from a corresponding transmitter and signals due to noise. This is done by subsequent time frame checks where the distances between 2 signal edges are continuously compared to a programmable time window. The maximum count of these edge-to-edge tests, before the receiver switches to receiving mode, is also programmable.

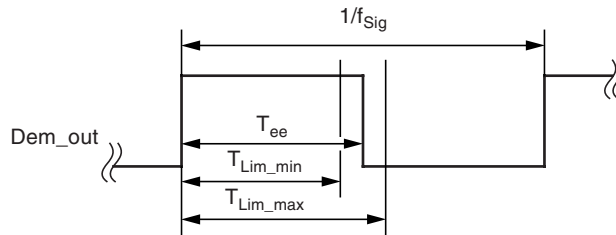
### 5.2.3 Configuring the Bit Check

Assuming a modulation scheme that contains 2 edges per bit, two time frame checks verify one bit. This is valid for Manchester, bi-phase and most other modulation schemes. The maximum count of bits to be checked can be set to 0, 3, 6 or 9 bits via the variable  $N_{\text{Bitcheck}}$  in the OPMODE register. This implies 0, 6, 12 and 18 edge-to-edge checks respectively. If  $N_{\text{Bitcheck}}$  is set to a higher value, the receiver is less likely to switch to receiving mode due to noise. In the presence of a valid transmitter signal, the bit check takes less time if  $N_{\text{Bitcheck}}$  is set to a lower value. In polling mode, the bit check time is not dependent on  $N_{\text{Bitcheck}}$ . [Figure 5-1 on page 11](#) shows an example where 3 bits are tested successfully and the data signal is transferred to pin DATA.

According to [Figure 5-2](#), the time window for the bit check is defined by two separate time limits. If the edge-to-edge time  $t_{\text{ee}}$  is in between the lower bit check limit  $T_{\text{Lim\_min}}$  and the upper bit check limit  $T_{\text{Lim\_max}}$ , the check will be continued. If  $t_{\text{ee}}$  is smaller than  $T_{\text{Lim\_min}}$  or  $t_{\text{ee}}$  exceeds  $T_{\text{Lim\_max}}$ , the bit check will be terminated and the receiver switches to sleep mode.



**Figure 5-2.** Valid Time Window for Bit Check



For best noise immunity it is recommended to use a low span between  $T_{Lim\_min}$  and  $T_{Lim\_max}$ . This is achieved using a fixed frequency at a 50% duty cycle for the transmitter preburst. A “11111...” or “10101...” sequence in Manchester or bi-phase is a good choice given this recommendation. A good compromise between receiver sensitivity and susceptibility to noise is a time window of  $\pm 25\%$  regarding the expected edge-to-edge time  $t_{ee}$ . Using preburst patterns that contain various edge-to-edge time periods, the bit check limits must be programmed according to the required span.

The bit check limits are determined by means of the formula below:

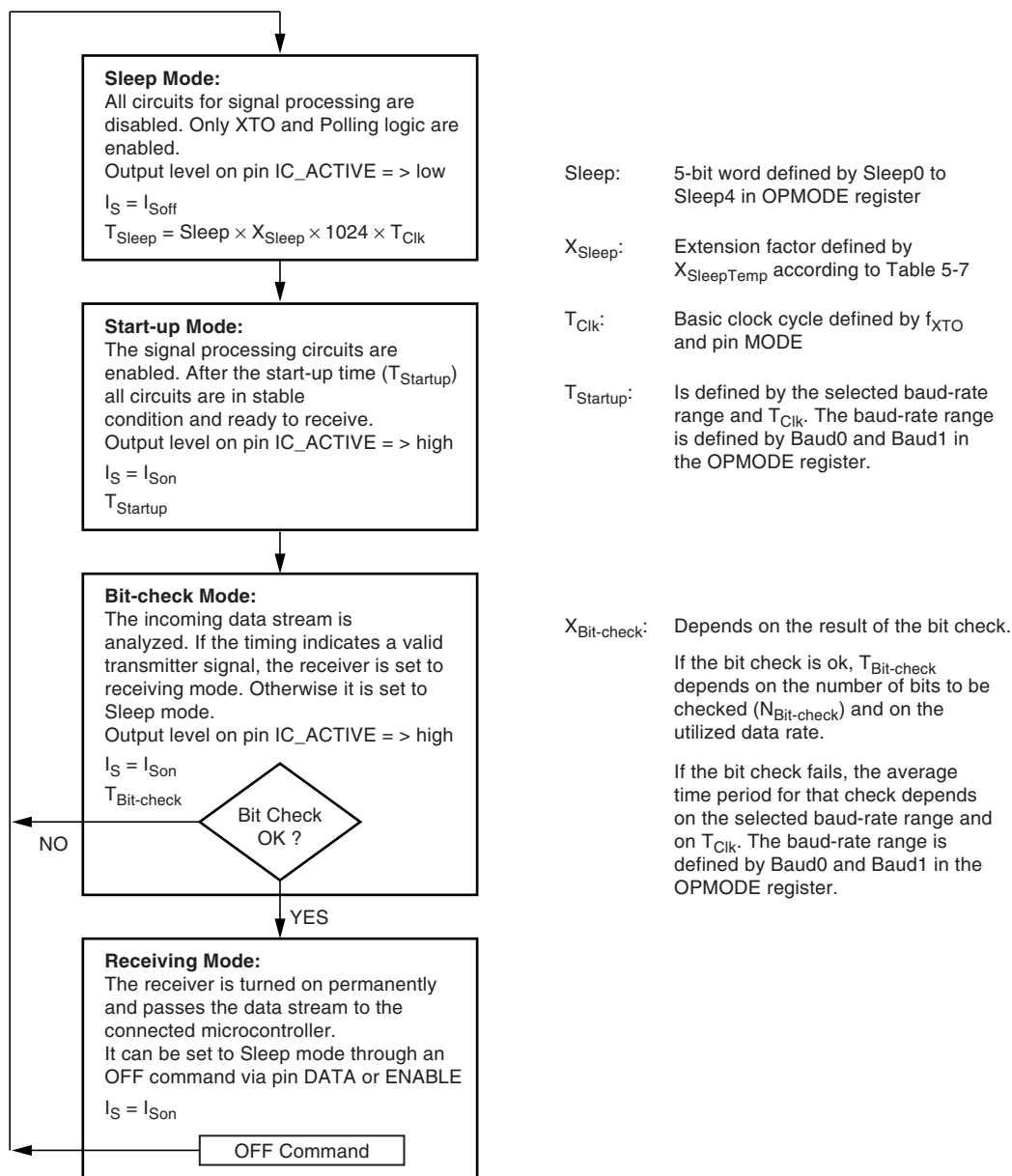
$$T_{Lim\_min} = Lim\_min \times T_{XClk}$$

$$T_{Lim\_max} = (Lim\_max - 1) \times T_{XClk}$$

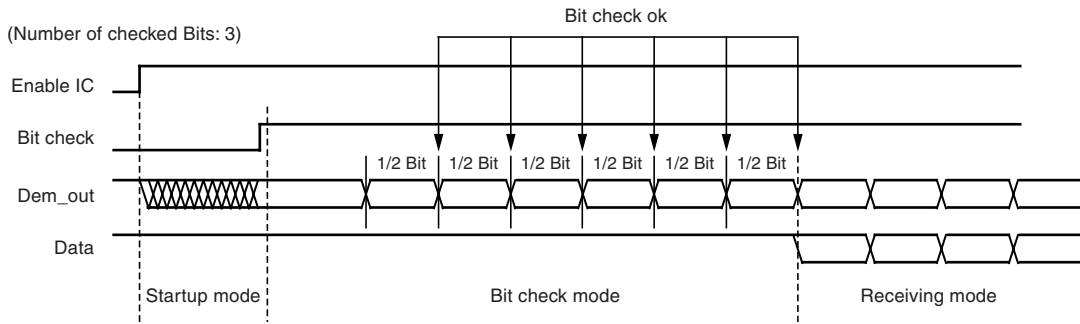
$Lim\_min$  and  $Lim\_max$  are defined by a 5-bit word each within the LIMIT register.

Using the above formulas,  $Lim\_min$  and  $Lim\_max$  can be determined according to the required  $T_{Lim\_min}$ ,  $T_{Lim\_max}$  and  $T_{XClk}$ . The time resolution when defining  $T_{Lim\_min}$  and  $T_{Lim\_max}$  is  $T_{XClk}$ . The minimum edge-to-edge time  $t_{ee}$  ( $t_{DATA\_L\_min}$ ,  $t_{DATA\_H\_min}$ ) is defined according to Section “[Receiving Mode](#)” on page 17. Due to this, the lower limit should be set to  $Lim\_min \geq 10$ . The maximum value of the upper limit is  $Lim\_max = 63$ .

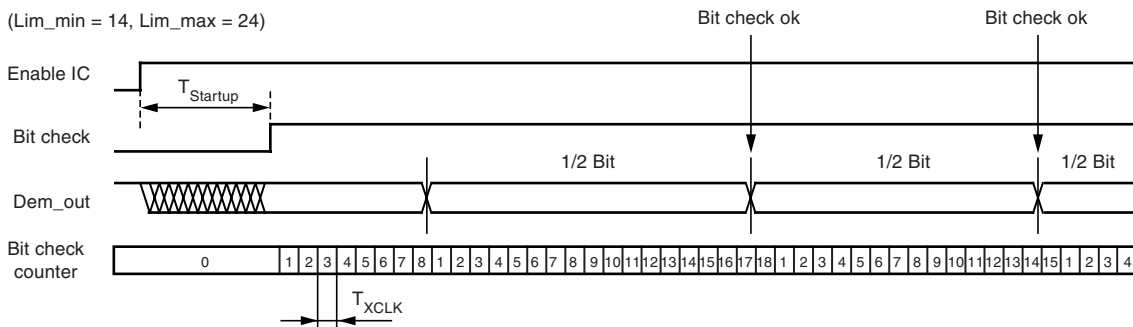
Figure 5-3. Polling Mode Flow Chart



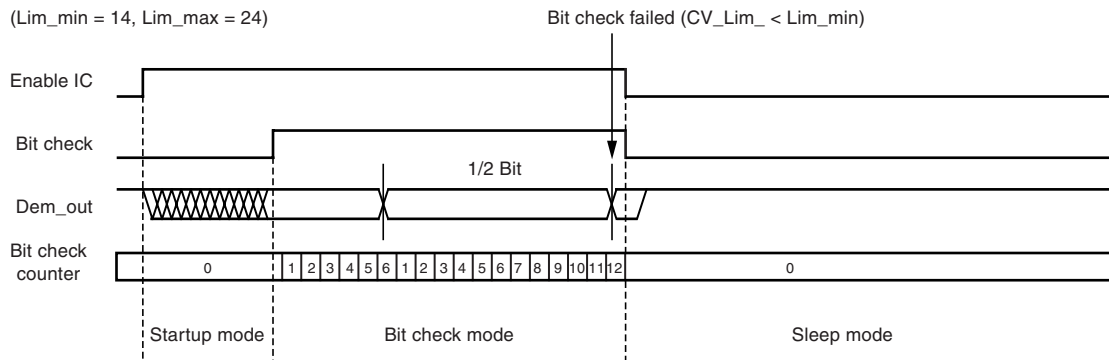
**Figure 5-4.** Timing Diagram for Complete Successful Bit Check



**Figure 5-5.** Timing Diagram During Bit Check



**Figure 5-6.** Timing Diagram for Failed Bit Check (Condition:  $CV\_Lim < Lim\_min$ )



**Figure 5-7.** Timing Diagram for Failed Bit Check (Condition:  $CV\_Lim \geq Lim\_max$ )

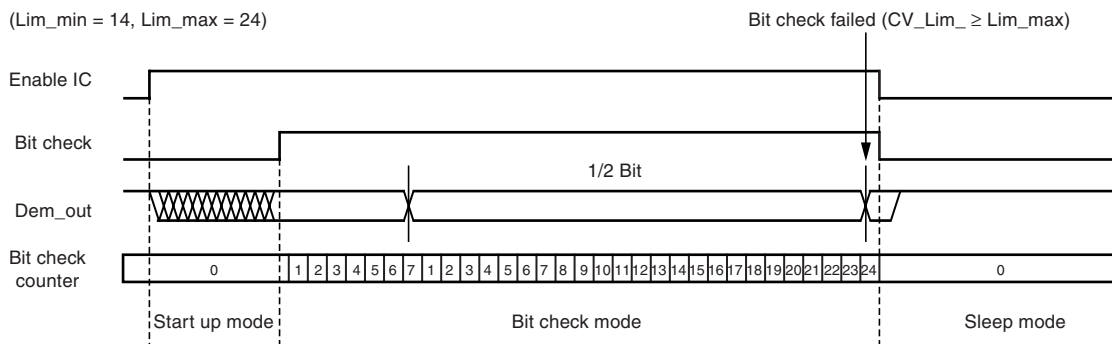


Figure 5-5 on page 16 to Figure 5-7 illustrate the bit check for the default bit check limits  $Lim_{min} = 14$  and  $Lim_{max} = 24$ . When the IC is enabled, the signal processing circuits are enabled during  $T_{Startup}$ . The output of the ASK/FSK demodulator (Dem\_out) is undefined during that period. When the bit check becomes active, the bit check counter is clocked with the cycle  $T_{XClk}$ .

Figure 5-5 on page 16 shows how the bit check proceeds if the bit check counter value  $CV_{Lim}$  is within the limits defined by  $Lim_{min}$  and  $Lim_{max}$  at the occurrence of a signal edge. In Figure 5-6 on page 16, the bit check fails as the value  $CV_{lim}$  is lower than the limit  $Lim_{min}$ . The bit check also fails if  $CV_{Lim}$  reaches  $Lim_{max}$ . This is illustrated in Figure 5-7.

#### 5.2.4 Duration of the Bit Check

If no transmitter signal is present during the bit check, the output of the ASK/FSK demodulator delivers random signals. The bit check is a statistical process and  $T_{Bitcheck}$  varies for each check. Therefore, an average value for  $T_{Bitcheck}$  is given in the electrical characteristics.  $T_{Bitcheck}$  depends on the selected baud rate range and on  $T_{Clk}$ . A higher baud rate range causes a lower value for  $T_{Bitcheck}$  resulting in a lower current consumption in polling mode.

In the presence of a valid transmitter signal,  $T_{Bitcheck}$  is dependent on the frequency of that signal,  $f_{Sig}$ , and on the count of the checked bits,  $N_{Bitcheck}$ . A higher value for  $N_{Bitcheck}$  thereby results in a longer period for  $T_{Bitcheck}$  requiring a higher value for the transmitter preburst  $T_{Preburst}$ .

### 5.3 Receiving Mode

If the bit check is successful for all bits specified by  $N_{Bitcheck}$ , the receiver switches to receiving mode. As shown in Figure 5-4 on page 16, the internal data signal is switched to pin DATA in that case. A connected microcontroller can be woken up by the negative edge at pin DATA. The receiver stays in that condition until it is switched back to polling mode explicitly.

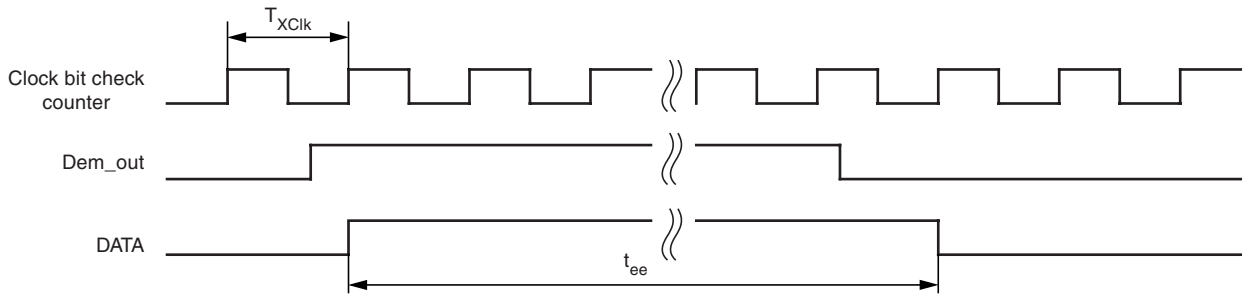
#### 5.3.1 Digital Signal Processing

The data from the ASK/FSK demodulator (Dem\_out) is digitally processed in different ways and as a result converted into the output signal data. This processing depends on the selected baud rate range (BR\_Range). Figure 5-8 on page 18 illustrates how Dem\_out is synchronized by the extended clock cycle  $T_{XClk}$ . This clock is also used for the bit check counter. Data can change its state only after  $T_{XClk}$  elapses. The edge-to-edge time period  $t_{ee}$  of the data signal as a result is always an integral multiple of  $T_{XClk}$ .

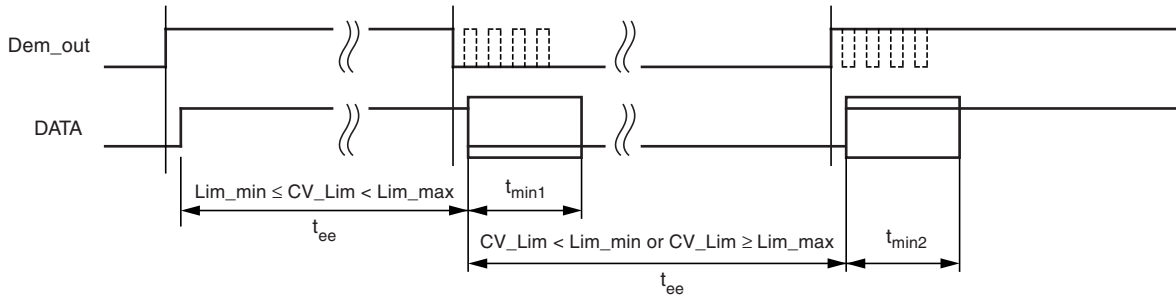
The minimum time period between two edges of the data signal is limited to  $t_{ee} \geq T_{DATA_{min}}$ . This implies an efficient suppression of spikes at the DATA output. At the same time, it limits the maximum frequency of edges at DATA. This eases the interrupt handling of a connected microcontroller.  $T_{DATA_{min}}$  is to some extent affected by the preceding edge-to-edge time interval  $t_{ee}$  as illustrated in Figure 5-9. If  $t_{ee}$  is in between the specified bit check limits, the following level is frozen for the time period  $T_{DATA_{min}} = tmin1$ , in case of  $t_{ee}$  being outside that bit check limits  $T_{DATA_{min}} = tmin2$  is the relevant stable time period.

The maximum time period for DATA to be Low is limited to  $T_{DATA_{L_{max}}}$ . This function ensures a finite response time during programming or switching off the receiver via pin DATA.  $T_{DATA_{L_{max}}}$  is thereby longer than the maximum time period indicated by the transmitter data stream. Figure 5-10 gives an example where Dem\_out remains Low after the receiver is in receiving mode.

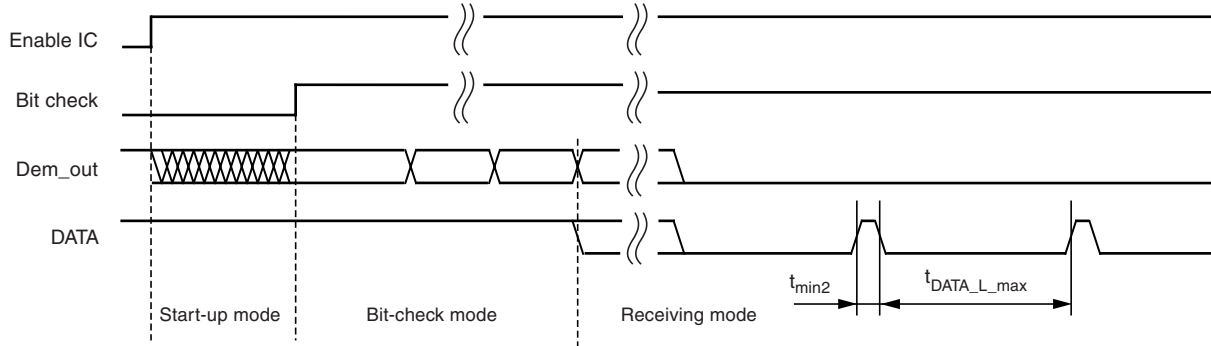
**Figure 5-8.** Synchronization of the Demodulator Output



**Figure 5-9.** Debouncing of the Demodulator Output



**Figure 5-10.** Steady L State Limited DATA Output Pattern after Transmission



After the end of data transmission, the receiver remains active and random noise pulses appear at pin DATA. The edge-to-edge time period  $t_{ee}$  of the majority of these noise pulses is equal to or slightly higher than  $T_{DATA\_min}$ .

### 5.3.2 Switching the Receiver Back to Sleep Mode

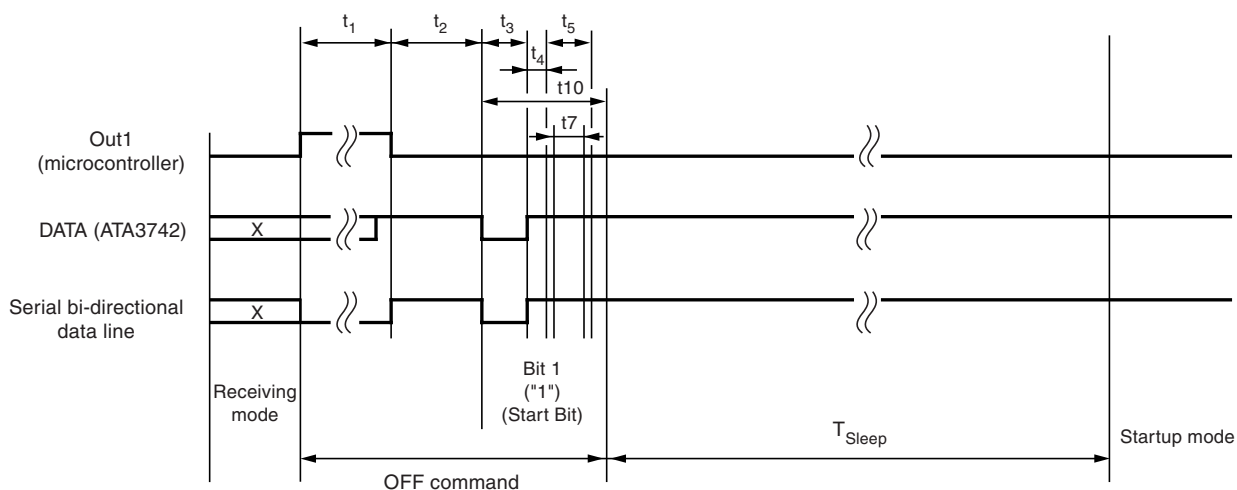
The receiver can be set back to polling mode via pin DATA or via pin ENABLE.

When using pin DATA, this pin must be pulled to Low for the period  $t_1$  by the connected microcontroller. Figure 5-11 illustrates the timing of the OFF command (see also Figure 5-15 on page 24). The minimum value of  $t_1$  depends on BR\_Range. The maximum value for  $t_1$  is not limited but it is recommended not to exceed the specified value to prevent erasing the reset marker. This item is explained in more detail in Section “Configuration of the Receiver” on page 20. Setting the receiver to sleep mode via DATA is achieved by programming bit 1 of the OPMODE register to be “1”. Only one sync pulse ( $t_3$ ) is issued.

The duration of the OFF command is determined by the sum of  $t_1$ ,  $t_2$  and  $t_{10}$ . After the OFF command, the sleep time  $T_{\text{Sleep}}$  elapses. Note that the capacitive load at pin DATA is limited. The resulting time constant  $\tau$  together with an optional external pull-up resistor may not be exceeded to ensure proper operation.

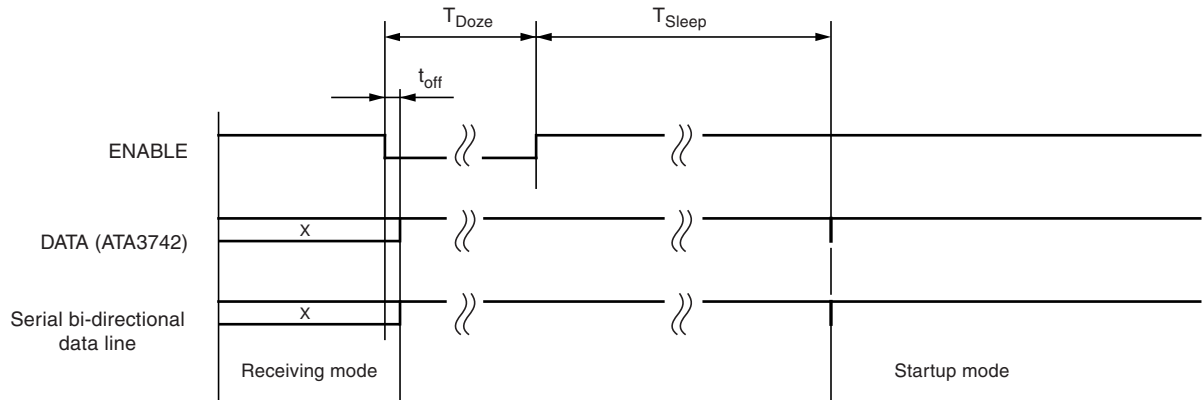
If the receiver is set to polling mode via pin ENABLE, an “L” pulse ( $T_{\text{Doze}}$ ) must be issued at that pin. Figure 5-12 on page 20 illustrates the timing of that command. After the positive edge of this pulse, the sleep time  $T_{\text{Sleep}}$  elapses. The receiver remains in sleep mode as long as ENABLE is held to “L”. If the receiver is polled exclusively by a microcontroller,  $T_{\text{Sleep}}$  can be programmed to “0” to enable an instantaneous response time. This command is a faster option than via pin DATA, at the cost of an additional connection to the microcontroller.

**Figure 5-11.** Timing Diagram of the OFF Command via Pin DATA





**Figure 5-12.** Timing Diagram of the OFF Command via Pin ENABLE



## 5.4 Configuration of the Receiver

The ATA3742 receiver is configured via two 12-bit RAM registers called OPMODE and LIMIT. The registers can be programmed by means of the bi-directional DATA port. If the register contents have changed due to a voltage drop, this condition is indicated by a certain output pattern called reset marker (RM). The receiver must be reprogrammed in that case. After a power-on reset (POR), the registers are set to default mode. If the receiver is operated in default mode, there is no need to program the registers.

Table 5-2 on page 21 shows the structure of the registers. Referring to Table 5-1, bit 1 defines if the receiver is set back to polling mode via the OFF command (see Section “Receiving Mode” on page 17), or if it is programmed. Bit 2 represents the register address. It selects the appropriate register to be programmed.

**Table 5-1.** Effect of Bit 1 and Bit 2 in Programming the Registers

Bit 1	Bit 2	Action
1	x	The receiver is set back to polling mode (OFF command)
0	1	The OPMODE register is programmed
0	0	The LIMIT register is programmed

Table 5-3 on page 21 and the following illustrate the effect of the individual configuration words. The default configuration is highlighted for each word.

BR\_Range sets the appropriate baud rate range. At the same time it defines XLim. XLim is used to define the bit check limits  $T_{Lim\_min}$  and  $T_{Lim\_max}$  as shown in Table 5-3 on page 21.

**Table 5-2.** Effect of the Configuration Words Within the Registers

Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14
<b>OFF Command</b>													
1													
<b>OPMODE Register</b>													
0	1	BR_Range		N <sub>Bitcheck</sub>		V <sub>POUT</sub>	Sleep				X <sub>Sleep</sub>		
0	1	Baud1	Baud0	BitChk1	BitChk0	POUT	Sleep4	Sleep3	Sleep2	Sleep1	Sleep0	X <sub>Sleep</sub> Std	X <sub>Sleep</sub> Temp
(Default)		0	0	1	0	0	0	1	0	1	1	0	0
<b>LIMIT Register</b>													
0	0	Lim_min						Lim_max					
0	0	Lim_min5	Lim_min4	Lim_min3	Lim_min2	Lim_min1	Lim_min0	Lim_max5	Lim_max4	Lim_max3	Lim_max2	Lim_max1	Lim_max0
(Default)		0	0	1	1	1	0	0	1	1	0	0	0

**Table 5-3.** Effect of the Configuration Word BR\_Range

BR_Range		Baud Rate Range/Extension Factor for Bit Check Limits (XLim)
Baud1	Baud0	
0	0	BR_Range0 (application USA/Europe: BR_Range0 = 1.0 kBaud to 1.8 kBaud) (Default) XLim = 8 (Default)
0	1	BR_Range1 (application USA/Europe: BR_Range1 = 1.8 kBaud to 3.2 kBaud) XLim = 4
1	0	BR_Range2 (application USA/Europe: BR_Range2 = 3.2 kBaud to 5.6 kBaud) XLim = 2
1	1	BR_Range3 (application USA/Europe: BR_Range3 = 5.6 kBaud to 10 kBaud) XLim = 1

**Table 5-4.** Effect of the Configuration Word N<sub>Bitcheck</sub>

N <sub>Bitcheck</sub>		Number of Bits to be Checked
BitChk1	BitChk0	
0	0	0
0	1	3
1	0	6 (Default)
1	1	9

**Table 5-5.** Effect of the Configuration Bit Reserved

Reserved Bit	No Function (Reserved for Future Use)
0	(Default)
1	-

**Table 5-6.** Effect of the Configuration Word Sleep

Sleep					Start Value for Sleep Counter ( $T_{\text{Sleep}} = \text{Sleep} \times X_{\text{Sleep}} \times 1024 \times T_{\text{Clk}}$ )
Sleep4	Sleep3	Sleep2	Sleep1	Sleep0	
0	0	0	0	0	0 (Receiver is continuously polling until a valid signal occurs)
0	0	0	0	1	1 ( $T_{\text{Sleep}} \approx 2$ ms for $X_{\text{Sleep}} = 1$ in US/European applications)
0	0	0	1	0	2
0	0	0	1	1	3
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
0	1	0	1	1	11 (USA: $T_{\text{Sleep}} = 22.96$ ms, Europe: $T_{\text{Sleep}} = 23.31$ ms) (Default)
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
1	1	1	0	1	29
1	1	1	1	0	30
1	1	1	1	1	31 (Permanent sleep mode)

**Table 5-7.** Effect of the Configuration Word  $X_{\text{Sleep}}$ 

$X_{\text{Sleep}}$		Extension Factor for Sleep Time ( $T_{\text{Sleep}} = \text{Sleep} \times X_{\text{Sleep}} \times 1024 \times T_{\text{Clk}}$ )
$X_{\text{SleepStd}}$	$X_{\text{SleepTemp}}$	
0	0	1 (Default)
0	1	8 ( $X_{\text{Sleep}}$ is reset to 1 if bit check fails once)
1	0	8 ( $X_{\text{Sleep}}$ is set permanently)
1	1	8 ( $X_{\text{Sleep}}$ is set permanently)

**Table 5-8.** Effect of the Configuration Word Lim\_min

Lim_min						Lower Limit Value for Bit Check ( $T_{\text{Lim\_min}} = \text{Lim\_min} \times X_{\text{Lim}} \times T_{\text{Clk}}$ )
Lim_min < 10 is not applicable						
0	0	1	0	1	0	10
0	0	1	0	1	1	11
0	0	1	1	0	0	12
0	0	1	1	0	1	13
0	0	1	1	1	0	14 (Default) (USA: $T_{\text{Lim\_min}} = 228$ $\mu$ s, Europe: $T_{\text{Lim\_min}} = 232$ $\mu$ s)
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
1	1	1	1	0	1	61
1	1	1	1	1	0	62
1	1	1	1	1	1	63

**Table 5-9.** Effect of the Configuration Word Lim\_max

Lim_max						Upper Limit Value for Bit Check
Lim_max < 12 is not applicable						$(T_{Lim\_max} = (Lim\_max - 1) \times XLim \times T_{Clk})$
0	0	1	1	0	0	12
0	0	1	1	0	1	13
0	0	1	1	1	0	14
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
0	1	1	0	0	0	24 (Default) (USA: $T_{Lim\_max} = 375 \mu s$ , Europe: $T_{Lim\_max} = 381 \mu s$ )
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
1	1	1	1	0	1	61
1	1	1	1	1	0	62
1	1	1	1	1	1	63

#### 5.4.1 Conservation of the Register Information

The ATA3742 has an integrated power-on reset (POR) and brown-out detection circuitry to provide a mechanism to preserve the RAM register information.

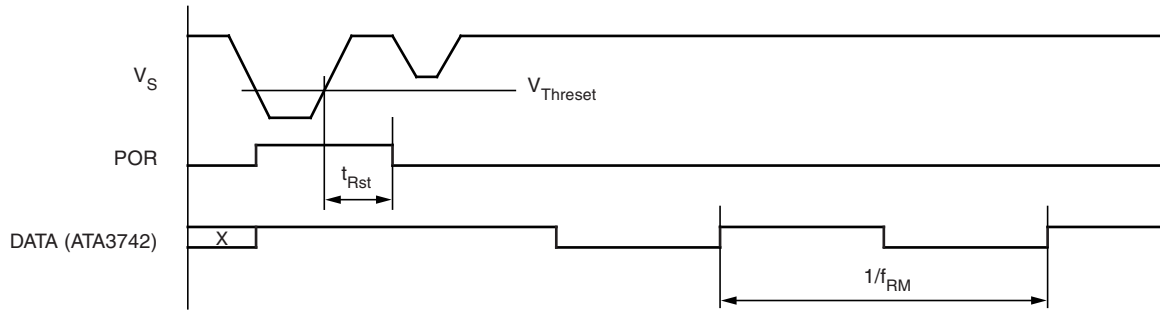
According to [Figure 5-13](#), a power-on reset is generated if the supply voltage  $V_S$  drops below the threshold voltage  $V_{ThReset}$ . The default parameters are programmed into the configuration registers in that condition. Once  $V_S$  exceeds  $V_{ThReset}$ , the POR is canceled after the minimum reset period  $t_{Rst}$ . A POR is also generated when the supply voltage of the receiver is turned on.

To indicate that condition, the receiver displays a reset marker (RM) at pin DATA after a reset. The RM is represented by the fixed frequency  $f_{RM}$  at a 50% duty cycle. RM can be canceled via an “L” pulse  $t_1$  at pin DATA. The RM implies the following characteristics:

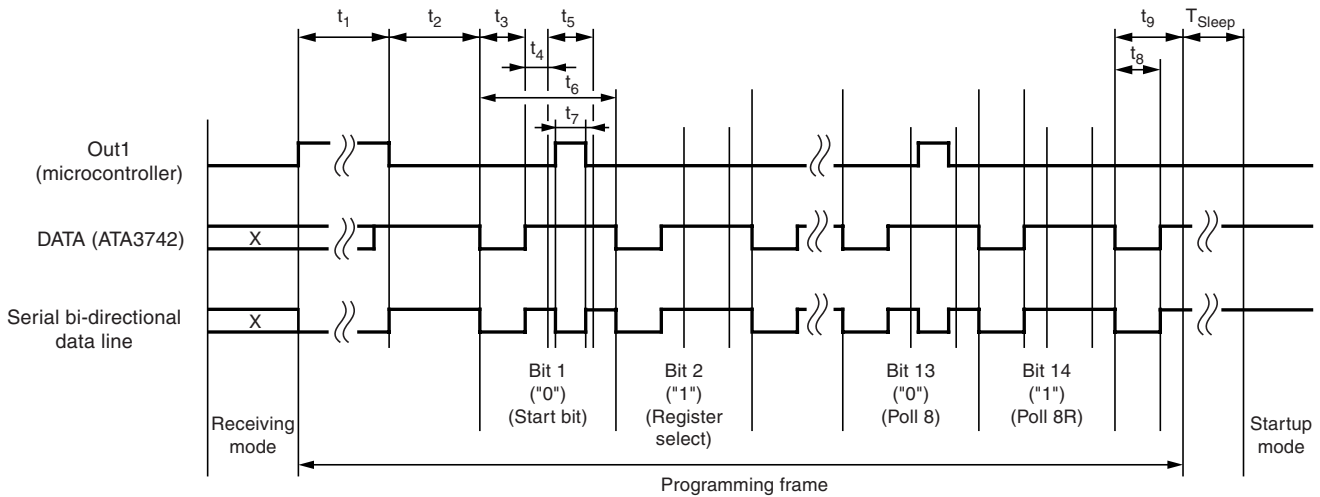
- $f_{RM}$  is lower than the lowest feasible frequency of a data signal. This means, RM cannot be misinterpreted by the connected microcontroller.
- If the receiver is set back to polling mode via pin DATA, RM cannot be cancelled by accident if  $t_1$  is applied according to the proposal in the [Section “Programming the Configuration Register” on page 24](#).

By means of that mechanism, the receiver cannot lose its register information without communicating that condition via the reset marker RM.

**Figure 5-13.** Generation of the Power-on Reset



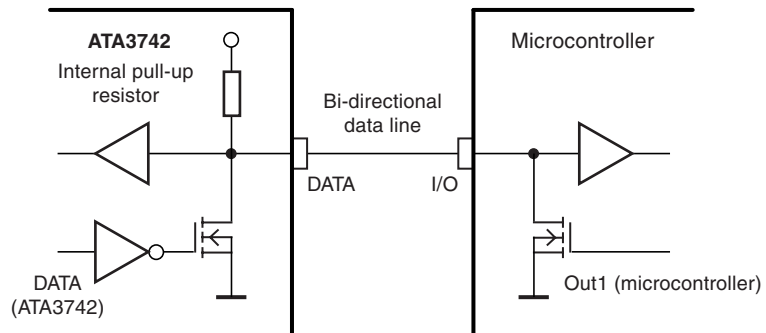
**Figure 5-14.** Timing of the Register Programming



### 5.4.2 Programming the Configuration Register

The configuration registers are programmed serially via the bi-directional data line according to [Figure 5-14](#) and [Figure 5-15](#).

**Figure 5-15.** One-wire Connection to a Microcontroller



To start programming, the serial data line DATA is pulled to “L” for the time period  $t_1$  by the microcontroller. When DATA has been released, the receiver becomes the master device. When the programming delay period  $t_2$  has elapsed, it emits 14 subsequent synchronization pulses with the pulse length  $t_3$ . After each of these pulses, a programming window occurs. The delay until the program window starts is determined by  $t_4$ , the duration is defined by  $t_5$ . Within the programming window, the individual bits are set. If the microcontroller pulls down pin DATA for the time period  $t_7$  during  $t_5$ , the bit is set to “0”. If no programming pulse  $t_7$  is issued, this bit is set to “1”. All 14 bits are subsequently programmed in this way. The time frame to program a bit is defined by  $t_6$ .

Bit 14 is followed by the equivalent time window  $t_9$ . During this window, the equivalent acknowledge pulse  $t_8$  (E\_Ack) occurs if the just-programmed mode word is equivalent to the mode word that was already stored in that register. E\_Ack should be used to verify that the mode word was correctly transferred to the register. The register must be programmed twice in that case.

Programming of a register is possible both during sleep and active mode of the receiver.

During programming, the LNA, LO, low-pass filter, IF amplifier and the FSK/ASK Manchester demodulator are disabled.

The programming start pulse  $t_1$  initiates the programming of the configuration registers. If bit 1 is set to “1”, it represents the OFF command to set the receiver back to polling mode at the same time. For the length of the programming start pulse  $t_1$ , the following convention should be considered:

- $t_1(\text{min}) < t_1 < 1535 \times T_{\text{Clk}}$ : [ $t_1(\text{min})$  is the minimum specified value for the relevant BR\_Range]

Programming (or the OFF command) is initiated if the receiver is not in reset mode. If the receiver is in reset mode, programming (or the OFF command) is not initiated, and the reset marker (RM) is still present at pin DATA.

This period is generally used to switch the receiver to polling mode. In a reset condition, RM is not canceled by accident.

- $t_1 > 5632 \times T_{\text{Clk}}$

Programming (or the OFF command) is initiated in any case. RM is canceled if present.

This period is used if the connected microcontroller detected RM. If a configuration register is programmed, this time period for  $t_1$  can generally be used. Note that the capacitive load at pin DATA is limited. The resulting time constant  $t$  together with an optional external pull-up resistor may not be exceeded to ensure proper operation.