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Features

- **Multi Channel Half–duplex Transceiver with Approximately ±2.5 MHz Programmable Tuning Range**
- **High FSK Sensitivity: –106 dBm at 20 kBaud/–109.5 dBm at 2.4 kBaud (433.92 MHz)**
- **High ASK Sensitivity: –112.5 dBm at 10 kBaud/–116.5 dBm at 2.4 kBaud (433.92 MHz)**
- **Low Supply Current: 10.5 mA in RX and TX Mode (3 V/TX with 5 dBm)**
- **Data Rate: 1 to 20 kBaud Manchester FSK, 1 to 10 kBaud Manchester ASK**
- **ASK/FSK Receiver Uses a Low–IF Architecture with High Selectivity, Blocking, and Low Intermodulation (Typical Blocking 55 dB at ±750 kHz/61 dB at ±1.5 MHz and 70 dB at ±10 MHz, System I1dBCP = –30 dBm/System IIP3 = –20 dBm)**
- **226 kHz IF Frequency with 30 dB Image Rejection and 170 kHz Usable IF Bandwidth (TBD)**
- **Transmitter Uses Closed Loop Fractional–N Synthesizer for FSK Modulation with a High PLL Bandwidth and an Excellent Isolation between PLL/VCO and PA**
- **Tolerances of XTAL Compensated by Fractional–N Synthesizer with 800 Hz RF Resolution**
- **Integrated RX/TX–Switch, Single–ended RF Input and Output**
- **RSSI (Received Signal Strength Indicator)**
- **Communication to Microcontroller with SPI Interface Working at Maximum 500 kBit/s**
- **Configurable Self Polling and RX/TX Protocol Handling with FIFO–RAM Buffering of Received and Transmitted Data**
- **5 Push Button Inputs and One Wake–up Input are Active in Power–down Mode**
- **Integrated XTAL Capacitors**
- **PA Efficiency: up to 38% (433.92 MHz/10 dBm/3 V)**
- **Low In–band Sensitivity Change of Typically ±1.8 dB within ±58 kHz Center Frequency Change in the Complete Temperature and Supply Voltage Range (TBD)**
- **Supply Voltage Switch, Supply Voltage Regulator, Reset Generation, Clock/Interrupt Generation and Low Battery Indicator for Microcontroller**
- **Fully Integrated PLL with Low Phase Noise VCO, PLL Loop Filter and Full Support of Multi–channel Operation with Arbitrary Channel Distance Due to Fractional–N Synthesizer**
- **Sophisticated Threshold Control and Quasi–peak Detector Circuit in the Data Slicer**
- **Power Management via Different Operation Modes**
- **315 MHz, 345 MHz, 433.92 MHz, 868.3 MHz and 915 MHz without External VCO and PLL Components**
- **Inductive Supply with Voltage Regulator if Battery is Empty (AUX Mode)**
- **Efficient XTO Start–up Circuit (> –1.5 kΩ Worst Case Real Start–up Impedance)**
- **Changing of Modulation Type ASK/FSK and Data Rate without Component Changes**
- **Minimal External Circuitry Requirements for Complete System Solution**
- **Adjustable Output Power: 0 to 10 dBm Adjusted and Stabilized with External Resistor**
- **ESD Protection at all Pins (2 kV HBM, 200 V MM, TBD FCDM)**
- **Supply Voltage Range: 2.4 V to 3.6 V or 4.4 V to 6.6 V**
- **Temperature Range: –40°C to +85°C**
- **Small 7 $\times$ 7 mm QFN48 Package**

Product Description

ATA5423
ATA5425
ATA5428
ATA5429

Preliminary

Applications

- **Consumer Industrial Segment**
- **Access Control Systems**
- **Remote Control Systems**
- **Alarm and Telemetry Systems**
- **Energy Metering**
- **Home Automation**

Benefits

- **Low System Cost Due to Very High System Integration Level**
- **Only One Crystal Needed in System**
- **Less Demanding Specification for the Microcontroller Due to Handling of Power–down Mode, Delivering of Clock, Reset, Low Battery Indication and Complete Handling of Receive/Transmit Protocol and Polling**
- **Single–ended Design with High Isolation of PLL/VCO from PA and the Power Supply Allows a Loop Antenna in the Remote Control Unit to Surround the Whole Application**

1. General Description

The ATA5423/25/28/29 is a highly integrated UHF ASK/FSK multi–channel half–duplex trans-
ceiver with low power consumption supplied in a small 7 x 7 mm QFN48 package. The receive
part is built as a fully integrated low–IF receiver, whereas direct PLL modulation with the frac-
tional–N synthesizer is used for FSK transmission and switching of the power amplifier for ASK
transmission.

The device supports data rates of 1 kBaud to 20 kBaud (FSK) and 1 kBaud to 10 kBaud (ASK)
in Manchester, Bi–phase and other codes in transparent mode. The ATA5428 can be used in
the 431.5 MHz to 436.5 MHz and in the 862 MHz to 872 MHz bands, the ATA5423 in the
312.5 MHz to 317.5 MHz band, the ATA5425 in the 342.5 MHz to 347.5 MHz band and the
ATA5429 in the 912.5 MHz to 917.5 MHz band. The very high system integration level results in
a small number of external components needed.

Due to its blocking and selectivity performance, together with the additional 15 dB to 20 dB loss
and the narrow bandwidth of a typical loop antenna in a remote control unit, a bulky blocking
SAW is not needed in the remote control unit. Additionally, the building blocks needed for a typi-
cal remote control and access control system on both sides (the base and the mobile stations)
are fully integrated.

Its digital control logic with self–polling and protocol generation enables a fast challenge–
response system without using a high–performance microcontroller. Therefore, the
ATA5423/ATA5425/ATA5428/ATA5429 contains a FIFO buffer RAM and can compose and
receive the physical messages themselves. This provides more time for the microcontroller to
carry out other functions such as calculating crypto algorithms, composing the logical messages,
and controlling other devices. Therefore, a standard 4–/8–bit microcontroller without special
periphery and clocked with the CLK output of about 4.5 MHz is sufficient to control the communi-
cation link. This is especially valid for passive entry and access control systems, where within
less than 100 ms several challenge–response communications with arbitration of the communi-
cation partner have to be handled.

It is hence possible to design bi–directional remote control and access control systems with a
fast challenge–response crypto function, with the same PCB board size and with the same cur-
rent consumption as uni–directional remote control systems.
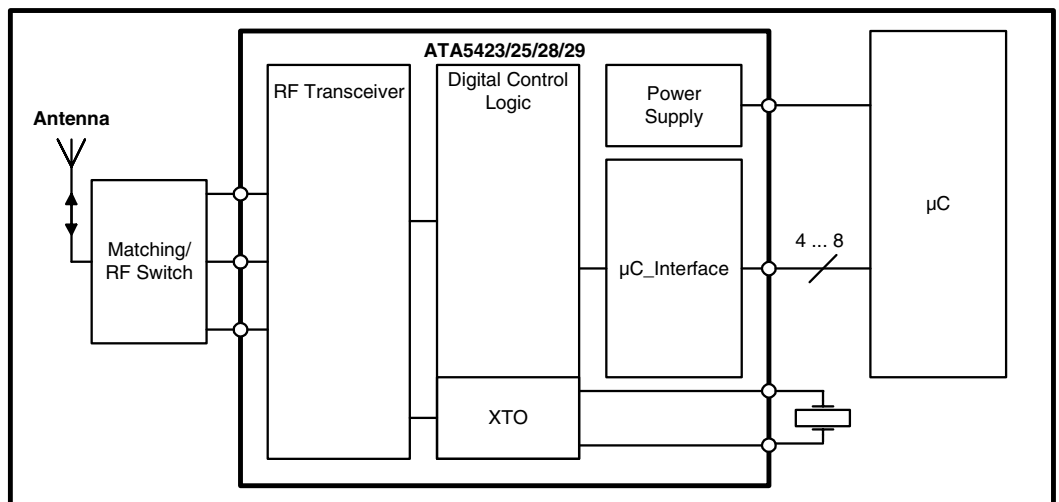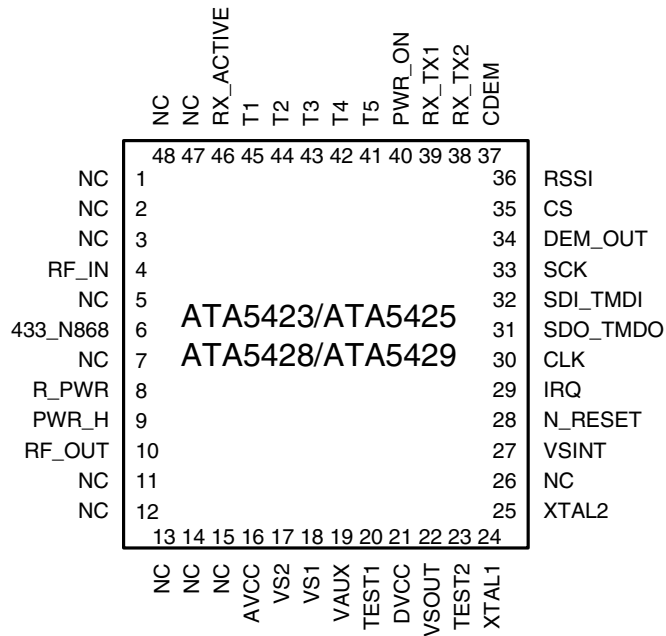
Figure 1-1. System Block Diagram

Figure 1-2. Pinning QFN48

Table 1-1. Pin Description

Pin	Symbol	Function
1	NC	Not connected
2	NC	Not connected
3	NC	Not connected
4	RF_IN	RF input
5	NC	Not connected
6	433_N868	Selects RF input/output frequency range
7	NC	Not connected
8	R_PWR	Resistor to adjust output power
9	PWR_H	Pin to select output power
10	RF_OUT	RF output
11	NC	Not connected
12	NC	Not connected
13	NC	Not connected
14	NC	Not connected
15	NC	Not connected
16	AVCC	Blocking of the analog voltage supply
17	VS2	Power supply input for voltage range 4.4 V to 6.6 V
18	VS1	Power supply input for voltage range 2.4 V to 3.6 V
19	VAUX	Auxiliary supply voltage input
20	TEST1	Test input, at GND during operation
21	DVCC	Blocking of the digital voltage supply

Table 1-1. Pin Description (Continued)

| Pin	Symbol	Function
22	VSOUT	Output voltage power supply for external devices
23	TEST2	Test input, at GND during operation
24	XTAL1	Reference crystal
25	XTAL2	Reference crystal
26	NC	Not connected
27	VSINT	Microcontroller interface supply voltage
28	N_RESET	Output pin to reset a connected microcontroller
29	IRQ	Interrupt request
30	CLK	Clock output to connect a microcontroller
31	SDO_TMDO	Serial data out/transparent mode data out
32	SDI_TMDI	Serial data in/transparent mode data in
33	SCK	Serial clock
34	DEM_OUT	Demodulator open drain output signal
35	CS	Chip select for serial interface
36	RSSI	Output of the RSSI amplifier
37	CDEM	Capacitor to adjust the lower cut–off frequency data filter
38	RX_TX2	GND pin to decouple LNA in TX mode
39	RX_TX1	Switch pin to decouple LNA in TX mode
40	PWR_ON	Input to switch on the system (active high)
41	T5	Key input 5 (can also be used to switch on the system (active low))
42	T4	Key input 4 (can also be used to switch on the system (active low))
43	T3	Key input 3 (can also be used to switch on the system (active low))
44	T2	Key input 2 (can also be used to switch on the system (active low))
45	T1	Key input 1 (can also be used to switch on the system (active low))
46	RX_ACTIVE	Indicates RX operation mode
47	NC	Not connected
48	NC	Not connected
	GND	Ground/backplane

Figure 1-3. Block Diagram
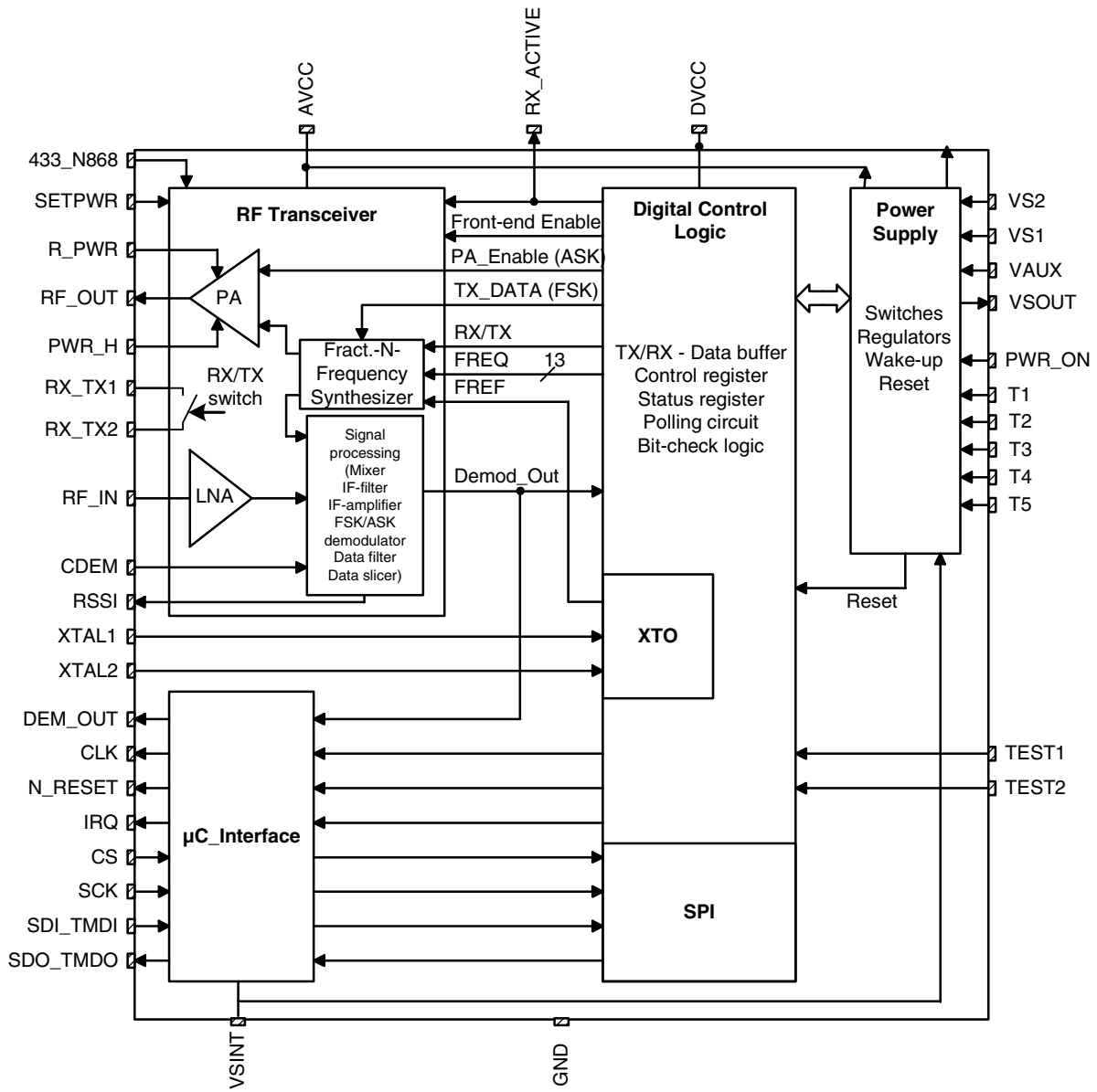
2. Application Circuits

2.1 Typical Remote Control Unit Application with 1 Battery

Figure 2-1 shows a typical 433.92 MHz Remote Control Unit application with one battery. The external components are 11 capacitors, 1 resistor, 2 inductors and a crystal. C_1 to C_4 are 68 nF voltage supply blocking capacitors. C_5 is a 10 nF supply blocking capacitor. C_6 is a 15 nF fixed capacitor used for the internal quasi–peak detector and for the high–pass frequency of the data filter. C_7 to C_{11} are RF matching capacitors in the range of 1 pF to 33 pF. L1 is a matching inductor of about 5.6 nH to 56 nH. L_2 is a feed inductor of about 120 nH. A load capacitor of 9 pF for the crystal is integrated. R_1 is typically 22 kΩ and sets the output power to about 5.5 dBm. The loop antenna's quality factor is somewhat reduced by this application due to the quality factor of L_2 and the RX/TX switch. On the other hand, this lower quality factor is necessary to have a robust design with a bandwidth that is broad enough for production tolerances. Due to the single–ended and ground–referenced design, the loop antenna can be a free–form wire around the application as it is usually employed in remote control uni–directional systems. The ATA5423/ATA5425/ATA5428/ATA5429 provides sufficient isolation and robust pulling behavior of internal circuits from the supply voltage as well as an integrated VCO inductor to allow this. Since the efficiency of a loop antenna is proportional to the square of the surrounded area it is beneficial to have a large loop around the application board with a lower quality factor in order to relax the tolerance specification of the RF components and to get a high antenna efficiency in spite of their lower quality factor.
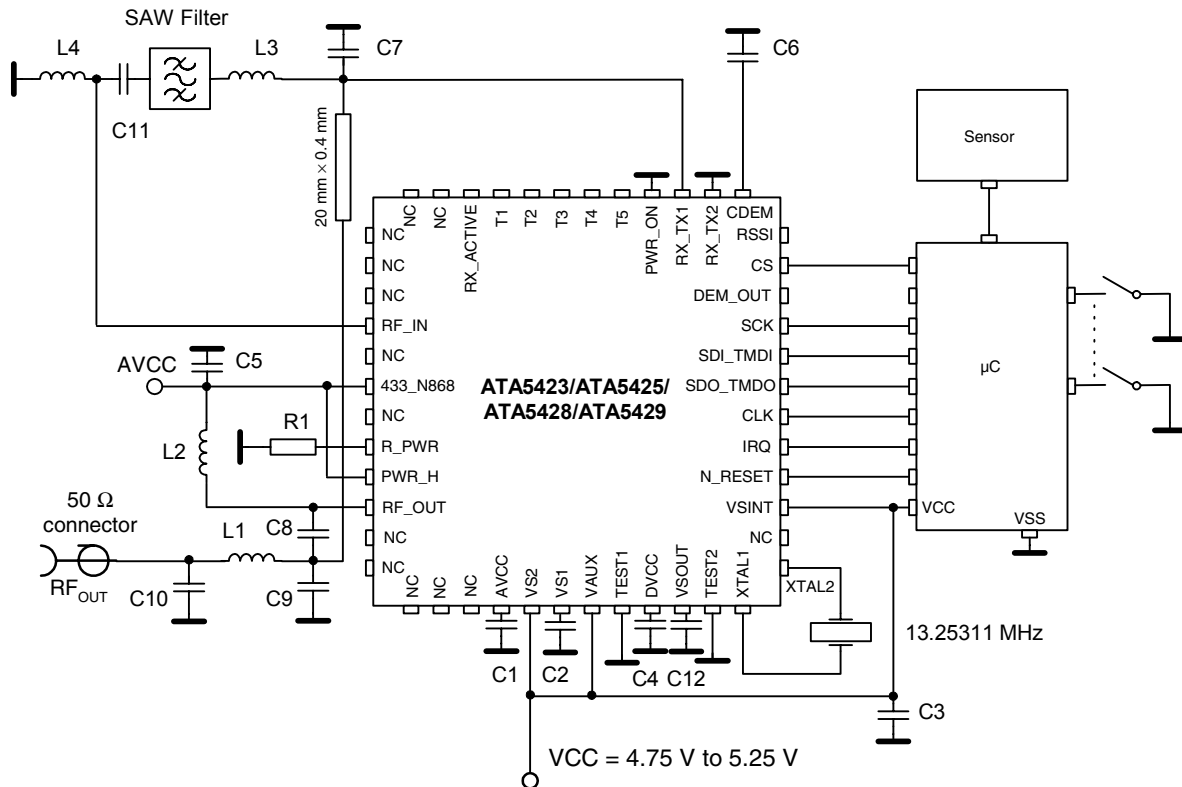
Figure 2-1. Typical Remote Control Unit Application, 433.92 MHz, 1 Battery
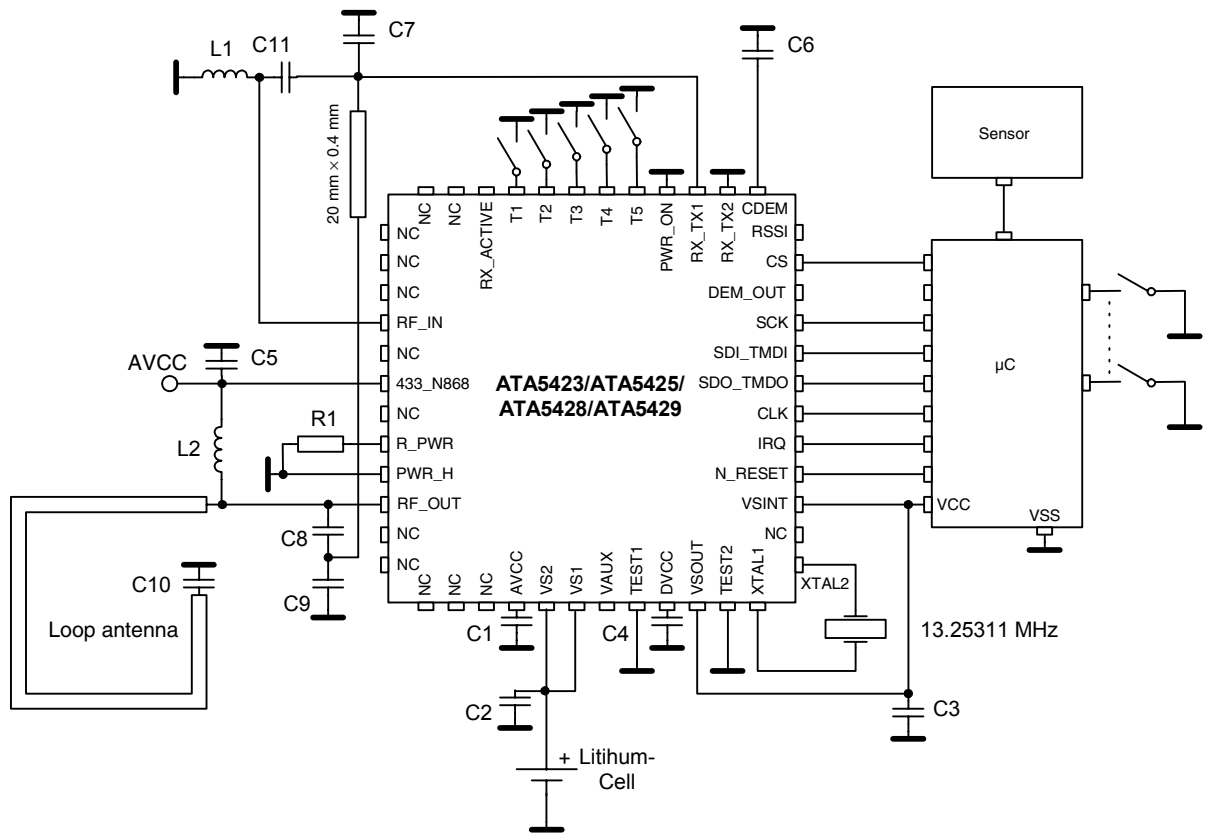
2.2 Typical Base–station Application

Figure 2.2 shows a typical 433.92 MHz V_{CC} = 4.75 V to 5.25 V base–station application. The external components are 12 capacitors, 1 resistor, 4 inductors, a SAW filter, and a crystal. C_1 and C_3 to C_4 are 68 nF voltage supply blocking capacitors. C_2 and C_{12} are 2.2 µF supply blocking capacitors for the internal voltage regulators. C_5 is a 10 nF supply blocking capacitor. C_6 is a 15 nF fixed capacitor used for the internal quasi–peak detector and for the high–pass frequency of the data filter. C_7 to C_{11} are RF matching capacitors in the range of 1 pF to 33 pF. L_2 to L_4 are matching inductors of about 5.6 nH to 56 nH. A load capacitor for the crystal of 9 pF is integrated. R_1 is typically 22 kΩ and sets the output power at RF_OUT to about 10 dBm. Since a quarter wave or PCB antenna, which has high efficiency and wide band operation, is typically used here, it is recommended to use a SAW filter to achieve high sensitivity in case of powerful out–of–band blockers. L_1, C_9 and C_{10} together form a low–pass filter, which is needed to filter out the harmonics in the transmitted signal to meet regulations. An internally regulated voltage at pin VSOUT can be used in case the microcontroller only supports 3.3 V operation, a blocking capacitor with a value of C_{12} = 2.2 µF has to be connected to VSOUT in any case.

Figure 2-2. Typical Base–station Application, 433.92 MHz

2.3 Typical Remote Control Unit Application, 2 Batteries

Figure 2-3 shows a typical 433.92 MHz 2–battery Remote Control Unit application. The external components are 11 capacitors, 1 resistor, 2 inductors and a crystal. C_1 and C_4 are 68 nF voltage supply blocking capacitors. C_2 and C_3 are 2.2 µF supply blocking capacitors for the internal voltage regulators. C_5 is a 10 nF supply blocking capacitor. C_6 is a 15 nF fixed capacitor used for the internal quasi–peak detector and for the high–pass frequency of the data filter. C_7 to C_{11} are RF matching capacitors in the range of 1 pF to 33 pF. L_1 is a matching inductor of about 5.6 nH to 56 nH. L_2 is a feed inductor of about 120 nH. A load capacitor for the crystal of 9 pF is integrated. R_1 is typically 22 kΩ and sets the output power to about 5.5 dBm.

Figure 2-3. Typical Remote Control Unit Application, 433.92 MHz, 2 Batteries
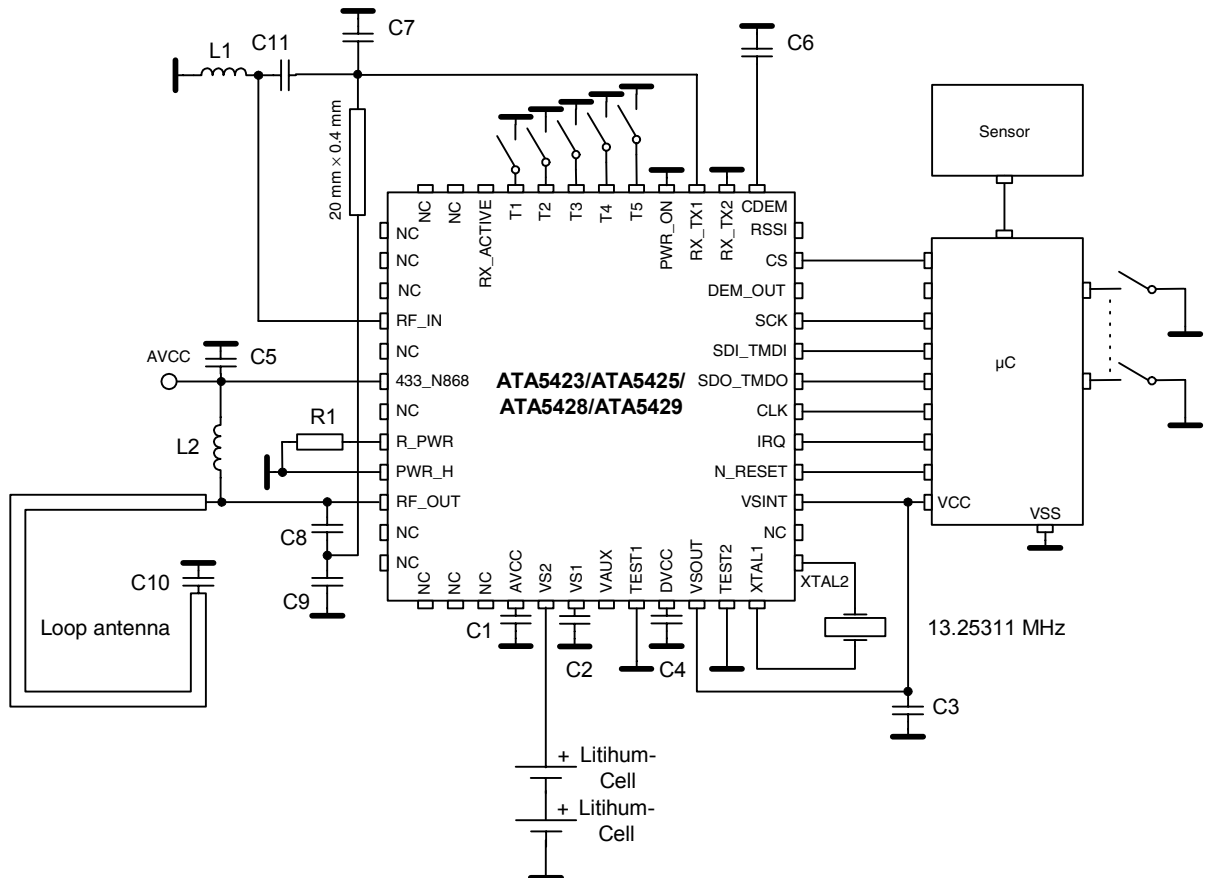
3. RF Transceiver

As seen in Figure 1-3 on page 6, the RF transceiver consists of an LNA (Low–noise Amplifier), PA (Power Amplifier), RX/TX switch, fractional–N frequency synthesizer and the signal processing part with mixer, IF filter, IF amplifier with analog RSSI, FSK/ASK demodulator, data filter, and data slicer.

In receive mode the LNA pre–amplifies the received signal which is converted down to 226 kHz (ATA5423/ATA5428) and 235 kHz (ATA5425/ATA5429), filtered and amplified before it is fed into an FSK/ASK demodulator, data filter, and data slicer. The RSSI (Received Signal Strength Indicator) signal and the raw digital output signal of the demodulator are available at the pins RSSI and DEM_OUT. The demodulated data signal Demod_Out is fed to the digital control logic where it is evaluated and buffered as described in the section "Digital Control Logic" .

In transmit mode, the fractional–N frequency synthesizer generates the TX frequency which is fed to the PA. In ASK mode the PA is modulated by the signal PA_Enable. In FSK mode the PA is enabled and the signal TX_DATA (FSK) modulates the fractional–N frequency synthesizer. The frequency deviation is digitally controlled and internally fixed to about ±16 kHz (see Table 4-1 on page 28 for exact values). The transmit data can also be buffered as described in the section "Digital Control Logic" . A lock detector within the synthesizer ensures that the transmission will start only if the synthesizer is locked.

The RX/TX switch can be used to combine the LNA input and the PA output to a single antenna with a minimum of losses.

Transparent modes without buffering of RX and TX data are also available to allow protocols and coding schemes other than the internally supported Manchester encoding.

3.1 Low–IF Receiver

The receive path consists of a fully integrated low–IF receiver. It fulfills the sensitivity, blocking, selectivity, supply voltage and supply current specification needed to manufacture, for example, an automotive remote control unit without the use of SAW blocking filter (see Figure 2-1 on page 7). In a base–station application the receiver can be used with an additional blocking SAW front–end filter as shown in Figure 2.2 on page 8.

At 433.92 MHz the receiver has a typical system noise figure of 7.0 dB, a system I1dBCP of -30 dBm and a system IIP3 of –20 dBm. There is no AGC or switching of the LNA needed; thus, a better blocking performance is achieved. This receiver uses an IF (Intermediate Frequency) of 226 kHz, the typical image rejection is 30 dB and the typical 3 dB IF filter bandwidth is 185 kHz (f_{IF} = 226 kHz ±92.5 kHz, f_{lo_IF} = 133.5 kHz and f_{hi_IF} = 318.5 kHz). The demodulator needs a signal to Gaussian noise ratio of 8 dB for 20 kBaud Manchester with ±16 kHz frequency deviation in FSK mode; thus, the resulting sensitivity at 433.92 MHz is typically -106 dBm at 20 kBaud Manchester.

Due to the low phase noise and spurious emissions of the synthesizer in receive mode[1] together with the eighth order integrated IF filter, the receiver has a better selectivity and blocking performance than more complex double superhet receivers but without external components and without numerous spurious receiving frequencies.

A low–IF architecture is also less sensitive to second–order intermodulation (IIP2) than direct conversion receivers, where every pulse or AM–modulated signal (especially the signals from TDMA systems like GSM) demodulates to the receiving signal band at second–order non–linearities.

Note: −120 dBC/Hz at ±1 MHz and −75 dBC at ±FREF at 433.92 MHz

3.2   Input Matching at RF_IN

The measured input impedances as well as the values of a parallel equivalent circuit of these impedances can be seen in Table 3-1. The highest sensitivity is achieved with power matching of these impedances to the source impedance of 50 Ω

Table 3-1.   Measured Input Impedances of the RF_IN Pin

f_{RF}/MHz	Z(RF_IN)	R_p//C_p
315	(44–j233)Ω	1278 Ω//2.1 pF
345	TBD	TBD
433.92	(32–j169)Ω	925 Ω//2.1 pF
868.3	(21–j78)Ω	311 Ω//2.2 pF
915	TBD	TBD

The matching of the LNA Input to 50 Ω was done with the circuit shown in Figure 3-1 and with the values given in Table 3-2 on page 12. The reflection coefficients were always ≤10 dB. Note that value changes of C_1 and L_1 may be necessary to compensate for individual board layouts. The measured typical FSK and ASK Manchester code sensitivities with a Bit Error Rate (BER) of 10^{-3} are shown in Table 3-3 and Table 3-4 on page 12. These measurements were done with inductors having a quality factor according to Table 3-2, resulting in estimated matching losses of 1.0 dB at 315 MHz, TBD dB at 345 MHz, 1.2 dB at 433.92 MHz, 0.6 dB at 868.3 MHz and TBD dB at 915 MHz. These losses can be estimated when calculating the parallel equivalent resistance of the inductor with $R_{loss} = 2 \times \pi \times f \times L \times Q_L$ and the matching loss with $10 \log(1 + R_p/R_{loss})$.

With an ideal inductor, for example, the sensitivity at 433.92 MHz/FSK/20 kBaud/ ±16 kHz/Manchester can be improved from -106 dBm to −107.2 dBm. The sensitivity depends on the control logic which examines the incoming data stream. The examination limits must be programmed in control registers 5 and 6. The measurements in Table 3-3 and Table 3-4 on page 12 are based on the values of registers 5 and 6 according to Table 9-3 on page 61.

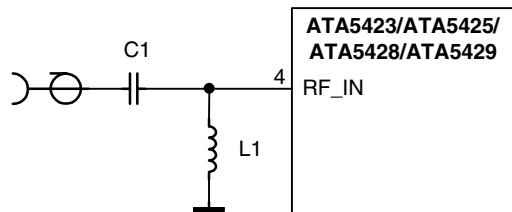**Figure 3-1.**   Input Matching to 50 Ω

Table 3-2. Input Matching to 50 Ω

f_{RF}/MHz	C_1/pF	L_1/nH	Q_{L1}
315	2.2	56	43
345	TBD	TBD	TBD
433.92	1.8	27	40
868.3	1.2	6.8	58
915	TBD	TBD	TBD

Table 3-3. Measured Sensitivity FSK, ±16 kHz, Manchester, dBm, BER = 10^{-3}

| RF Frequency	BR_Range_0 1.0 kBaud	BR_Range_0 2.4 kBaud	BR_Range_1 5.0 kBaud	BR_Range_2 10 kBaud	BR_Range_3 20 kBaud
315 MHz	−110.0 dBm	−110.5 dBm	−109.0 dBm	−108.0 dBm	−107.0 dBm
345 MHz	TBD	TBD	TBD	TBD	TBD
433.92 MHz	−109.0 dBm	−109.5 dBm	−108.0 dBm	−107.0 dBm	−106.0 dBm
868.3 MHz	−106.0 dBm	−106.5 dBm	−105.5 dBm	−104.0 dBm	−103.5 dBm
915 MHz	TBD	TBD	TBD	TBD	TBD

Table 3-4. Measured Sensitivity 100% ASK, Manchester, dBm, BER = 10^{-3}

RF Frequency	BR_Range_0 1.0 kBaud	BR_Range_0 2.4 kBaud	BR_Range_1 5.0 kBaud	BR_Range_2 10 kBaud
315 MHz	−117.0 dBm	−117.5 dBm	−115 dBm	−113.5 dBm
345 MHz	TBD	TBD	TBD	TBD
433.92 MHz	−116.0 dBm	−116.5 dBm	−114.0 dBm	−112.5 dBm
868.3 MHz	−112.5 dBm	−113.0 dBm	−111.5 dBm	−109.5 dBm
915 MHz	TBD	TBD	TBD	TBD

3.3 Sensitivity versus Supply Voltage, Temperature and Frequency Offset

To calculate the behavior of a transmission system it is important to know the reduction of the sensitivity due to several influences. The most important are frequency offset due to crystal oscillator (XTO) and crystal frequency (XTAL) errors, temperature and supply voltage dependency of the noise figure and IF filter bandwidth of the receiver. Figure 3-2 shows the typical sensitivity at 433.92 MHz/FSK/20kBaud/±16 kHz/Manchester versus the frequency offset between transmitter and receiver with T_{amb} = -40°C, +25°C and +105°C and supply voltage VS1 = VS2 = 2.4 V, 3.0 V and 3.6 V.

Figure 3-2. Measured Sensitivity 433.92 MHz/FSK/20 kBaud/±16 kHz/Manchester versus Frequency Offset, Temperature and Supply Voltage
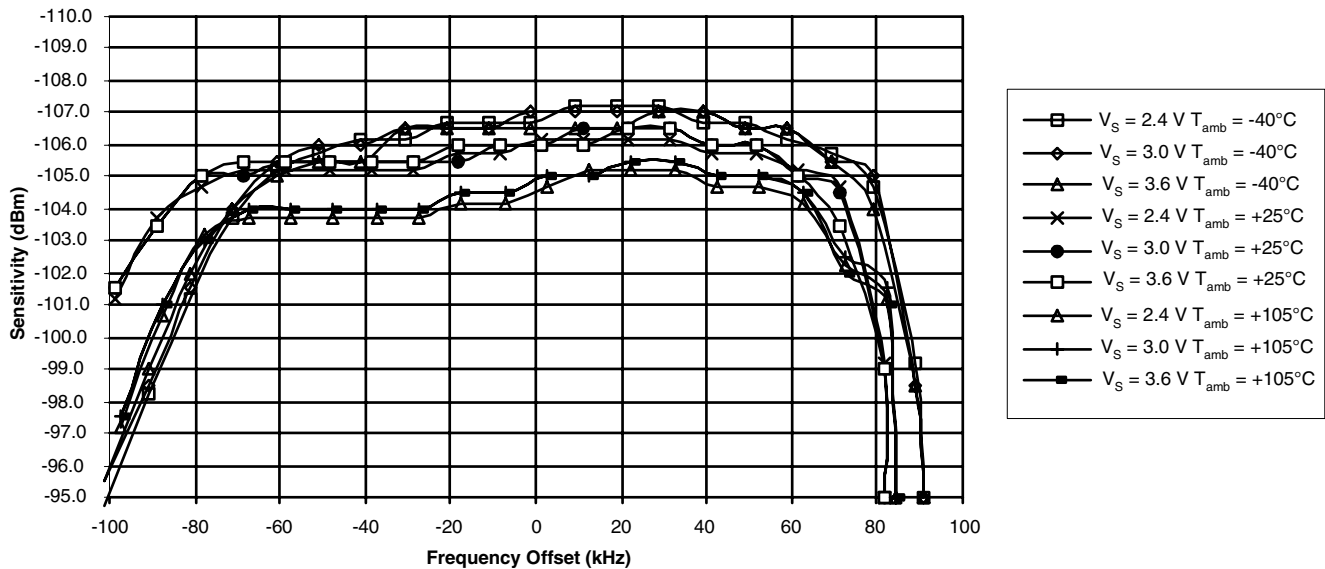
As can be seen in Figure 3-2 on page 13 the supply voltage has almost no influence. The temperature has an influence of about +1.5/–0.7 dB, and a frequency offset of ±65 kHz also influences by about ±1 dB. All these influences, combined with the sensitivity of a typical IC, are then within a range of -103.7 dBm and –107.3 dBm over temperature, supply voltage and frequency offset which is -105.5 dBm ±1.8dB. The integrated IF filter has an additional production tolerance of only ±7 kHz, hence, a frequency offset between the receiver and the transmitter of ±58 kHz can be accepted for XTAL and XTO tolerances.

Note: For the demodulator used in the ATA5423/ATA5425, the tolerable frequency offset does not change with the data frequency, hence, the value of ±58 kHz is valid for up to 1 kBaud. (TBD)

This small sensitivity spread over supply voltage, frequency offset and temperature is very unusual in such a receiver. It is achieved by an internal, very fast and automatic frequency correction in the FSK demodulator after the IF filter, which leads to a higher system margin. This frequency correction tracks the input frequency very quickly; if, however, the input frequency makes a larger step (for example, if the system changes between different communication partners), the receiver has to be restarted. This can be done by switching back to IDLE mode and then again to RX mode. For that purpose, an automatic mode is also available. This automatic mode switches to IDLE mode and back into RX mode every time a bit error occurs. (See "Digital Control Logic" on page 36.)

3.4 Frequency Accuracy of the Crystals

The XTO is an amplitude regulated Pierce oscillator with integrated load capacitors. The initial tolerances (due to the frequency tolerance of the XTAL, the integrated capacitors on XTAL1, XTAL2 and the XTO's initial transconductance gm) can be compensated to a value within ±0.5 ppm by measuring the CLK output frequency and programming the control registers 2 and 3 (see Table 7-7 on page 39 and Table 7-10 on page 40). The XTO then has a remaining influence of less than ±2 ppm over temperature and supply voltage due to the band gap controlled gm of the XTO.

The needed frequency stability of the used crystals over temperature and aging is hence ±58 kHz/433.92 MHz – 2 × ±2.5 ppm = ±128.66 ppm for 433.92 MHz and ±58 kHz/868.3 MHz – 2 × ±2.5 ppm = ±61.8 ppm for 868.3 MHz. 315, 345, 915 MHz (TBD). Thus, the crystals used in the receiver and transmitter each need to be better than ±64.33 ppm for 433.92 MHz and ±30.9 ppm for 868.3 MHz. 315, 345, 915MHz (TBD). In access control systems it may be advantageous to have a tighter tolerance at the base station in order to relax the requirement for the remote control unit.

3.5 RX Supply Current versus Temperature and Supply Voltage

Table 3-5 shows the typical supply current at 433.92 MHz of the transceiver in RX mode versus supply voltage and temperature with VS = VS1 = VS2. As can be seen, the supply current at 2.4 V and –40°C is less than the typical supply current; this is useful because this is also the operation point where a lithium cell has the worst performance. The typical supply current at 315 MHz, 345 MHz, 868.3 MHz or 915 MHz in RX mode is about the same as for 433.92 MHz

Table 3-5. Measured 433.92 MHz Receive Supply Current in FSK Mode

VS = VS1 = VS2	2.4 V	3.0 V	3.6 V
$T_{amb} = -40°C$	8.4 mA	8.8 mA	9.2 mA
$T_{amb} = 25°C$	9.9 mA	10.3 mA	10.8 mA
$T_{amb} = 85°C$	11.4 mA	11.9 mA	12.4 mA

3.6 Blocking, Selectivity

As can be seen in Figure 3-3 and Figure 3-4 on page 15, the receiver can receive signals 3 dB higher than the sensitivity level in the presence of very large blockers of –47 dBm/–34 dBm with small frequency offsets of ±1/ ±10 MHz.

Figure 3-3 shows narrow band blocking and Figure 3-4 wide band blocking characteristics. The measurements were done with a signal of 433.92 MHz/FSK/20 kBaud/±16 kHz/ Manchester, and with a level of -106 dBm + 3 dB = -103 dBm which is 3 dB above the sensitivity level. The figures show how much larger than –103dBm a continuous wave signal can be before the BER is higher than 10^{-3}. The measurements were done at the 50 Ω input according to Figure 3-1 on page 11. At 1 MHz, for example, the blocker can be 56 dB higher than –103 dBm which is -103 dBm + 56 dB = –47 dBm. These values, together with the good intermodulation performance, avoid the need for a SAW filter in the remote control unit application.

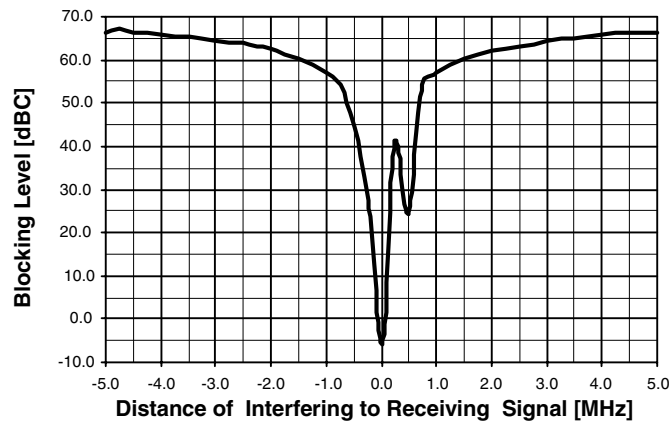**Figure 3-3.** Narrow Band 3 dB Blocking Characteristic at 433.92 MHz

Figure 3-4. Wide Band 3 dB Blocking Characteristic at 433.92 MHz
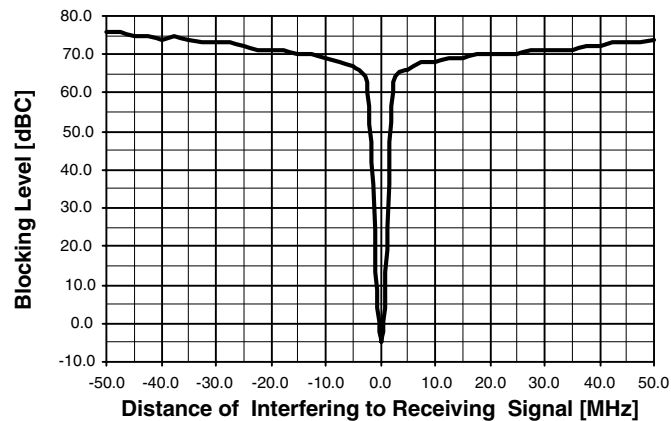

Figure 3-5 on page 16 shows the blocking measurement close to the received frequency to illustrate the selectivity and image rejection. This measurement was done 6 dB above the sensitivity level with a useful signal of 433.92 MHz/FSK/20kBaud/±16 kHz/ Manchester with a level of -106 dBm + 6 dB = −100 dBm. The figure shows to which extent a continuous wave signal can surpass −100 dBm until the BER is higher than 10^{-3}. For example, at 1 MHz the blocker can then be 59 dB higher than −100 dBm which is -100 dBm + 59 dB = −41 dBm.

Table 3-6 on page 16 shows the blocking performance measured relative to −100 dBm for some other frequencies. Note that sometimes the blocking is measured relative to the sensitivity level (dBS) instead of the carrier (dBC).

Table 3-6. Blocking 6 dB Above Sensitivity Level with BER < 10^{-3}

Frequency Offset	Blocker Level	Blocking
+0.75 MHz	−45 dBm	55 dBC/61 dBS
−0.75 MHz	−45 dBm	55 dBC/61 dBS
+1.5 MHz	−38 dBm	62 dBC/68 dBS
−1.5 MHz	−38 dBm	62 dBC/68 dBS
+10 MHz	−30 dBm	70 dBC/76 dBS
−10 MHz	−30 dBm	70 dBC/76 dBS

The ATA5423/ATA5425/ATA5428/ATA5429 can also receive FSK and ASK modulated signals if they are much higher than the I1dBCP. It can typically receive useful signals at 10 dBm. This is often referred to as the nonlinear dynamic range which is the maximum to minimum receiving signal and is 116 dB for 20 kBaud Manchester. This value is useful if two transceivers have to communicate and are very close to each other.

Figure 3-5. Close In 6 dB Blocking Characteristic and Image Response at 433.92 MHz
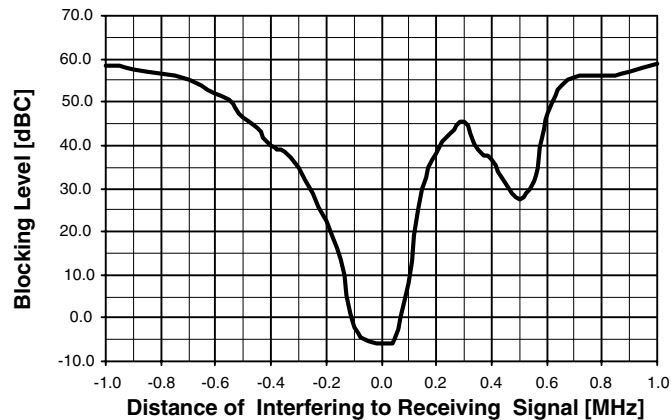
This high blocking performance even makes it possible for some applications using quarter wave whip antennas to use a simple LC band–pass filter instead of a SAW filter in the receiver. When designing such an LC filter take into account that the 3 dB blocking at 433.92 MHz/2 = 216.96 MHz is 43 dBC and at 433.92 MHz/3 = 144.64 MHz is 48 dBC and at $2 \times$ (433.92 MHz + 226 kHz) + −226 kHz = 868.066 MHz/868.518 MHz is 56 dBC. And especially that at $3 \times$ (433.92 MHz + 226 kHz) + 226 kHz = 1302.664 MHz the receiver has its second LO harmonic receiving frequency with only 12 dBC blocking.

3.7 In–band Disturbers, Data Filter, Quasi–peak Detector, Data Slicer

If a disturbing signal falls into the received band or a blocker is not continuous wave, the performance of a receiver strongly depends on the circuits after the IF filter. The demodulator, data filter and data slicer are important, in that case.

The data filter of the ATA5423/ATA5425/ATA5428/ATA5429 implies a quasi–peak detector. This results in a good suppression of the above mentioned disturbers and exhibits a good carrier to Gaussian noise performance. The required useful signal to disturbing signal ratio to be received with a BER of 10^{-3} is less than 12 dB in ASK mode and less than 3 dB (BR_Range_0 … BR_Range_2)/6 dB (BR_Range_3) in FSK mode. Due to the many different waveforms possible these numbers are measured for signal as well as for disturbers with peak amplitude values. Note that these values are worst case values and are valid for any type of modulation and modulating frequency of the disturbing signal as well as the receiving signal. For many combinations, lower carrier to disturbing signal ratios are needed.

3.8 DEM_OUT Output

The internal raw output signal of the demodulator Demod_Out is available at pin DEM_OUT. DEM_OUT is an open drain output and must be connected to a pull–up resistor if it is used (typically 100 kΩ) otherwise no signal is present at that pin.

3.9 RSSI Output

The output voltage of the pin RSSI is an analog voltage, proportional to the input power level. Using the RSSI output signal, the signal strength of different transmitters can be distinguished. The usable dynamic range of the RSSI amplifier is 70 dB, the input power range $P(RF_{IN})$ is –115 dBm to –45 dBm and the gain is 8 mV/dB. Figure 3-6 shows the RSSI characteristic of a typical device at 433.92 MHz with VS1 = VS2 = 2.4 to 3.6 V and T_{amb} = –40°C to +85°C with a matched input according to Table 3-2 on page 12 and Figure 3-1 on page 11. At 915 MHz about TBD dB and at 868.3 MHz about 2.7 dB more signal level, at 345 MHz about TBD dB and at 315 MHz about 1 dB less signal level is needed for the same RSSI results.

Figure 3-6. Typical RSSI Characteristic versus Temperature and Supply Voltage
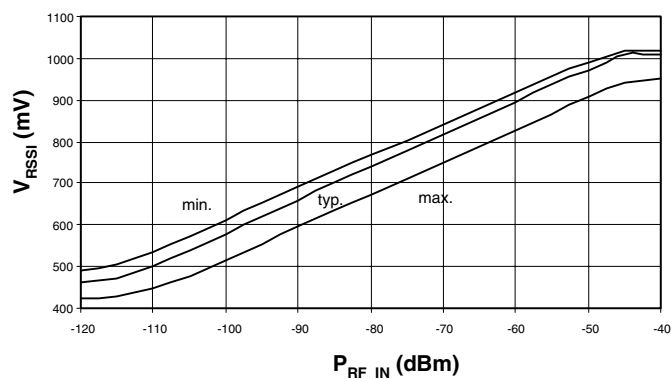
3.10 Frequency Synthesizer

The synthesizer is a fully integrated fractional–N design with internal loop filters for receive and transmit mode. The XTO frequency f_{XTO} is the reference frequency FREF for the synthesizer. The bits FR0 to FR12 in control registers 2 and 3 (see Table 7-7 on page 39 and Table 7-10 on page 40) are used to adjust the deviation of f_{XTO}. In transmit mode, at 433.92 MHz, the carrier has a phase noise of –111 dBC/Hz at 1 MHz and spurious emissions at FREF of -66 dBC with a high PLL loop bandwidth allowing the direct modulation of the carrier with 20 kBaud Manchester data. Due to the closed loop modulation any spurious emissions caused by this modulation are effectively filtered out as can be seen in Figure 3-9 on page 20. In RX mode the synthesizer has a phase noise of -120 dBC/Hz at 1 MHz and spurious emissions of -75 dBC.

The initial tolerances of the crystal oscillator due to crystal tolerances, internal capacitor tolerances and the parasitics of the board have to be compensated at manufacturing setup with control registers 2 and 3 as can be seen in Table 4-1 on page 28. The other control words for the synthesizer needed for ASK, FSK and receive/transmit switching are calculated internally. The RF (Radio Frequency) resolution is equal to the XTO frequency divided by 16384 which is 777.1 Hz at 315.0 MHz, 851.1 Hz at 345.0 MHz, 808.9 Hz at 433.92 MHz, 818.6 Hz at 868.3 MHz and 862.6 Hz at 915.0 MHz.

For the multi–channel system the frequency control word FREQ in control registers 2 and 3 can be programmed in the range of 1000 to 6900, this is equivalent to a programmable tuning range of ±2.5 MHz hence every frequency within the 315 MHz, 345 MHz, 433 MHz, 868 MHz and 915 MHz ISM bands can be programmed as receive and as transmit frequency, and the position of channels within these ISM bands can be chosen arbitrarily (see Table 4-1).

Care must be taken as to the harmonics of the CLK output signal as well as to the harmonics produced by a microprocessor clocked with it, since these harmonics can disturb the reception of signals. In a single–channel system, using FREQ = 3803 to 4053 ensures that harmonics of this signal do not disturb the receive mode.

3.11 FSK/ASK Transmission

Due to the fast modulation capability of the synthesizer and the high resolution, the carrier can be internally FSK modulated, which simplifies the application of the transceiver. The deviation of the transmitted signal is ±20 digital frequency steps of the synthesizer which is equal to ±15.54 kHz for 315 MHz, ±17.02 kHz for 345 MHz, ±16.17 kHz for 433.92 MHz, ±16.37 kHz for 868.3 MHz and ±17.25 kHz for 915 MHz.

Due to closed loop modulation with PLL filtering the modulated spectrum is very clean, meeting ETSI and CEPT regulations when using a simple LC filter for the power amplifier harmonics as it is shown in Figure 2.2 on page 8. In ASK mode the frequency is internally connected to the center of the FSK transmission and the power amplifier is switched on and off to perform the modulation. Figure 3-7 on page 19 to Figure 3-9 on page 20 show the spectrum of the FSK modulation with pseudo–random data with 20 kBaud/±16.17 kHz/Manchester and 5 dBm output power.

Figure 3-7. FSK–modulated TX Spectrum (433.92MHz/20 kBaud/±16.17 kHz/Manchester Code)
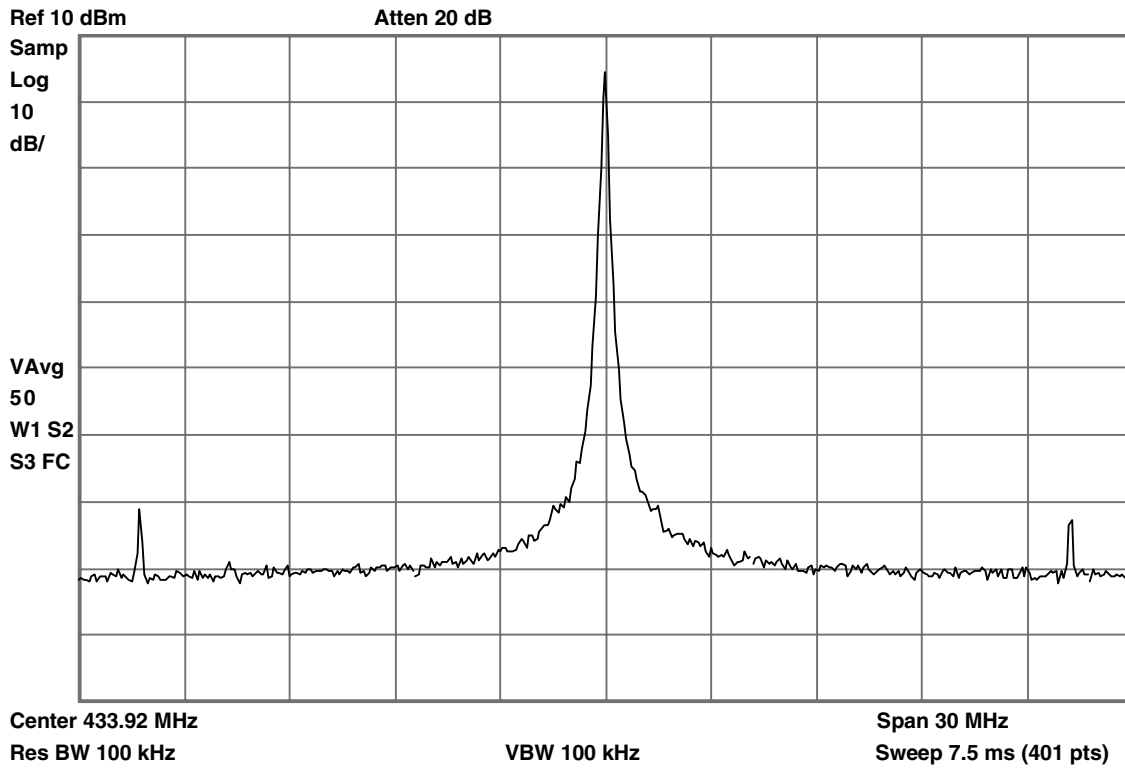
Ref 10 dBm   Atten 20 dB

Samp
Log
10
dB/

VAvg
50
W1 S2
S3 FC

Center 433.92 MHz   Span 30 MHz
Res BW 100 kHz   VBW 100 kHz   Sweep 7.5 ms (401 pts)

Figure 3-8. Unmodulated TX Spectrum 433.92 MHz – 16.17 kHz (f_{FSK_L})

Ref 10 dBm   Atten 20 dB

Samp
Log
10
dB/

VAvg
50
W1 S2
S3 FC

Center 433.92 MHz   Span 1 MHz
Res BW 10 kHz   VBW 10 kHz   Sweep 27.5 ms (401 pts)

19
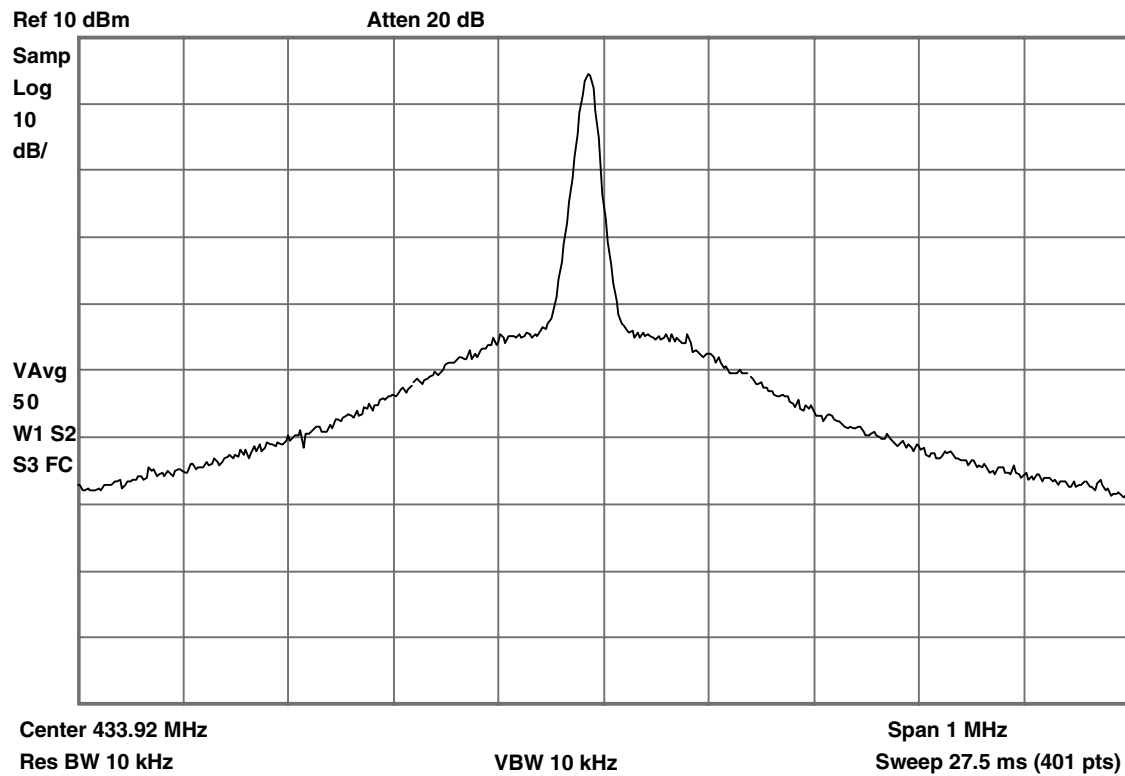
Figure 3-9. FSK–modulated TX Spectrum (433.92MHz/20 kBaud/±16.17 kHz/Manchester Code)

Ref 10 dBm   Atten 20 dB
Samp
Log
10
dB/

VAvg
50
W1 S2
S3 FC

Center 433.92 MHz   Span 1 MHz
Res BW 10 kHz   VBW 10 kHz   Sweep 27.5 ms (401 pts)
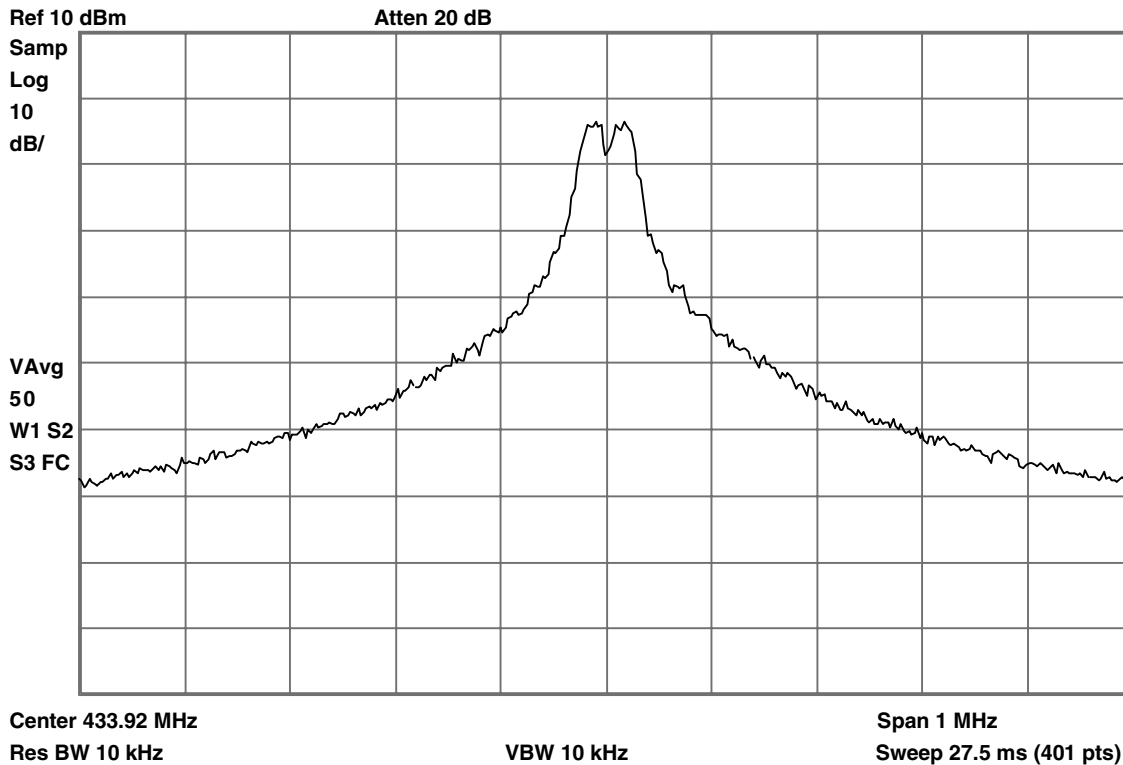
3.12   Output Power Setting and PA Matching at RF_OUT

The Power Amplifier (PA) is a single–ended open collector stage which delivers a current pulse which is nearly independent of supply voltage, temperature and tolerances due to band gap stabilization. Resistor R_1, see Figure 3-10 on page 21, sets a reference current which controls the current in the PA. A higher resistor value results in a lower reference current, a lower output power and a lower current consumption of the PA. The usable range of R_1 is 15 kΩ to 56 kΩ Pin PWR_H switches the output power range between about 0 dBm to 5 dBm (PWR_H = GND) and 5 dBm to 10 dBm (PWR_H = AVCC) by multiplying this reference current by a factor 1 (PWR_H = GND) and 2.5 (PWR_H = AVCC), which corresponds to about 5 dB more output power.

If the PA is switched off in TX mode, the current consumption without output stage with VS1 = VS2 = 3 V, T_{amb} = 25°C is typically 6.5 mA for 868.3 MHz and 6.95 mA for 315 MHz and 433.92 MHz.

The maximum output power is achieved with optimum load resistances R_{Lopt} according to Table 3-7 on page 22 with compensation of the 1.0 pF output capacitance of the RF_OUT pin by absorbing it into the matching network consisting of L_1, C_1, C_3 as shown in Figure 3-10 on page 21. There must also be a low resistive DC path to AVCC to deliver the DC current of the power amplifier's last stage. The matching of the PA output was done with the circuit shown in Figure 3-10 on page 21 with the values in Table 3-7 on page 22. Note that value changes of these elements may be necessary to compensate for individual board layouts.

Example:
According to Table 3-7 on page 22, with a frequency of 433.92 MHz and output power of 11 dBm the overall current consumption is typically 17.8 mA; hence, the PA needs 17.8 mA - 6.95 mA = 10.85 mA in this mode, which corresponds to an overall power amplifier efficiency of the PA of $(10^{(11dBm/10)} \times 1 \text{ mW})/(3 \text{ V} \times 10.85 \text{ mA}) \times 100\% = 38.6\%$ in this case.

Using a higher resistor in this example of $R_1 = 1.091 \times 22 \text{ k}\Omega = 24 \text{ k}\Omega$ results in 9.1% less current in the PA of 10.85 mA/1.091 = 9.95 mA and $10 \times \log(1.091) = 0.38$ dB less output power if using a new load resistance of $300 \Omega \times 1.091 = 327 \Omega$. The resulting output power is then 11 dBm - 0.38 dB = 10.6 dBm and the overall current consumption is 6.95 mA + 9.95 mA = 16.9 mA.

The values of Table 3-7 on page 22 were measured with standard multi–layer chip inductors with quality factors Q according to Table 3-7 on page 22. Looking to the 433.92 MHz/11 dBm case with the quality factor of $Q_{L1} = 43$ the loss in this inductor is estimated with the parallel equivalent resistance of the inductor $R_{loss} = 2 \times \pi \times f \times L \times Q_{L1}$ and the matching loss with $10 \log (1 + R_{Lopt}/R_{loss})$ which is equal to 0.32 dB losses in this inductor. Taking this into account, the PA efficiency is then 42% instead of 38.6%.

Be aware that the high power mode (PWR_H = AVCC) can only be used with a supply voltage higher than 2.7 V, whereas the low power mode (PWR_H = GND) can be used down to 2.4 V as can be seen in the "Electrical Characteristics: General" on page 66.

The supply blocking capacitor C_2 (10 nF) has to be placed close to the matching network because of the RF current flowing through it.

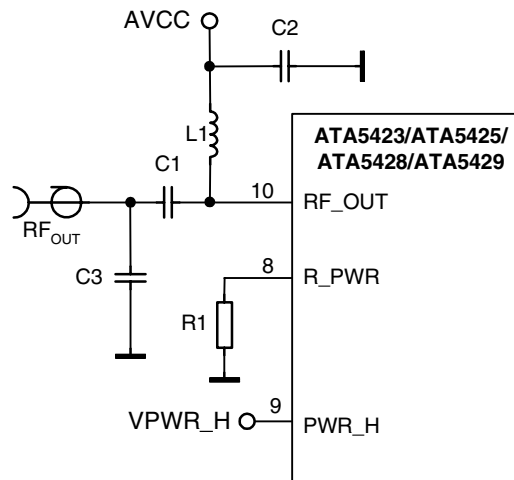**Figure 3-10.** Power Setting and Output Matching

Table 3-7. Measured Output Power and Current Consumption with VS1 = VS2 = 3 V, T$_{amb}$ = 25°C

Frequency (MHz)	TX Current (mA)	Output Power (dBm)	R1 (kΩ)	VPWR_H	R$_{Lopt}$ (Ω)	L1 (nH)	Q$_{L1}$	C1 (pF)	C3 (pF)
315	8.5	0.4	56	GND	2500	82	28	1.5	0
315	10.5	5.7	27	GND	920	68	32	2.2	0
315	16.7	10.5	27	AVCC	350	56	35	3.9	0
345				GND					
345				GND					
345				AVCC					
433.92	8.6	0.1	56	GND	2300	56	40	0.75	0
433.92	11.2	6.2	22	GND	890	47	38	1.5	0
433.92	17.8	11	22	AVCC	300	33	43	2.7	0
868.3	9.3	−0.3	33	GND	1170	12	58	1.0	3.3
868.3	11.5	5.4	15	GND	471	15	54	1.0	0
868.3	16.3	9.5	22	AVCC	245	10	57	1.5	0
915				GND					
915				GND					
915				AVCC					

3.13 Output Power and TX Supply Current versus Supply Voltage and Temperature

Table 3-8 on page 22 shows the measurement of the output power for a typical device with VS = VS1 = VS2 in the 433.92 MHz and 6.2 dBm case versus temperature and supply voltage measured according to Figure 3-10 on page 21 with components according to Table 3-7. As opposed to the receiver sensitivity, the supply voltage has here the major impact on output power variations because of the large signal behavior of a power amplifier. Thus, a two battery system with voltage regulator or a 5 V system shows much less variation than a 2.4 V to 3.6 V one battery system because the supply voltage is then well within 3.0 V and 3.6 V.

The reason is that the amplitude at the output RF_OUT with optimum load resistance is AVCC - 0.4 V and the power is proportional to (AVCC − 0.4 V)^2 if the load impedance is not changed. This means that the theoretical output power reduction if reducing the supply voltage from 3.0 V to 2.4 V is 10 log ((3 V − 0.4 V)^2/(2.4 V − 0.4 V)^2) = 2.2 dB. Table 3-8 shows that principle behavior in the measurement. This is not the same case for higher voltages, since here increasing the supply voltage from 3 V to 3.6 V should theoretical increase the power by 1.8 dB; but a gain of only 0.8 dB in the measurement shows that the amplitude does not increase with the supply voltage because the load impedance is optimized for 3 V and the output amplitude stays more constant.

Table 3-8. Measured Output Power and Supply Current at 433.92 MHz, PWR_H = GND

VS =	2.4 V	3.0 V	3.6 V
T$_{amb}$ = −40°C	10.19 mA 3.8 dBm	10.19 mA 5.5 dBm	10.78 mA 6.2 dBm
T$_{amb}$ = +25°C	10.62 mA 4.6 dBm	11.19 mA 6.2 dBm	11.79 mA 7.1 dBm
T$_{amb}$ = +85°C	11.4 mA 3.8 dBm	12.02 mA 5.4 dBm	12.73 mA 6.3 dBm

Table 3-9 shows the relative changes of the output power of a typical device compared to 3.0 V/25°C. As can be seen, a temperature change to –40°C as well as to +85°C reduces the power by less than 1 dB due to the band gap regulated output current. Measurements of all the cases in Table 3-7 on page 22 over temperature and supply voltage have shown about the same relative behavior as shown in Table 3-9.

Table 3-9. Measurements of Typical Output Power Relative to 3 V/25°C

| VS =	2.4 V	3.0 V	3.6 V
T_{amb} = −40°C	−2.4 dB	−0.7 dB	0 dB
T_{amb} = +25°C	−1.6 dB	0 dB	+0.9 dB
T_{amb} = +85°C	−2.4 dB	−0.8 dB	+0.1 dB

3.14 RX/TX Switch

The RX/TX switch decouples the LNA from the PA in TX mode, and directs the received power to the LNA in RX mode. To do this, it has a low impedance to GND in TX mode and a high impedance to GND in RX mode. To design a proper RX/TX decoupling, a linear simulation tool for radio frequency design together with the measured device impedances of Table 3-1 on page 11, Table 3-7 on page 22, Table 3-10 and Table 3-11 on page 24 should be used, but the exact element values have to be found on–board. Figure 3-11 shows an approximate equivalent circuit of the switch. The principal switching operation is described here according to the application of Figure 2-1 on page 7. The application of Figure 2.2 on page 8 works similarly.

Table 3-10. Impedance of the RX/TX Switch RX_TX2 Shorted to GND

Frequency	Z(RX_TX1) TX Mode	Z(RX_TX1) RX Mode
315 MHz	(4.8 + j3.2) Ω	(11.3 − j214) Ω
345 MHz	TBD	TBD
433.92 MHz	(4.5 + j4.3) Ω	(10.3 − j153) Ω
868.3 MHz	(5 + j9) Ω	(8.9 − j73) Ω
915 MHz	TBD	TBD

Figure 3-11. Equivalent Circuit of the Switch
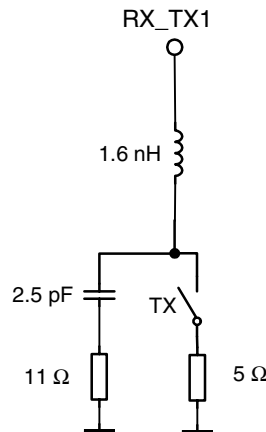
3.15 Matching Network in TX Mode

In TX mode the 20 mm long and 0.4 mm wide transmission line which is much shorter than $\lambda/4$ is approximately switched in parallel to the capacitor C_9 to GND. The antenna connection between C_8 and C_9 has an impedance of about 50 Ω locking from the transmission line into the loop antenna with pin RF_OUT, L_2, C_{10}, C_8 and C_9 connected (using a C_9 without the added 7.6 pF as discussed later). The transmission line can be approximated with a 16 nH inductor in series with a 1.5 Ω resistor, the closed switch can be approximated according to Table 3-10 on page 23 with the series connection of 1.6 nH and 5 Ω in this mode. To have a parallel resonant high impedance circuit with little RF power going into it looking from the loop antenna into the transmission line a capacitor of about 7.6 pF to GND is needed at the beginning of the transmission line (this capacitor is later absorbed into C_9 which is then higher, as needed for 50 Ω transformation). To keep the 50 Ω impedance in RX mode at the end of this transmission line, C_7 also has to be about 7.6 pF. This reduces the TX power by about 0.5 dB at 433.92 MHz compared to the case the where the LNA path is completely disconnected.

3.16 Matching Network in RX Mode

In RX mode the RF_OUT pin has a high impedance of about 7 kΩ in parallel with 1.0 pF at 433.92 MHz as can be seen in Table 3-11. This, together with the losses of the inductor L_2 with 120 nH and $Q_{L_2} = 25$, gives about 3.7 kΩ loss impedance at RF_OUT. Since the optimum load impedance in TX mode for the power amplifier at RF_OUT is 890 Ω the loss associated with the inductor L_2 and the RF_OUT pin can be estimated to be $10 \times \log(1 + 890/3700) = 0.95$ dB compared to the optimum matched loop antenna without L_2 and RF_OUT. The switch represents, in this mode at 433.92 MHz, approximately an inductor of 1.6 nH in series with the parallel connection of 2.5 pF and 2.0 kΩ. Since the impedance level at pin RX_TX1 in RX mode is about 50 Ω this only negligibly dampens the received signal (by about 0.1 dB). When matching the LNA to the loop antenna, the transmission line and the 7.6 pF part of C_9 have to be taken into account when choosing the values of C_{11} and L_1 so that the impedance seen from the loop antenna into the transmission line with the 7.6 pF capacitor connected is 50 Ω. Since the loop antenna in RX mode is loaded by the LNA input impedance, the loaded Q of the loop antenna is lowered by about a factor of 2 in RX mode; hence the antenna bandwidth is higher than in TX mode.

Table 3-11. Impedance RF_OUT Pin in RX Mode

Frequency	Z(RF_OUT)RX	$R_P//C_P$
315 MHz	(36 – j502) Ω	7 kΩ//1.0 pF
345 MHz	TBD	TBD
433.92 MHz	(19 – j366) Ω	7 kΩ//1.0 pF
868.3 MHz	(2.8 – j141) Ω	7 kΩ//1.3 pF
915 MHz	TBD	TBD

Note that if matching to 50 Ω, like in Figure 2.2 on page 8, a high Q wire–wound inductor with a Q > 70 should be used for L_2 to minimize its contribution to RX losses that will otherwise be dominant. The RX and TX losses will be in the range of 1.0 dB there.

4. XTO

The XTO is an amplitude–regulated Pierce oscillator type with integrated load capacitances ($2 \times$ 18 pF with a tolerance of ±17%) hence C_{Lmin} = 7.4 pF and C_{Lmax} = 10.6 pF. The XTO oscillation frequency f_{XTO} is the reference frequency FREF for the fractional–N synthesizer. When designing the system in terms of receiving and transmitting frequency offset, the accuracy of the crystal and XTO have to be considered.

The synthesizer can adjust the local oscillator frequency for the initial frequency error in f_{XTO}. This is done at nominal supply voltage and temperature with the control registers 2 and 3 (see Table 7-7 and Table 7-10). The remaining local oscillator tolerance at nominal supply voltage and temperature is then < ±0.5 ppm. The XTO's gm has very low influence of less than ±2 ppm on the frequency at nominal supply voltage and temperature.

In a single channel system less than ±150 ppm should be corrected to avoid that harmonics of the CLK output disturb the receive mode. If the CLK is not used or if it is carefully laid out on the application PCB (as needed for multi channel systems), more than ±150 ppm can be compensated.

Over temperature and supply voltage, the XTO's additional pulling is only ±2 ppm. The XTAL versus temperature and its aging is then the main source of frequency error in the local oscillator.

The XTO frequency depends on XTAL properties and the load capacitances $C_{L1, 2}$ at pin XTAL1 and XTAL2. The pulling of f_{XTO} from the nominal f_{XTAL} is calculated using the following formula:

$$P = \frac{C_m}{2} \times \frac{C_{LN} - C_L}{(C_0 + C_{LN}) \times (C_0 + C_L)} \times 10^6 \text{ ppm.}$$

C_m is the crystal's motional, C_0 the shunt and C_{LN} the nominal load capacitance of the XTAL found in its data sheet. C_L is the total actual load capacitance of the crystal in the circuit and consists of C_{L1} and C_{L2} in series connection.

Figure 4-1. XTAL with Load Capacitance
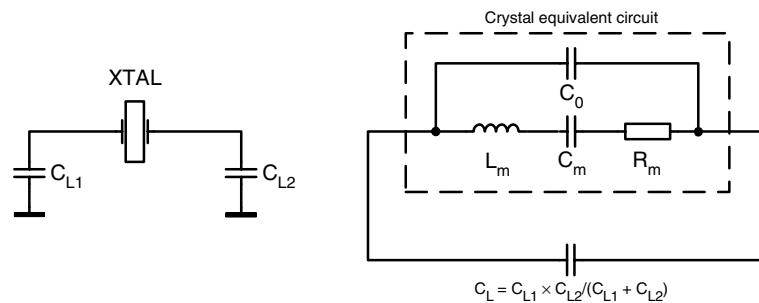
With $C_m \leq 14$ fF, $C_0 \geq 1.5$ pF, C_{LN} = 9 pF and C_L = 7.4 pF to 10.6 pF, the pulling amounts to $P \leq \pm100$ ppm and with $C_m \leq 7$ fF, $C_0 \geq 1.5$ pF, C_{LN} = 9 pF and C_L = 7.4 pF to 10.6 pF, the pulling is $P \leq \pm50$ ppm.

Since typical crystals have less than ±50 ppm tolerance at 25°C, the compensation is not critical, and can in both cases be done with the ±150 ppm.