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ATA5428

UHF ASK/FSK Transceiver

DATASHEET

Features

- Multi channel half-duplex transceiver with approximately ±2.5MHz programmable tuning range
- High FSK sensitivity: –106dBm at 20Kbit/s/–109.5dBm at 2.4Kbit/s (433.92MHz)
- High ASK sensitivity: –112.5dBm at 10Kbit/s/–116.5dBm at 2.4Kbit/s (433.92MHz)
- Low supply current: 10.5mA in RX and TX Mode (3V/TX with 5dBm)
- Data Rate: 1 to 20Kbit/s Manchester FSK, 1 to 10Kbit/s Manchester ASK
- ASK/FSK receiver uses a low-IF architecture with high selectivity, blocking, and low intermodulation (typical blocking 55dB at ±750kHz/61dB at ±1.5MHz and 70dB at ±10MHz, system I1dBCP = –30dBm/system IIP3 = –20dBm)
- 226kHz/237kHz IF frequency with 30dB image rejection and 170kHz usable IF bandwidth
- Transmitter uses closed loop fractional-N synthesizer for FSK modulation with a high PLL bandwidth and an excellent isolation between PLL/VCO and PA
- Tolerances of XTAL compensated by fractional-N synthesizer with 800Hz RF resolution
- Integrated RX/TX-switch, single-ended RF input and output
- RSSI (Received Signal Strength Indicator)
- Communication to microcontroller with SPI interface working at max.500kBit/s
- Configurable self polling and RX/TX protocol handling with FIFO-RAM buffering of received and transmitted data
- Five push button inputs and one wake-up input are active in power-down mode
- integrated XTAL capacitors
- PA efficiency: up to 38% (433.92MHz/10dBm/3V)
- Low in-band sensitivity change of typically ±1.8dB within ±58kHz center frequency change in the complete temperature and supply voltage range
- Supply voltage switch, supply voltage regulator, reset generation, clock/interrupt generation and low battery indicator for microcontroller

- Fully integrated PLL with low phase noise VCO, PLL loop filter and full support of multi-channel operation with arbitrary channel distance due to fractional-N synthesizer
- Sophisticated threshold control and quasi-peak detector circuit in the data slicer
- Power management via different operation modes
- 433.92MHz and 868.3MHz without external VCO and PLL components
- Inductive supply with voltage regulator if battery is empty (AUX mode)
- Efficient XTO start-up circuit (> –1.5kΩ worst case real start-up impedance)
- Changing of modulation type ASK/FSK and data rate without component changes
- Minimal external circuitry requirements for complete system solution
- Adjustable output power: 0 to 10dBm adjusted and stabilized with external resistor
- ESD protection at all pins (1.5kV HBM, 200V MM, 1kV FCDM)
- Supply voltage range: 2.4V to 3.6V or 4.4V to 6.6V
- Temperature range: –40°C to +85°C
- Small 7 × 7mm QFN48 package

Applications

- Consumer industrial segment
- Access control systems
- Remote control systems
- Alarm and telemetry systems
- Energy metering
- Home automation

Benefits

- Low system cost due to very high system integration level
- Only one crystal needed in system
- Less demanding specification for the microcontroller due to handling of power-down mode, delivering of clock, reset, low battery indication and complete handling of receive/transmit protocol and polling
- Single-ended design with high isolation of PLL/VCO from PA and the power supply allows a loop antenna in the remote control unit to surround the whole application

1. General Description

The Atmel® ATA5428 is a highly integrated UHF ASK/FSK multi-channel half-duplex transceiver with low power consumption supplied in a small 7 x 7mm QFN48 package. The receive part is built as a fully integrated low-IF receiver, whereas direct PLL modulation with the fractional-N synthesizer is used for FSK transmission and switching of the power amplifier for ASK transmission.

The device supports data rates of 1Kbit/s to 20Kbit/s (FSK) and 1Kbit/s to 10Kbit/s (ASK) in Manchester, Bi-phase and other codes in transparent mode. The ATA5428 can be used in the 431.5MHz to 436.5MHz and in the 862MHz to 872MHz bands. The very high system integration level results in a small number of external components needed.

Due to its blocking and selectivity performance, together with the additional 15dB to 20dB loss and the narrow bandwidth of a typical loop antenna in a remote control unit, a bulky blocking SAW is not needed in the remote control unit. Additionally, the building blocks needed for a typical remote control and access control system on both sides (the base and the mobile stations) are fully integrated.

Its digital control logic with self-polling and protocol generation enables a fast challenge-response system without using a high-performance microcontroller. Therefore, the ATA5428 contains a FIFO buffer RAM and can compose and receive the physical messages themselves. This provides more time for the microcontroller to carry out other functions such as calculating crypto algorithms, composing the logical messages, and controlling other devices. Therefore, a standard 4-/8-bit microcontroller without special periphery and clocked with the CLK output of about 4.5MHz is sufficient to control the communication link. This is especially valid for passive entry and access control systems, where within less than 100ms several challenge-response communications with arbitration of the communication partner have to be handled.

It is hence possible to design bi-directional remote control and access control systems with a fast challenge-response crypto function, with the same PCB board size and with the same current consumption as uni-directional remote control systems.

Figure 1-1. System Block Diagram

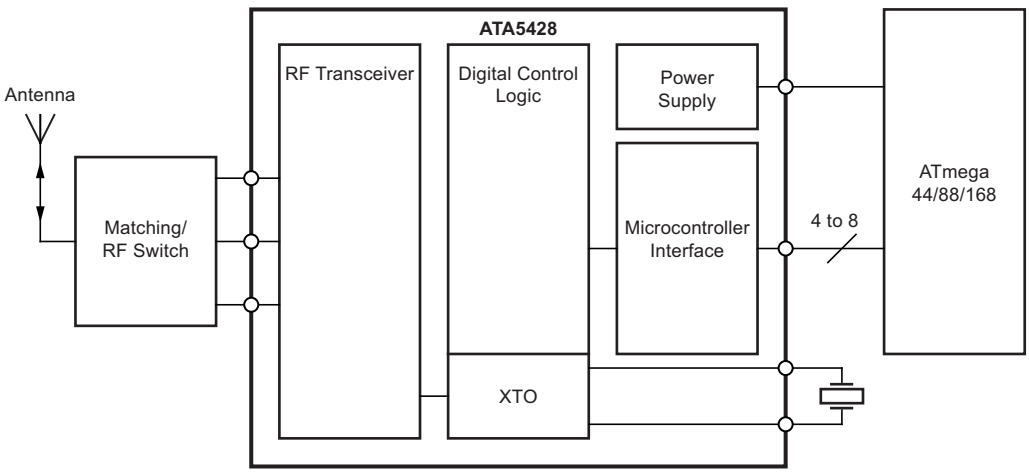


Figure 1-2. Pinning QFN48

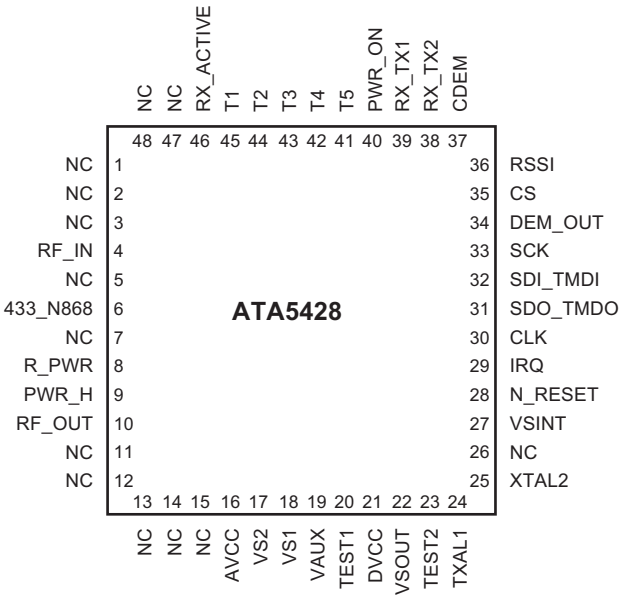


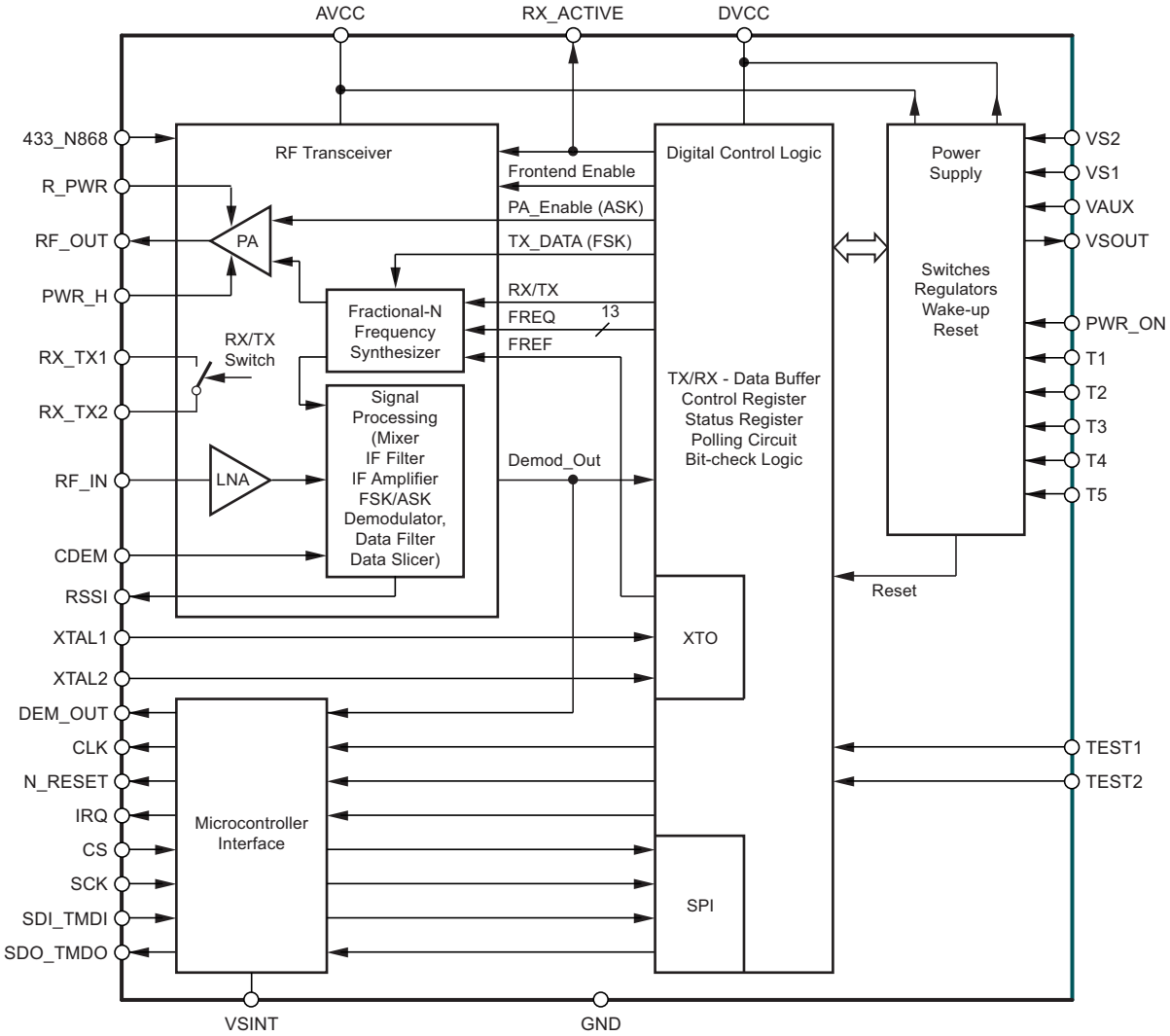
Table 1-1. Pin Description

Pin	Symbol	Function
1	NC	Not connected
2	NC	Not connected
3	NC	Not connected
4	RF_IN	RF input
5	NC	Not connected
6	433_N868	Selects RF input/output frequency range
7	NC	Not connected
8	R_PWR	Resistor to adjust output power
9	PWR_H	Pin to select output power
10	RF_OUT	RF output
11	NC	Not connected
12	NC	Not connected
13	NC	Not connected
14	NC	Not connected
15	NC	Not connected
16	AVCC	Blocking of the analog voltage supply
17	VS2	Power supply input for voltage range 4.4V to 6.6V
18	VS1	Power supply input for voltage range 2.4V to 3.6V
19	VAUX	Auxiliary supply voltage input
20	TEST1	Test input, at GND during operation
21	DVCC	Blocking of the digital voltage supply
22	VSOUT	Output voltage power supply for external devices
23	TEST2	Test input, at GND during operation
24	XTAL1	Reference crystal

Table 1-1. Pin Description (Continued)

Pin	Symbol	Function
25	XTAL2	Reference crystal
26	NC	Not connected
27	VSINT	Microcontroller interface supply voltage
28	N_RESET	Output pin to reset a connected microcontroller
29	IRQ	Interrupt request
30	CLK	Clock output to connect a microcontroller
31	SDO_TMDO	Serial data out/transparent mode data out
32	SDI_TMDI	Serial data in/transparent mode data in
33	SCK	Serial clock
34	DEM_OUT	Demodulator open drain output signal
35	CS	Chip select for serial interface
36	RSSI	Output of the RSSI amplifier
37	CDEM	Capacitor to adjust the lower cut-off frequency data filter
38	RX_TX2	GND pin to decouple LNA in TX mode
39	RX_TX1	Switch pin to decouple LNA in TX mode
40	PWR_ON	Input to switch on the system (active high)
41	T5	Key input 5 (can also be used to switch on the system (active low))
42	T4	Key input 4 (can also be used to switch on the system (active low))
43	T3	Key input 3 (can also be used to switch on the system (active low))
44	T2	Key input 2 (can also be used to switch on the system (active low))
45	T1	Key input 1 (can also be used to switch on the system (active low))
46	RX_ACTIVE	Indicates RX operation mode
47	NC	Not connected
48	NC	Not connected
	GND	Ground/backplane

Figure 1-3. Block Diagram

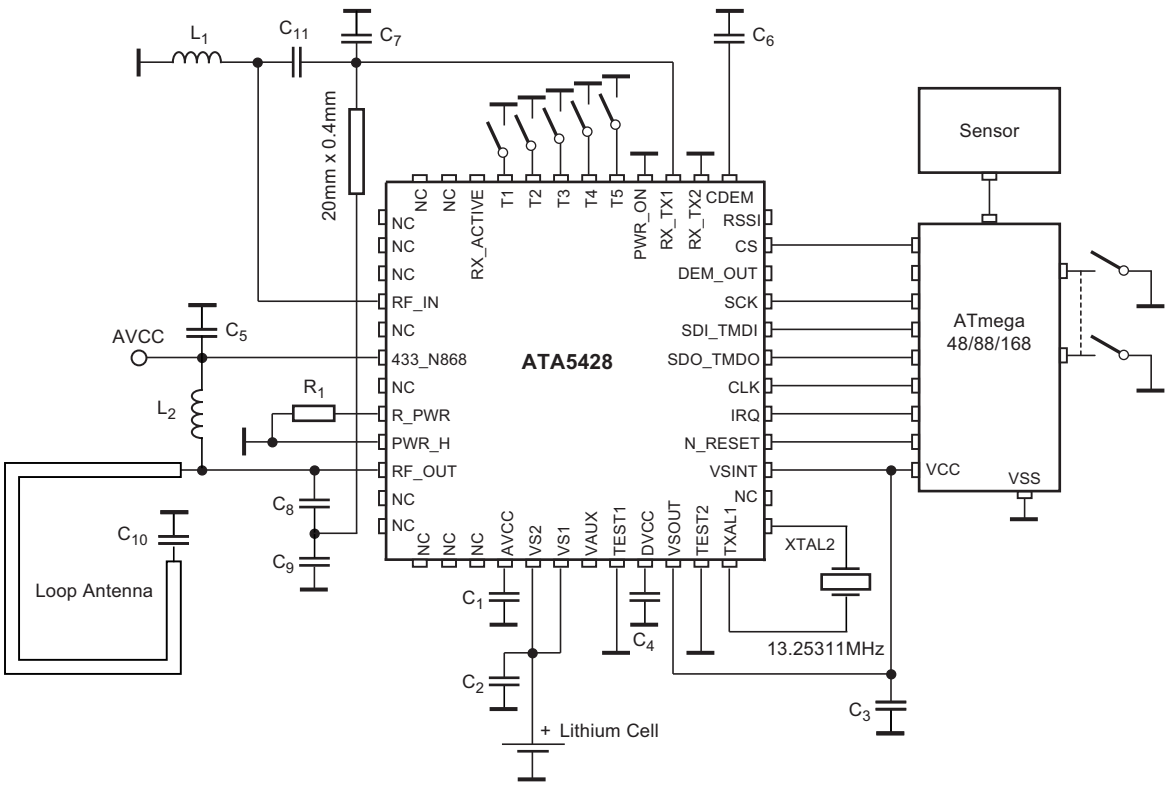


2. Application Circuits

2.1 Typical Remote Control Unit Application with 1 Li Battery (3V)

Figure 2-1 shows a typical 433.92MHz Remote Control Unit application with one battery. The external components are 11 capacitors, 1 resistor, 2 inductors and a crystal. C_1 to C_4 are 68nF voltage supply blocking capacitors. C_5 is a 10nF supply blocking capacitor. C_6 is a 15nF fixed capacitor used for the internal quasi-peak detector and for the high-pass frequency of the data filter. C_7 to C_{11} are RF matching capacitors in the range of 1pF to 33pF. L1 is a matching inductor of about 5.6nH to 56nH. L_2 is a feed inductor of about 120nH. A load capacitor of 9pF for the crystal is integrated. R_1 is typically 22kΩ and sets the output power to about 5.5dBm. The loop antenna's quality factor is somewhat reduced by this application due to the quality factor of L_2 and the RX/TX switch. On the other hand, this lower quality factor is necessary to have a robust design with a bandwidth that is broad enough for production tolerances. Due to the single-ended and ground-referenced design, the loop antenna can be a free-form wire around the application as it is usually employed in remote control uni-directional systems. The ATA5428 provides sufficient isolation and robust pulling behavior of internal circuits from the supply voltage as well as an integrated VCO inductor to allow this. Since the efficiency of a loop antenna is proportional to the square of the surrounded area it is beneficial to have a large loop around the application board with a lower quality factor in order to relax the tolerance specification of the RF components and to get a high antenna efficiency in spite of their lower quality factor.

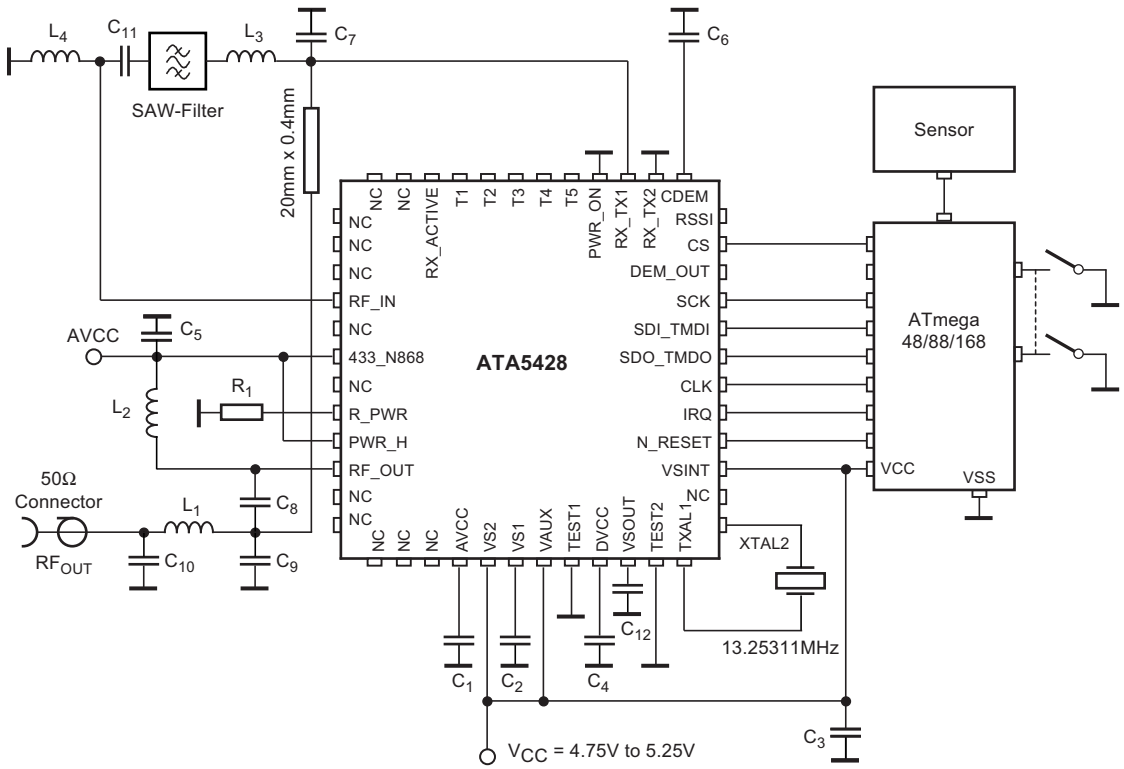
Figure 2-1. Typical Remote Control Unit Application, 433.92MHz, 1 Li Battery (3V)



2.2 Typical Base-station Application (5V)

Figure 2.2 shows a typical 433.92MHz V_{CC} = 4.75V to 5.25V Base-station Application (5V). The external components are 12 capacitors, 1 resistor, 4 inductors, a SAW filter, and a crystal. C_1 and C_3 to C_4 are 68nF voltage supply blocking capacitors. C_2 and C_{12} are 2.2µF supply blocking capacitors for the internal voltage regulators. C_5 is a 10nF supply blocking capacitor. C_6 is a 15 nF fixed capacitor used for the internal quasi-peak detector and for the high-pass frequency of the data filter. C_7 to C_{11} are RF matching capacitors in the range of 1pF to 33pF. L_2 to L_4 are matching inductors of about 5.6nH to 56nH. A load capacitor for the crystal of 9pF is integrated. R_1 is typically 22kΩ and sets the output power at RF_OUT to about 10dBm. Since a quarter wave or PCB antenna, which has high efficiency and wide band operation, is typically used here, it is recommended to use a SAW filter to achieve high sensitivity in case of powerful out-of-band blockers. L_1, C_9 and C_{10} together form a low-pass filter, which is needed to filter out the harmonics in the transmitted signal to meet regulations. An internally regulated voltage at pin VSOUT can be used in case the microcontroller only supports 3.3V operation, a blocking capacitor with a value of C_{12} = 2.2µF has to be connected to VSOUT in any case.

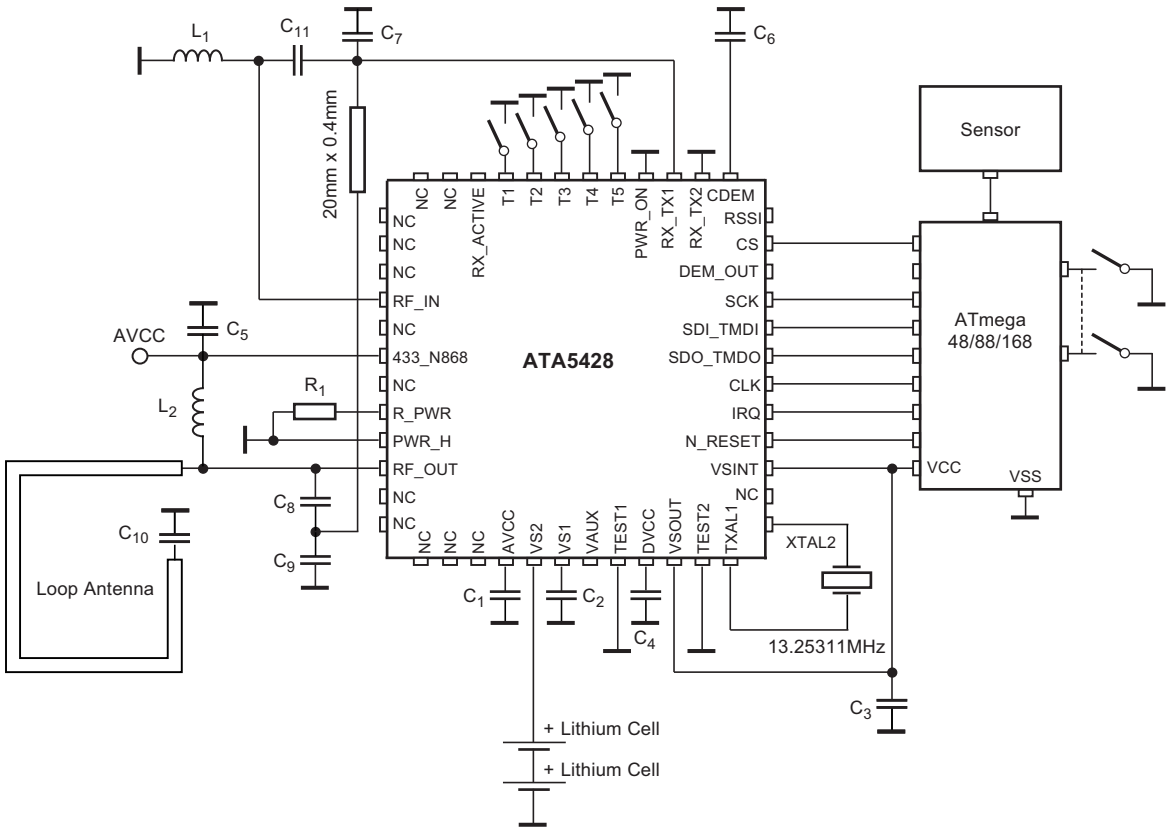
Figure 2-2. Typical Base-station Application (5V), 433.92MHz



2.3 Typical Remote Control Unit Application, 2 Li Batteries (6V)

Figure 2-3 shows a typical 433.92Hz 2 Li battery Remote Control Unit application. The external components are 11 capacitors, 1 resistor, 2 inductors and a crystal. C_1 and C_4 are 68nF voltage supply blocking capacitors. C_2 and C_3 are 2.2µF supply blocking capacitors for the internal voltage regulators. C_5 is a 10nF supply blocking capacitor. C_6 is a 15nF fixed capacitor used for the internal quasi-peak detector and for the high-pass frequency of the data filter. C_7 to C_{11} are RF matching capacitors in the range of 1pF to 33pF. L_1 is a matching inductor of about 5.6nH to 56nH. L_2 is a feed inductor of about 120nH. A load capacitor for the crystal of 9pF is integrated. R_1 is typically 22kΩ and sets the output power to about 5.5dBm.

Figure 2-3. Typical Remote Control Unit Application, 433.92MHz, 2 Li Batteries (6V)



3. RF Transceiver

As seen in Figure 1-3 on page 6, the RF transceiver consists of an LNA (Low-noise Amplifier), PA (Power Amplifier), RX/TX switch, fractional-N frequency synthesizer and the signal processing part with mixer, IF filter, IF amplifier with analog RSSI, FSK/ASK demodulator, data filter, and data slicer.

In receive mode the LNA pre-amplifies the received signal which is converted down to 226kHz (ATA5428), filtered and amplified before it is fed into an FSK/ASK demodulator, data filter, and data slicer. The RSSI (Received Signal Strength Indicator) signal and the raw digital output signal of the demodulator are available at the pins RSSI and DEM_OUT. The demodulated data signal Demod_Out is fed to the digital control logic where it is evaluated and buffered as described in section "Digital Control Logic" on page 30.

In transmit mode, the fractional-N frequency synthesizer generates the TX frequency which is fed to the PA. In ASK mode the PA is modulated by the signal PA_Enable. In FSK mode the PA is enabled and the signal TX_DATA (FSK) modulates the fractional-N frequency synthesizer. The frequency deviation is digitally controlled and internally fixed to about ±16kHz (see Table 4-1 on page 23 for exact values). The transmit data can also be buffered as described in section "Digital Control Logic" on page 30. A lock detector within the synthesizer ensures that the transmission will start only if the synthesizer is locked.

The RX/TX switch can be used to combine the LNA input and the PA output to a single antenna with a minimum of losses.

Transparent modes without buffering of RX and TX data are also available to allow protocols and coding schemes other than the internally supported Manchester encoding.

3.1 Low-IF Receiver

The receive path consists of a fully integrated low-IF receiver. It fulfills the sensitivity, blocking, selectivity, supply voltage and supply current specification needed to manufacture, for example, an automotive remote control unit without the use of SAW blocking filter (see Figure 2-1 on page 7). In a Base-station Application (5V) the receiver can be used with an additional blocking SAW front-end filter as shown in Figure 2.2 on page 8.

At 433.92MHz the receiver has a typical system noise figure of 7.0dB, a system I1dBCP of -30dBm and a system IIP3 of –20dBm. There is no AGC or switching of the LNA needed; thus, a better blocking performance is achieved. This receiver uses an IF (Intermediate Frequency) of 226kHz, the typical image rejection is 30dB and the typical 3dB IF filter bandwidth is 185kHz (f_{IF} = 226kHz ±92.5kHz, f_{lo_IF} = 133.5kHz and f_{hi_IF} = 318.5kHz). The demodulator needs a signal to Gaussian noise ratio of 8dB for 20Kbit/s Manchester with ±16kHz frequency deviation in FSK mode; thus, the resulting sensitivity at 433.92MHz is typically –106dBm at 20Kbit/s Manchester.

Due to the low phase noise and spurious emissions of the synthesizer in receive mode(1) together with the eighth order integrated IF filter, the receiver has a better selectivity and blocking performance than more complex double superhet receivers but without external components and without numerous spurious receiving frequencies.

A low-IF architecture is also less sensitive to second-order intermodulation (IIP2) than direct conversion receivers, where every pulse or AM-modulated signal (especially the signals from TDMA systems like GSM) demodulates to the receiving signal band at second-order non-linearities.

Note: 1. –120dBC/Hz at ±1MHz and –75dBC at ±FREF at 433.92MHz

3.2 Input Matching at RF_IN

The measured input impedances as well as the values of a parallel equivalent circuit of these impedances can be seen in the Table 3-1. The highest sensitivity is achieved with power matching of these impedances to the source impedance of 50Ω.

Table 3-1. Measured Input Impedances of the RF_IN Pin

f_{RF}/MHz	Z(RF_IN)	R_p//C_p
433.92	(32-j169)Ω	925Ω//2.1pF
868.3	(21-j78)Ω	311Ω//2.2pF

The matching of the LNA Input to 50Ω was done with the circuit shown in Figure 3-1 and with the values given in Table 3-2 on page 11. The reflection coefficients were always ≤ 10dB. Note that value changes of C_1 and L_1 may be necessary to compensate for individual board layouts. The measured typical FSK and ASK Manchester code sensitivities with a Bit Error Rate (BER) of 10^{-3} are shown in Table 3-3 on page 11 and Table 3-4 on page 11. These measurements were done with inductors having a quality factor according to Table 3-2 on page 11, resulting in estimated matching losses of 0.7dB at 433.92MHz, 0.7dB at 868.3MHz. These losses can be estimated when calculating the parallel equivalent resistance of the inductor with $R_{loss} = 2 \times \pi \times f \times L \times Q_L$ and the matching loss with $10 \log(1 + R_p/R_{loss})$.

With an ideal inductor, for example, the sensitivity at 433.92MHz/FSK/20Kbit/s/±16kHz/Manchester can be improved from –106dBm to –106.7dBm. The sensitivity depends on the control logic which examines the incoming data stream. The examination limits must be programmed in control registers 5 and 6. The measurements in Table 3-3 on page 11 and Table 3-4 on page 11 are based on the values of registers 5 and 6 according to Table 9-3 on page 53.

Figure 3-1. Input Matching to 50Ω

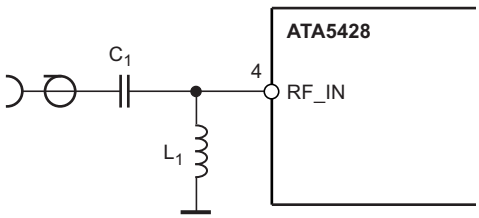


Table 3-2. Input Matching to 50Ω

f_{RF}/MHz	C_1/pF	L_1/nH	Q_{L1}
433.92	1.8	27	70
868.3	1.2	6.8	50

Table 3-3. Measured Sensitivity FSK, ±16kHz, Manchester, dBm, BER = 10^{-3}

RF Frequency	BR_Range_0 1.0Kbit/s	BR_Range_0 2.4Kbit/s	BR_Range_1 5.0Kbit/s	BR_Range_2 10Kbit/s	BR_Range_3 20Kbit/s
433.92MHz	–109.0dBm	–109.5dBm	–108.0dBm	–107.0dBm	–106.0dBm
868.3MHz	–106.0dBm	–106.5dBm	–105.5dBm	–104.0dBm	–103.5dBm

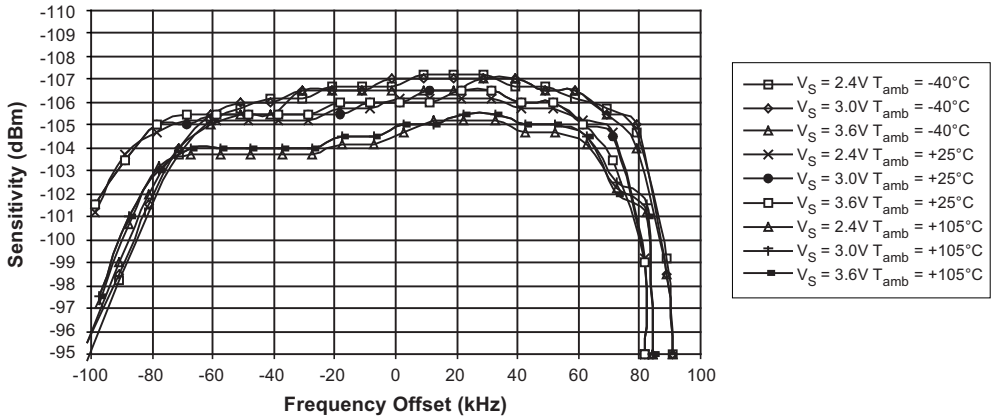
Table 3-4. Measured Sensitivity 100% ASK, Manchester, dBm, BER = 10^{-3}

RF Frequency	BR_Range_0 1.0Kbit/s	BR_Range_0 2.4Kbit/s	BR_Range_1 5.0Kbit/s	BR_Range_2 10Kbit/s
433.92MHz	–116.0dBm	–116.5dBm	–114.0dBm	–112.5dBm
868.3MHz	–112.5dBm	–113.0dBm	–111.5dBm	–109.5dBm

3.3 Sensitivity versus Supply Voltage, Temperature and Frequency Offset

To calculate the behavior of a transmission system it is important to know the reduction of the sensitivity due to several influences. The most important are frequency offset due to crystal oscillator (XTO) and crystal frequency (XTAL) errors, temperature and supply voltage dependency of the noise figure and IF filter bandwidth of the receiver. Figure 3-2 shows the typical sensitivity at 433.92MHz/FSK/20Kbit/s/±16kHz/Manchester versus the frequency offset between transmitter and receiver with T_{amb} = –40°C, +25°C and +105°C and supply voltage VS1 = VS2 = 2.4V, 3.0V and 3.6V.

Figure 3-2. Measured Sensitivity 433.92MHz/FSK/20Kbit/s/±16kHz/Manchester versus Frequency Offset, Temperature and Supply Voltage



As can be seen in Figure 3-2 on page 12 the supply voltage has almost no influence. The temperature has an influence of about +1.5/–0.7dB, and a frequency offset of ±65kHz also influences by about ±1dB. All these influences, combined with the sensitivity of a typical IC, are then within a range of –103.7dBm and –107.3dBm over temperature, supply voltage and frequency offset which is –105.5dBm ±1.8dB. The integrated IF filter has an additional production tolerance of only ±7kHz, hence, a frequency offset between the receiver and the transmitter of ±58kHz can be accepted for XTAL and XTO tolerances.

This small sensitivity spread over supply voltage, frequency offset and temperature is very unusual in such a receiver. It is achieved by an internal, very fast and automatic frequency correction in the FSK demodulator after the IF filter, which leads to a higher system margin. This frequency correction tracks the input frequency very quickly; if, however, the input frequency makes a larger step (for example, if the system changes between different communication partners), the receiver has to be restarted. This can be done by switching back to IDLE mode and then again to RX mode. For that purpose, an automatic mode is also available. This automatic mode switches to IDLE mode and back into RX mode every time a bit error occurs (see Section 7. on page 30).

3.4 Frequency Accuracy of the Crystals

The XTO is an amplitude regulated Pierce oscillator with integrated load capacitors. The initial tolerances (due to the frequency tolerance of the XTAL, the integrated capacitors on XTAL1, XTAL2 and the XTO's initial transconductance gm) can be compensated to a value within ±0.5ppm by measuring the CLK output frequency and programming the control registers 2 and 3 (see Table 7-7 on page 32 and Table 7-10 on page 33). The XTO then has a remaining influence of less than ±2ppm over temperature and supply voltage due to the band gap controlled gm of the XTO.

The needed frequency stability of the used crystals over temperature and aging is hence

±58kHz/433.92MHz – 2 × ±2.5ppm = ±128.6ppm for 433.92Mz,
±58kHz/868.3MHz – 2 × ±2.5ppm = ±61.8ppm for 868.3MHz.

Thus, the used crystals in receiver and transmitter each need to be better than ±64.3ppm for 433.92MHz, ±30.9ppm for 868.3MHz. In access control systems it may be advantageous to have a more tight tolerance at the Base-station in order to relax the requirement for the remote control unit.

3.5 RX Supply Current versus Temperature and Supply Voltage

Table 3-5 shows the typical supply current at 433.92MHz of the transceiver in RX mode versus supply voltage and temperature with VS = VS1 = VS2. As can be seen, the supply current at 2.4V and –40°C is less than the typical supply current; this is useful because this is also the operation point where a lithium cell has the worst performance. The typical supply current at 868.3MHz in RX mode is about the same as for 433.92MHz.

Table 3-5. Measured 433.92 MHz Receive Supply Current in FSK Mode

VS = VS1 = VS2	2.4V	3.0V	3.6V
T_{amb} = –40°C	8.4mA	8.8mA	9.2mA
T_{amb} = 25°C	9.9mA	10.3mA	10.8mA
T_{amb} = 85°C	10.9mA	11.3mA	11.8mA

3.6 Blocking, Selectivity

As can be seen in Figure 3-3 and Figure 3-4 on page 13, the receiver can receive signals 3dB higher than the sensitivity level in the presence of very large blockers of –47dBm/–34dBm with small frequency offsets of ±1/±10MHz.

Figure 3-3 shows narrow band blocking and Figure 3-4 wide band blocking characteristics. The measurements were done with a signal of 433.92MHz/FSK/20Kbit/s/±16kHz/Manchester, and with a level of –106dBm + 3dB = –103dBm which is 3dB above the sensitivity level. The figures show how much larger than –103dBm a continuous wave signal can be before the BER is higher than 10^{-3}. The measurements were done at the 50Ω input according to Figure 3-1 on page 11. At 1MHz, for example, the blocker can be 56dB higher than –103dBm which is -103dBm + 56dB = –47dBm. These values, together with the good intermodulation performance, avoid the need for a SAW filter in the remote control unit application.

Figure 3-3. Narrow Band 3dB Blocking Characteristic at 433.92MHz

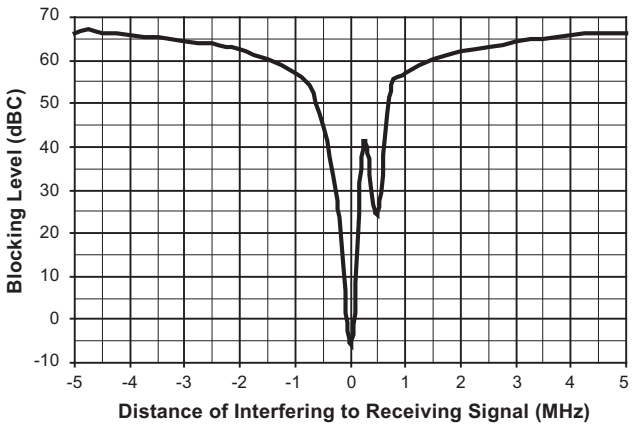


Figure 3-4. Wide Band 3dB Blocking Characteristic at 433.92MHz

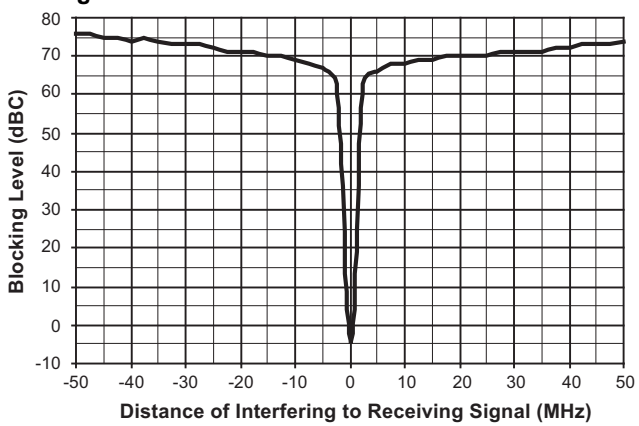


Figure 3-5 on page 14 shows the blocking measurement close to the received frequency to illustrate the selectivity and image rejection. This measurement was done 6dB above the sensitivity level with a useful signal of 433.92MHz/FSK/20Kbit/s/±16kHz/Manchester with a level of –106dBm + 6dB = –100dBm. The figure shows to which extent a continuous wave signal can surpass –100dBm until the BER is higher than 10^{-3}. For example, at 1MHz the blocker can then be 59dB higher than –100dBm which is –100dBm + 59dB = –41dBm.

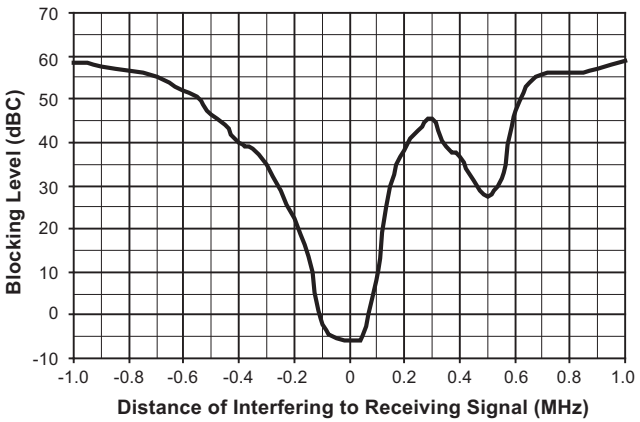
Table 3-6 on page 14 shows the blocking performance measured relative to –100dBm for some other frequencies. Note that sometimes the blocking is measured relative to the sensitivity level (dBS) instead of the carrier (dBC).

Table 3-6. Blocking 6dB Above Sensitivity Level with BER < 10^{-3}

Frequency Offset	Blocker Level	Blocking
+0.75MHz	–45dBm	55dBC/61dBS
–0.75MHz	–45dBm	55dBC/61dBS
+1.5MHz	–38dBm	62dBC/68dBS
–1.5MHz	–38dBm	62dBC/68dBS
+10MHz	–30dBm	70dBC/76dBS
–10MHz	–30dBm	70dBC/76dBS

The ATA5428 can also receive FSK and ASK modulated signals if they are much higher than the I1dBCP. It can typically receive useful signals at 10dBm. This is often referred to as the nonlinear dynamic range which is the maximum to minimum receiving signal and is 116dB for 20Kbit/s Manchester. This value is useful if two transceivers have to communicate and are very close to each other.

Figure 3-5. Close In 6dB Blocking Characteristic and Image Response at 433.92MHz



This high blocking performance even makes it possible for some applications using quarter wave whip antennas to use a simple LC band-pass filter instead of a SAW filter in the receiver.

When designing such an LC filter take into account that the 3dB blocking at 433.92MHz/2 = 216.96MHz is 43dBC and at 433.92MHz/3 = 144.64MHz is 48dBC and at 2 × (433.92MHz + 226kHz) + –226kHz = 868.066MHz/868.518MHz is 56dBC.

And especially that at 3 × (433.92MHz + 226kHz) + 226kHz = 1302.664MHz the receiver has its second LO harmonic receiving frequency with only 12dBC blocking.

3.7 In-band Disturbers, Data Filter, Quasi-peak Detector, Data Slicer

If a disturbing signal falls into the received band or a blocker is not continuous wave, the performance of a receiver strongly depends on the circuits after the IF filter. The demodulator, data filter and data slicer are important, in that case.

The data filter of the ATA5428 implies a quasi-peak detector. This results in a good suppression of the above mentioned disturbers and exhibits a good carrier to Gaussian noise performance. The required useful signal to disturbing signal ratio to be received with a BER of 10^{-3} is less than 12dB in ASK mode and less than 3dB (BR_Range_0 to BR_Range_2)/6dB (BR_Range_3) in FSK mode.

Due to the many different waveforms possible these numbers are measured for signal as well as for disturbers with peak amplitude values. Note that these values are worst case values and are valid for any type of modulation and modulating frequency of the disturbing signal as well as the receiving signal. For many combinations, lower carrier to disturbing signal ratios are needed.

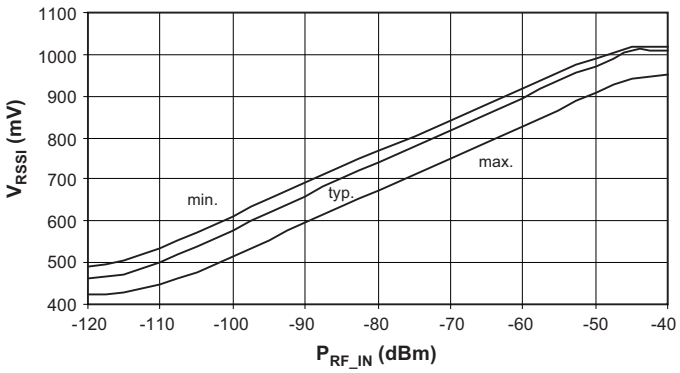
3.8 DEM_OUT Output

The internal raw output signal of the demodulator Demod_Out is available at pin DEM_OUT. DEM_OUT is an open drain output and must be connected to a pull-up resistor if it is used (typically 100kΩ) otherwise no signal is present at that pin.

3.9 RSSI Output

The output voltage of the pin RSSI is an analog voltage, proportional to the input power level. Using the RSSI output signal, the signal strength of different transmitters can be distinguished. The usable dynamic range of the RSSI amplifier is 70dB, the input power range P(RF_{IN}) is –115dBm to –45dBm and the gain is 8mV/dB. Figure 3-6 shows the RSSI characteristic of a typical device at 433.92MHz with VS1 = VS2 = 2.4V to 3.6V and T_{amb} = –40°C to +85°C with a matched input according to Table 3-2 on page 11 and Figure 3-1 on page 11. At 868.3MHz about 2.7dB more signal level is needed for the same RSSI results.

Figure 3-6. Typical RSSI Characteristic versus Temperature and Supply Voltage



3.10 Frequency Synthesizer

The synthesizer is a fully integrated fractional-N design with internal loop filters for receive and transmit mode. The XTO frequency f_{XTO} is the reference frequency FREF for the synthesizer. The bits FR0 to FR12 in control registers 2 and 3 (see Table 7-7 on page 32 and Table 7-10 on page 33) are used to adjust the deviation of f_{XTO}. In transmit mode, at 433.92MHz, the carrier has a phase noise of –111dBC/Hz at 1MHz and spurious emissions at FREF of –66dBC with a high PLL loop bandwidth allowing the direct modulation of the carrier with 20Kbit/s Manchester data. Due to the closed loop modulation any spurious emissions caused by this modulation are effectively filtered out as can be seen in Figure 3-9 on page 17. In RX mode the synthesizer has a phase noise of –120dBC/Hz at 1MHz and spurious emissions of –75dBC.

The initial tolerances of the crystal oscillator due to crystal tolerances, internal capacitor tolerances and the parasitics of the board have to be compensated at manufacturing setup with control registers 2 and 3 as can be seen in Table 4-1 on page 23. The other control words for the synthesizer needed for ASK, FSK and receive/transmit switching are calculated internally. The RF (Radio Frequency) resolution is equal to the XTO frequency divided by 16384 which is 808.9Hz at 433.92MHz, 818.6Hz at 868.3MHz.

For the multi-channel system the frequency control word FREQ in control registers 2 and 3 can be programmed in the range of 1000 to 6900, this is equivalent to a programmable tuning range of ±2.5MHz hence every frequency within the 433MHz, 868MHz ISM bands can be programmed as receive and as transmit frequency, and the position of channels within these ISM bands can be chosen arbitrarily (see Table 4-1 on page 23).

Care must be taken as to the harmonics of the CLK output signal as well as to the harmonics produced by a microprocessor clocked with it, since these harmonics can disturb the reception of signals. In a single-channel system, using FREQ = 3803 to 4053 ensures that harmonics of this signal do not disturb the receive mode.

3.11 FSK/ASK Transmission

Due to the fast modulation capability of the synthesizer and the high resolution, the carrier can be internally FSK modulated, which simplifies the application of the transceiver. The deviation of the transmitted signal is ±20 digital frequency steps of the synthesizer which is equal to ±16.17kHz for 433.92MHz, ±16.37kHz for 868.3MHz.

Due to closed loop modulation with PLL filtering the modulated spectrum is very clean, meeting ETSI and CEPT regulations when using a simple LC filter for the power amplifier harmonics as it is shown in Figure 2.2 on page 8. In ASK mode the frequency is internally connected to the center of the FSK transmission and the power amplifier is switched on and off to perform the modulation. Figure 3-7 to Figure 3-9 on page 17 show the spectrum of the FSK modulation with pseudo-random data with 20Kbit/s/±16.17kHz/Manchester and 5dBm output power.

Figure 3-7. FSK-modulated TX Spectrum (433.92MHz/20Kbit/s/±16.17kHz/Manchester Code)

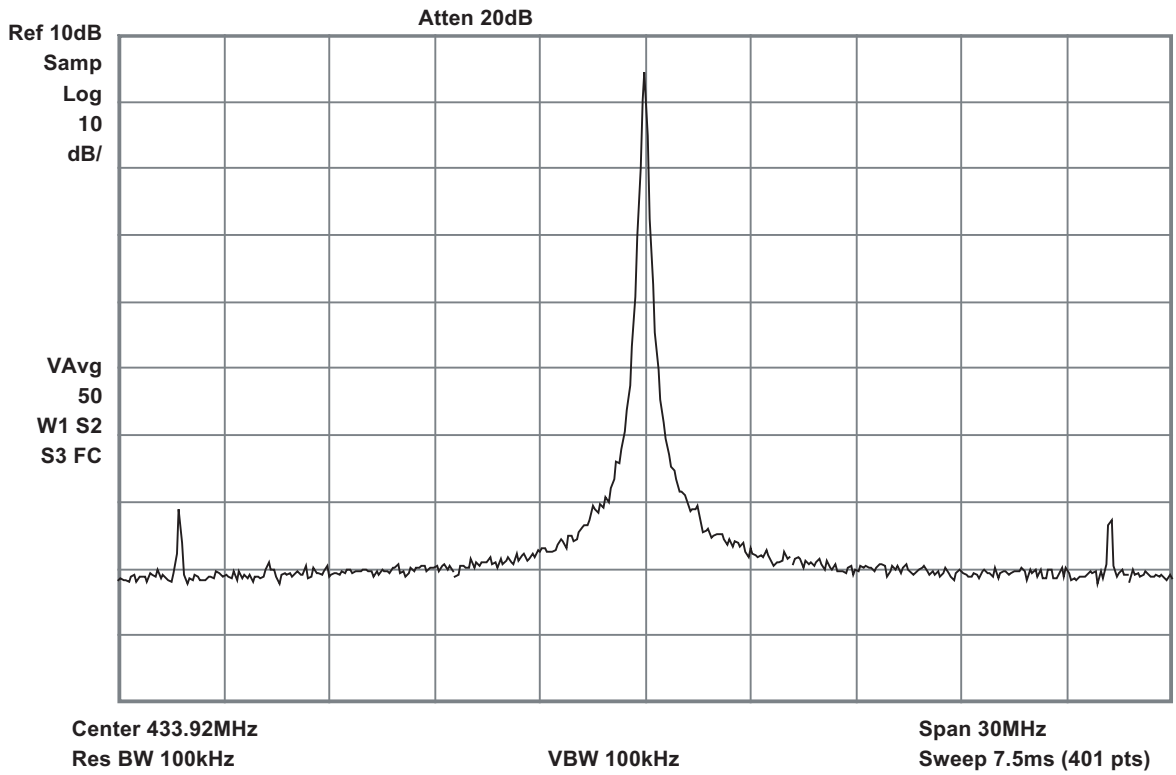


Figure 3-8. Unmodulated TX Spectrum 433.92MHz – 16.17kHz (f_{FSK_L})

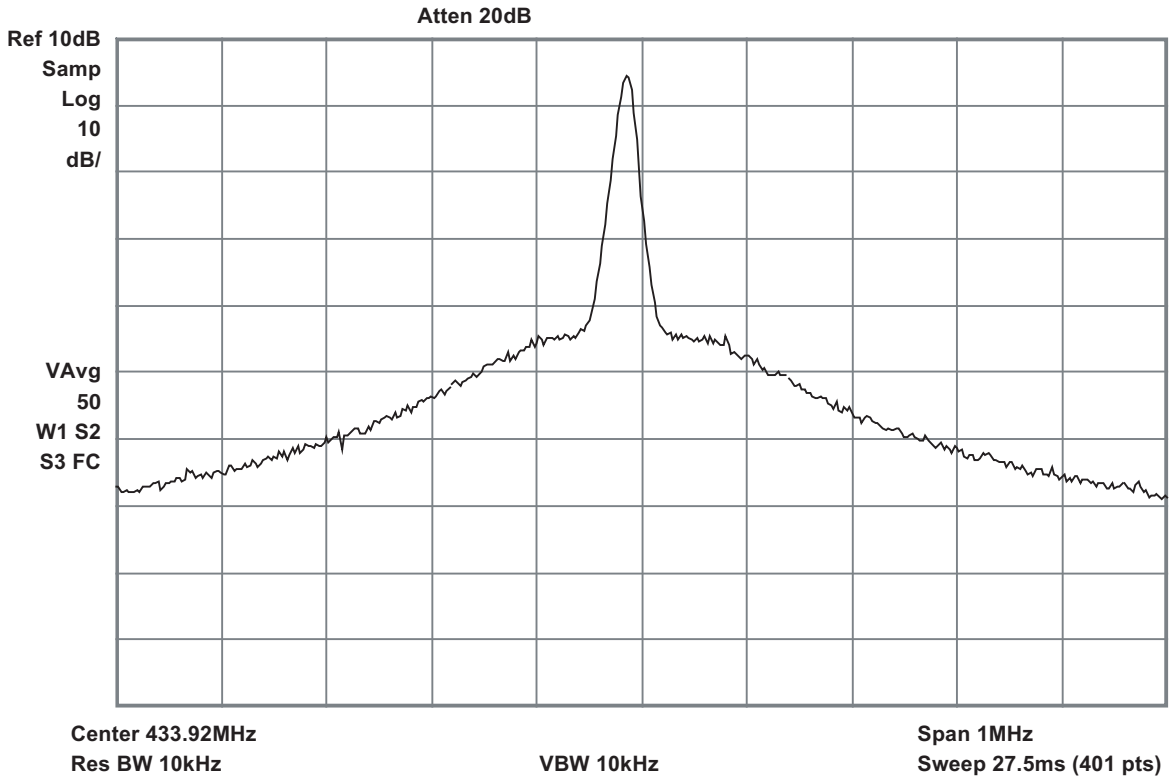
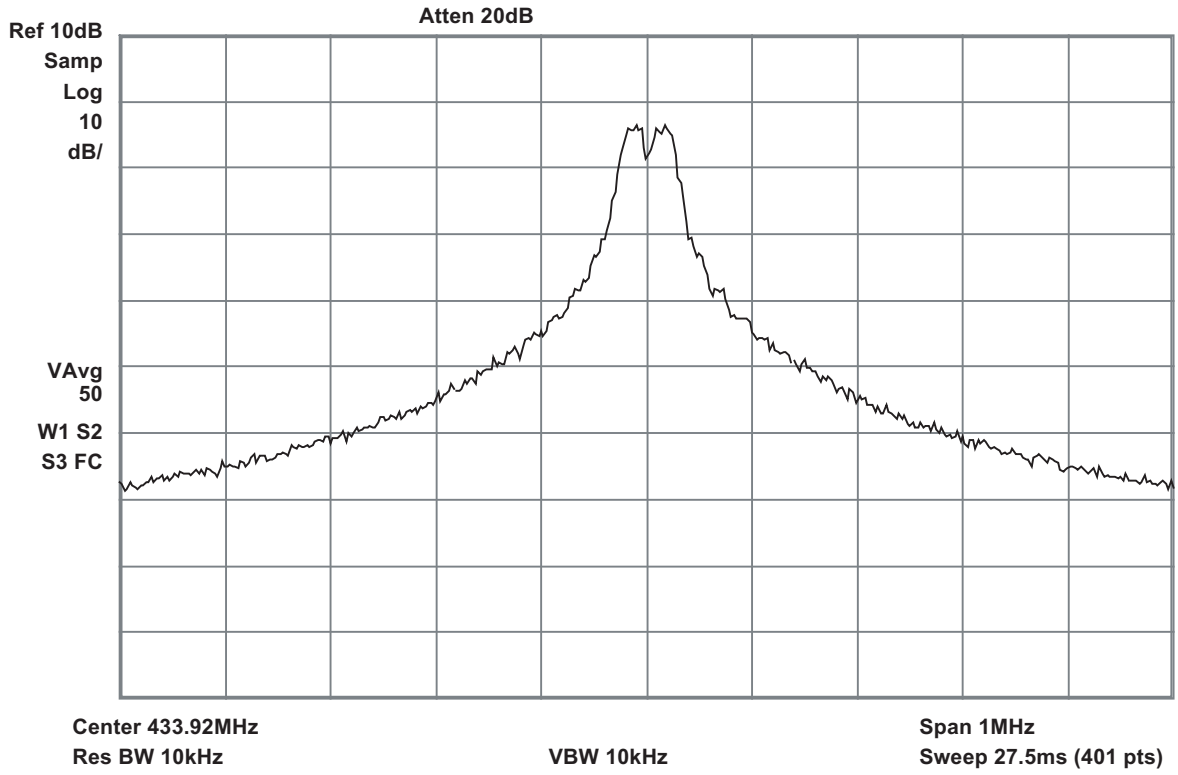


Figure 3-9. FSK-modulated TX Spectrum (433.92MHz/20Kbit/s/±16.17kHz/Manchester Code)



3.12 Output Power Setting and PA Matching at RF_OUT

The Power Amplifier (PA) is a single-ended open collector stage which delivers a current pulse which is nearly independent of supply voltage, temperature and tolerances due to band gap stabilization. Resistor R_1, see Figure 3-10, sets a reference current which controls the current in the PA. A higher resistor value results in a lower reference current, a lower output power and a lower current consumption of the PA. The usable range of R_1 is 15kΩ to 56kΩ. Pin PWR_H switches the output power range between about 0dBm to 5dBm (PWR_H = GND) and 5dBm to 10dBm (PWR_H = AVCC) by multiplying this reference current by a factor 1 (PWR_H = GND) and 2.5 (PWR_H = AVCC), which corresponds to about 5dB more output power.

If the PA is switched off in TX mode, the current consumption without output stage with VS1 = VS2 = 3V, T_{amb} = 25°C is typically 6.5mA for 868.3MHz and 6.95mA for 433.92MHz.

The maximum output power is achieved with optimum load resistances R_{Lopt} according to Table 3-7 on page 19 with compensation of the 1.0pF output capacitance of the RF_OUT pin by absorbing it into the matching network consisting of L_1, C_1, C_3 as shown in Figure 3-10 on page 18. There must also be a low resistive DC path to AVCC to deliver the DC current of the power amplifier's last stage. The matching of the PA output was done with the circuit shown in Figure 3-10 on page 18 with the values in Table 3-7 on page 19. Note that value changes of these elements may be necessary to compensate for individual board layouts.

Example:

According to Table 3-7 on page 19, with a frequency of 433.92 MHz and output power of 11dBm the overall current consumption is typically 17.8mA; hence, the PA needs 17.8mA - 6.95mA = 10.85mA in this mode, which corresponds to an overall power amplifier efficiency of the PA of $(10^{(11dBm/10)} \times 1\ mW)/(3V \times 10.85mA) \times 100\% = 38.6\%$ in this case.

Using a higher resistor in this example of $R_1 = 1.091 \times 22k\Omega = 24k\Omega$ results in 9.1% less current in the PA of 10.85mA/1.091 = 9.95mA and $10 \times \log(1.091) = 0.38dB$ less output power if using a new load resistance of $300\Omega \times 1.091 = 327\Omega$. The resulting output power is then 11dBm – 0.38dB = 10.6dBm and the overall current consumption is 6.95mA + 9.95mA = 16.9mA.

The values of Table 3-7 on page 19 were measured with standard multi-layer chip inductors with quality factors Q according to Table 3-7 on page 19. Looking to the 433.92MHz/11dBm case with the quality factor of Q_{L1} = 43 the loss in this inductor is estimated with the parallel equivalent resistance of the inductor $R_{loss} = 2 \times \pi \times f \times L \times Q_{L1}$ and the matching loss with $10 \log (1 + R_{Lopt}/R_{loss})$ which is equal to 0.32dB losses in this inductor. Taking this into account, the PA efficiency is then 42% instead of 38.6%.

Be aware that the high power mode (PWR_H = AVCC) can only be used with a supply voltage higher than 2.7V, whereas the low power mode (PWR_H = GND) can be used down to 2.4V as can be seen in the "Electrical Characteristics: General" on page 58.

The supply blocking capacitor C_2 (10nF) has to be placed close to the matching network because of the RF current flowing through it.

Figure 3-10. Power Setting and Output Matching

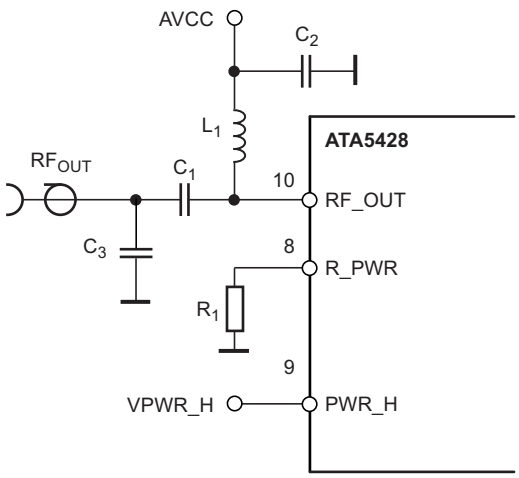


Table 3-7. Measured Output Power and Current Consumption with VS1 = VS2 = 3V, T_{amb} = 25°C

Frequency (MHz)	TX Current (mA)	Output Power (dBm)	R1 (kΩ)	VPWR_H	R_{Lopt} (Ω)	L1 (nH)	Q_{L1}	C1 (pF)	C3 (pF)
433.92	8.6	0.1	56	GND	2300	56	40	0.75	0
433.92	11.2	6.2	22	GND	890	47	38	1.5	0
433.92	17.8	11	22	AVCC	300	33	43	2.7	0
868.3	9.3	-0.3	33	GND	1170	12	58	1.0	3.3
868.3	11.5	5.4	15	GND	471	15	54	1.0	0
868.3	16.3	9.5	22	AVCC	245	10	57	1.5	0

3.13 Output Power and TX Supply Current versus Supply Voltage and Temperature

Table 3-8 shows the measurement of the output power for a typical device with VS = VS1 = VS2 in the 433.92MHz and 6.2dBm case versus temperature and supply voltage measured according to Figure 3-10 on page 18 with components according to Table 3-7. As opposed to the receiver sensitivity, the supply voltage has here the major impact on output power variations because of the large signal behavior of a power amplifier. Thus, a two battery system with voltage regulator or a 5V system shows much less variation than a 2.4V to 3.6V one battery system because the supply voltage is then well within 3.0V and 3.6V.

The reason is that the amplitude at the output RF_OUT with optimum load resistance is AVCC – 0.4V and the power is proportional to $(AVCC – 0.4V)^2$ if the load impedance is not changed. This means that the theoretical output power reduction if reducing the supply voltage from 3.0V to 2.4V is 10 log $((3V – 0.4V)^2/(2.4V – 0.4V)^2)$ = 2.2dB. Table 3-8 shows that principle behavior in the measurement. This is not the same case for higher voltages, since here increasing the supply voltage from 3V to 3.6V should theoretical increase the power by 1.8dB; but a gain of only 0.8dB in the measurement shows that the amplitude does not increase with the supply voltage because the load impedance is optimized for 3V and the output amplitude stays more constant.

Table 3-8. Measured Output Power and Supply Current at 433.92MHz, PWR_H = GND

VS =	2.4V	3.0V	3.6V
T_{amb} = –40°C	10.19mA 3.8dBm	10.19mA 5.5dBm	10.78mA 6.2dBm
T_{amb} = +25°C	10.62mA 4.6dBm	11.19mA 6.2dBm	11.79mA 7.1dBm
T_{amb} = +85°C	11.4mA 3.9dBm	12.02mA 5.5dBm	12.73mA 6.6dBm

Table 3-9 shows the relative changes of the output power of a typical device compared to 3.0V/25°C. As can be seen, a temperature change to –40°C as well as to +85°C reduces the power by less than 1dB due to the band gap regulated output current. Measurements of all the cases in Table 3-7 on page 19 over temperature and supply voltage have shown about the same relative behavior as shown in Table 3-9.

Table 3-9. Measurements of Typical Output Power Relative to 3V/25°C

VS =	2.4V	3.0V	3.6V
T_{amb} = –40°C	–2.4dB	–0.7dB	0dB
T_{amb} = +25°C	–1.6dB	0dB	+0.9dB
T_{amb} = +85°C	–2.3dB	–0.7dB	+0.4dB

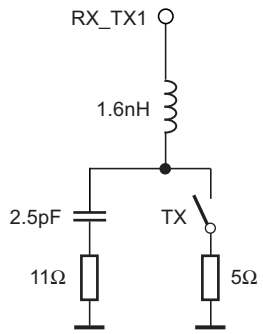
3.14 RX/TX Switch

The RX/TX switch decouples the LNA from the PA in TX mode, and directs the received power to the LNA in RX mode. To do this, it has a low impedance to GND in TX mode and a high impedance to GND in RX mode. To design a proper RX/TX decoupling, a linear simulation tool for radio frequency design together with the measured device impedances of Table 3-1 on page 10, Table 3-7 on page 19, Table 3-10 and Table 3-11 on page 21 should be used, but the exact element values have to be found on-board. Figure 3-11 shows an approximate equivalent circuit of the switch. The principal switching operation is described here according to the application of Figure 2-1 on page 7. The application of Figure 2.2 on page 8 works similarly.

Table 3-10. Impedance of the RX/TX Switch RX_TX2 Shorted to GND

Frequency	Z(RX_TX1) TX Mode	Z(RX_TX1) RX Mode
433.92MHz	(4.5 + j4.3)Ω	(10.3 – j153)Ω
868.3MHz	(5 + j9)Ω	(8.9 – j73)Ω

Figure 3-11. Equivalent Circuit of the Switch



3.15 Matching Network in TX Mode

In TX mode the 20mm long and 0.4mm wide transmission line which is much shorter than λ/4 is approximately switched in parallel to the capacitor C_9 to GND. The antenna connection between C_8 and C_9 has an impedance of about 50Ω locking from the transmission line into the loop antenna with pin RF_OUT, L_2, C_{10}, C_8 and C_9 connected (using a C_9 without the added 7.6pF as discussed later). The transmission line can be approximated with a 16nH inductor in series with a 1.5Ω resistor, the closed switch can be approximated according to Table 3-10 with the series connection of 1.6nH and 5Ω in this mode. To have a parallel resonant high impedance circuit with little RF power going into it looking from the loop antenna into the transmission line a capacitor of about 7.6pF to GND is needed at the beginning of the transmission line (this capacitor is later absorbed into C_9 which is then higher, as needed for 50Ω transformation). To keep the 50Ω impedance in RX mode at the end of this transmission line, C_7 also has to be about 7.6pF. This reduces the TX power by about 0.5dB at 433.92MHz compared to the case the where the LNA path is completely disconnected.

3.16 Matching Network in RX Mode

In RX mode the RF_OUT pin has a high impedance of about 7kΩ in parallel with 1.0pF at 433.92MHz as can be seen in Table 3-11. This, together with the losses of the inductor L_2 with 120nH and Q_{L2} = 25, gives about 3.7kΩ loss impedance at RF_OUT. Since the optimum load impedance in TX mode for the power amplifier at RF_OUT is 890Ω the loss associated with the inductor L_2 and the RF_OUT pin can be estimated to be 10 × log(1 + 890/3700) = 0.95dB compared to the optimum matched loop antenna without L_2 and RF_OUT. The switch represents, in this mode at 433.92MHz, approximately an inductor of 1.6nH in series with the parallel connection of 2.5pF and 2.0kΩ. Since the impedance level at pin RX_TX1 in RX mode is about 50Ω this only negligibly dampens the received signal (by about 0.1dB). When matching the LNA to the loop antenna, the transmission line and the 7.6pF part of C_9 have to be taken into account when choosing the values of C_{11} and L_1 so that the impedance seen from the loop antenna into the transmission line with the 7.6pF capacitor connected is 50Ω. Since the loop antenna in RX mode is loaded by the LNA input impedance, the loaded Q of the loop antenna is lowered by about a factor of 2 in RX mode; hence the antenna bandwidth is higher than in TX mode.

Table 3-11. Impedance RF_OUT Pin in RX Mode

Frequency	Z(RF_OUT)RX	R_P//C_P
433.92MHz	19Ω – j 366Ω	7kΩ//1.0pF
868.3MHz	2.8Ω – j 141Ω	7kΩ//1.3pF

Note that if matching to 50Ω, like in Figure 2.2 on page 8, a high Q wire-wound inductor with a Q > 70 should be used for L_2 to minimize its contribution to RX losses that will otherwise be dominant. The RX and TX losses will be in the range of 1.0dB there.

4. XTO

The XTO is an amplitude-regulated Pierce oscillator type with integrated load capacitances (2 × 18pF with a tolerance of ±17%) hence C_{Lmin} = 7.4pF and C_{Lmax} = 10.6pF. The XTO oscillation frequency f_{XTO} is the reference frequency FREF for the fractional-N synthesizer. When designing the system in terms of receiving and transmitting frequency offset, the accuracy of the crystal and XTO have to be considered.

The synthesizer can adjust the local oscillator frequency for the initial frequency error in f_{XTO}. This is done at nominal supply voltage and temperature with the control registers 2 and 3 (see Table 7-7 on page 32 and Table 7-10 on page 33). The remaining local oscillator tolerance at nominal supply voltage and temperature is then < ±0.5ppm. The XTO's gm has very low influence of less than ±2ppm on the frequency at nominal supply voltage and temperature.

In a single channel system less than ±150ppm should be corrected to avoid that harmonics of the CLK output disturb the receive mode. If the CLK is not used or if it is carefully laid out on the application PCB (as needed for multi channel systems), more than ±150ppm can be compensated.

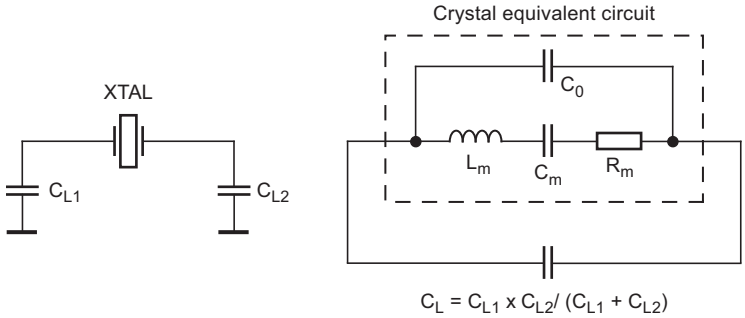
Over temperature and supply voltage, the XTO's additional pulling is only ±2ppm. The XTAL versus temperature and its aging is then the main source of frequency error in the local oscillator.

The XTO frequency depends on XTAL properties and the load capacitances $C_{L1, 2}$ at pin XTAL1 and XTAL2. The pulling of f_{XTO} from the nominal f_{XTAL} is calculated using the following formula:

$$P = \frac{C_m}{2} \times \frac{C_{LN} - C_L}{(C_0 + C_{LN}) \times (C_0 + C_L)} \times 10^6 \quad \text{ppm.}$$

C_m is the crystal's motional, C_0 the shunt and C_{LN} the nominal load capacitance of the XTAL found in its data sheet. C_L is the total actual load capacitance of the crystal in the circuit and consists of C_{L1} and C_{L2} in series connection.

Figure 4-1. XTAL with Load Capacitance



With $C_m \leq 14fF$, $C_0 \geq 1.5pF$, $C_{LN} = 9pF$ and $C_L = 7.4pF$ to $10.6pF$, the pulling amounts to $P \leq \pm 100ppm$ and with $C_m \leq 7fF$, $C_0 \geq 1.5pF$, $C_{LN} = 9pF$ and $C_L = 7.4pF$ to $10.6pF$, the pulling is $P \leq \pm 50ppm$.

Since typical crystals have less than ±50ppm tolerance at 25°C, the compensation is not critical, and can in both cases be done with the ±150ppm.

C_0 of the XTAL has to be lower than $C_{Lmin}/2 = 3.7pF$ for a Pierce oscillator type in order to not enter the steep region of pulling versus load capacitance where there is a risk of an unstable oscillation.

To ensure proper start-up behavior the small signal gain, and thus the negative resistance, provided by this XTO at start is very large; for example, oscillation starts up even in worst case with a crystal series resistance of 1.5kΩ at $C_0 \leq 2.2pF$ with this XTO. The negative resistance is approximately given by

$$\mathrm{Re}\{Z_{XTOcore}\} = \mathrm{Re}\left\{\frac{Z_1 \times Z_3 + Z_2 \times Z_3 + Z_1 \times Z_2 \times Z_3 \times g_m}{Z_1 + Z_2 + Z_3 + Z_1 \times Z_2 \times g_m}\right\}$$

with Z_1, Z_2 as complex impedances at pin XTAL1 and XTAL2, hence
$Z_1 = -j/(2 \times \pi \times f_{XTO} \times C_{L1}) + 5\Omega$ and $Z_2 = -j/(2 \times \pi \times f_{XTO} \times C_{L2}) + 5\Omega$.

Z_3 consists of crystals C_0 in parallel with an internal 110 kΩ resistor hence
$Z_3 = -j/(2 \times \pi \times f_{XTO} \times C_0) / 110k\Omega$, gm is the internal transconductance between XTAL1 and XTAL2 with typically 19mS at 25°C.

With $f_{XTO} = 13.5MHz$, gm = 19mS, $C_L = 9pF$, and $C_0 = 2.2pF$, this results in a negative resistance of about 2kΩ. The worst case for technological, temperature and supply voltage variations is then for $C_0 \leq 2.2pF$ always higher than 1.5kΩ.

Due to the large gain at startup, the XTO is able to meet a very low start-up time. The oscillation start-up time can be estimated with the time constant τ.

$$\tau = \frac{2}{4 \times \pi^2 \times f_m^2 \times C_m \times (\mathrm{Re}(Z_{XTOcore}) + R_m)}$$

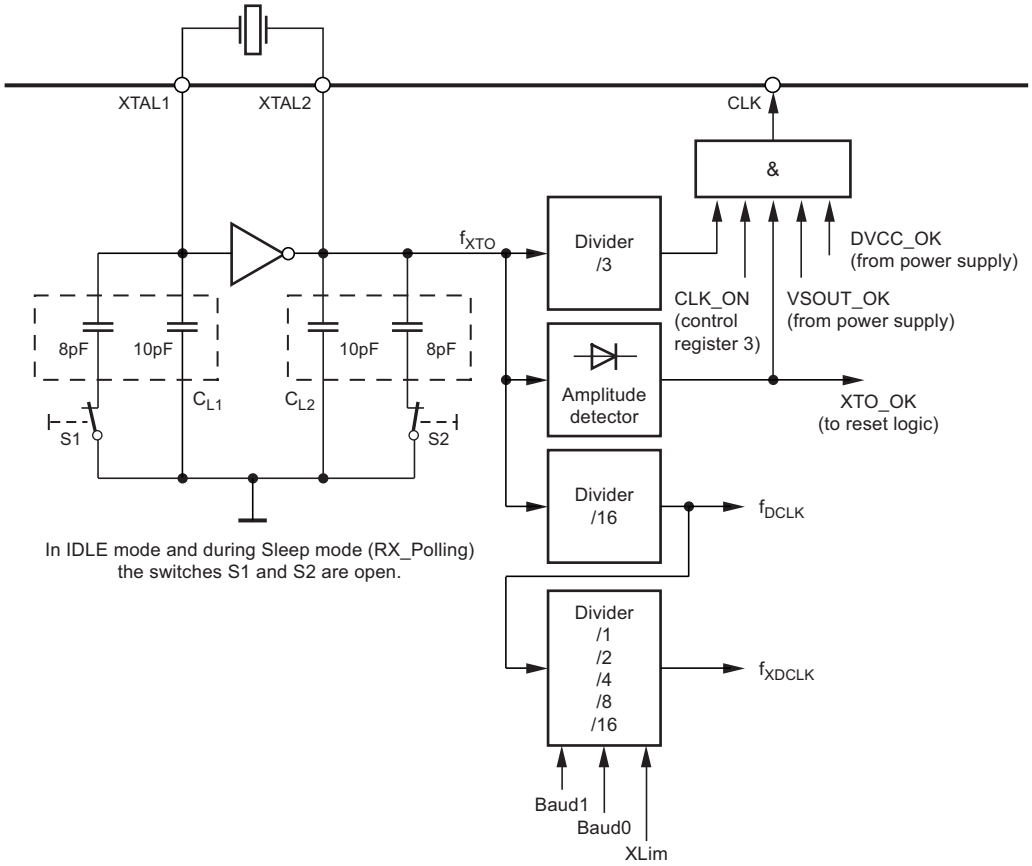
After 10τ to 20τ an amplitude detector detects the oscillation amplitude and sets XTO_OK to High if the amplitude is large enough. This sets N_RESET to High and activates the CLK output if CLK_ON in control register 3 is High (see Table 7-7 on page 32). Note that the necessary conditions of the VSOUT and DVCC voltage also have to be fulfilled (see Figure 4-2 on page 23 and Figure 5-1 on page 25).

To save current in IDLE and Sleep modes, the load capacitors are partially switched off in these modes with S1 and S2, as seen in Figure 4-2 on page 23.

It is recommended to use a crystal with $C_m = 3.0fF$ to $7.0fF$, $C_{LN} = 9pF$, $R_m < 120\Omega$ and $C_0 = 1.0pF$ to $2.2pF$.

Lower values of C_m can be used, this increases the start-up time slightly. Lower values of C_0 or higher values of C_m (up to 15fF) can also be used, this has only little influence on pulling.

Figure 4-2. XTO Block Diagram



To find the right values used in control registers 2 and 3 (see Table 7-7 on page 32 and Table 7-10 on page 33), the relationship between f_{XTO} and the f_{RF} is shown in Table 4-1 on page 23. To determine the right content, the frequency at pin CLK as well as the output frequency at RF_OUT in ASK mode can be measured, then the FREQ value can be calculated according to Table 4-1 on page 23 so that f_{RF} is exactly the desired radio frequency.

Table 4-1. Calculation of f_{RF}

Frequency (MHz)	Pin 6 433_N868	CREG1 Bit(4) FS	f_{XTO} (MHz)	$f_{RF} = f_{TX\_ASK} = f_{RX}$	$f_{TX\_FSK\_L}$	$f_{TX\_FSK\_H}$	Frequency Resolution
433.92	AVCC	0	13.25311	$f_{XTO} \times \left(32.5 + \frac{FREQ + 20.5}{16384}\right)$	f_{RF} – 16.17kHz	f_{RF} + 16.17kHz	808.9Hz
868.3	GND	0	13.41191	$f_{XTO} \times \left(64.5 + \frac{FREQ + 20.5}{16384}\right)$	f_{RF} – 16.37kHz	f_{RF} + 16.37kHz	818.6Hz

The variable FREQ depends on FREQ2 and FREQ3, which are defined by the bits FR0 to FR12 in control register 2 and 3, and is calculated as follows:

FREQ = FREQ2 + FREQ3

Care must be taken to the harmonics of the CLK output signal f_{CLK} as well as to the harmonics produced by an microprocessor clocked with it, since these harmonics can disturb the reception of signals if they get to the RF input. In a single channel system, using FREQ = 3803 to 4053 ensures that the harmonics of this signal do not disturb the receive mode. In a multichannel system, the CLK signal can either be not used or carefully laid out on the application PCB. The supply voltage of the microcontroller must also be carefully blocked in a multichannel system.

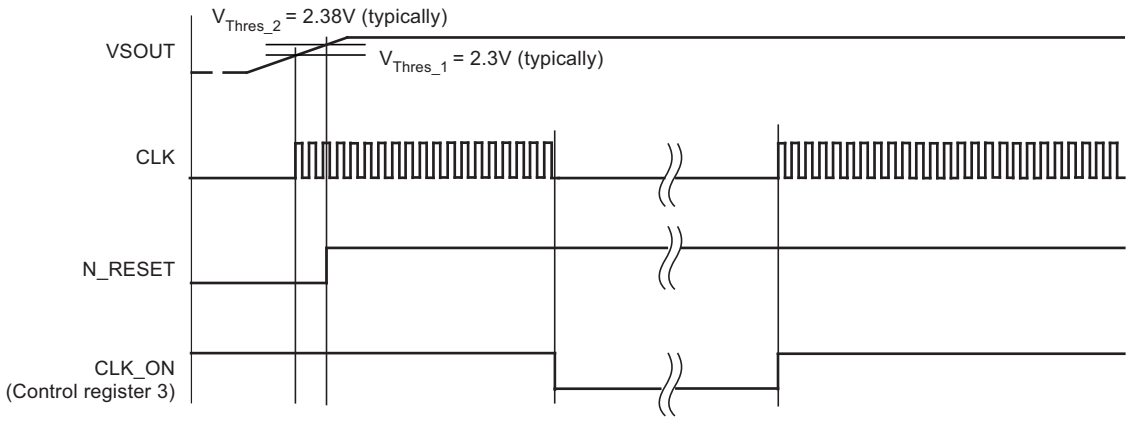
4.1 Pin CLK

Pin CLK is an output to clock a connected microcontroller. The clock frequency f_{CLK} is calculated as follows:

$$f_{CLK} = \frac{f_{XTO}}{3}$$

Because the enabling of pin CLK is asynchronous, the first clock cycle may be incomplete. The signal at CLK output has a nominal 50% duty cycle.

Figure 4-3. Clock Timing



4.2 Basic Clock Cycle of the Digital Circuitry

The complete timing of the digital circuitry is derived from one clock. As shown in Figure 4-2 on page 23, this clock cycle T_{DCLK} is derived from the crystal oscillator (XTO) in combination with a divider.

$$f_{DCLK} = \frac{f_{XTO}}{16}$$

T_{DCLK} controls the following application relevant parameters:

- Timing of the polling circuit including bit check
- TX bit rate

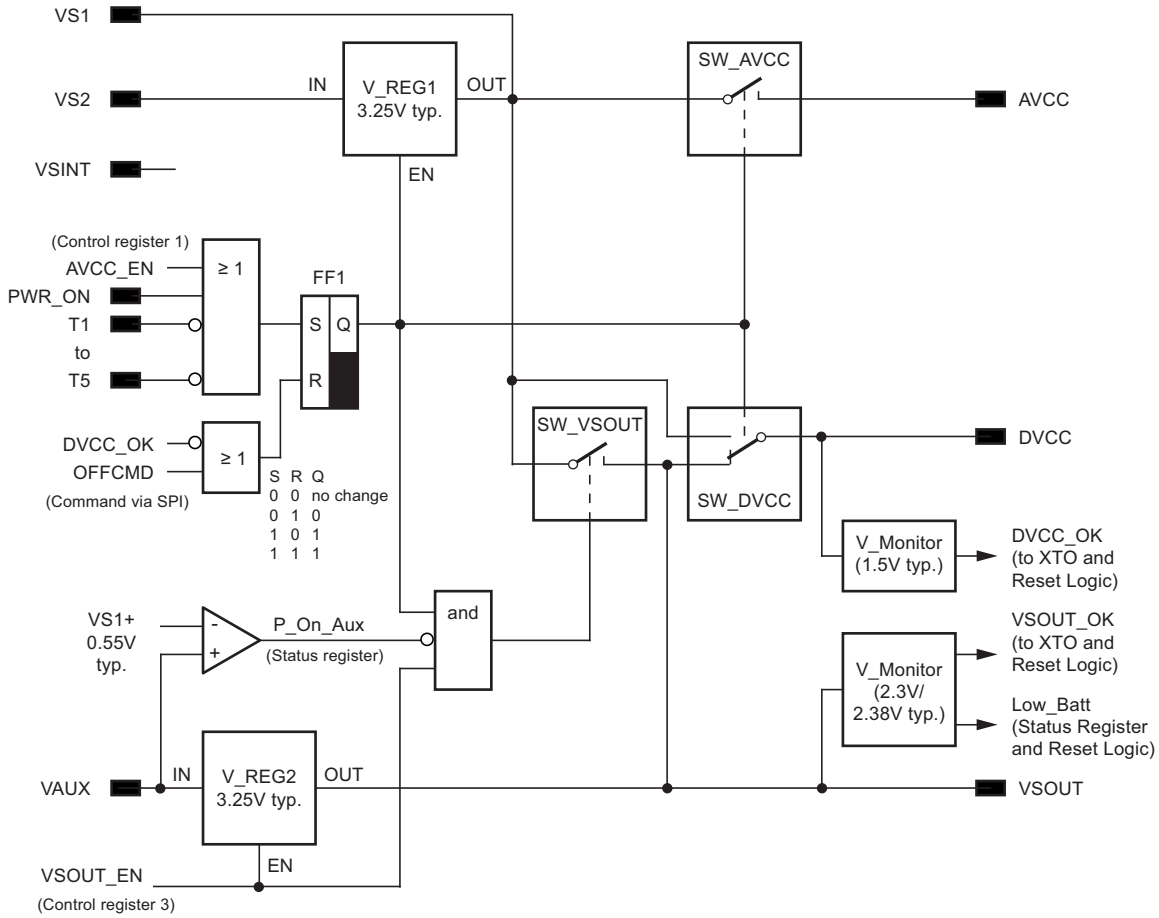
The clock cycle of the bit check and the TX bit rate depends on the selected bit-rate range (BR_Range) which is defined in control register 6 (see Table 7-20 on page 35) and XLim which is defined in control register 4 (see Table 7-13 on page 33). This clock cycle T_{XDCLK} is defined by the following formulas for further reference:

BR_Range ⇒

BR_Range 0: $T_{XDCLK} = 8 \times T_{DCLK} \times X_{Lim}$
BR_Range 1: $T_{XDCLK} = 4 \times T_{DCLK} \times X_{Lim}$
BR_Range 2: $T_{XDCLK} = 2 \times T_{DCLK} \times X_{Lim}$
BR_Range 3: $T_{XDCLK} = 1 \times T_{DCLK} \times X_{Lim}$

5. Power Supply

Figure 5-1. Power Supply



The supply voltage range of the ATA5428 is 2.4V to 3.6V or 4.4V to 6.6V.

Pin VS1 is the supply voltage input for the range 2.4V to 3.6V and is used in 1 Li battery applications (3V) using a single lithium 3V cell. Pin VS2 is the voltage input for the range 4.4V to 6.6V (2 Li battery application (6V) and Base-station Application (5V); in this case, the voltage regulator V_REG1 regulates VS1 to typically 3.25V. If the voltage regulator is active, a blocking capacitor of 2.2µF has to be connected to VS1.

Pin VAUX is an input for an additional auxiliary voltage supply and can be connected, for example, to an inductive supply (see Figure 5-6 on page 29). This input can only be used together with a rectifier or as in the application shown in Figure 2.2 on page 8 and must otherwise be left open.

Pin VSINT is the voltage input for the Microcontoller_Interface and must be connected to the power supply of the microcontroller. The voltage range of V_{VSINT} is 2.4V to 5.25V (see Figure 5-5 on page 29 and Figure 5-6 on page 29).

AVCC is the internal operation voltage of the RF transceiver and is fed by VS1 via the switch SW_AVCC. AVCC must be blocked with a 68nF capacitor (see Figure 2-1 on page 7, Figure 2.2 on page 8 and Figure 2-3 on page 9).

DVCC is the internal operation voltage of the digital control logic and is fed by VS1 or VSOUT via the switch SW_DVCC. DVCC must be blocked on pin DVCC with 68 nF (see Figure 2-1 on page 7, Figure 2.2 on page 8 and Figure 2-3 on page 9).

Pin VSOUT is a power supply output voltage for external devices (for example, microcontrollers) and is fed by VS1 via the switch SW_VSOUT, or by the auxiliary voltage supply VAUX via V_REG2. The voltage regulator V_REG2 regulates VSOUT to typically 3.25V. If the voltage regulator is active, a blocking capacitor of 2.2µF has to be connected to VSOUT. VSOUT can be switched off by the VSOUT_EN bit in control register 3 and is then reactivated by conditions found in Figure 5-2 on page 26.