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ATA5575M1

Read/Write LF RFID IDIC 100kHz to 150kHz

DATASHEET

Features

- Contactless power supply
- Contactless read/write data transmission
- Radio frequency f_{RF} from 100kHz to 150kHz
- 128-bit EEPROM user memory: 16Bytes (8Bits each)
- 8-bit configuration memory
- High Q-antenna tolerance due to built-in options
- Access control applications
  - UNIQUE data format (Manchester, RF/64)
  - 40-bit data memory
  - 15-bit parity memory
  - 9-bit header memory
- On-chip trimmed antenna capacitor
  - 330pF ±3%
  - 250pF ±3%
- Mega pads 200µm × 400µm
- Mega pads 200µm × 400µm with 25µm gold bumps for direct coil bonding
- Other options:
  - Direct access mode
  - OTP functionality

1. Description

The Atmel® ATA5575M1 is a contactless read/write identification IC (IDIC®) for applications in the 100-kHz to 150-kHz frequency band. A single coil connected to the chip serves as the IC's power supply and bi-directional communication interface. This antenna coil together with the chip form a transponder or tag.

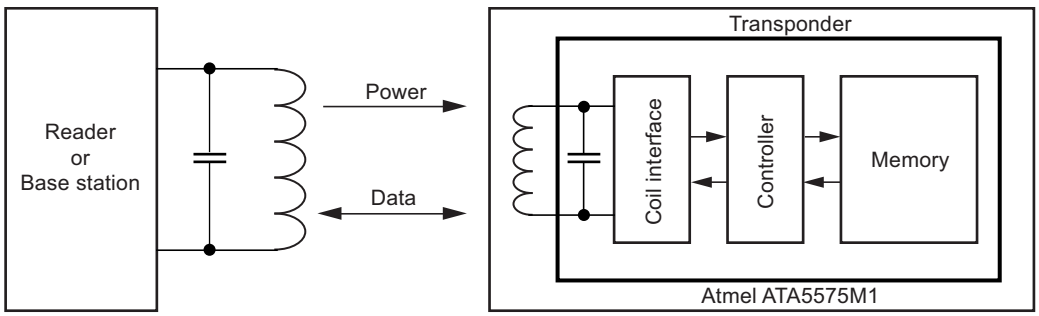
The on-chip 128-bit user EEPROM (16 bytes with 8 bits each) can be read and written byte-wise from a base station (reader). Data is transmitted from the IDIC (uplink) using load modulation. This is achieved by damping the RF field with a resistive load between the two terminals Coil 1 and Coil 2. The IC receives and decodes serial base station commands (downlink), which are encoded as 100% amplitude-modulated (OOK) pulse-interval-encoded bit streams.

The Atmel ATA5575M1 is an EEPROM-based circuit. It is optimized for maximum read range. Programming is also possible, but the write range is limited.

The chip has to be locked after loading the application-specific data into the device. Until the lock bits are set properly, the Atmel ATA5575M1 transmits all digits '0' in UNIQUE Format with appropriate header. Typical applications run at 125kHz.

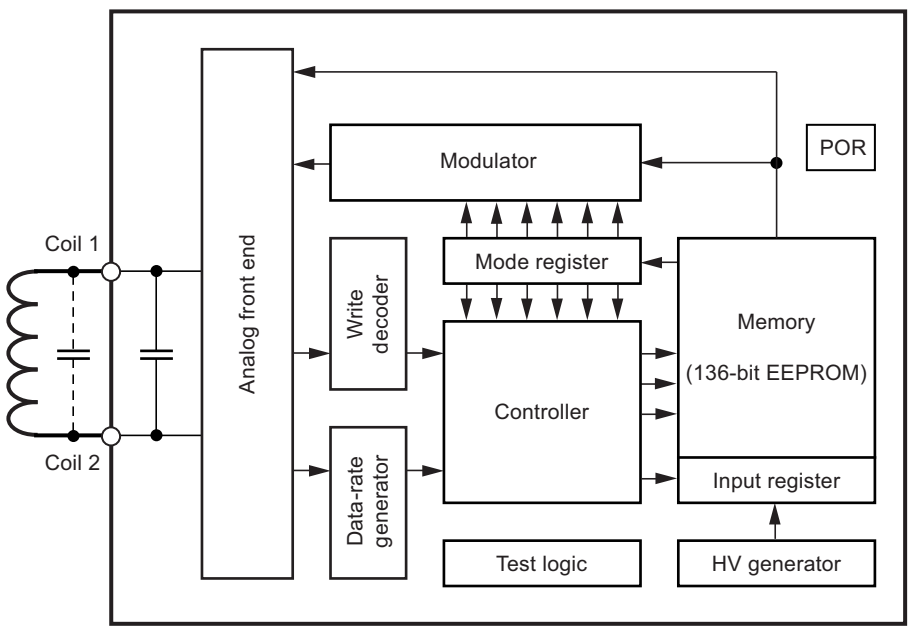
2. System Block Diagram

Figure 2-1. RFID System Using Atmel ATA5575M1 Tag



3. Atmel ATA5575M1 - Functional Blocks

Figure 3-1. Block Diagram



4. Analog Front End (AFE)

The AFE includes all circuits which are directly connected to the coil terminals, it generates the IC's power supply and handles the bi-directional data communication with the reader. The AFE consists of the following blocks:

- Rectifier to generate a DC supply voltage from the AC coil voltage
- Clock extractor
- Switchable load between Coil 1 and Coil 2 for data transmission from tag to the reader
- Field-gap detector for data transmission from the base station to the tag
- ESD protection circuitry

4.1 Data Rate Generator

The data rate is fixed to RF/64.

4.2 Write Decoder

The write decoder detects the write gaps and verifies the validity of the data stream according to the Atmel® downlink protocol (pulse interval encoding).

4.3 HV Generator

This on-chip charge pump circuit generates the high voltage required for programming the EEPROM.

4.4 DC Supply

Power is externally supplied to the IDIC® via the two coil connections. The IC rectifies and regulates this RF source and uses it to generate its supply voltage.

4.5 Power-On Reset (POR)

The power-on reset circuit blocks the voltage supply to the IDIC until an acceptable voltage threshold has been reached. This, in turn, triggers the default initialization delay sequence. During this configuration period of 98 field clocks, the ATA5575M1 is initialized with the configuration data stored in EEPROM byte 16.

4.6 Clock Extraction

The clock extraction circuit uses the external RF signal as its internal clock source.

4.7 Controller

The control logic module executes the following functions:

- Load mode register with configuration data from EEPROM byte 16 after power-on and during reading
- Controls each EEPROM memory read/write access and handles the data protection
- Handle the downlink command decoding, detecting protocol violations and error conditions

4.8 Mode Register

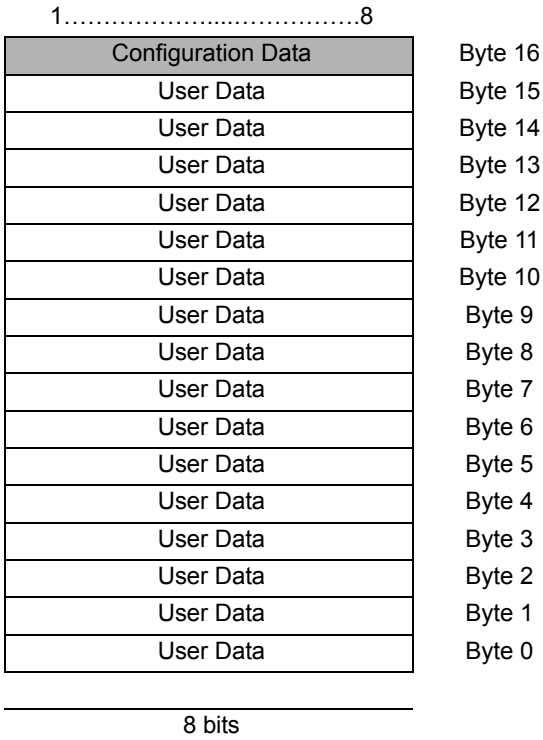
The mode register maintains a readable shadow copy of the configuration data held in byte 16 of the EEPROM. It is continually refreshed during read mode and (re-)loaded after every POR event or reset command. The configuration data is pre-programmed when leaving Atmel's production according to Table 10-1 on page 16.

4.9 Modulator

The modulator encodes the serialized EEPROM data for transmission to a tag reader or base station. The implemented encoding is Manchester.

4.10 Memory

Figure 4-1. Memory Map



The memory is a 136-bit EEPROM, which is arranged in 17 bytes of 8 bits each. Programming is carried out byte-wise, so a complete byte will be programmed with a single command.

Byte 16 contains the mode/configuration data, which is not transmitted during regular read operations.

A special bit combination (see Table 5-1 and Section 5.1.1 “Lock Bits” on page 5) will lock the whole memory. Once locked, the memory (including byte 16 itself) can not be reprogrammed once more via the RF field.

5. Operating the Atmel ATA5575M1

5.1 Configuration

The Atmel® ATA5575M1 is mainly designed for access control applications. The configuration register, byte 16, enables the customer to configure the chip according to the individual application. Modulation is Manchester coding with a data bit rate of RF/64. Default ID length is 64 bit. For specific applications, the ID length can be switched to 128 bit by setting bit 8 of byte 16 to '1'.

Table 5-1. Atmel ATA5575M1: Byte 16 Configuration Register Mapping

1	2	3	4	5	6	7	8	
					1	1		
							ID Length	
							0	64 bit
							1	128 bit
					Fixed '11'			
Lock Bits								
0	0	0	0	0	Memory reprogrammable, read dummy data			
0	1	1	0	1	Memory locked, read user data			
	- otherwise -				unassigned			

Note: Bits 6 and 7 must always be set to '1', otherwise, malfunction will occur

5.1.1 Lock Bits

The lock bits of the configuration register are the bits 1 to 5 of the configuration byte and are able to prevent the whole memory of the Atmel ATA5575M1 from reprogramming.

As long as the lock bits are set to '00000b' the memory is alterable and the device can be programmed by the customer. In this case the Atmel ATA5575M1 sends out dummy data (UNIQUE format with header and all digits set to '0'; see Section 5.3.3 "Dummy Data" on page 6) after Reset.

By setting the lock bits to '01101b' the whole memory is locked and cannot be altered. After Reset the Atmel ATA5575M1 enters regular read mode and sends out the programmed user data.

Consequently the user of a transponder with an Atmel ATA5575M1 can be sure that the device is locked if the programmed data are read out after reset.

In delivery state the lock bits are programmed to '00000b'.

All other combinations of bit 1 - bit 5 are not defined and may lead to malfunction of the IC.

5.1.2 Modulation

The modulator of the Atmel ATA5575M1 is fixed to Manchester coding with a data bit rate of RF/64.

Table 5-2. Atmel ATA5575M1: Types of Modulation

Mode	Direct Data Output Encoding
Manchester	0 = falling edge, 1 = rising edge on mid-bit

5.1.3 ID Length

The Atmel ATA5575M1 offers two settings for the different ID lengths. If bit 8 of byte 16 is set to '1' the ID length is 128 bit. Resetting bit 8 of byte 16 to '0' the ID length is 64 bit.

5.2 UNIQUE Data Format and Unique ID

During Atmel's production process the Atmel ATA5575M1 will be pre-configured in the worldwide well-known UNIQUE data format and a unique ID (UID) will be stored in the user data. The unique ID consists of Atmel's production information like lot number, wafer number, and die-on-wafer number. With these data each chip can be traced and concurrently each chip has its own unique ID for identification purposes.

For UNIQUE data format please refer to Section 7. "Programming Examples" on page 13. Section 10.2 "ATA5575M1 Configuration on Delivery" on page 16 describes the formation of the unique ID based on Atmel's production information.

5.3 Tag-to-reader Communication (Uplink)

Immediately after entering the reader field, generating the internal supply voltage and the analog POR, the tag cycles either its data stored in EEPROM or, in the delivery state, sends dummy data by load modulation according to the configuration setting. This resistive load modulation can be detected at the reader device.

5.3.1 Regular Read Mode

In regular read mode data from the memory is transmitted serially, starting with byte 0, bit 1, up to the last byte, bit 8. Last byte is defined in bit 8 of byte 16, ID Length. When the last bit of the last byte has been read, data transmission restarts with byte 0, bit 1.

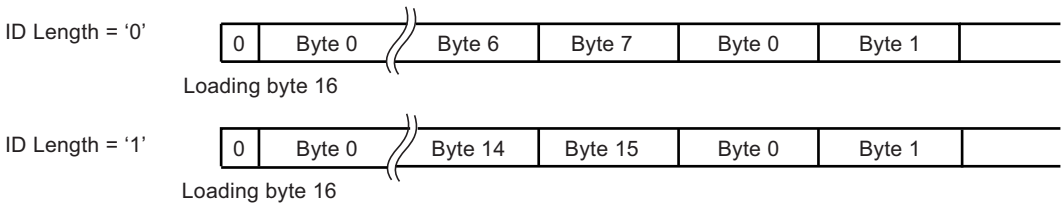
The device only enters regular read mode if the lock bits are set to '01101b' (please refer to Section 5.1.1 "Lock Bits" on page 5).

Last byte is 15, when ID Length = 1 (128 bit).

Last byte is 7, when ID Length = 0 (64 bit).

Every time the Atmel ATA5575M1 enters regular or byte read mode, the first bit transmitted is a logical '0'. The data stream starts with bit 1 of byte 0 or bit 1 of the addressed byte.

Figure 5-1. Examples for Different ID Length Settings



5.3.2 Byte Read Mode

With the direct access command, only the addressed byte is read repetitively. This mode is called byte-read mode. Direct access is entered by transmitting the opcode ('10'), a single 0 bit and the requested 5-bit byte address.

5.3.3 Dummy Data

The dummy data are a predefined bit sequence in the UNIQUE format. They consist of a header of nine '1' bit ('111111111b') followed by 55 times '0' bit if ID length is set to 64 bit or 119 times '0' bit if ID length is set to 128 bits.

In contrast to the regular read mode the dummy data are transmitted if the lock bits are set to '00000b'. Therefore they can be used to check the integrity of the device e.g. in delivery state.

Consequently if the dummy data are read out after Reset the memory is not locked.

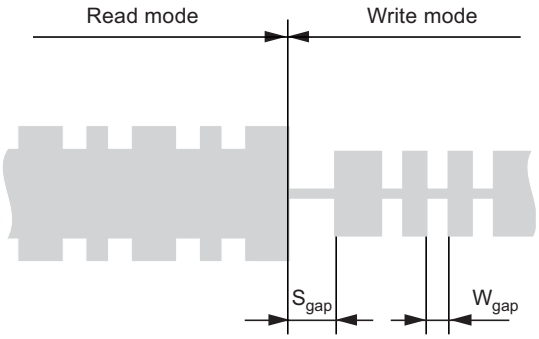
5.4 Reader-to-tag Communication (Downlink)

Data is transmitted to the tag by interrupting the RF field with short field gaps (on-off keying) according to the Atmel® ATA5577 fixed-bit-length protocol (downlink mode). The duration of these field gaps is, for example, 100µs. The time between two gaps encodes the 0/1 information to be transmitted (pulse interval encoding). The time between two gaps is nominally 25 field clocks for a 0 and 58 field clocks for a 1. When there is no gap for more than 64 field clocks after a previous gap, the ATA5575M1 exits the downlink mode. The tag starts with the command execution if the correct number of bits were received. If a failure is detected, the ATA5575M1 does not continue command execution and enters read mode depending on the setting of the lock bits.

The initial gap, called start gap, triggers the reader-to-tag communication. The start gap may need to be longer than the subsequent gaps - so-called write gaps - in order to be detected reliably.

A start gap will be accepted at any time after the mode register has been loaded (≥ 1ms).

Figure 5-2. Start of Reader-to-tag Communication (Downlink)



Downlink data decoding scheme in number of field clocks (T_C)

Table 5-3. Downlink Data Decoding Scheme in Number of Field Clocks (T_C)

Parameter	Remark	Symbol	Min.	Typ.	Max.	Unit
Start gap		S_{gap}	8	15	50	T_C
Write gap		W_{gap}	8	10	20	T_C
Write data coding (gap separation)	0 data	d_0	18	25	33	T_C
	1 data	d_1	50	58	65	T_C

Note: All absolute times are given under the assumption of $T_C = 1/f_C = 8µs$ ($f_C = 125kHz$)

5.4.1 Downlink Data Protocol

The Atmel® ATA5575M1 expects to receive a dual bit opcode as a part of a reader command sequence. There are three valid opcodes and overall five different commands (please refer to Figure 5-4 on page 8).

- The RESET opcode '00' starts an initialization cycle
- A single '10' opcode (Read ID) leads to reading the ID out of the EEPROM memory. This is suitable to check the programmed user data if the memory is not locked already.
- The opcode '10' precedes all downlink operations for writing data into the EEPROM
- The opcode ‘11’ reads the upper bytes when the ID length (bit 8 of byte 16) is set to ‘0’
  If the ID length is set to ‘1’ opcode ‘11’ is the same as opcode ‘10’
- The *Write Byte* requires the opcode ‘10’, a ‘0’ bit, 8 data bits and the 5-bit address (16 bits total)
- For *Direct* access, the opcode ‘10’, a ‘0’ bit and a 5-bit address (8 bits total), is required

Note: The data bits are read in the same order as being written.

Figure 5-3. Complete Write Sequence

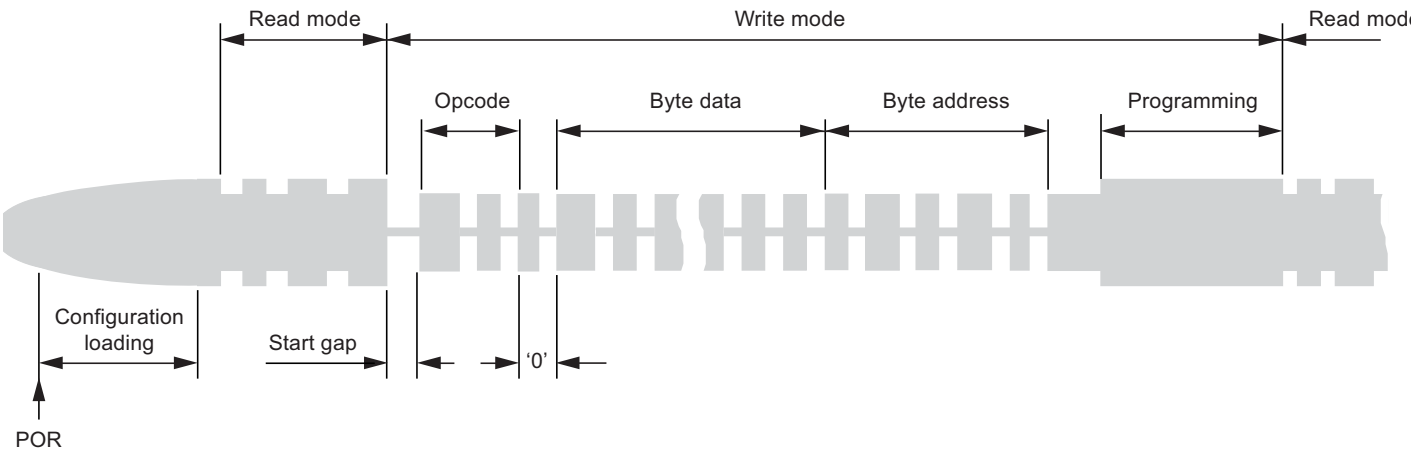
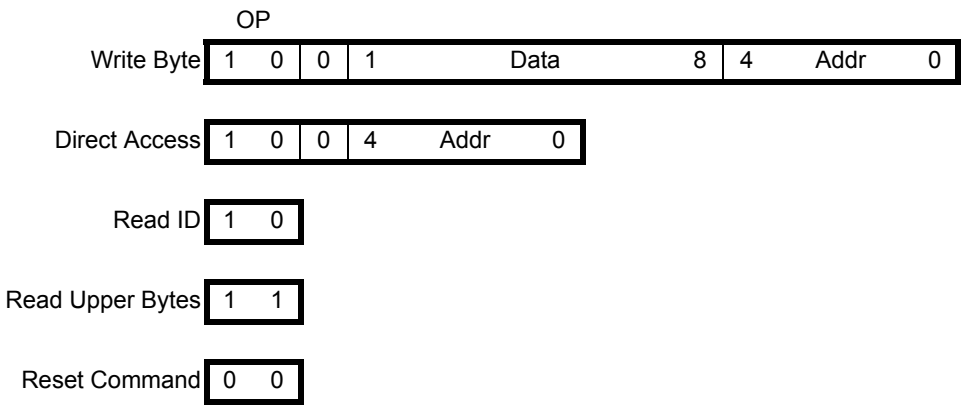


Figure 5-4. ATA5575M1 Command Formats



5.5 Programming

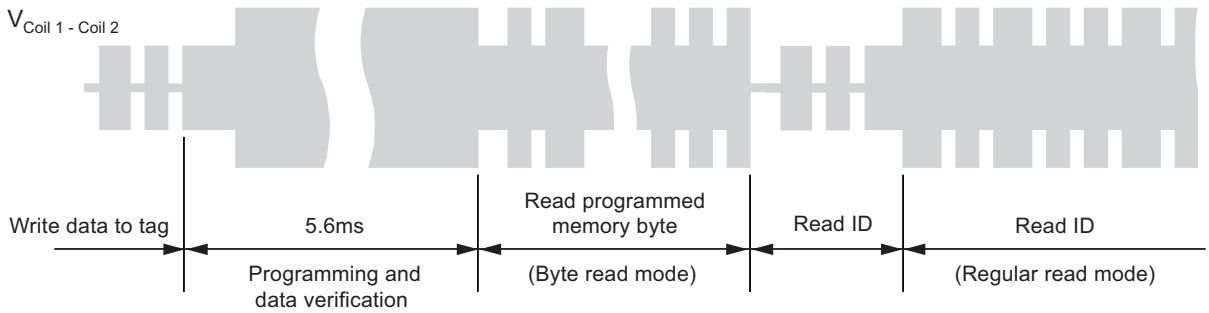
When all necessary information has been received by the Atmel® ATA5575M1, programming may proceed. There is a clock delay between the end of the writing sequence and the start of programming.

Typical programming time is 5.6ms. This cycle includes a data verification read to grant secure and correct programming. After successful programming, the Atmel ATA5575M1 enters byte read mode, transmitting the byte just programmed.

After validation of the command sequence, the new data will be programmed into the EEPROM memory.

Each programming cycle consists of four consecutive steps: erase byte, erase verification (data = 0), programming, programming verification (corresponding data bits = 1).

Figure 5-5. Coil Voltage after Programming a Byte



6. Error Handling

To prevent that invalid bits are programmed into the EEPROM, the device is able to detect two main error types and several error conditions.

6.1 Errors During Command Sequence

The following detectable errors may occur when sending a command sequence to the Atmel® ATA5575M1:

- Wrong number of field clocks between two gaps (i.e., not a valid 1 or 0 pulse stream)
- The number of bits received in the command sequence is incorrect

Table 6-1. Bit Counts of Command Sequences

Command	Number of Bits
Write byte	16
Direct access	8
Read ID	2
Read upper bytes	2
Reset command	2

6.2 Errors Before/During Programming the EEPROM

If the command sequence was received successfully, the following errors may still prevent programming:

- The lock bits of the memory are already set
- If the memory is locked, programming is not possible. The Atmel ATA5575M1 enters byte read mode, continuously transmitting the currently addressed byte.
- If a data verification error is detected after the programming of an executed data byte, the tag will stop modulation (modulation defeat) until a new command is transmitted.

Figure 6-1. Atmel ATA5575M1 Functional Diagram

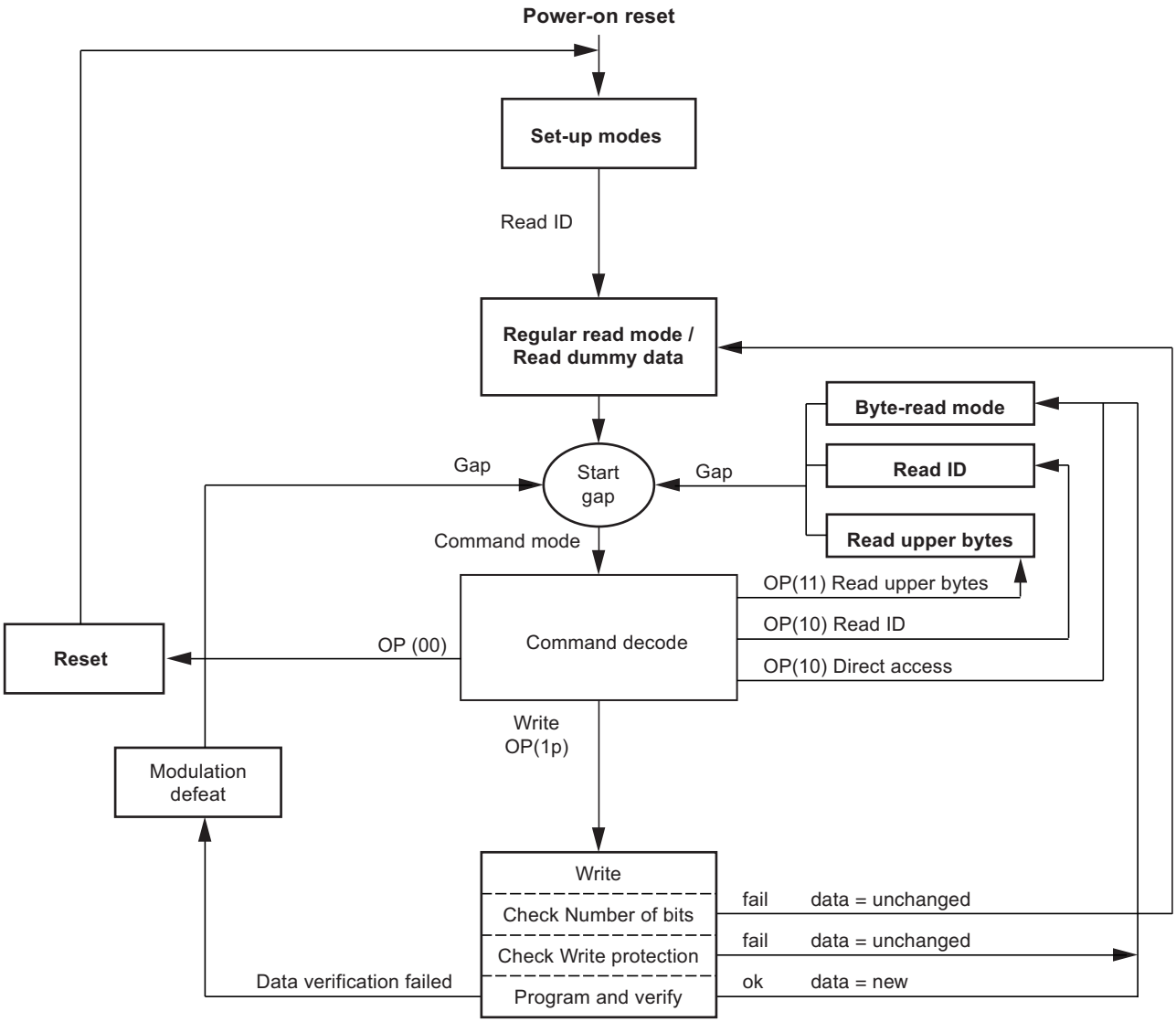
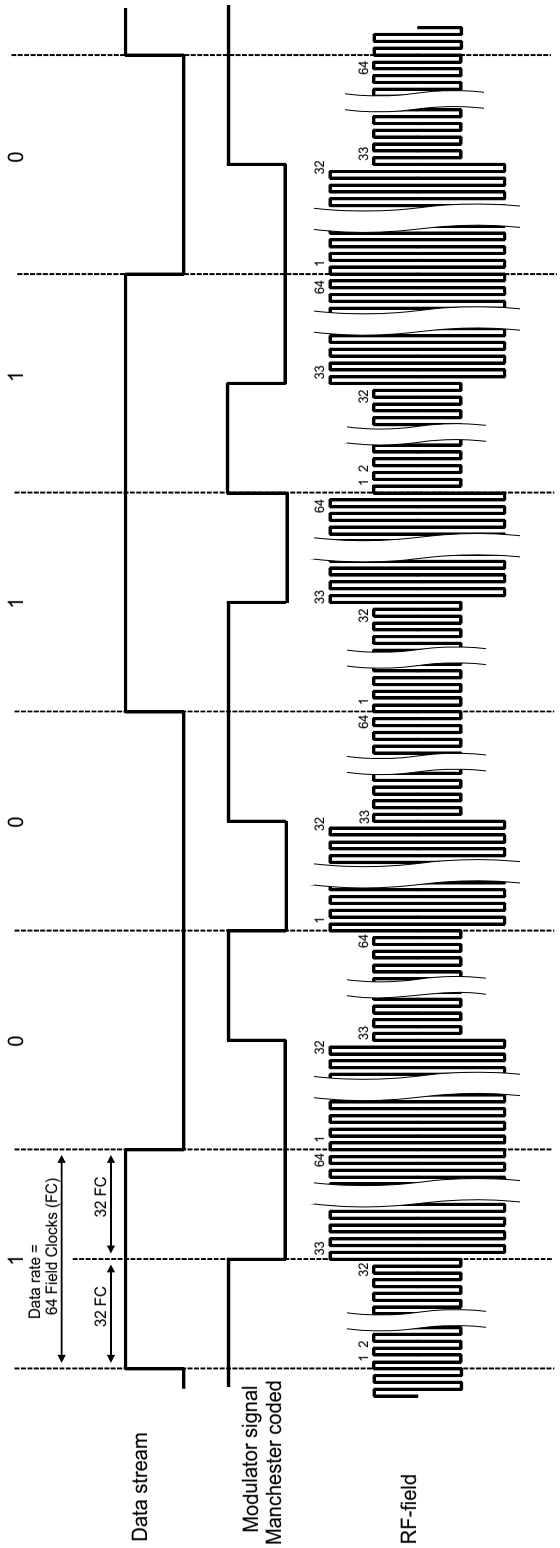


Figure 6-2. Example of Manchester Coding with Data Rate RF/64



7. Programming Examples

A typical application with Manchester Coding and data rate RF/64 is access control with the UNIQUE Format data structure of 64 bit as described in Figure 7-1.

Figure 7-1. ATA5575M1: 64-bit User Data in UNIQUE Format

‘1’	‘1’	‘1’	‘1’	‘1’	‘1’	‘1’	‘1’	‘1’	9 header bits
bit 1			Digit 0	D00	D01	D02	D03	PR0	even row parity bit per digit
			Digit 1	D10	D11	D12	D13	PR1	
	byte 0 to byte 3		Digit 2	D20	D21	D22	D23	PR2	
			Digit 3	D30	D31	D32	D33	PR3	
			Digit 4	D40	D41	D42	D43	PR4	
			Digit 5	D50	D51	D52	D53	PR5	
			Digit 6	D60	D61	D62	D63	PR6	
	byte 4 to byte 7		Digit 7	D70	D71	D72	D73	PR7	
			Digit 8	D80	D81	D82	D83	PR8	
			Digit 9	D90	D91	D92	D93	PR9	
				PC0	PC1	PC2	PC3	‘0’	
				even column parity bits				bit 64	

Table 7-1 on page 13 describes a programming of Atmel® ATA5575M1 with UNIQUE format example data:

Digit 0, Digit 1, …, Digit 9 = 0, 1, 2, 3, 4, 5, 6, 7, 8, 9

Table 7-1. Programming Atmel ATA5575M1 with UNIQUE Format Example Data

Base Station	ATA5575M1
Field on for t = 5ms	POR and regular read mode
Command: 00	Reset
Command: 10 0 0000 0110 10000	Programming byte 16 with ‘06h’ (UNIQUE mode (Man RF/64, 64 bit), memory reprogrammable)
Command: 10 0 1111 1111 00000	Programming byte 0 with ‘FFh’
Command: 10 0 1000 0000 00001	Programming byte 1 with ‘80h’
Command: 10 0 0110 0101 00010	Programming byte 2 with ‘65h’
Command: 10 0 0011 0010 00011	Programming byte 3 with ‘32h’
Command: 10 0 0101 0100 00100	Programming byte 4 with ‘54h’
Command: 10 0 1100 0111 00101	Programming byte 5 with ‘C7h’
Command: 10 0 1100 0110 00110	Programming byte 6 with ‘C6h’
Command: 10 0 0100 0010 00111	Programming byte 7 with ‘42h’
Command: 10	Read ID
Field on for t = 50ms Read and verify data in UNIQUE format	Send data in UNIQUE format
Command: 10 0 0110 1110 10000	Programming byte 16 with ‘6Eh’ (memory locked, UNIQUE mode: Man RF/64, 64bit)
Command: 00	Reset
Field on for t = 50ms Read and verify data in UNIQUE format	Send data in UNIQUE format

8. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Value	Unit
Maximum DC current into Coil1/Coil2	I_{coil}	20	mA
Maximum AC current into Coil1/Coil2 f = 125kHz	$I_{coil\ p}$	20	mA
Power dissipation (dice) (free-air condition, time of application: 1s)	P_{tot}	100	mW
Electrostatic discharge maximum to ANSI/ESD-STM5.1-2001 standard (HBM)	V_{max}	2000	V
Operating ambient temperature range	T_{amb}	–40 to +85	°C
Storage temperature range	T_{stg}	–40 to +150	°C

Note: For data retention please refer to Section 9. “Electrical Characteristics” on page 14

9. Electrical Characteristics

T_{amb} = +25°C; f_{coil} = 125kHz; unless otherwise specified

No.	Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit	Type*
1	RF frequency range		f_{RF}	100	125	150	kHz	
2.1	Supply current (without current consumed by the external LC tank circuit)	T_{amb} = 25°C(1)	I_{DD}		1.5	3	µA	T
2.2		Read – full temperature range			2	5	µA	Q
2.3		Programming – full temperature range			25		µA	Q
3.1	Coil voltage (AC supply)	Read mode and write command(2)	$V_{coil\ pp}$	6		V_{clamp}	V	Q
3.2		Program EEPROM(2)		16		V_{clamp}	V	Q

*) Type means: T: directly or indirectly tested during production; Q: guaranteed based on initial product qualification data

Notes:
1. I_{DD} measurement setup: EEPROM programmed to 00 ... 000 (erase all); chip in modulation defeat.
2. Current into Coil1/Coil2 is limited to 10mA.
3. Since the EEPROM performance is influenced by assembly processes, Atmel can not confirm the parameters for -DDW (tested die on unsawn wafer) delivery.
4. See Section 10. “Ordering Information” on page 16.

9. Electrical Characteristics (Continued)

T_{amb} = +25°C; f_{coil} = 125kHz; unless otherwise specified

No.	Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit	Type*
4	Start-up time	$V_{coil\ pp}$ = 6V	$t_{startup}$		1.1		ms	Q
5.1	Clamp	3mA current into Coil1/2	V_{pp}	15	18	21	V	T
5.2		20mA current into Coil1/2	V_{pp}	17	20	24	V	T
6.1	Modulation parameters	3mA current into Coil1/2 and modulation ON	V_{pp}	2	3	4	V	T
6.2		20mA current into Coil1/2 and modulation ON	V_{pp}	4.5	5	8.5	V	T
6.3	Thermal stability of modulation parameter		V_p/T_{amb}		–1		mV/°C	Q
7.1	Clock detection level	$V_{coil\ pp}$ = 8V	V_{clkdet}	400	550	750	mV	T
7.2	Gap detection level	$V_{coil\ pp}$ = 8V	$V_{gapdet\ med}$	400	550	750	mV	T
8	Programming time	From last command gap to re-enter read mode (64 + 648 internal clocks)	T_{prog}	5	5.7	6	ms	T
9	Endurance	Erase all / write all(3)	n_{cycle}	100000			Cycles	Q
10.1	Data retention	Top = 55°C(3)	$t_{retention}$	10	20	50	Years	Q
10.2		Top = 150°C(3)	$t_{retention}$	96			hrs	T
10.3		Top = 250°C(3)	$t_{retention}$	24			hrs	Q
11.1	Resonance capacitor	Mask option(4) $V_{coil\ pp}$ = 1V	C_r	320	330	340	pF	T
11.2				242	250	258		

*) Type means: T: directly or indirectly tested during production; Q: guaranteed based on initial product qualification data

Notes:
1. I_{DD} measurement setup: EEPROM programmed to 00 ... 000 (erase all); chip in modulation defeat.
2. Current into Coil1/Coil2 is limited to 10mA.
3. Since the EEPROM performance is influenced by assembly processes, Atmel can not confirm the parameters for -DDW (tested die on unsawn wafer) delivery.
4. See Section 10. “Ordering Information” on page 16.

10. Ordering Information

ATA5575M1	ccc	-xxx	Package		Drawing
			DDB	6” sawn wafer on foil with ring, thickness 150µm (approx. 6mil)	Figure 11-1 on page 18
			DBB	6” sawn wafer on foil with ring and gold bumps 25µm, thickness 150µm (approx. 6mil)	Figure 11-2 on page 19
			DBQ	Die in blister tape with gold bumps 25µm, thickness 280µm	Figure 11-3 on page 20
		On-chip capacity value in pF			
			250	(planned)	
			330		
	33L		DDB	As ATA5575M1330-DDB, pre-programmed in unique format and locked	Figure 11-1 on page 18
	33L		DBB	As ATA5575M1330-DBB, pre-programmed in unique format and locked	Figure 11-2 on page 19

10.1 Available Order Codes

Atmel ATA5575M1330-DDB

Atmel ATA5575M1330-DBB

Atmel ATA5575M1330-DBQ

Atmel ATA5575M133L-DDB

Atmel ATA5575M133L-DBB

New order codes will be created by customer request if order quantities exceed 250k pieces.

10.2 ATA5575M1 Configuration on Delivery

On delivery Atmel’s production information is stored in EEPROM user data in UNIQUE format as described in Figure 7-1 on page 13.

Table 10-1. ATA5575M1: Configuration on Delivery

Byte	Address	Value	Comment
User data byte 0 to byte 7	0b 0 0000 to 0b 0 0111	Variable data	Unique ID in UNIQUE format
User data byte 8 to byte 15	0b 0 1000 to 0b 0 1111	Variable data	Unique ID in UNIQUE format (copy of byte 0 to byte 7)
Configuration (byte 16)	0b 1 0000	0x 06	Send UNIQUE format (Man RF/64, ID length = 64) with all digits ‘0’

The user data contains Atmel's lot and production information, which builds a unique ID numbering system as described in Table 10-2 on page 17.

Table 10-2. Atmel ATA5575M1: Meaning of the Digits in Delivery State

	Denotation	Bit	Bitcount	Description
LSB first:	IC revision:	D00	1	D00 is LSB of IC revision
	Lot ID and wafer number:	D01-D60	24	D01 is LSB of lot ID & wafer number
	DoW:	D61-D93	15	D61 is LSB of die on wafer

The lot ID and wafer number. (D01 to D60) contain the lot information and the wafer number. Including the die-on-wafer number, this information is used to build a unique ID numbering system, which means that each ATA5575M1 has a unique ID to distinguish from each other.

Atmel's lot ID has the following topology:

YQNNNN(#Wf)

- Y: alphanumeric 0, …, 9
- Q: character F, G, H and J
- NNNN: alphanumeric consecutive number 0, …, 9999
- (#Wf): alphanumeric for wafer number 1, …, 25

Lot ID and Wf No. is built in the following way:

- Transform Q = F, G, H, J into QQ = 0, …, 3
- Transform wafer = 1, …, 25 into WW = 0, …, 24
- Lot ID and wafer number = Y × 1.000.000 + QQ × 250.000 + NNNN × 25 + WW

This number is written binary into D01 to D60 with LSB first.

10.2.1 ATA5575M1 Example for Memory Content on Delivery

- ICR: '1b'
- Lot number: 9F0164
- Wafer number: 12
- Die on wafer: 9.127

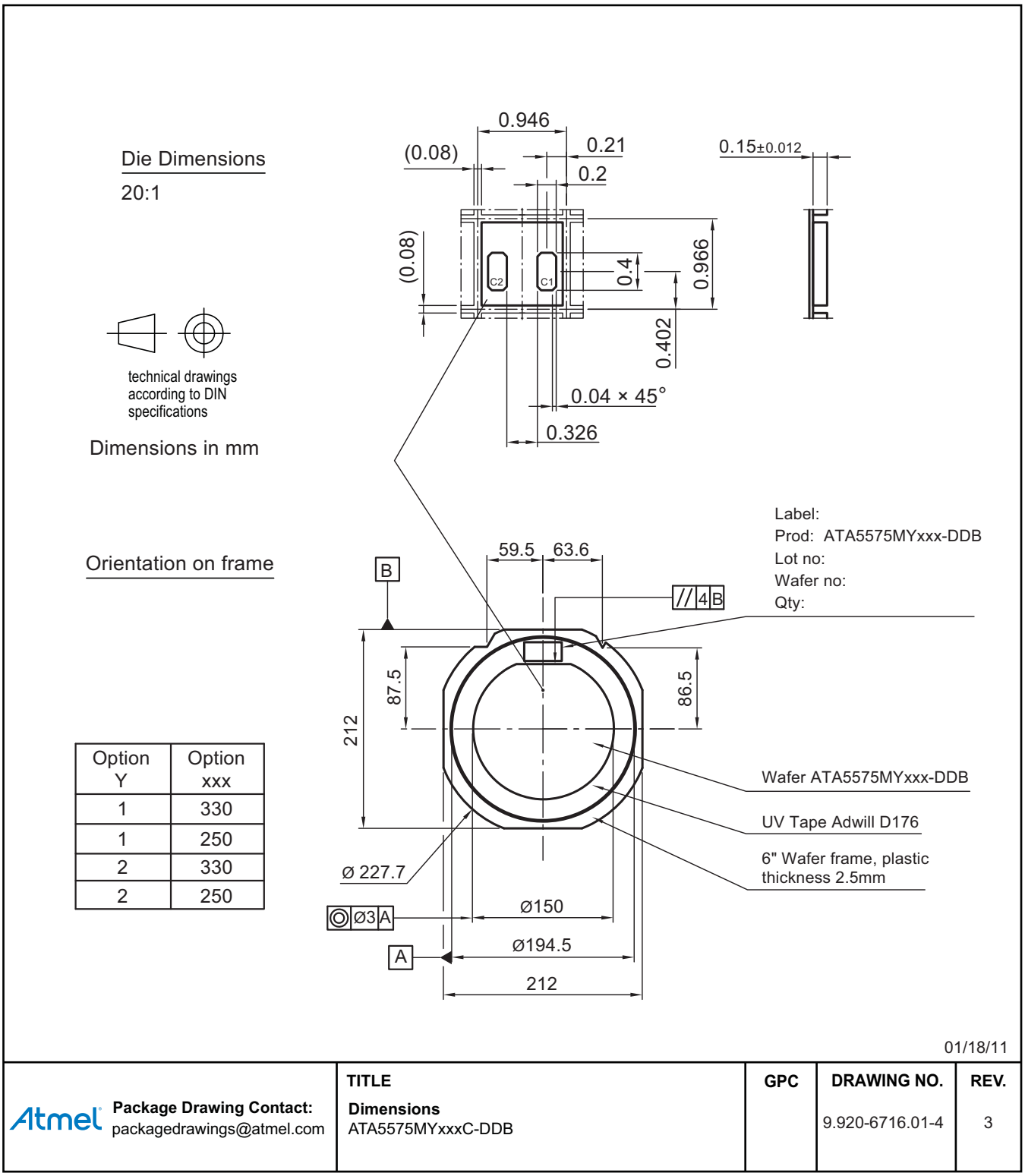
Lot ID and Wf No = 9 × 1.000.000 + 0 × 250.000 + 0164 × 25 + 11 = 9.004.111

Table 10-3. ATA5575M1: Example of Memory Content on Delivery

Byte#	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Meaning	Header	Header / ICR / lot ID and wafer no.	Lot ID and wafer no.	Lot ID and wafer no.	Lot ID and wafer no.	Lot ID and wafer no./ DoW	DoW	DoW	Header	Header / ICR / Lot ID and wafer no.	Lot ID and wafer no.	Lot ID and wafer no.	Lot ID and wafer no.	Lot ID and wafer no./ DoW	DoW	DoW	Confi-guration
Value [hex]	FF	FA	43	32	63	E2	F4	B2	FF	FA	43	32	63	E2	F4	B2	06

11. Package Information

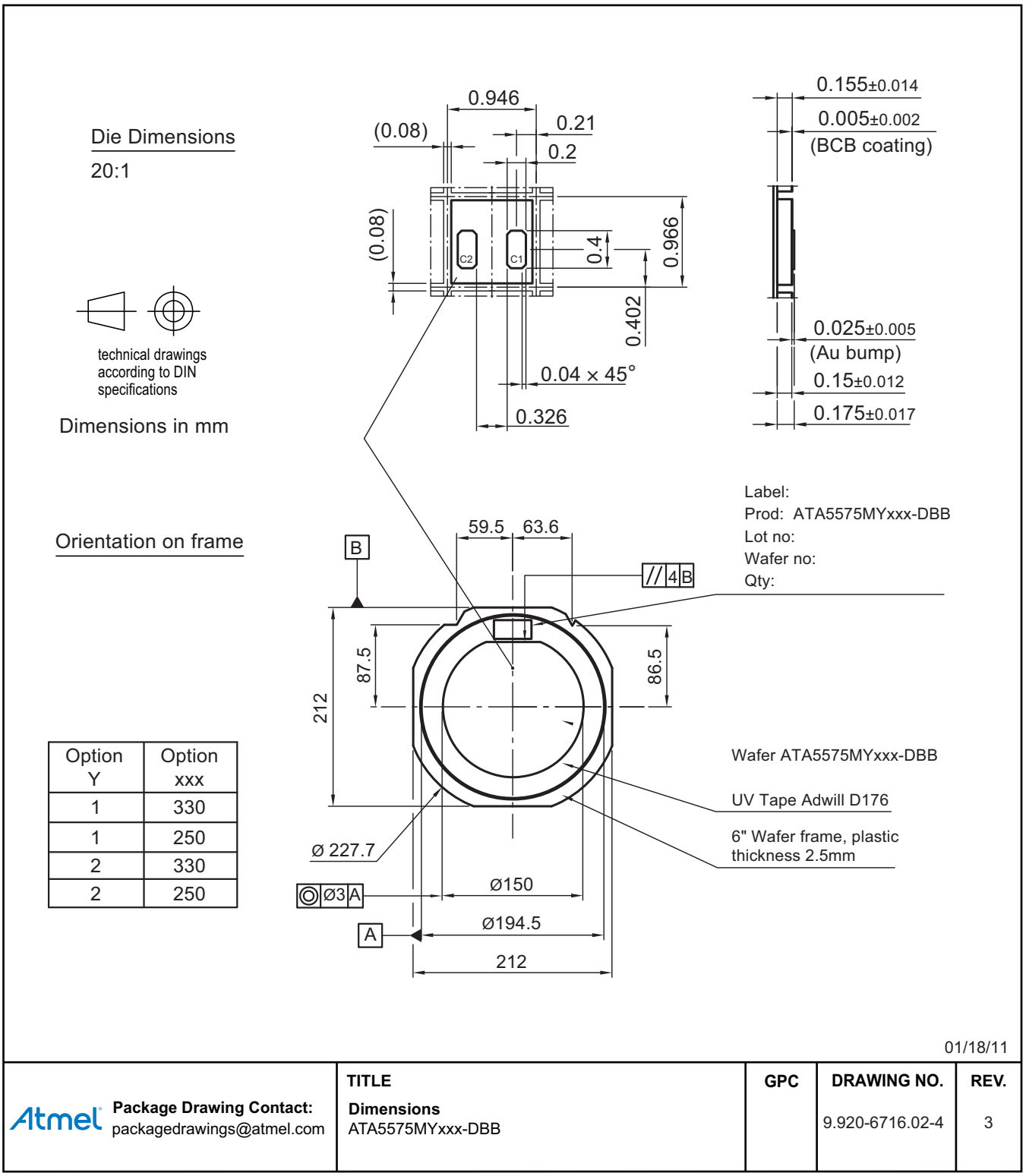
Figure 11-1. 6” Wafer on Foil with Ring



Option Y	Option xxx
1	330
1	250
2	330
2	250

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	**Dimensions** ATA5575MYxxxC-DDB		9.920-6716.01-4	3

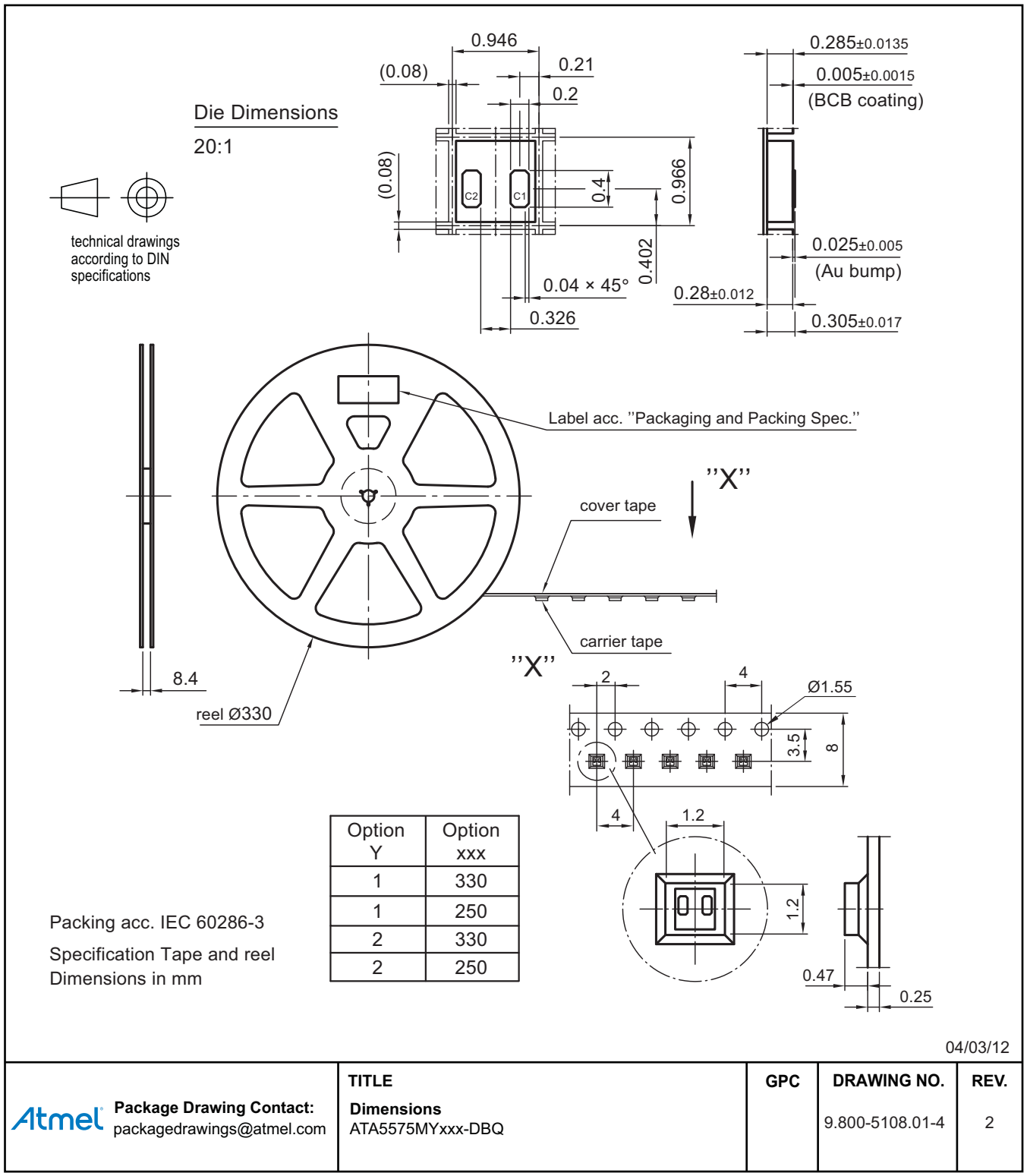
Figure 11-2. 6” Wafer on Foil with Ring and Gold Bumps 25µm



Option Y	Option xxx
1	330
1	250
2	330
2	250

Package Drawing Contact: packagedrawings@atmel.com	TITLE	GPC	DRAWING NO.	REV.
	Dimensions ATA5575MYxxx-DBB		9.920-6716.02-4	3

Figure 11-3. Die in Blister Tape with Gold Bumps 25µm



Option Y	Option xxx
1	330
1	250
2	330
2	250

04/03/12

Package Drawing Contact: packagedrawings@atmel.com	TITLE Dimensions ATA5575MYxxx-DBQ	GPC	DRAWING NO.	REV.
			9.800-5108.01-4	2

12. Revision History

Revision No.	History
9167G-RFID-08/14	• Put datasheet in the latest template
9167F-RFID-04/13	• Section 10 “Ordering Information” on page 16 updated • Section 11 “Package Information” on page 20 updated
9167E-RFID-07/12	• Section 10 “Ordering Information” on page 16: Ordering codes added
9167D-RFID-12/11	• Set datasheet from Preliminary to Standard
9167C-RFID-04/11	• Features on page 1 updated • Section 1 “Description” on page 1 changed • Section 4 “Analog Front End (AFE) on pages 3 to 4 changed • Section 5 “Operating the Atmel ATA5575M1” on pages 5 to 9 changed • Section 6 “Error Handling” on pages 10 to 11 changed • Section 7 “Programming Examples” on pages 13 to 14 changed • Section 8 “Absolute Maximum Ratings” on page 15 updated • Section 9 “Electrical Characteristics” on pages 15 to 16 updated • Section 11 “Package Information” on pages 19 to 21 updated
9167B-RFID-10/10	• Section 8 “Absolute Maximum Ratings” on page 15 changed • Section 9 “Electrical Characteristics” on pages 15 to 16 changed • Section 10.2 “Atmel ATA5575M1 Configuration on Delivery” on pages 17 to 18 changed

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