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Features

- Frequency Receiving Range of (3 Versions)
  - f_0 = 312.5 MHz to 317.5 MHz or
  - f_0 = 431.5 MHz to 436.5 MHz or
  - f_0 = 868 MHz to 870 MHz
- 30 dB Image Rejection
- Receiving Bandwidth
  - B_{IF} = 300 kHz for 315 MHz/433 MHz Version
  - B_{IF} = 600 kHz for 868 MHz Version
- Fully Integrated LC-VCO and PLL Loop Filter
- Very High Sensitivity with Power Matched LNA
  - ATA5723/ATA5724:
    –107 dBm, FSK, BR_0 (1.0 kBit/s to 1.8 kBit/s), Manchester, BER 10E-3
    –113 dBm, ASK, BR_0 (1.0 kBit/s to 1.8 kBit/s), Manchester, BER 10E-3
  - ATA5728:
    –105 dBm, FSK, BR_0 (1.0 kBit/s to 1.8 kBit/s), Manchester, BER 10E-3
    –111 dBm, ASK, BR_0 (1.0 kBit/s to 1.8 kBit/s), Manchester, BER 10E-3
- High System IIP3
  - –18 dBm at 868 MHz
  - –23 dBm at 433 MHz
  - –24 dBm at 315 MHz
- System 1-dB Compression Point
  - –27.7 dBm at 868 MHz
  - –32.7 dBm at 433 MHz
  - –33.7 dBm at 315 MHz
- High Large-signal Capability at GSM Band (Blocking –33 dBm at +10 MHz, IIP3 = –24 dBm at +20 MHz)
- Logarithmic RSSI Output
- XTO Start-up with Negative Resistor of 1.5 kΩ
- 5V to 20V Automotive Compatible Data Interface
- Data Clock Available for Manchester and Bi-phase-coded Signals
- Programmable Digital Noise Suppression
- Low Power Consumption Due to Configurable Polling
- Temperature Range –40°C to +105°C
- ESD Protection 2 kV HBM, All Pins
- Communication to Microcontroller Possible using a Single Bi-directional Data Line
- Low-cost Solution Due to High Integration Level with Minimum External Circuitry Requirements
- Supply Voltage Range 4.5V to 5.5V

Benefits

- Low BOM List Due to High Integration
- Use of Low-cost 13 MHz Crystal
- Lowest Average Current Consumption for Application Due to Self Polling Feature
- Reuse of ATA5743 Software
- World-wide Coverage with One PCB Due to 3 Versions are Pin Compatible

UHF ASK/FSK Receiver

ATA5723
ATA5724
ATA5728

9106E–RKE–07/08

1. Description

The ATA5723/ATA5724/ATA5728 is a multi-chip PLL receiver device supplied in an SSO20 package. It has been specially developed for the demands of RF low-cost data transmission systems with data rates from 1 kBit/s to 10 kBbit/s in Manchester or Bi-phase code. Its main applications are in the areas of keyless entry systems, tire pressure monitoring systems, telemetering, and security technology systems. It can be used in the frequency receiving range of f_0 = 312.5 MHz to 317.5 MHz, f_0 = 431.5 MHz to 436.5 MHz or f_0 = 868 MHz to 870 MHz for ASK or FSK data transmission. All the statements made below refer to 315 MHz, 433 MHz and 868.3 MHz applications.

Figure 1-1. System Block Diagram

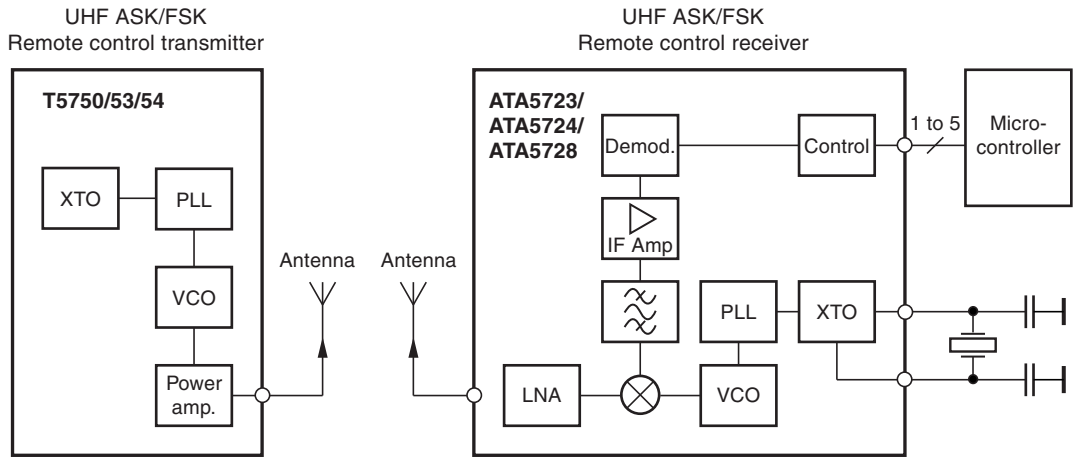
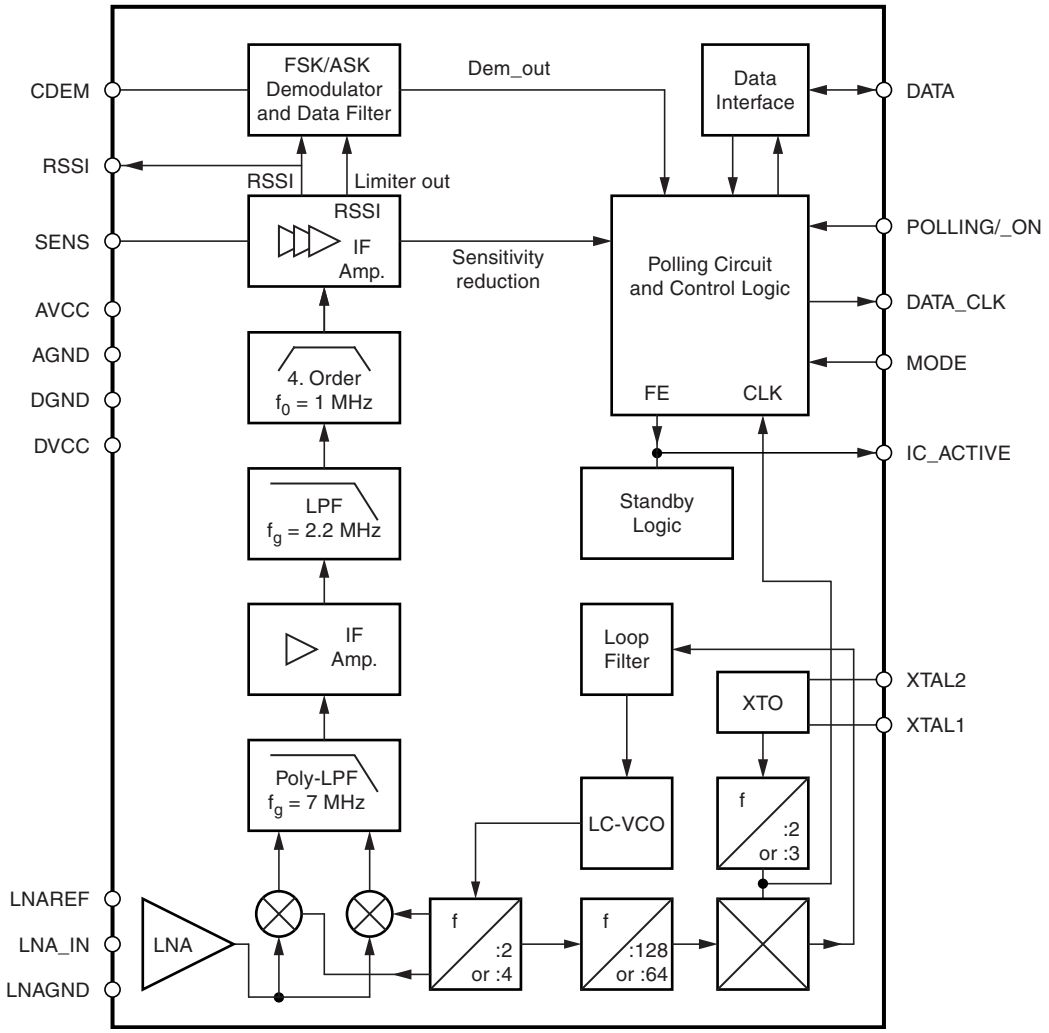


Figure 1-2. Block Diagram



2. Pin Configuration

Figure 2-1. Pinning SSO20

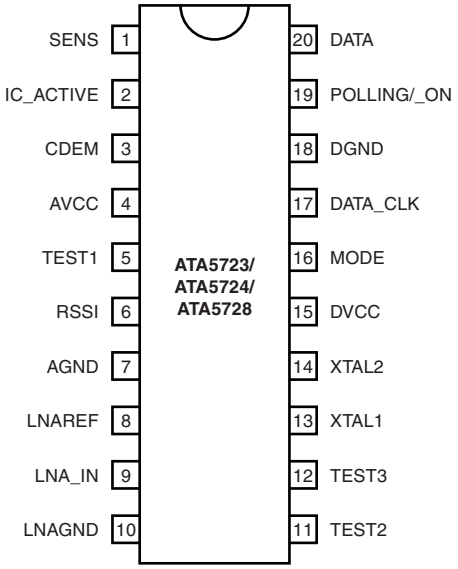


Table 2-1. Pin Description

Pin	Symbol	Function
1	SENS	Sensitivity-control resistor
2	IC_ACTIVE	IC condition indicator: Low = sleep mode, High = active mode
3	CDEM	Lower cut-off frequency data filter
4	AVCC	Analog power supply
5	TEST 1	Test pin, during operation at GND
6	RSSI	RSSI output
7	AGND	Analog ground
8	LNAREF	High-frequency reference node LNA and mixer
9	LNA_IN	RF input
10	LNAGND	DC ground LNA and mixer
11	TEST 2	Do not connect during operating
12	TEST 3	Test pin, during operation at GND
13	XTAL1	Crystal oscillator XTAL connection 1
14	XTAL2	Crystal oscillator XTAL connection 2
15	DVCC	Digital power supply
16	MODE	Selecting 315 MHz/other versions Low: 315 MHz version (ATA5723) High: 433 MHz/868 MHz versions (ATA5724/ATA5728)
17	DATA_CLK	Bit clock of data stream
18	DGND	Digital ground
19	POLLING/_ON	Selects polling or receiving mode; Low: receiving mode, High: polling mode
20	DATA	Data output/configuration input

3. RF Front-end

The RF front-end of the receiver is a low-IF heterodyne configuration that converts the input signal into about 1 MHz IF signal with a typical image rejection of 30 dB. According to Figure Figure 1-2 on page 3 the front-end consists of an LNA (Low Noise Amplifier), LO (Local Oscillator), I/Q mixer, polyphase low-pass filter and an IF amplifier.

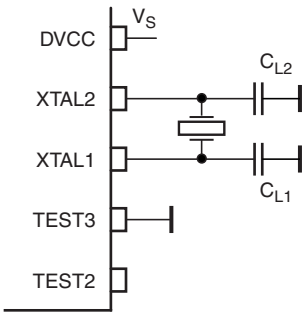
The PLL generates the drive frequency f_{LO} for the mixer using a fully integrated synthesizer with integrated low noise LC-VCO (Voltage Controlled Oscillator) and PLL-loop filter. The XTO (crystal oscillator) generates the reference frequency $f_{REF} = f_{XTO}/2$ (868 MHz and 433 MHz versions) or $f_{REF} = f_{XTO}/3$ (315 MHz version). The integrated LC-VCO generates two or four times the mixer drive frequency f_{VCO}. The I/Q signals for the mixer are generated with a divide by two or four circuit ($f_{LO} = f_{VCO}/2$ for 868 MHz version, $f_{LO} = f_{VCO}/4$ for 433 MHz and 315 MHz versions). f_{VCO} is divided by a factor of 128 or 64 and feeds into a phase frequency detector and is compared with f_{REF}. The output of the phase frequency detector is fed into an integrated loop filter and thereby generates the control voltage for the VCO. If f_{LO} is determined, f_{XTO} can be calculated using the following formula:

$f_{REF} = f_{LO}/128$ for 868 MHz band, $f_{REF} = f_{LO}/64$ for 433 MHz bands, $f_{REF} = f_{LO}/64$ for 315 MHz bands.

The XTO is a two-pin oscillator that operates at the series resonance of the quartz crystal with high current but low voltage signal, so that there is only a small voltage at the crystal oscillator frequency at pins XTAL1 and XTAL2. According to Figure 3-1, the crystal should be connected to GND with two capacitors C_{L1} and C_{L2} from XTAL1 and XTAL2 respectively. The value of these capacitors are recommended by the crystal supplier. Due to an inductive impedance at steady state oscillation and some PCB parasitics, a lower value of C_{L1} and C_{L2} is normally necessary.

The value of C_{Lx} should be optimized for the individual board layout to achieve the exact value of f_{XTO} and hence of f_{LO}. (The best way is to use a crystal with known load resonance frequency to find the right value for this capacitor.) When designing the system in terms of receiving bandwidth and local oscillator accuracy, the accuracy of the crystal and the XTO must be considered.

Figure 3-1. XTO Peripherals



The nominal frequency f_{LO} is determined by the RF input frequency f_{RF} and the IF frequency f_{IF} using the following formula (low-side injection):

$f_{LO} = f_{RF} - f_{IF}$

To determine f_{LO}, the construction of the IF filter must be considered. The nominal IF frequency is f_{IF} = 950 kHz. To achieve a good accuracy of the filter corner frequencies, the filter is tuned by the crystal frequency f_{XTO}. This means that there is a fixed relationship between f_{IF} and f_{LO}.

$f_{IF} = f_{LO}/318$ for the 315 MHz band (ATA5723)
$f_{IF} = f_{LO}/438$ for the 433.92 MHz band (ATA5724)
$f_{IF} = f_{LO}/915$ for the 868.3 MHz band (ATA5728)

The relationship is designed to achieve the nominal IF frequency of:

f_{IF} = 987 kHz for the 315 MHz and B_{IF} = 300 kHz (ATA5723)
f_{IF} = 987 kHz for the 433.92 MHz and B_{IF} = 300 kHz (ATA5724)
f_{IF} = 947.8 kHz for the 868.3 MHz and B_{IF} = 600 kHz (ATA5728)

The RF input either from an antenna or from an RF generator must be transformed to the RF input pin LNA_IN. The input impedance of this pin is provided in the electrical parameters. The parasitic board inductances and capacitances influence the input matching. The RF receiver ATA5723/ATA5724/ATA5728 exhibits its highest sensitivity if the LNA is power matched. Because of this, matching to a SAW filter, a 50Ω or an antenna is easier.

Figure 14-1 on page 32 “Application Circuit” shows a typical input matching network for f_{RF} = 315 MHz, f_{RF} = 433.92 MHz or f_{RF} = 868.3 MHz to 50Ω. The input matching network shown in Table 14-2 on page 32 is the reference network for the parameters given in the electrical characteristics.

4. Analog Signal Processing

4.1 IF Filter

The signals coming from the RF front-end are filtered by the fully integrated 4th-order IF filter. The IF center frequency is:

f_{IF} = 987 kHz for the 315 MHz and B_{IF} = 300 kHz (ATA5723)
f_{IF} = 987 kHz for the 433.92 MHz and B_{IF} = 300 kHz (ATA5724)
f_{IF} = 947.9 kHz for the 868.3 MHz and B_{IF} = 600 kHz (ATA5728)

The nominal bandwidth is 300 kHz for ATA5723 and ATA5724 and 600 kHz for ATA5728.

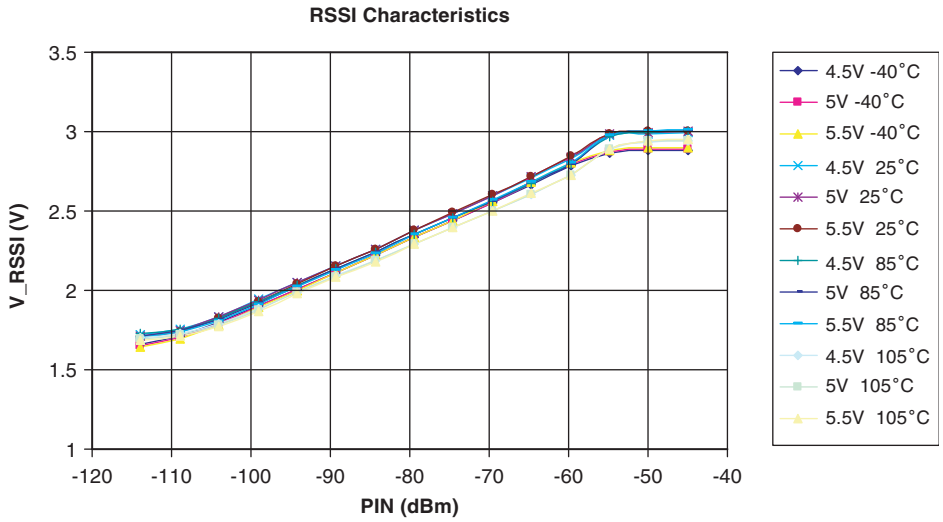
4.2 Limiting RSSI Amplifier

The subsequent RSSI amplifier enhances the output signal of the IF amplifier before it is fed into the demodulator. The dynamic range of this amplifier is ΔR_{RSSI} = 60 dB. If the RSSI amplifier is operated within its linear range, the best S/N ratio is maintained in ASK mode. If the dynamic range is exceeded by the transmitter signal, the S/N ratio is defined by the ratio of the maximum RSSI output voltage and the RSSI output voltage due to a disturber. The dynamic range of the RSSI amplifier is exceeded if the RF input signal is approximately 60 dB higher compared to the RF input signal at full sensitivity.

The S/N ratio is not affected by the dynamic range of the RSSI amplifier in FSK mode because only the hard limited signal from a high-gain limiting amplifier is used by the demodulator.

The output voltage of the RSSI amplifier (VRSSI) is available at pin RSSI. Using the RSSI output signal, the signal strength of different transmitters can be distinguished. The usable input power range P_{Ref} is –100 dBm to –55 dBm.

Figure 4-1. RSSI Characteristics ATA5724



The output voltage of the RSSI amplifier is internally compared to a threshold voltage V_{Th_red}. V_{Th_red} is determined by the value of the external resistor R_{Sens}. R_{Sens} is connected between pin SENS and GND or V_S. The output of the comparator is fed into the digital control logic. By this means, it is possible to operate the receiver at a lower sensitivity.

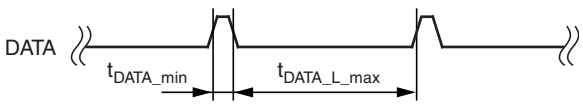
If R_{Sens} is connected to GND, the receiver switches to full sensitivity. It is also possible to connect the pin SENS directly to GND to get the maximum sensitivity.

If R_{Sens} is connected to V_S, the receiver operates at a lower sensitivity. The reduced sensitivity is defined by the value of R_{Sens}, and the maximum sensitivity is defined by the signal-to-noise ratio of the LNA input. The reduced sensitivity depends on the signal strength at the output of the RSSI amplifier.

Since different RF input networks may exhibit slightly different values for the LNA gain, the sensitivity values given in the electrical characteristics refer to a specific input matching. This matching is described and illustrated in Section 14. “Data Interface” on page 32.

R_{Sens} can be connected to V_S or GND using a microcontroller. The receiver can be switched from full sensitivity to reduced sensitivity or vice versa at any time. In polling mode, the receiver does not wake up if the RF input signal does not exceed the selected sensitivity. If the receiver is already active, the data stream at pin DATA disappears when the input signal is lower than defined by the reduced sensitivity. Instead of the data stream, the pattern according to Figure 4-2 “Steady L State Limited DATA Output Pattern” is issued at pin DATA to indicate that the receiver is still active (see Figure 13-2 on page 30 “Data Interface”).

Figure 4-2. Steady L State Limited DATA Output Pattern



4.3 FSK/ASK Demodulator and Data Filter

The signal coming from the RSSI amplifier is converted into the raw data signal by the ASK/FSK demodulator. The operating mode of the demodulator is set using the bit ASK/_FSK in the OPMODE register. Logic L sets the demodulator to FSK, applying H to ASK mode.

In ASK mode an automatic threshold control circuit (ATC) is employed to set the detection reference voltage to a value where a good signal to noise ratio is achieved. This circuit also implements the effective suppression of any kind of in-band noise signals or competing transmitters. If the S/N (ratio to suppress in-band noise signals) exceeds about 10 dB the data signal can be detected properly. However, better values are found for many modulation schemes of the competing transmitter.

The FSK demodulator is intended to be used for an FSK deviation of 10 kHz ≤Δf ≤100 kHz. The data signal in FSK mode can be detected if the S/N (ratio to suppress in-band noise signals) exceeds about 2 dB. This value is valid for all modulation schemes of a disturber signal.

The output signal of the demodulator is filtered by the data filter before it is fed into the digital signal processing circuit. The data filter improves the S/N ratio as its pass-band can be adopted to the characteristics of the data signal. The data filter consists of a 1st order high-pass and a 2nd order low-pass filter.

The high-pass filter cut-off frequency is defined by an external capacitor connected to pin CDEM. The cut-off frequency of the high-pass filter is defined by the following formula:

$$fcu\_DF = \frac{1}{2 \times \pi \times 30\ k\Omega \times CDEM}$$

In self-polling mode the data filter must settle very rapidly to achieve a low current consumption. Therefore, CDEM cannot be increased to very high values if self-polling is used. On the other hand, CDEM must be large enough to meet the data filter requirements according to the data signal. Recommended values for CDEM are given in the electrical characteristics.

The cut-off frequency of the low-pass filter is defined by the selected baud-rate range (BR_Range). The BR_Range is defined in the OPMODE register (refer to Section 11. “Configuring the Receiver” on page 25). The BR_Range must be set in accordance to the baud-rate used.

The ATA5723/ATA5724/ATA5728 is designed to operate with data coding where the DC level of the data signal is 50%. This is valid for Manchester and Bi-phase coding. If other modulation schemes are used, the DC level should always remain within the range of V_{DC_min} = 33% and V_{DC_max} = 66%. The sensitivity may be reduced by up to 2 dB in that condition.

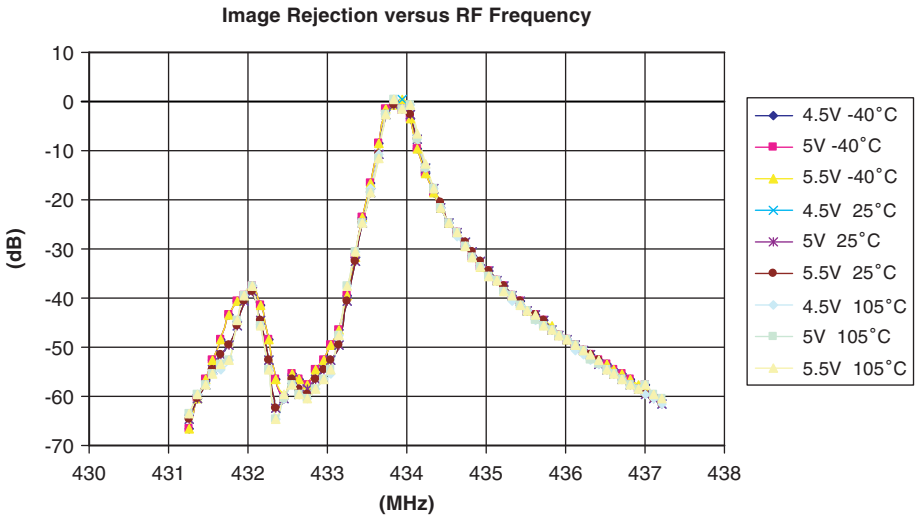
Each BR_Range is also defined by a minimum and a maximum edge-to-edge time (t_{ee_sig}). These limits are defined in the electrical characteristics. They should not be exceeded to maintain full sensitivity of the receiver.

5. Receiving Characteristics

The RF receiver ATA5723/ATA5724/ATA5728 can be operated with and without a SAW front-end filter. In a typical automotive application, a SAW filter is used to achieve better selectivity and large signal capability. The receiving frequency response without a SAW front-end filter is illustrated in Figure 5-1 “Narrow Band Receiving Frequency Response ATA5724”. This example relates to ASK mode. FSK mode exhibits a similar behavior. The plots are printed relatively to the maximum sensitivity. If a SAW filter is used, an insertion loss of about 3 dB must be considered, but the overall selectivity is much better.

When designing the system in terms of receiving bandwidth, the LO deviation must be considered as it also determines the IF center frequency. The total LO deviation is calculated, to be the sum of the deviation of the crystal and the XTO deviation of the ATA5723/ATA5724/ATA5728. Low-cost crystals are specified to be within ±90 ppm over tolerance, temperature, and aging. The XTO deviation of the ATA5723/ATA5724/ATA5728 is an additional deviation due to the XTO circuit. This deviation is specified to be ±10 ppm worst case for a crystal with CM = 7 fF. If a crystal of ±90 ppm is used, the total deviation is ±100 ppm in that case. Note that the receiving bandwidth and the IF-filter bandwidth are equivalent in ASK mode but not in FSK mode.

Figure 5-1. Narrow Band Receiving Frequency Response ATA5724



6. Polling Circuit and Control Logic

The receiver is designed to consume less than 1 mA while being sensitive to signals from a corresponding transmitter. This is achieved using the polling circuit. This circuit enables the signal path periodically for a short time. During this time the bit-check logic verifies the presence of a valid transmitter signal. Only if a valid signal is detected, the receiver remains active and transfers the data to the connected microcontroller. If there is no valid signal present, the receiver is in sleep mode most of the time resulting in low current consumption. This condition is called polling mode. A connected microcontroller is disabled during that time.

All relevant parameters of the polling logic can be configured by the connected microcontroller. This flexibility enables the user to meet the specifications in terms of current consumption, system response time, data rate etc.

The receiver is very flexible with regards to the number of connection wires to the microcontroller. It can be either operated by a single bi-directional line to save ports to the connected microcontroller or it can be operated by up to five uni-directional ports.

7. Basic Clock Cycle of the Digital Circuitry

The complete timing of the digital circuitry and the analog filtering is derived from one clock. This clock cycle T_{Clk} is derived from the crystal oscillator (XTO) in combination with a divide by 28 or 30 circuit. According to Section 3. “RF Front-end” on page 5, the frequency of the crystal oscillator (f_{XTO}) is defined by the RF input signal (f_{RFin}) which also defines the operating frequency of the local oscillator (f_{LO}). The basic clock cycle for ATA5724 and ATA5728 is T_{Clk} 28/f_{XTO} giving T_{Clk} = 2.066 µs for f_{RF} = 868.3 MHz and T_{Clk} = 2.069 µs for f_{RF} = 433.92 MHz. For ATA5723 the basic clock cycle is T_{Clk} = 30/f_{REF} giving T_{Clk} = 2.0382 µs for f_{RF} = 315 MHz.

T_{Clk} controls the following application-relevant parameters:

- Timing of the polling circuit including bit check
- Timing of the analog and digital signal processing
- Timing of the register programming
- Frequency of the reset marker
- IF filter center frequency (fIF0)

Most applications are dominated by three transmission frequencies: $f_{Transmit}$ = 315 MHz is mainly used in USA, $f_{Transmit}$ = 868.3 MHz and 433.92 MHz in Europe. All timings are based on T_{Clk}. For the aforementioned frequencies, T_{Clk} is given as:

- Application 315 MHz band (f_{XTO} = 14.71875 MHz, f_{LO} = 314.13 MHz, T_{Clk} = 2.0382 µs)
- Application 868.3 MHz band (f_{XTO} = 13.55234 MHz, f_{LO} = 867.35 MHz, T_{Clk} = 2.066 µs)
- Application 433.92 MHz band (f_{XTO} = 13.52875 MHz, f_{LO} = 432.93 MHz, T_{Clk} = 2.0696 µs)

For calculation of T_{Clk} for applications using other frequency bands, see table in Section 18. “Electrical Characteristics ATA5724, ATA5728” on page 37.

The clock cycle of some function blocks depends on the selected baud-rate range (BR_Range), which is defined in the OPMODE register. This clock cycle T_{XClk} is defined by the following formulas:

BR_Range =	BR_Range0:	$T_{XClk} = 8 \times T_{Clk}$
	BR_Range1:	$T_{XClk} = 4 \times T_{Clk}$
	BR_Range2:	$T_{XClk} = 2 \times T_{Clk}$
	BR_Range3:	$T_{XClk} = 1 \times T_{Clk}$

8. Polling Mode

According to Figure 8-1 on page 12, the receiver stays in polling mode in a continuous cycle of three different modes. In sleep mode the signal processing circuitry is disabled for the time period T_{Sleep} while consuming low current of $I_S = I_{Soff}$. During the start-up period, $T_{Startup}$, all signal processing circuits are enabled and settled. In the following bit-check mode, the incoming data stream is analyzed bit-by-bit and compared with a valid transmitter signal. If no valid signal is present, the receiver is set back to sleep mode after the period $T_{Bit\text{-}check}$. This period varies according to each check as it is a statistical process. An average value for $T_{Bitcheck}$ is given in the electrical characteristics. During $T_{Startup}$ and $T_{Bit\text{-}check}$, the current consumption is $I_S = I_{Son}$. The condition of the receiver is indicated on pin IC_ACTIVE. The average current consumption in polling mode is dependent on the duty cycle of the active mode and can be calculated as:

$$I_{Spoll} = \frac{I_{Soff} \times T_{Sleep} + I_{Son} \times (T_{Startup} + T_{Bit\text{-}check})}{T_{Sleep} + T_{Startup} + T_{Bit\text{-}check}}$$

During T_{Sleep} and $T_{Startup}$, the receiver is not sensitive to a transmitter signal. To guarantee the reception of a transmitted command, the transmitter must start the telegram with an adequate preburst. The required length of the preburst depends on the polling parameters T_{Sleep}, $T_{Startup}$, $T_{Bit\text{-}check}$ and the start-up time of a connected microcontroller, $T_{Start\_microcontroller}$. Thus, $T_{Bit\text{-}check}$ depends on the actual bit rate and the number of bits ($N_{Bit\text{-}check}$) to be tested.

The following formula indicates how to calculate the preburst length.

$$T_{Preburst} \geq T_{Sleep} + T_{Startup} + T_{Bit\text{-}check} + T_{Start\_microcontroller}$$

8.1 Sleep Mode

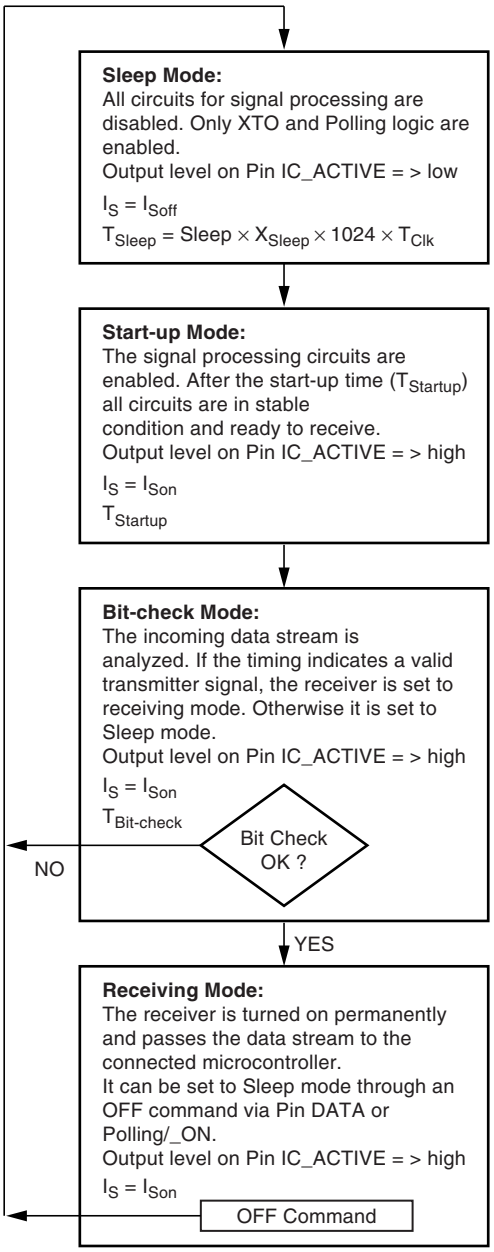
The length of period T_{Sleep} is defined by the 5-bit word Sleep of the OPMODE register, the extension factor X_{Sleep} (according to Table 11-8 on page 27), and the basic clock cycle T_{Clk}. It is calculated to be:

$$T_{Sleep} = Sleep \times X_{Sleep} \times 1024 \times T_{Clk}$$

The maximum value of T_{Sleep} is about 60 ms if X_{Sleep} is set to 1. The time resolution is about 2 ms in that case. The sleep time can be extended to almost half a second by setting X_{Sleep} to 8. X_{Sleep} can be set to 8 by bit $X_{SleepStd}$ to “1”.

Setting the configuration word Sleep to its maximal value puts the receiver into a permanent sleep mode. The receiver remains in this state until another value for Sleep is programmed into the OPMODE register. This is particularly useful when several devices share a single data line. (It can also be used for microcontroller polling: using pin POLLING/_ON, the receiver can be switched on and off.)

Figure 8-1. Polling Mode Flow Chart



Sleep: 5-bit word defined by Sleep 0 to Sleep 4 in OPMODE register

X_{Sleep}: Extension factor defined by XSleepStd according to Table 11-8

T_{Clk}: Basic clock cycle defined by f_{XTO} and Pin MODE

$T_{Startup}$: Is defined by the selected baud rate range and TClk. The baud-rate range is defined by Baud 0 and Baud 1 in the OPMODE register.

$T_{Bit\text{-}check}$: Depends on the result of the bit check

If the bit check is ok, $T_{Bit\text{-}check}$ depends on the number of bits to be checked ($N_{Bit\text{-}check}$) and on the data rate used.

If the bit check fails, the average time period for that check depends on the selected baud-rate range and on T_{Clk}. The baud-rate range is defined by Baud 0 and Baud 1 in the OPMODE register.

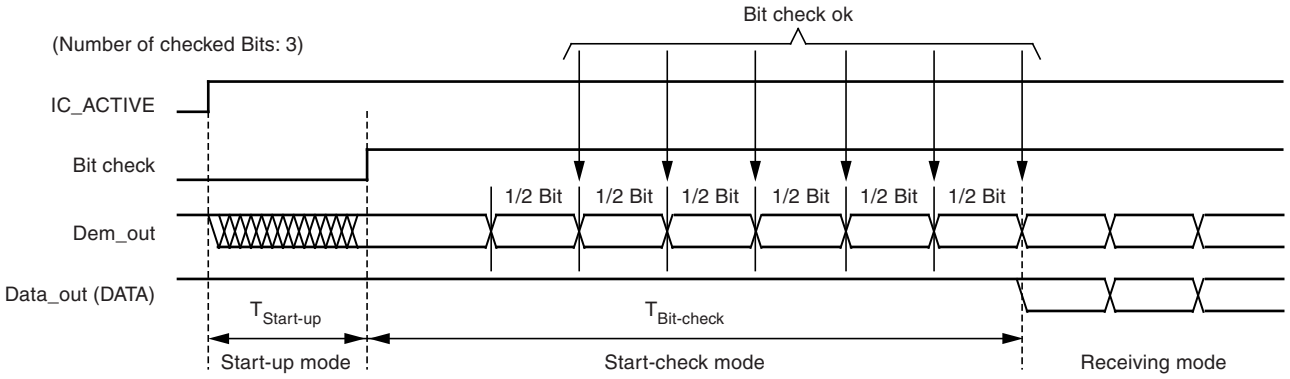
8.2 Bit-check Mode

In bit-check mode the incoming data stream is examined to distinguish between a valid signal from a corresponding transmitter and signals due to noise. This is done by subsequent time frame checks where the distances between 2 signal edges are continuously compared to a programmable time window. The maximum number of these edge-to-edge tests, before the receiver switches to receiving mode, is also programmable.

8.3 Configuring the Bit Check

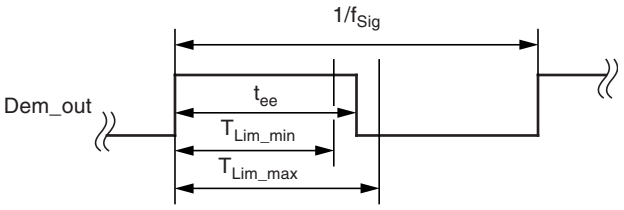
Assuming a modulation scheme that contains two edges per bit, two time frame checks verify one bit. This is valid for Manchester, Bi-phase, and most other modulation schemes. The maximum count of bits to be checked can be set to 0, 3, 6, or 9 bits using the variable $N_{Bit\text{-}check}$ in the OPMODE register. This implies 0, 6, 12, and 18 edge-to-edge checks respectively. If $N_{Bit\text{-}check}$ is set to a higher value, the receiver is less likely to switch to receiving mode due to noise. In the presence of a valid transmitter signal, the bit check takes less time if $N_{Bit\text{-}check}$ is set to a lower value. In polling mode, the bit-check time is not dependent on NBit-check. Figure 8-2 shows an example where three bits are tested successfully and the data signal is transferred to pin DATA.

Figure 8-2. Timing Diagram for Complete Successful Bit Check



According to Figure 8-3, the time window for the bit check is defined by two separate time limits. If the edge-to-edge time t_{ee} is in between the lower bit-check limit T_{Lim_min} and the upper bit-check limit T_{Lim_max}, the check continues. If t_{ee} is smaller than T_{Lim_min} or t_{ee} exceeds T_{Lim_max}, the bit check is terminated and the receiver switches to sleep mode.

Figure 8-3. Valid Time Window for Bit Check



For best noise immunity using a low span between T_{Lim_min} and T_{Lim_max} is recommended. This is achieved using a fixed frequency at a 50% duty cycle for the transmitter preburst. A “11111...” or a “10101...” sequence in Manchester or Bi-phase is suitable for this. A good compromise between receiver sensitivity and susceptibility to noise is a time window of ±30% regarding the expected edge-to-edge time t_{ee}. Using pre-burst patterns that contain various edge-to-edge time periods, the bit-check limits must be programmed according to the required span.

The bit-check limits are determined by means of the formula below.

$$T_{Lim\_min} = Lim\_min \times T_{XClk}$$
$$T_{Lim\_max} = (Lim\_max - 1) \times T_{XClk}$$

Lim_min and Lim_max are defined by a 5-bit word each within the LIMIT register.

Using above formulas, Lim_min and Lim_max can be determined according to the required T_{Lim_min}, T_{Lim_max} and T_{XClk}. The time resolution defining T_{Lim_min} and T_{Lim_max} is T_{XClk}. The minimum edge-to-edge time t_{ee} ($t_{DATA\_L\_min}$, $t_{DATA\_H\_min}$) is defined according to the Section 8.6 “Digital Signal Processing” on page 16. The lower limit should be set to Lim_min ≥ 10. The maximum value of the upper limit is Lim_max = 63.

If the calculated value for Lim_min is < 19, it is recommended to check 6 or 9 bits ($N_{Bit\text{-}check}$) to prevent switching to receiving mode due to noise.

Figure 8-4, Figure 8-5, and Figure 8-6 illustrate the bit check for the bit-check limits Lim_min = 14 and Lim_max = 24. When the IC is enabled, the signal processing circuits are enabled during $T_{Startup}$. The output of the ASK/FSK demodulator (Dem_out) is undefined during that period. When the bit check becomes active, the bit-check counter is clocked with the cycle T_{XClk}.

Figure 8-4 shows how the bit check proceeds if the bit-check counter value CV_Lim is within the limits defined by Lim_min and Lim_max at the occurrence of a signal edge. In Figure 8-5 the bit check fails as the value CV_Lim is lower than the limit Lim_min. The bit check also fails if CV_Lim reaches Lim_max. This is illustrated in Figure 8-6.

Figure 8-4. Timing Diagram During Bit Check

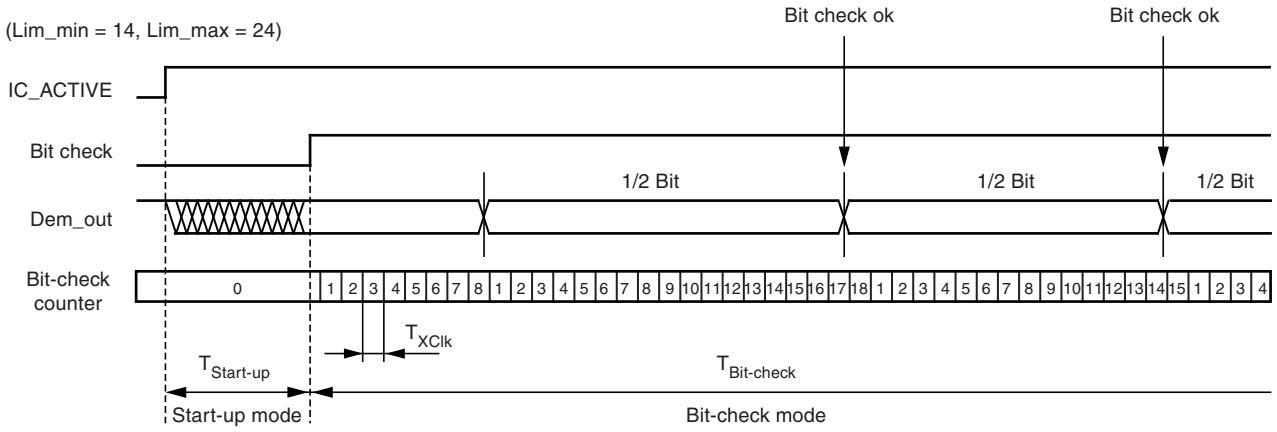


Figure 8-5. Timing Diagram for Failed Bit Check (Condition: CV_Lim < Lim_min)

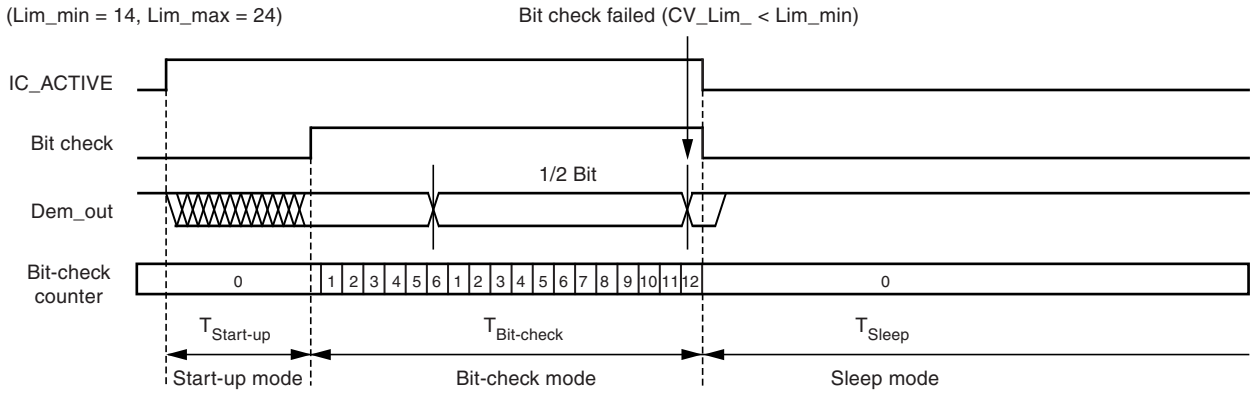
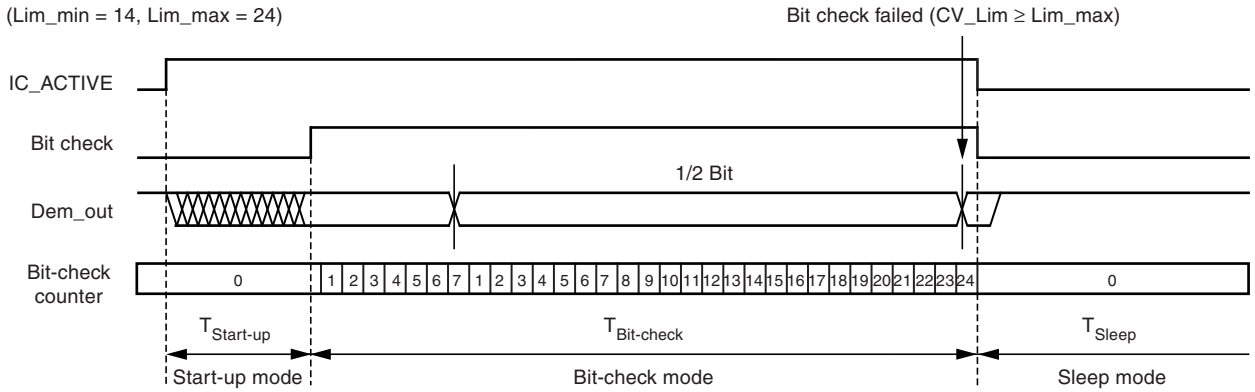


Figure 8-6. Timing Diagram for Failed Bit Check (Condition: CV_Lim ≥ Lim_max)



8.4 Duration of the Bit Check

If no transmitter signal is present during the bit check, the output of the ASK/FSK demodulator delivers random signals. The bit check is a statistical process and $T_{Bit\text{-}check}$ varies for each check. Therefore, an average value for $T_{Bit\text{-}check}$ is given in the electrical characteristics. $T_{Bit\text{-}check}$ depends on the selected baud-rate range and on T_{Clk}. A higher baud-rate range causes a lower value for $T_{Bit\text{-}check}$ resulting in a lower current consumption in polling mode.

In the presence of a valid transmitter signal, $T_{Bit\text{-}check}$ is dependent on the frequency of that signal, f_{Sig}, and the count of the checked bits, $N_{Bit\text{-}check}$. A higher value for $N_{Bit\text{-}check}$ thereby results in a longer period for $T_{Bit\text{-}check}$ requiring a higher value for the transmitter pre-burst $T_{Preburst}$.

8.5 Receiving Mode

If the bit check was successful for all bits specified by $N_{Bit\text{-}check}$, the receiver switches to receiving mode. According to Figure 8-2 on page 13, the internal data signal is switched to pin DATA in that case, and the data clock is available after the start bit has been detected (see Figure 9-1 on page 20). A connected microcontroller can be woken up by the negative edge at pin DATA or by the data clock at pin DATA_CLK. The receiver stays in that condition until it is switched back to polling mode explicitly.

8.6 Digital Signal Processing

The data from the ASK/FSK demodulator (Dem_out) is digitally processed in different ways and as a result converted into the output signal data. This processing depends on the selected baud-rate range (BR_Range). Figure 8-7 illustrates how Dem_out is synchronized by the extended clock cycle T_{XClk}. This clock is also used for the bit-check counter. Data can change its state only after T_{XClk} has elapsed. The edge-to-edge time period t_{ee} of the Data signal as a result is always an integral multiple of T_{XClk}.

The minimum time period between two edges of the data signal is limited to $t_{ee} \geq T_{DATA\_min}$. This implies an efficient suppression of spikes at the DATA output. At the same time it limits the maximum frequency of edges at DATA. This eases the interrupt handling of a connected microcontroller.

The maximum time period for DATA to stay low is limited to $T_{DATA\_L\_max}$. This function is employed to ensure a finite response time in programming or switching off the receiver via pin DATA. $T_{DATA\_L\_max}$ is therefore longer than the maximum time period indicated by the transmitter data stream. Figure 8-9 on page 17 gives an example where Dem_out remains Low after the receiver has switched to receiving mode.

Figure 8-7. Synchronization of the Demodulator Output

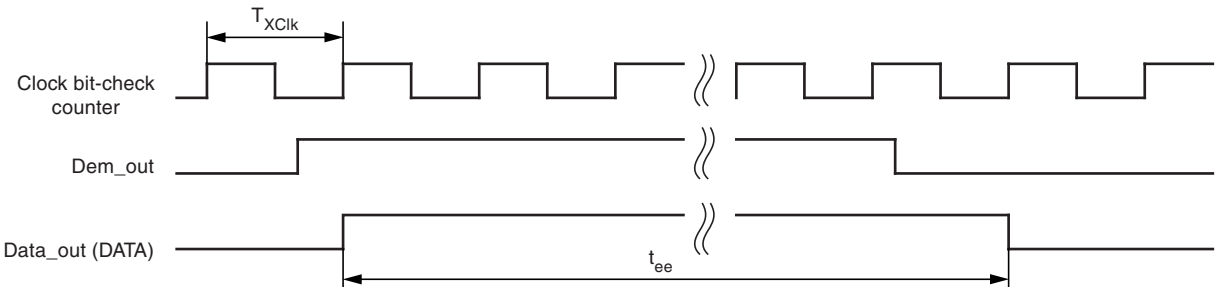


Figure 8-8. Debouncing of the Demodulator Output

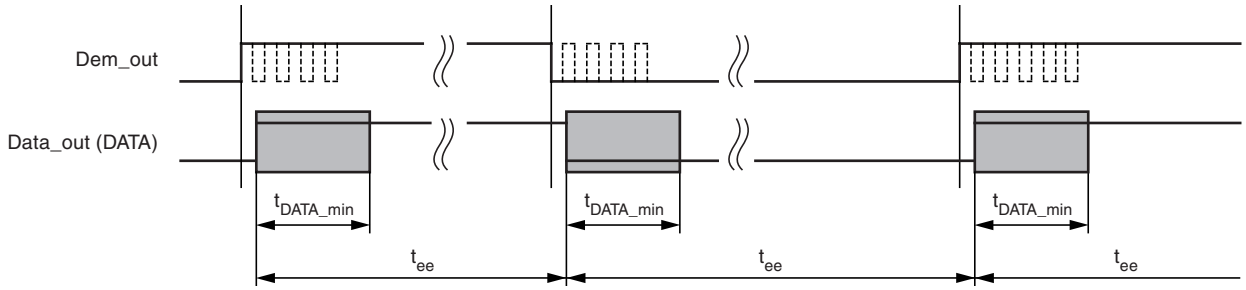
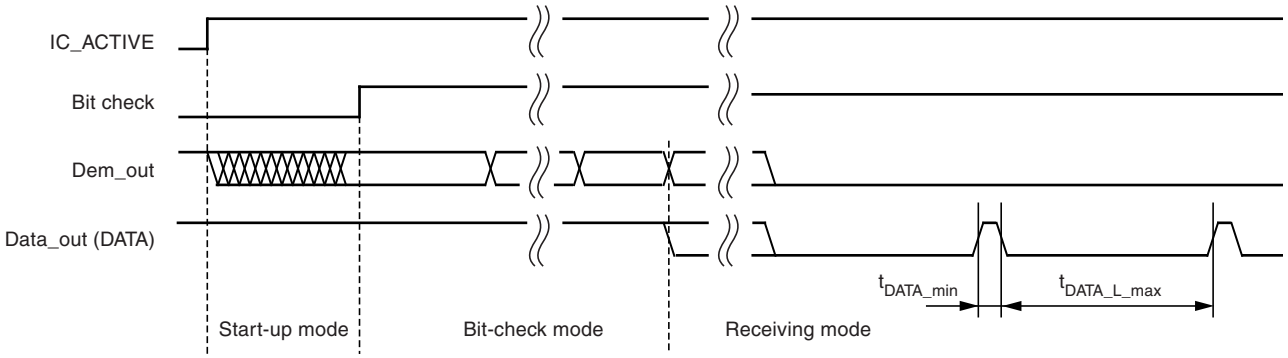


Figure 8-9. Steady L State Limited DATA Output Pattern After Transmission



After the end of a data transmission, the receiver remains active. Depending of the bit Noise_Disable in the OPMODE register, the output signal at pin DATA is high or random noise pulses appear at pin DATA (see Section 10. “Digital Noise Suppression” on page 23). The edge-to-edge time period t_{ee} of the majority of these noise pulses is equal or slightly higher than T_{DATA_min}.

8.7 Switching the Receiver Back to Sleep Mode

The receiver can be set back to polling mode via pin DATA or via pin POLLING/_ON.

When using pin DATA, this pin must be pulled to low by the connected microcontroller for the period t1. Figure 8-10 on page 18 illustrates the timing of the OFF command (see Figure 13-2 on page 30). The minimum value of t1 depends on the BR_Range. The maximum value for t1 is not limited; however, exceeding the specified value to prevent erasing the reset marker is not recommended. Note also that an internal reset for the OPMODE and the LIMIT register is generated if t1 exceeds the specified values. This item is explained in more detail in the Section 11. “Configuring the Receiver” on page 25. Setting the receiver to sleep mode via DATA is achieved by programming bit 1 to “1” during the register configuration. Only one sync pulse (t3) is issued.

The duration of the OFF command is determined by the sum of t1, t2, and t10. The sleep time T_{Sleep} elapses after the OFF command. Note that the capacitive load at pin DATA is limited (see Section 14. “Data Interface” on page 32).

Figure 8-10. Timing Diagram of the OFF Command using Pin DATA

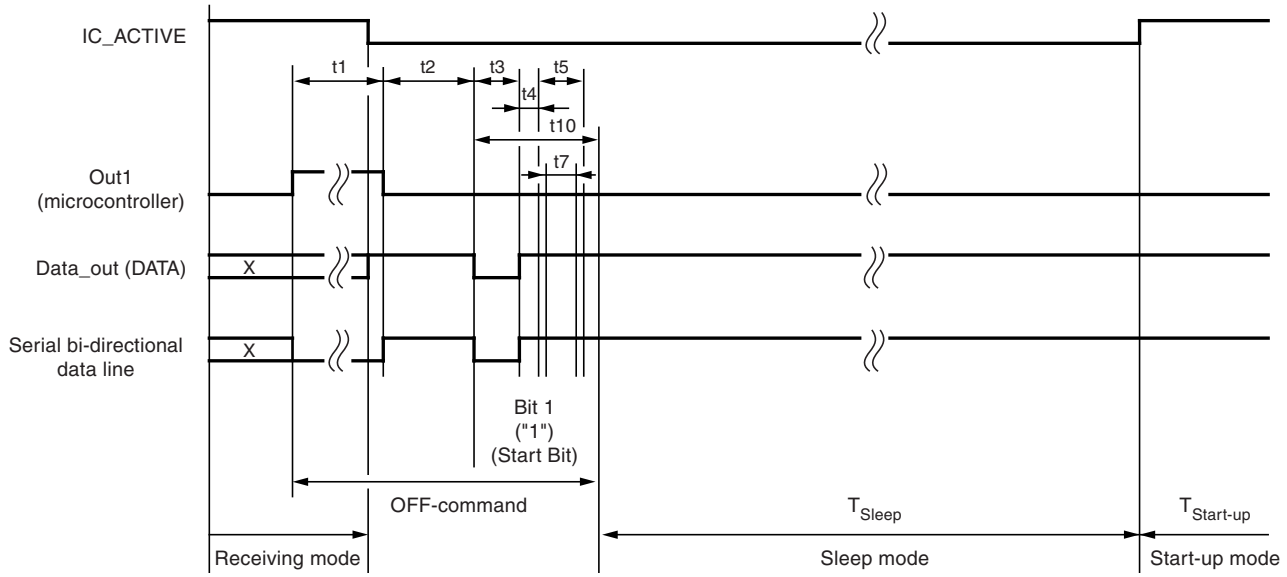


Figure 8-11. Timing Diagram of the OFF Command using Pin POLLING/_ON

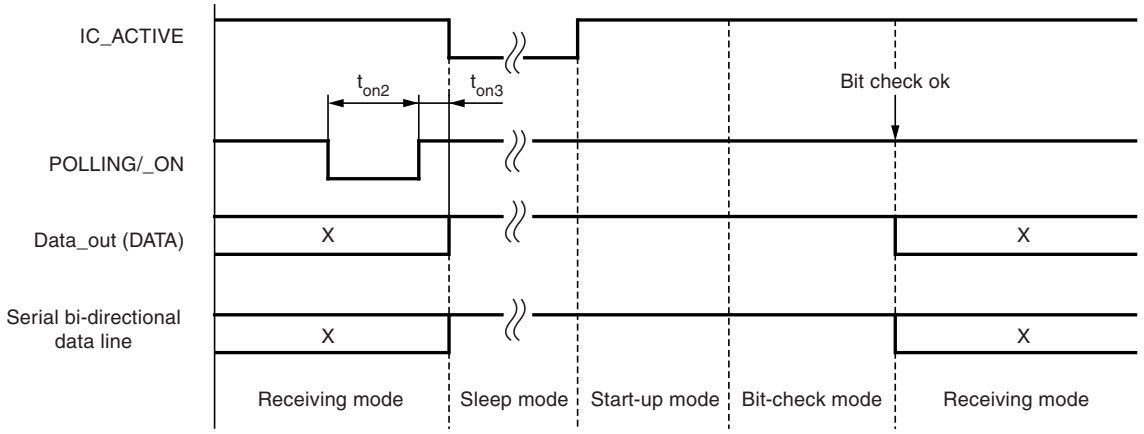


Figure 8-12. Activating the Receiving Mode using Pin POLLING/_ON

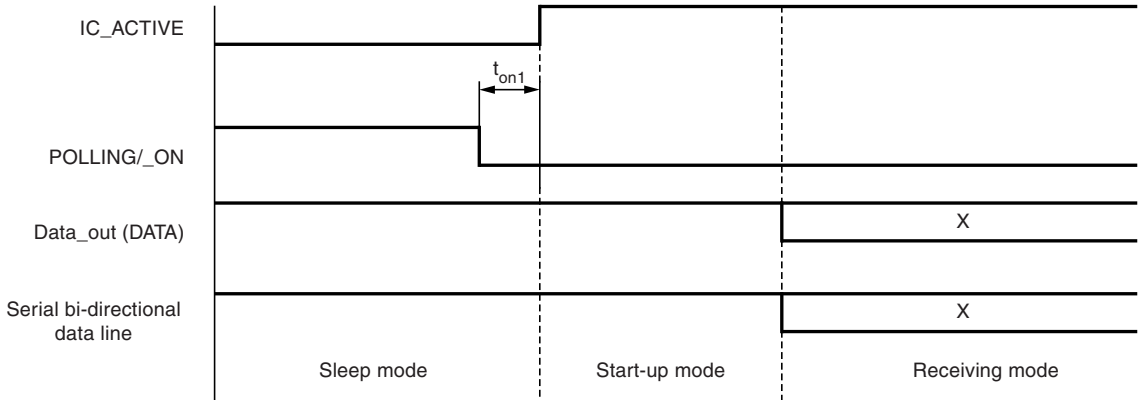


Figure 8-11 “Timing Diagram of the OFF Command using Pin POLLING/_ON” illustrates how to set the receiver back to polling mode using pin POLLING/_ON. The pin POLLING/_ON must be held to low for the time period t_{on2}. After the positive edge on pin POLLING/_ON and the delay t_{on3}, the polling mode is active and the sleep time T_{Sleep} elapses.

Using the POLLING/_ON command is faster than using pin DATA; however, this requires the use of an additional connection to the microcontroller.

Figure 8-12 “Activating the Receiving Mode using Pin “POLLING/_ON” illustrates how to set the receiver to receiving mode using the pin POLLING/_ON. The pin POLLING/_ON must be held to low. After the delay t_{on1}, the receiver changes from sleep mode to start-up mode regardless of the programmed values for T_{Sleep} and $N_{Bit\text{-}check}$. As long as POLLING/_ON is held to low, the values for T_{Sleep} and $N_{Bit\text{-}check}$ is ignored, but not deleted (see Section 10. “Digital Noise Suppression” on page 23).

If the receiver is polled exclusively by a microcontroller, T_{Sleep} must be programmed to 31 (permanent sleep mode). In this case the receiver remains in sleep mode as long as POLLING/_ON is held to high.

9. Data Clock

The pin DATA_CLK makes a data shift clock available to sample the data stream into a shift register. Using this data clock, a microcontroller can easily synchronize the data stream. This clock can only be used for Manchester and Bi-phase coded signals.

9.1 Generation of the Data Clock

After a successful bit check, the receiver switches from polling mode to receiving mode and the data stream is available at pin DATA. In receiving mode, the data clock control logic (Manchester/Bi-phase demodulator) is active and examines the incoming data stream. This is done, as with the bit check, by subsequent time frame checks where the distance between two edges is continuously compared to a programmable time window. As illustrated in Figure 9-1 on page 20, only two distances between two edges in Manchester and Bi-phase coded signals are valid (T and 2T).

The limits for T are the same as used with the bit check. They can be programmed in the LIMIT-register (Lim_min and Lim_max, see Table 11-10 on page 28 and Table 11-11 on page 28).

The limits for 2T are calculated as follows:

Lower limit of 2T: Lim_min_2T = (Lim_min + Lim_max) – (Lim_max – Lim_min)/2

Upper limit of 2T: Lim_max_2T= (Lim_min + Lim_max) + (Lim_max – Lim_min)/2

(If the result for ’Lim_min_2T’ or ’Lim_max_2T’ is not an integer value, it is rounded up.)

The data clock is available, after the data clock control logic has detected the distance 2T (Start bit) and is issued with the delay t_{Delay} after the edge on pin DATA (see Figure 9-1 on page 20).

If the data clock control logic detects a timing or logical error (Manchester code violation), as illustrated in Figure 9-2 on page 20 and Figure 9-3 on page 21, it stops the output of the data clock. The receiver remains in receiving mode and starts with the bit check. If the bit check was successful and the start bit has been detected, the data clock control logic starts again with the generation of the data clock (see Figure 9-4 on page 21).

Use the function of the data clock only in conjunction with the bit check 3, 6 or 9 is recommended. If the bit check is set to 0 or the receiver is set to receiving mode using the pin POLLING/_ON, the data clock is available if the data clock control logic has detected the distance 2T (Start bit).

Note that for Bi-phase-coded signals, the data clock is issued at the end of the bit.

Figure 9-1. Timing Diagram of the Data Clock

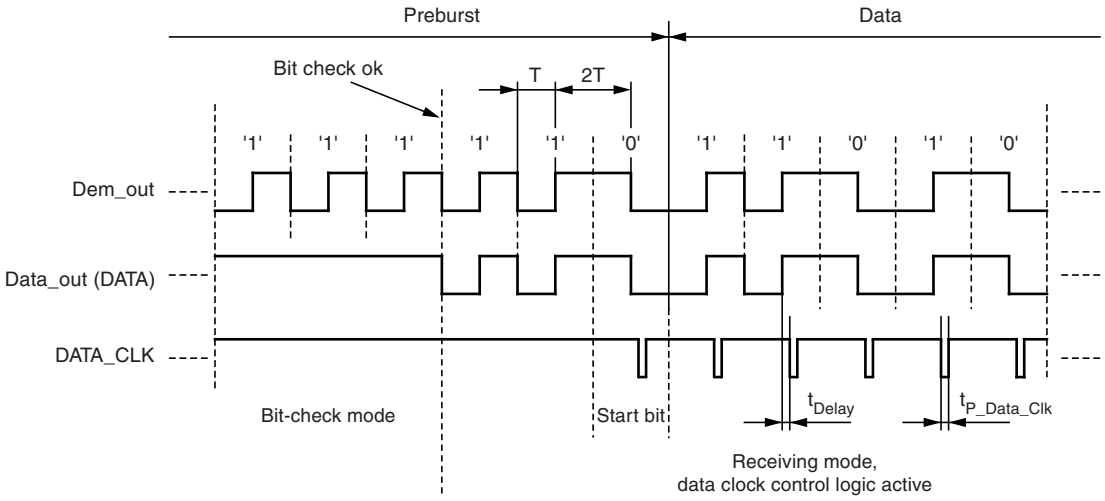


Figure 9-2. Data Clock Disappears Because of a Timing Error

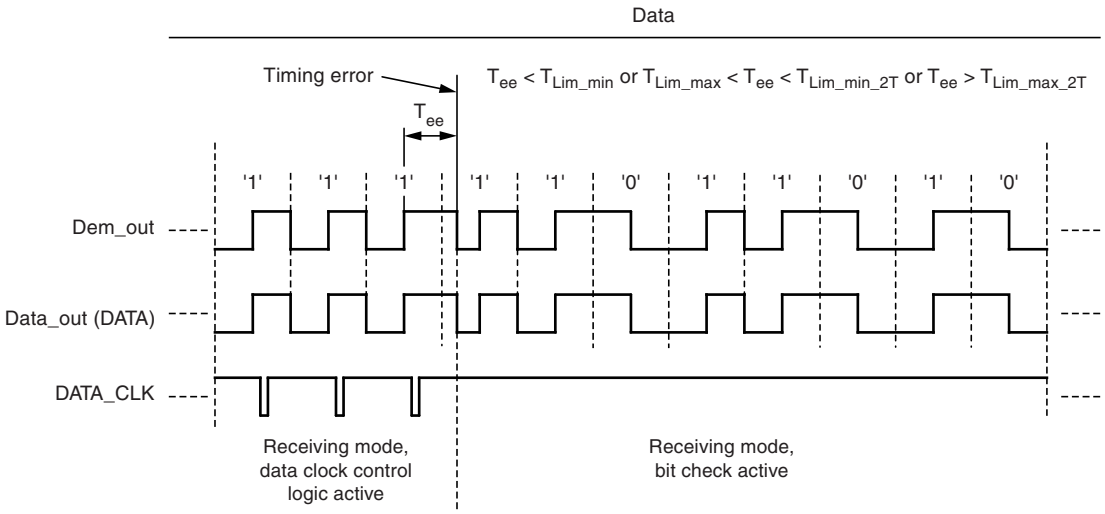


Figure 9-3. Data Clock Disappears Because of a Logical Error

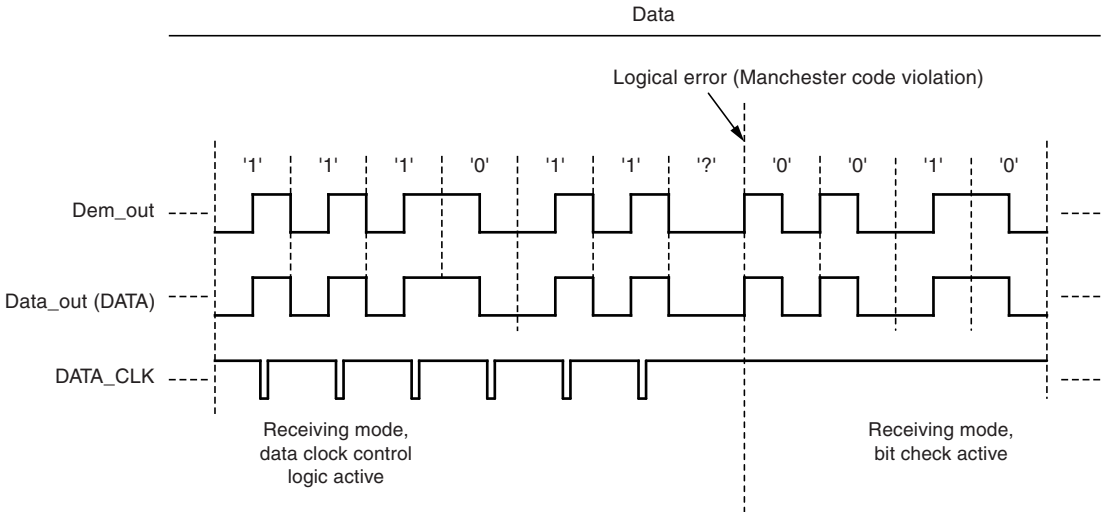
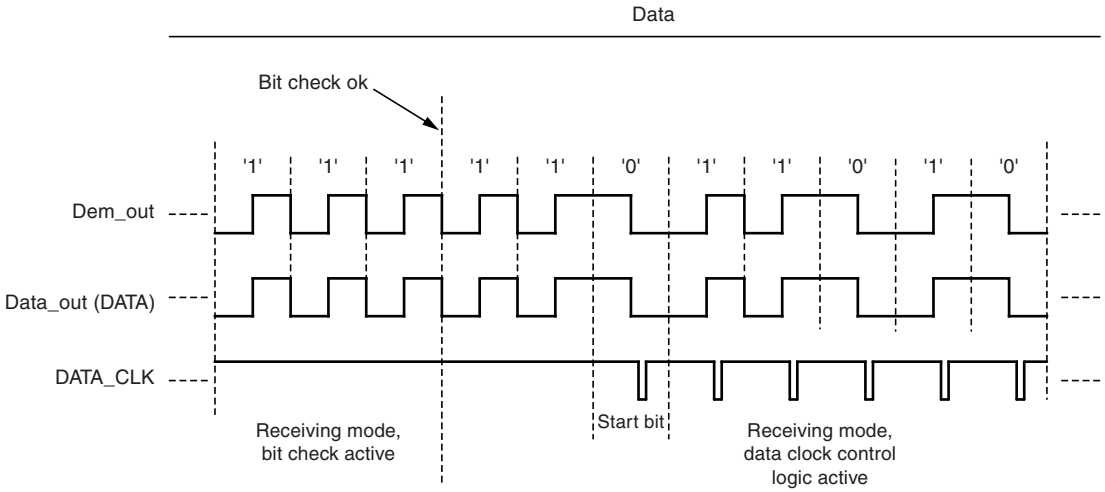


Figure 9-4. Output of the Data Clock After a Successful Bit Check



The delay of the data clock is calculated as follows: $t_{Delay} = t_{Delay1} + t_{Delay2}$

t_{Delay1} is the delay between the internal signals Data_Out and Data_In. For the rising edge, t_{Delay1} depends on the capacitive load C_L at pin DATA and the external pull-up resistor R_{pup}. For the falling edge, t_{Delay1} depends additionally on the external voltage V_X (see Figure 9-5, Figure 9-6 on page 22 and Figure 13-2 on page 30). When the level of Data_In is equal to the level of Data_Out, the data clock is issued after an additional delay t_{Delay2}.

Note that the capacitive load at pin DATA is limited. If the maximum tolerated capacitive load at pin DATA is exceeded, the data clock disappears (see Section 14. “Data Interface” on page 32).

Figure 9-5. Timing Characteristic of the Data Clock (Rising Edge on Pin DATA)

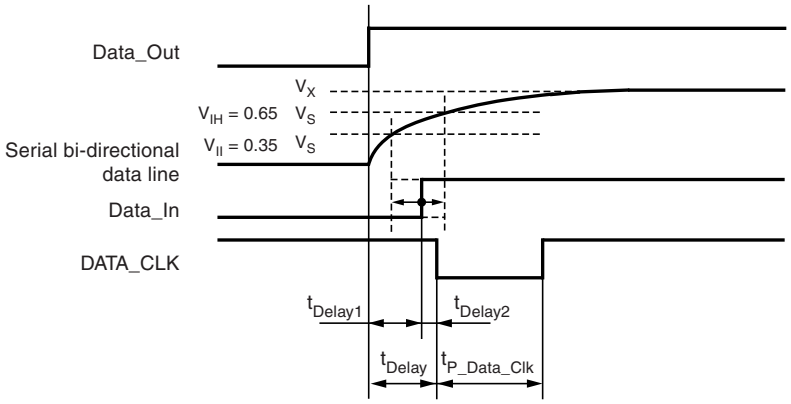
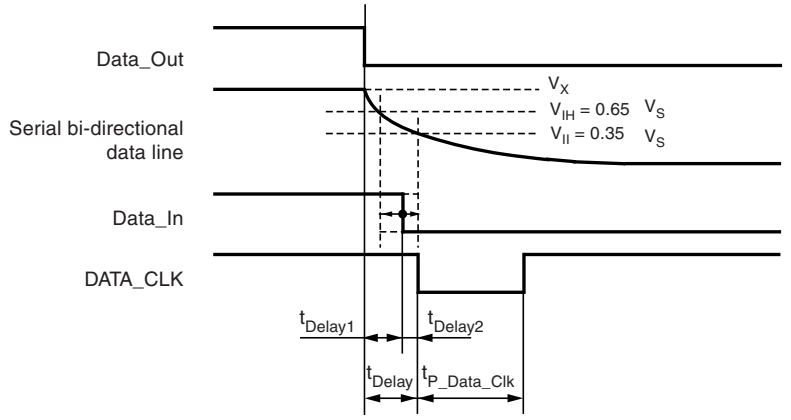


Figure 9-6. Timing Characteristic of the Data Clock (Falling Edge of the Pin DATA)



10. Digital Noise Suppression

After a data transmission, digital noise appears on the data output (see Figure 10-1 “Output of Digital Noise at the End of the Data Stream”). To prevent digital noise keeping the connected microcontroller busy, it can be suppressed in two different ways:

- Automatic Noise Suppression
- Controlled Noise Suppression by the Microcontroller

10.1 Automatic Noise Suppression

The receiver changes to bit-check mode at the end of a valid data stream if the bit Noise_Disable (Table 11-9 on page 27) in the OPMODE register is set to 1 (default). The digital noise is suppressed, and the level at pin DATA is high. The receiver changes back to receiving mode, if the bit check was successful.

This method of noise suppression is recommended if the data stream is Manchester or Bi-phase coded and is active after power on.

Figure 10-3 “Occurrence of a Pulse at the End of the Data Stream” illustrates the behavior of the data output at the end of a data stream. If the last period of the data stream is a high period (rising edge to falling edge), a pulse occurs on pin DATA. The length of the pulse depends on the selected baud-rate range.

Figure 10-1. Output of Digital Noise at the End of the Data Stream

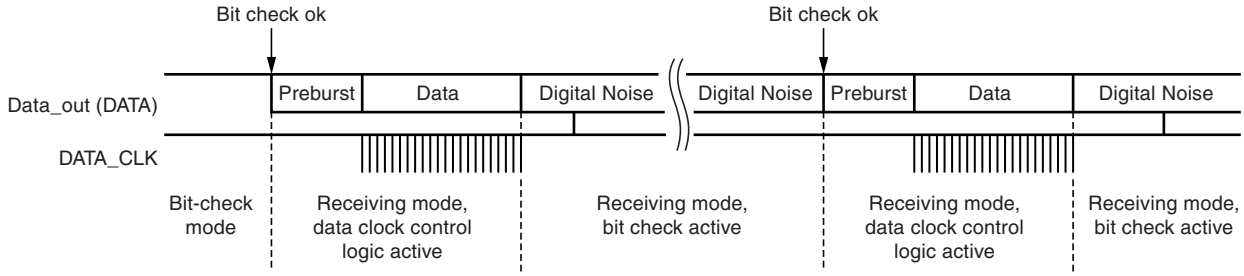


Figure 10-2. Automatic Noise Suppression

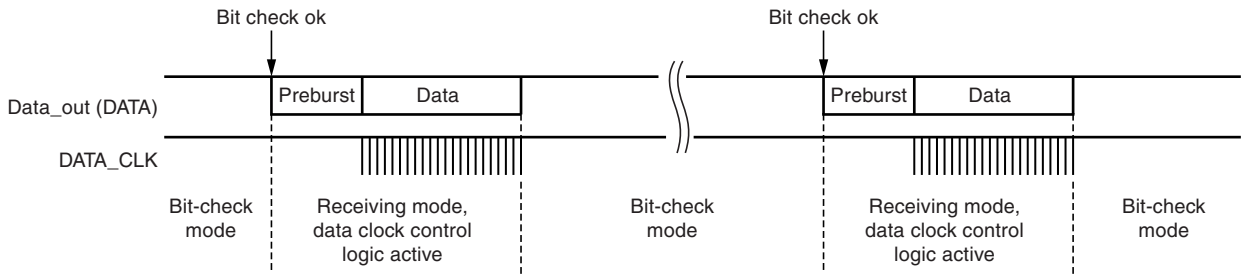
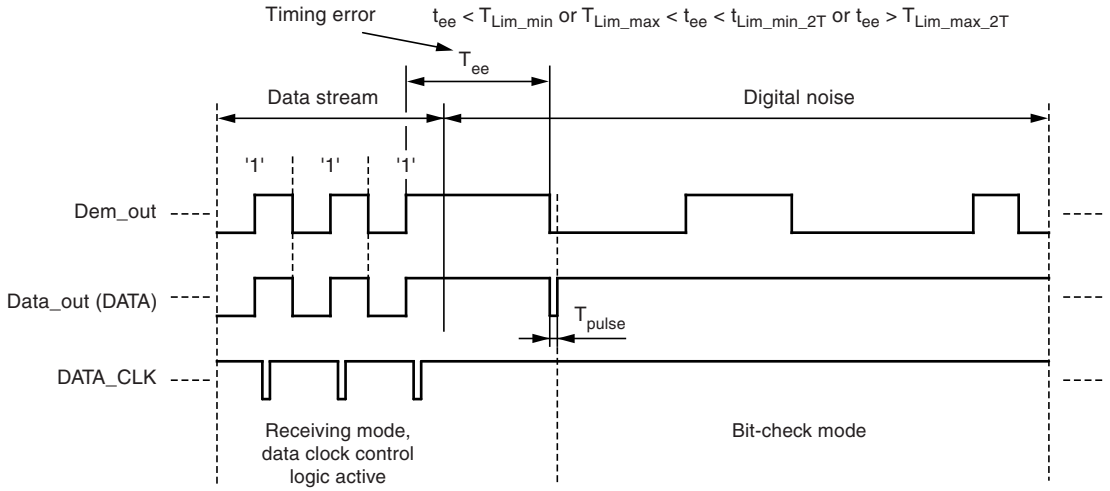


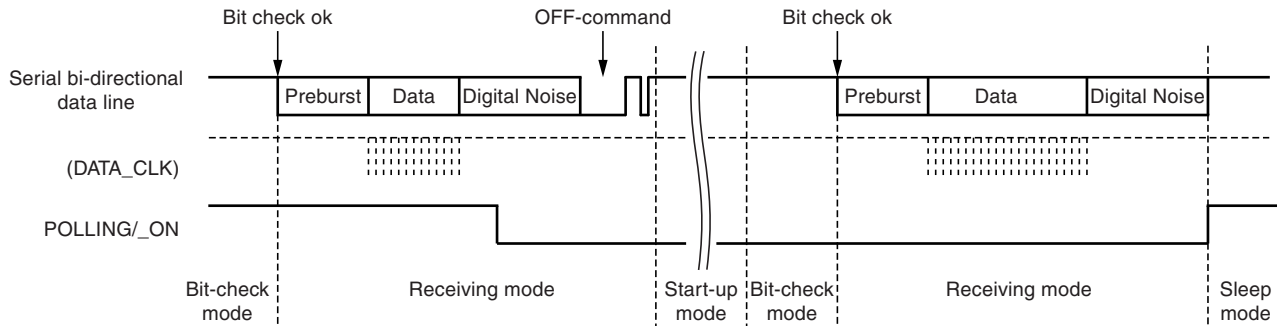
Figure 10-3. Occurrence of a Pulse at the End of the Data Stream



10.2 Controlled Noise Suppression by the Microcontroller

Digital noise appears at the end of a valid data stream if the bit Noise_Disable (see Table 11-9 on page 27) in the OPMODE register is set to 0. To suppress the noise, the pin POLLING/_ON must be set to low. The receiver remains in receiving mode. The OFF command then causes a change to start-up mode. The programmed sleep time (see Table 11-7 on page 27) is not executed because the level at pin POLLING/_ON is low; however, the bit check is active in this case. The OFF command also activates the bit check if the pin POLLING/_ON is held to low. The receiver changes back to receiving mode if the bit check was successful. To activate the polling mode at the end of the data transmission, the pin POLLING/_ON must be set to high. This way of suppressing the noise is recommended if the data stream is not Manchester or Bi-phase coded.

Figure 10-4. Controlled Noise Suppression



11. Configuring the Receiver

The ATA5723/ATA5724/ATA5728 receiver is configured using two 12-bit RAM registers called OPMODE and LIMIT. The registers can be programmed by means of the bidirectional DATA port. If the register content has changed due to a voltage drop, this condition is indicated by a the output pattern called reset marker (RM). If this occurs, the receiver must be reprogrammed. After a Power-On Reset (POR), the registers are set to default mode. If the receiver is operated in default mode, there is no need to program the registers. Table 11-3 on page 25 shows the structure of the registers. According to Table 11-1, bit 1 defines whether the receiver is set back to polling mode using the OFF command (see "Receiving Mode" on page 15) or whether it is programmed. Bit 2 represents the register address. It selects the appropriate register to be programmed. For high programming reliability, bit 15 (Stop bit), at the end of the programming operation, must be set to 0.

Table 11-1. Effect of Bit 1 and Bit 2 on Programming the Registers

Bit 1	Bit 2	Action
1	x	The receiver is set back to polling mode (OFF command)
0	1	The OPMODE register is programmed
0	0	The LIMIT register is programmed

Table 11-2. Effect of Bit 15 on Programming the Register

Bit 15	Action
0	The values are written into the register (OPMODE or LIMIT)
1	The values are not written into the register

Table 11-3. Effect of the Configuration Words within the Registers

Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15
OFF command														
1	–	–	–	–	–	–	–	–	–	–	–	–	–	–
–		OPMODE register												–
0	1	BR_Range		$N_{Bit-check}$		Modu-lation	Sleep					X_{Sleep}	Noise Suppression	0
		Baud1	Baud0	BitChk1	BitChk0	ASK/ _FSK	Sleep4	Sleep3	Sleep2	Sleep1	Sleep0	$X_{SleepStd}$	Noise_ Disable	
Default values of Bit 3...14		0	0	0	1	0	0	0	1	1	0	0	1	–
–		LIMIT register												–
0	0	Lim_min						Lim_max						–
		Lim_ min5	Lim_ min4	Lim_ min3	Lim_ min2	Lim_ min1	Lim_ min0	Lim_ max5	Lim_ max4	Lim_ max3	Lim_ max2	Lim_ max1	Lim_ max0	0
Default values of Bit 3...14		0	1	0	1	0	1	1	0	1	0	0	1	–