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Features

- Two Different IF Receiving Bandwidth Versions are Available (B_{IF} = 300 kHz or 600 kHz)
- 5V to 20V Automotive-Compatible Data Interface
- IC Condition Indicator, Sleep or Active Mode
- Data Clock Available for Manchester- and Bi-phase-coded Signals
- Fully Integrated VCO
- Supply Voltage 4.5V to 5.5V, Operating Temperature Range -40°C to +105°C
- Single-ended RF Input for Easy Adaptation to λ/4 Antenna or Printed Antenna on PCB
- ESD Protection According to MIL-STD. 883 (2KV HBM)
- High Image Frequency Suppression Due to 1 MHz IF in Conjunction with a SAW Front-end Filter; Up to 40 dB is Achievable with State-of-the-art SAWs
- Communication to Microcontroller Possible Via a Single, Bi-directional Data Line
- Power Management (Polling) is also Possible by Means of a Separate Pin Via the Microcontroller
- Programmable Digital Noise Suppression
- SSO20 Package

Pb Lead Free

Benefits

- Low Power Consumption Due to Configurable Self Polling with a Programmable Time frame Check
- High Sensitivity, Especially at Low Data Rates
- Minimal External Circuitry Requirements, no RF Components on the PC Board Except Matching to the Receiver Antenna
- Sensitivity Reduction Possible Even While Receiving
- Low-cost Solution Due to High Integration Level

1. Description

The ATA5743 is a multi-chip PLL receiver device supplied in an SSO20 package. It has been especially developed for the demands of RF low-cost data transmission systems with data rates from 1 kBaud to 10 kBaud in Manchester or Bi-phase code. The receiver is well suited to operate with Atmel's PLL RF transmitter U2741B. Its main applications are in the areas of telemetering, security technology, and keyless-entry systems. It can be used in the frequency receiving range of f_0 = 300 MHz to 450 MHz for ASK or FSK data transmission. All the statements made below refer to 433.92 MHz and 315 MHz applications.

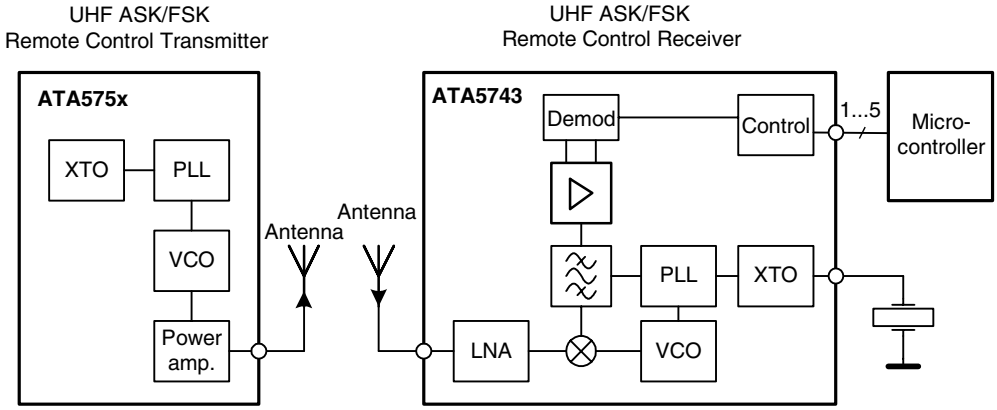
UHF ASK/FSK Receiver

ATA5743

Rev. 4839B–RKE–08/05

2. System Block Diagram

Figure 2-1. System Block Diagram



3. Pin Configuration

Figure 3-1. Pinning SSO20

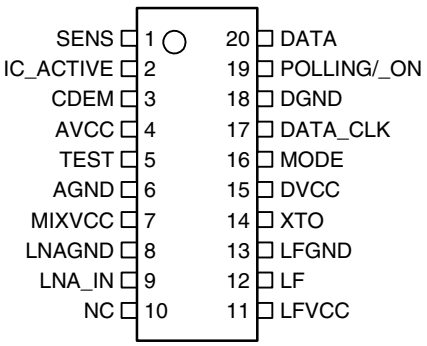
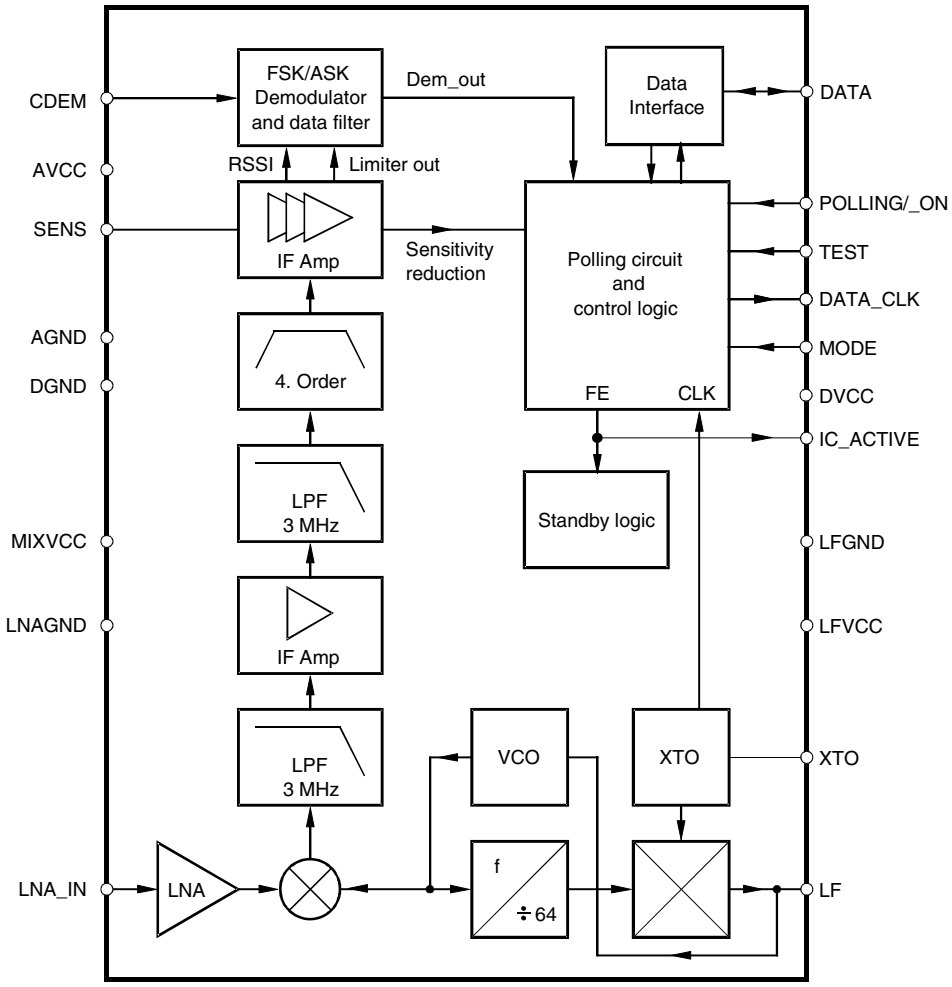


Table 3-1. Pin Description

Pin	Symbol	Function
1	SENS	Sensitivity-control resistor
2	IC_ACTIVE	IC condition indicator Low = sleep mode High = active mode
3	CDEM	Lower cut-off frequency data filter
4	AVCC	Analog power supply
5	TEST	Test pin, during operation at GND
6	AGND	Analog ground
7	MIXVCC	Power supply mixer
8	LNAGND	High-frequency ground LNA and mixer
9	LNA_IN	RF input
10	NC	Not connected
11	LFVCC	Power supply VCO
12	LF	Loop filter
13	LFGND	Ground VCO
14	XTO	Crystal oscillator
15	DVCC	Digital power supply
16	MODE	Selecting 433.92 MHz/315 MHz Low: f_{XT0} = 4.90625 MHz (USA) High: f_{XT0} = 6.76438 MHz (Europe)
17	DATA_CLK	Bit clock of data stream
18	DGND	Digital ground
19	POLLING/_ON	Selects polling or receiving mode Low: receiving mode High: polling mode
20	DATA	Data output/configuration input

Figure 3-2. Block Diagram



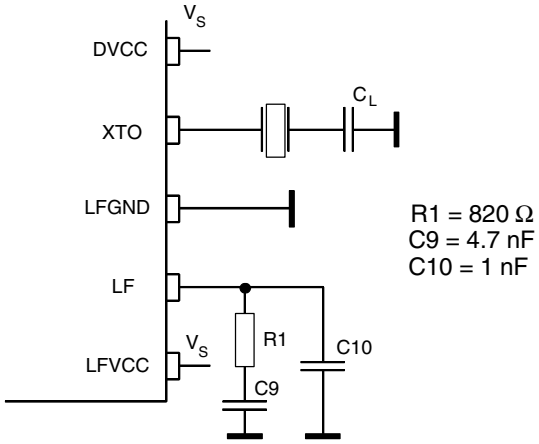
4. RF Front-end

The RF front-end of the receiver is a heterodyne configuration that converts the input signal into a 1 MHz IF signal. As seen in Figure 3-2 on page 4, the front-end consists of an LNA (Low-Noise Amplifier), an LO (Local Oscillator), a mixer, and an RF amplifier.

The LO generates the carrier frequency for the mixer via a PLL synthesizer. The XTO (crystal oscillator) generates the reference frequency f_{XTO}. The VCO (voltage-controlled oscillator) generates the drive voltage frequency f_{LO} for the mixer. f_{LO} is dependent on the voltage at pin LF, and is then divided by 64. The divided frequency is compared to f_{XTO} by the phase frequency detector. The current output of the phase frequency detector is connected to a passive loop filter and thereby generates the control voltage V_{LF} for the VCO. By means of that configuration, V_{LF} is controlled in a way that $f_{LO}/64$ is equal to f_{XTO}. If f_{LO} is determined, f_{XTO} can be calculated using the following formula: $f_{XTO} = f_{LO}/64$.

The XTO is a one-pin oscillator that operates at the series resonance of the quartz crystal. As demonstrated in Figure 4-1, the crystal should be connected to GND via a capacitor C_L. The value of that capacitor is recommended by the crystal supplier. The value of C_L should be optimized for the individual board layout to achieve the exact value of f_{XTO} and hereby of f_{LO}. When designing the system in terms of receiving bandwidth, the accuracy of the crystal and the XTO must be considered.

Figure 4-1. PLL Peripherals



The passive loop filter connected to pin LF is designed for a loop bandwidth of B_{Loop} = 100 kHz. This value for B_{Loop} exhibits the best possible noise performance of the LO. Figure 4-1 shows the appropriate loop filter components to achieve the desired loop bandwidth. If the filter components are changed for any reason, please note that the maximum capacitive load at pin LF is limited. If the capacitive load is exceeded, a bit check may no longer be possible since f_{LO} cannot settle in time before the bit check starts to evaluate the incoming data stream. Self polling will also not work in that case.

f_{LO} is determined by the RF input frequency f_{RF} and the IF frequency f_{IF} using the following formula: $f_{LO} = f_{RF} - f_{IF}$

To determine f_{LO}, the construction of the IF filter must be considered at this point. The nominal IF frequency is f_{IF} = 1 MHz. To achieve a good accuracy of the filter's corner frequencies, the filter is tuned by the crystal frequency f_{XTO}. This means that there is a fixed relation between f_{IF} and f_{LO}. This relation is dependent on the logic level at pin MODE.

This is described by the following formulas:

$$\text{MODE} = 0\ (\text{USA}) : f_{IF} = \frac{f_{LO}}{314}$$

$$\text{MODE} = 1\ (\text{Europe}) : f_{IF} = \frac{f_{LO}}{432.92}$$

The relation is designed to achieve the nominal IF frequency of f_{IF} = 1 MHz for most applications. For applications where f_{RF} = 315 MHz, MODE must be set to “0”. In the case of f_{RF} = 433.92 MHz, MODE must be set to “1”. For other RF frequencies, f_{IF} is not equal to 1 MHz. f_{IF} is then dependent on the logical level at pin MODE and on f_{RF}. Table 4-1 summarizes the different conditions.

The RF input either from an antenna or from a generator must be transformed to the RF input pin LNA_IN. The input impedance of that pin is provided in the electrical parameters. The parasitic board inductances and capacitances also influence the input matching. The RF receiver ATA5743 exhibits its highest sensitivity at the best signal-to-noise ratio (SNR) in the LNA. Hence, noise matching is the best choice for designing the transformation network.

A good practice when designing the network is to start with power matching. From that starting point, the values of the components can be varied to some extent to achieve the best sensitivity.

If a SAW is implemented into the input network, a mirror frequency suppression of ΔP_{Ref} = 40 dB can be achieved. There are SAWs available that exhibit a notch at Δf = 2 MHz. These SAWs work best for an intermediate frequency of f_{IF} = 1 MHz. The selectivity of the receiver is also improved by using a SAW. In typical automotive applications, a SAW is used.

Figure 4-2 on page 7 shows a typical input matching network, for f_{RF} = 315 MHz and f_{RF} = 433.92 MHz, using a SAW. Figure 4-3 on page 7 illustrates an according input matching to 50Ω without a SAW. The input matching networks shown in Figure 4-3 on page 7 are the reference networks for the parameters given in the table “Electrical Characteristics” on page 33.

Table 4-1. Calculation of LO and IF Frequency

Conditions	Local Oscillator Frequency	Intermediate Frequency
f_{RF} = 315 MHz, MODE = 0	f_{LO} = 314 MHz	f_{IF} = 1 MHz
f_{RF} = 433.92 MHz, MODE = 1	f_{LO} = 432.92 MHz	f_{IF} = 1 MHz
300 MHz < f_{RF} < 365 MHz, MODE = 0	$f_{LO} = \frac{f_{RF}}{1 + \frac{1}{314}}$	$f_{IF} = \frac{f_{LO}}{314}$
365 MHz < f_{RF} < 450 MHz, MODE = 1	$f_{LO} = \frac{f_{RF}}{1 + \frac{1}{432.32}}$	$f_{IF} = \frac{f_{LO}}{432.92}$

Figure 4-2. Input Matching Network with SAW Filter

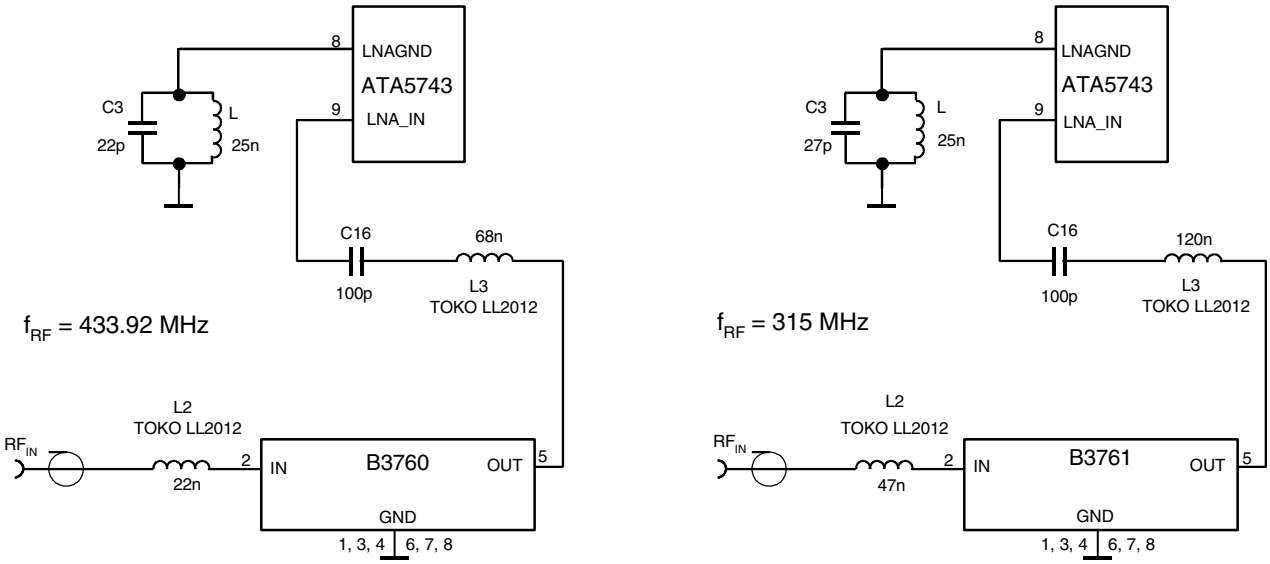
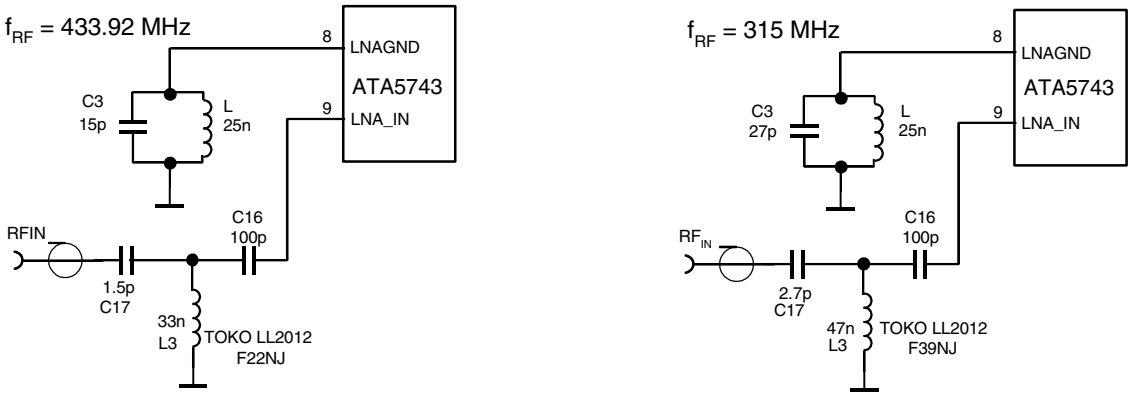


Figure 4-3. Input Matching Network without SAW Filter



Please notice that for all coupling conditions (see Figure 4-2 and Figure 4-3), the bond wire inductivity of the LNA ground is compensated. C3 forms a series resonance circuit together with the bond wire. L = 25 nH is a feed inductor to establish a DC path. Its value is not critical, but must be large enough not to detune the series resonance circuit. For cost reduction this inductor can be easily printed on the PCB. This configuration improves the sensitivity of the receiver by about 1 to 2 dB.

5. Analog Signal Processing

5.1 IF Amplifier

The signals coming from the RF front-end are filtered by the fully integrated 4th-order IF filter. The IF center frequency is f_{IF} = 1 MHz for applications where f_{RF} = 315 MHz or f_{RF} = 433.92 MHz. For other RF input frequencies refer to Table 4-1 on page 6 to determine the center frequency.

The ATA5743 is available with two different IF bandwidths. ATA5743P3, the version with B_{IF} = 300 kHz, is well suited for ASK systems where Atmel's PLL transmitter U2741B is used. The receiver ATA5743P6 employs an IF bandwidth of B_{IF} = 600 kHz. Both versions can be used together with the U2741B in ASK and FSK mode. If used in ASK applications, higher tolerances for the receiver and PLL transmitter crystals are allowed. SAW transmitters exhibit much higher transmit frequency tolerances compared to PLL transmitters. Generally, it is necessary to use B_{IF} = 600 kHz together with SAW transmitters.

5.2 RSSI Amplifier

The subsequent RSSI amplifier enhances the output signal of the IF amplifier before it is fed into the demodulator. The dynamic range of this amplifier is DR_{RSSI} = 60 dB. If the RSSI amplifier is operated within its linear range, the best SNR is maintained in ASK mode. If the dynamic range is exceeded by the transmitter signal, the SNR is defined by the ratio of the maximum RSSI output voltage and the RSSI output voltage due to a disturber. The dynamic range of the RSSI amplifier is exceeded if the power of the input signal is 60 dB higher than the sensitivity of the receiver.

In FSK mode the SNR is not affected by the dynamic range of the RSSI amplifier.

The output voltage of the RSSI amplifier is internally compared to a threshold voltage V_{Th_red}. V_{Th_red} is determined by the value of the external resistor R_{Sense}. R_{Sense} is connected between pin SENS and GND or V_S. The output of the comparator is fed into the digital control logic. By this means it is possible to operate the receiver at a lower sensitivity.

If R_{Sense} is connected to GND, the receiver operates at full sensitivity.

If R_{Sense} is connected to V_S, the receiver operates at a lower sensitivity. The reduced sensitivity is defined by the value of R_{Sense}, the maximum sensitivity by the SNR of the LNA input. The reduced sensitivity depends on the signal strength at the output of the RSSI amplifier.

Since different RF input networks may exhibit slightly different values for the LNA gain, the sensitivity values given in the electrical characteristics refer to a specific input matching. This matching is illustrated in Figure 4-3 on page 7 and exhibits the best possible sensitivity.

R_{Sense} can be connected to V_S or GND via a microcontroller. The receiver can be switched from full sensitivity to reduced sensitivity or vice versa at any time. In polling mode, the receiver will not wake up if the RF input signal does not exceed the selected sensitivity. If the receiver is already active, the data stream at pin DATA will disappear when the input signal is lower than defined by the reduced sensitivity. Instead of the data stream, the pattern shown in Figure 5-1 on page 9 is issued at pin DATA to indicate that the receiver is still active (see Figure 6-26 on page 29).

Figure 5-1. Steady L State Limited DATA Output Pattern

5.3 FSK/ASK Demodulator and Data Filter

The signal coming from the RSSI amplifier is converted into the raw data signal by the ASK/FSK demodulator. The operating mode of the demodulator is set via the bit ASK/_FSK in the OPMODE register. Logic 'L' sets the demodulator to FSK, applying 'H' to ASK mode.

In ASK mode, an automatic threshold control circuit (ATC) is used to set the detection reference voltage to a value where a good SNR is achieved. This circuit effectively suppresses any kind of inband noise signals or competing transmitters. If the SNR (ratio to suppress inband noise signals) exceeds 10 dB, the data signal can be detected properly.

The FSK demodulator is intended to be used for an FSK deviation of 10 kHz $\leq \Delta f \leq$ 100 kHz. In FSK mode the data signal can be detected if the SNR (ratio to suppress inband noise signals) exceeds 2 dB. This value is guaranteed for all modulation schemes of a disturber signal.

The output signal of the demodulator is filtered by the data filter before it is fed into the digital signal processing circuit. The data filter improves the SNR as its passband can be adopted to the characteristics of the data signal. The data filter consists of a 1st-order high-pass and a 2nd-order low-pass filter.

The high-pass filter cut-off frequency is defined by an external capacitor connected to pin CDEM. The cut-off frequency of the high-pass filter is defined by the following formula:

$$fcu\_DF = \frac{1}{2 \times \pi \times 30\ k\Omega \times CDEM}$$

In self-polling mode, the data filter must settle very rapidly to achieve a low current consumption. Therefore, CDEM cannot be increased to very high values if self-polling is used. On the other hand, CDEM must be large enough to meet the data filter requirements according to the data signal. Recommended values for CDEM are given in the electrical characteristics.

The cut-off frequency of the low-pass filter is defined by the selected baud-rate range (BR_Range). The BR_Range is defined in the OPMODE register (refer to section "Configuration of the Receiver" on page 24). The BR_Range must be set in accordance to the used baud rate.

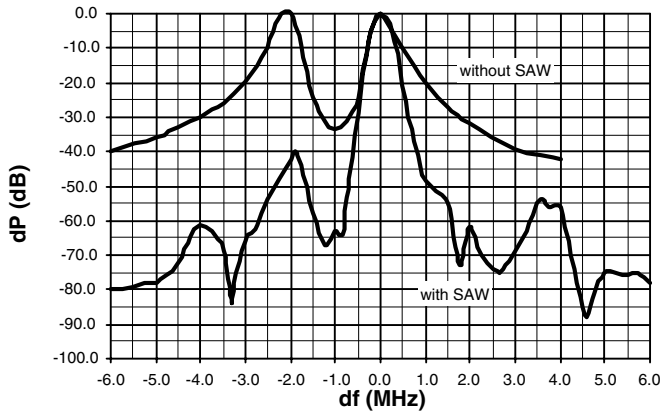
The ATA5743 is designed to operate with data coding where the DC level of the data signal is 50%. This is valid for Manchester and Bi-phase coding. If other modulation schemes are used, the DC level should always remain within the range of V_{DC_min} = 33% and V_{DC_max} = 66%. Even then, the sensitivity will be reduced by up to 2 dB.

Each BR_Range is also defined by a minimum and a maximum edge-to-edge time (t_{ee_sig}). These limits are defined in the electrical characteristics; to maintain full sensitivity of the receiver, they should not be exceeded.

5.4 Receiving Characteristics

The RF receiver ATA5743 can be operated with and without a SAW front-end filter. In a typical automotive application, a SAW filter is used to achieve better selectivity. The selectivity with and without a SAW front-end filter is illustrated in Figure 5-2. This example relates to ASK mode and the 300-kHz bandwidth version of the ATA5743. FSK mode and the 600-kHz bandwidth version of the receiver exhibit similar behavior. Note that the mirror frequency is reduced by 40 dB. The plots are printed relative to the maximum sensitivity. If a SAW filter is used, an insertion loss of about 4 dB must be considered.

Figure 5-2. Receiving Frequency Response



When designing the system in terms of receiving bandwidth, the LO deviation must be considered as it also determines the IF center frequency. The total LO deviation is calculated to be the sum of the deviation of the crystal and the XTO deviation of the ATA5743. Low-cost crystals are specified to be within ±100 ppm. The XTO deviation of the ATA5743 is an additional deviation due to the XTO circuit. This deviation is specified to be ±30 ppm. If a crystal of ±100 ppm is used, the total deviation is ±130 ppm in that case. Note that the receiving bandwidth and the IF-filter bandwidth are equivalent in ASK mode, but not in FSK mode.

6. Polling Circuit and Control Logic

The receiver is designed to consume less than 1 mA while being sensitive to signals from a corresponding transmitter. This is achieved via the polling circuit. This circuit enables the signal path periodically for a short time. During this time the bit-check logic verifies the presence of a valid transmitter signal. Only if a valid signal is detected will the receiver remain active and transfer the data to the connected microcontroller. If there is no valid signal present, the receiver remains in sleep mode most of the time, resulting in low current consumption; this condition is called polling mode. A connected microcontroller is disabled during this time.

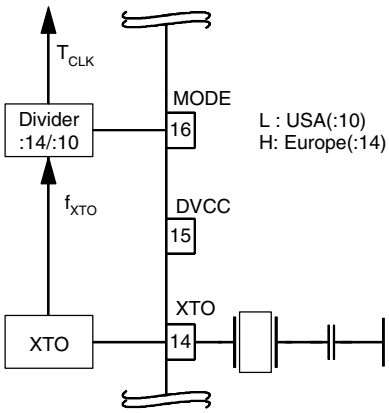
All relevant parameters of the polling logic can be configured by the connected microcontroller. This flexibility enables the user to meet the specifications in terms of current consumption, system response time, data rate, etc.

Regarding the number of connection wires to the microcontroller, the receiver is very flexible. It can be either operated by a single bi-directional line (to save ports to the connected microcontroller), or it can be operated by up to five uni-directional ports.

6.1 Basic Clock Cycle of the Digital Circuitry

The complete timing of the digital circuitry and the analog filtering is derived from one clock. As seen in Figure 6-1, this clock cycle T_{Clk} is derived from the crystal oscillator (XTO) in combination with a divider. The division factor is controlled by the logical state at pin MODE. As described in section "RF Front-end" on page 5, the frequency of the crystal oscillator (f_{XTO}) is defined by the RF input signal (f_{RFin}) which also defines the operating frequency of the local oscillator (f_{LO}).

Figure 6-1. Generation of the Basic Clock Cycle



Pin MODE can now be set in accordance with the desired clock cycle T_{Clk}, which controls the following application relevant parameters:

- Timing of the polling circuit including bit check
- Timing of the analog and digital signal processing
- Timing of the register programming
- Frequency of the reset marker
- IF filter center frequency (f_{IF0})

Most applications are dominated by two transmission frequencies: f_{Send} = 315 MHz is mainly used in the USA, f_{Send} = 433.92 MHz in Europe. In order to ease the usage of all T_{Clk}-dependent parameters on these electrical characteristics, here are displayed the three conditions for each parameter.

- Application USA (f_{XTO} = 4.90625 MHz, MODE = L, T_{Clk} = 2.0383 µs)
- Application Europe (f_{XTO} = 6.76438 MHz, MODE = H, T_{Clk} = 2.0697 µs)
- Other applications (T_{Clk} is dependent on f_{XTO} and on the logical state of pin MODE. The electrical characteristic is given as a function of T_{Clk}).

The clock cycle of some function blocks depends on the selected baud-rate range (BR_Range) which is defined in the OPMODE register. This clock cycle T_{XClk} is defined by the following formulas for further reference:

BR_Range =	BR_Range0:	$T_{XClk} = 8 \times T_{Clk}$
	BR_Range1:	$T_{XClk} = 4 \times T_{Clk}$
	BR_Range2:	$T_{XClk} = 2 \times T_{Clk}$
	BR_Range3:	$T_{XClk} = 1 \times T_{Clk}$

6.2 Polling Mode

As shown in Figure 6-2 on page 13, the receiver's polling mode consists of a continuous cycle of three different modes. In sleep mode, the signal processing circuitry is disabled for the time period T_{Sleep} while consuming low current of $I_S = I_{Soff}$. During the start-up period, $T_{Startup}$, all signal processing circuits are enabled and settled. In the following bit-check mode, the incoming data stream is analyzed bit-by-bit, looking for a valid transmitter signal. If no valid signal is present, the receiver is set back to sleep mode after the period $T_{Bit\text{-}check}$. This period varies check-by-check as it is a statistical process. An average value for $T_{Bit\text{-}check}$ is given in the electrical characteristics. During $T_{Startup}$ and $T_{Bit\text{-}check}$, the current consumption is $I_S = I_{Son}$. The condition of the receiver is indicated on pin IC_ACTIVE.

The average current consumption in polling mode is dependent on the duty cycle of the active mode and can be calculated as:

$$I_{Spoll} = \frac{I_{Soff} \times T_{Sleep} + I_{Son} \times (T_{Startup} + T_{Bit\text{-}check})}{T_{Sleep} + T_{Startup} + T_{Bit\text{-}check}}$$

During T_{Sleep} and $T_{Startup}$, the receiver is not sensitive to a transmitter signal. To guarantee the reception of a transmitted command, the transmitter must start the telegram with an adequate preburst. The required length of the preburst depends on the polling parameters T_{Sleep}, $T_{Startup}$, $T_{Bit\text{-}check}$, and the start-up time of a connected microcontroller ($T_{Start,\ \mu C}$). Thus, $T_{Bit\text{-}check}$ depends on the actual bit rate and the number of bits ($N_{Bit\text{-}check}$) to be tested.

The following formula indicates how to calculate the preburst length.

$$T_{Preburst} \geq T_{Sleep} + T_{Startup} + T_{Bit\text{-}check} + T_{Start\_\mu C}$$

6.3 Sleep Mode

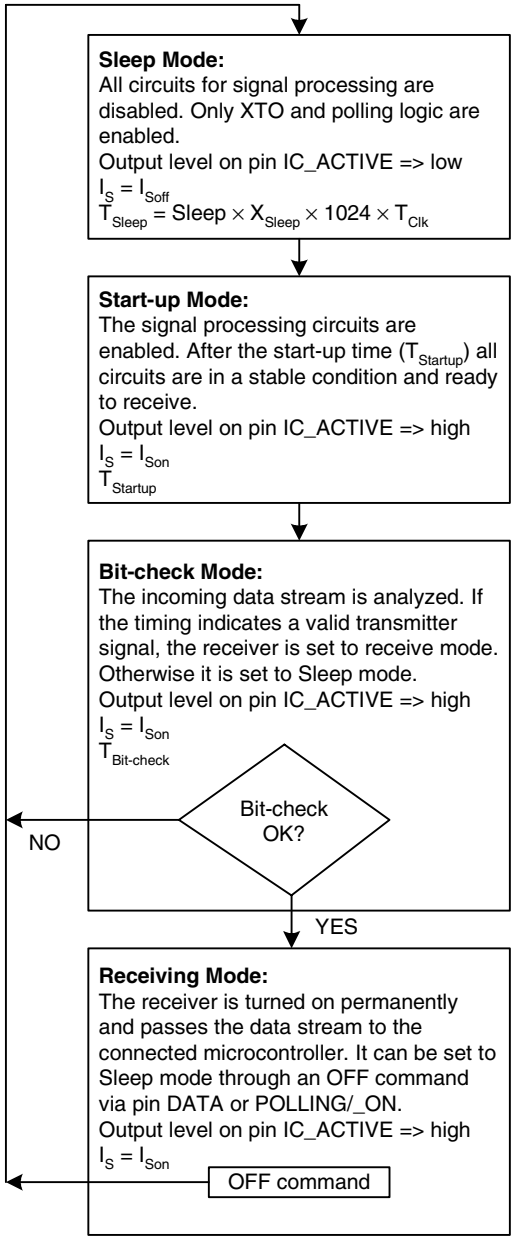
The length of period T_{Sleep} is defined by the 5-bit word Sleep of the OPMODE register, the extension factor X_{Sleep} (see Table 6-8 on page 26), and the basic clock cycle T_{Clk}. It is calculated to be:

$$T_{Sleep} = Sleep \times X_{Sleep} \times 1024 \times T_{Clk}$$

In US and European applications, the maximum value of T_{Sleep} is about 60 ms if X_{Sleep} is set to "1"; the time resolution is about 2 ms in that case. The sleep time can be extended to almost half a second by setting X_{Sleep} to 8. X_{Sleep} can be set to 8 by setting bit $X_{SleepStd}$ to "1".

As seen in Table 6-7 on page 26, the highest register value of sleep sets the receiver into a permanent sleep condition. The receiver remains in that condition until another value for Sleep is programmed into the OPMODE register. This function is desirable where several devices share a single data line and may also be used for microcontroller polling – via pin POLLING/_ON, the receiver can be switched on and off.

Figure 6-2. Polling Mode Flow Chart



Sleep: 5-bit word defined by Sleep0 to Sleep4 in OPMODE register

X_{Sleep}: Extension factor defined by $X_{SleepStd}$ according to Table 9

T_{Clk}: Basic clock cycle defined by f_{XTO} and pin MODE

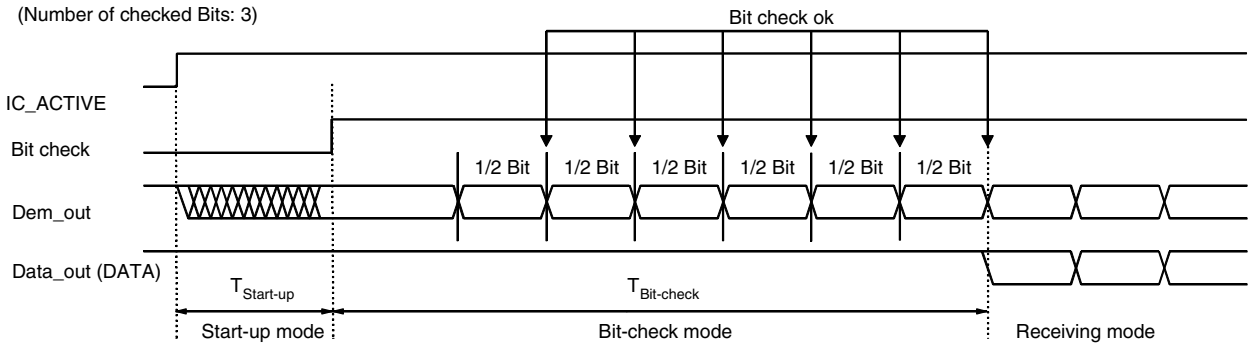
$T_{Startup}$: Defined by the selected baud rate range and T_{Clk}. The baud-rate range is defined by Baud0 and Baud1 in the OPMODE register

$T_{Bit\text{-}check}$: Depends on the result of the bit check

If the bit check is ok, $T_{Bit\text{-}check}$ depends on the number of bits to be checked ($N_{Bit\text{-}check}$), and on the utilized data rate

If the bit check fails, the average time period for that check depends on the selected baud-rate range on T_{Clk}. The baud-rate range is defined by Baud0 and Baud1 in the OPMODE register

Figure 6-3. Timing Diagram for Complete Successful Bit Check



6.3.1 Bit-check Mode

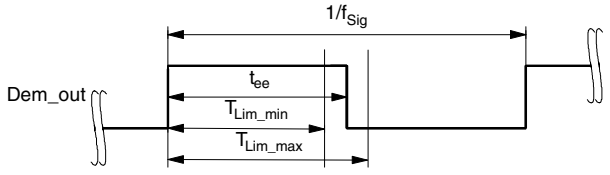
In bit-check mode the incoming data stream is examined to distinguish between a valid signal from a corresponding transmitter, and signals due to noise. This is done by subsequent time frame checks where the distances between two signal edges are continuously compared to a programmable time window. The maximum count of this edge-to-edge test before the receiver switches to receiving mode is also programmable.

6.3.2 Configuring the Bit Check

Assuming a modulation scheme that contains two edges per bit, two time frame checks verify one bit. This is valid for Manchester, Bi-phase, and most other modulation schemes. The maximum count of bits to be checked can be set to 0, 3, 6 or 9 bits via the variable $N_{Bit\text{-}check}$ in the OPMODE register. This implies 0, 6, 12 and 18 edge-to-edge checks, respectively. If $N_{Bit\text{-}check}$ is set to a higher value, the receiver is less likely to switch to receiving mode due to noise. In the presence of a valid transmitter signal, the bit check takes less time if $N_{Bit\text{-}check}$ is set to a lower value. In polling mode, the bit-check time is not dependent on $N_{Bit\text{-}check}$. Figure 6-3 shows an example where 3 bits are tested successfully and the data signal is transferred to pin DATA.

As demonstrated in Figure 6-4, the time window for the bit check is defined by two separate time limits. If the edge-to-edge time t_{ee} is between the lower bit-check limit, T_{Lim_min}, and the upper bit-check limit, T_{Lim_max}, the check will be continued. If t_{ee} is smaller than T_{Lim_min}, or t_{ee} exceeds T_{Lim_max}, the bit check will be terminated and the receiver will switch to sleep mode.

Figure 6-4. Valid Time Window for Bit Check



For best noise immunity it is recommended to use a low span between T_{Lim_min} and T_{Lim_max}. This is achieved by using a fixed frequency at a 50% duty cycle for the transmitter preburst. For this reason, a “11111...” or a “10101...” sequence in Manchester or Bi-phase is a good choice. A good compromise between receiver sensitivity and susceptibility to noise is a time window of ±25% regarding the expected edge-to-edge time t_{ee}. Using preburst patterns that contain various edge-to-edge time periods, the bit-check limits must be programmed according to the required span.

The bit-check limits are determined by means of the formula below.

$T_{Lim\_min} = Lim\_min \times T_{XClk}$
$T_{Lim\_max} = (Lim\_max -1) \times T_{XClk}$

Lim_min and Lim_max are defined by a 5-bit word each within the LIMIT register.

Using the above formulas, Lim_min and Lim_max can be determined according to the required T_{Lim_min}, T_{Lim_max} and T_{XClk}. The time resolution defining T_{Lim_min} and T_{Lim_max} is T_{XClk}. The minimum edge-to-edge time t_{ee} ($t_{DATA\_L\_min}$, $t_{DATA\_H\_min}$) is defined in the section "Digital Signal Processing" on page 16. The lower limit should be set to Lim_min ≥ 10. The maximum value of the upper limit is Lim_max = 63.

If the calculated value for Lim_min is < 19, it is recommended to check 6 or 9 bits ($N_{Bit\text{-}check}$) to prevent switching to receiving mode due to noise.

Figure 6-5, Figure 6-6 and Figure 6-7 on page 16 illustrate the bit check for the bit-check limits Lim_min = 14 and Lim_max = 24. When the IC is enabled, the signal processing circuits are enabled during $T_{Startup}$. The output of the ASK/FSK demodulator (Dem_out) is undefined during that period. When the bit check becomes active, the bit-check counter is clocked with the cycle T_{XClk}.

Figure 6-5 shows how the bit check proceeds if the bit-check counter value CV_Lim is within the limits defined by Lim_min and Lim_max at the occurrence of a signal edge. In Figure 6-6 the bit check fails as the value CV_lim is lower than the limit Lim_min. The bit check also fails if CV_Lim reaches Lim_max. This is illustrated in Figure 6-7 on page 16.

Figure 6-5. Timing Diagram During Bit Check

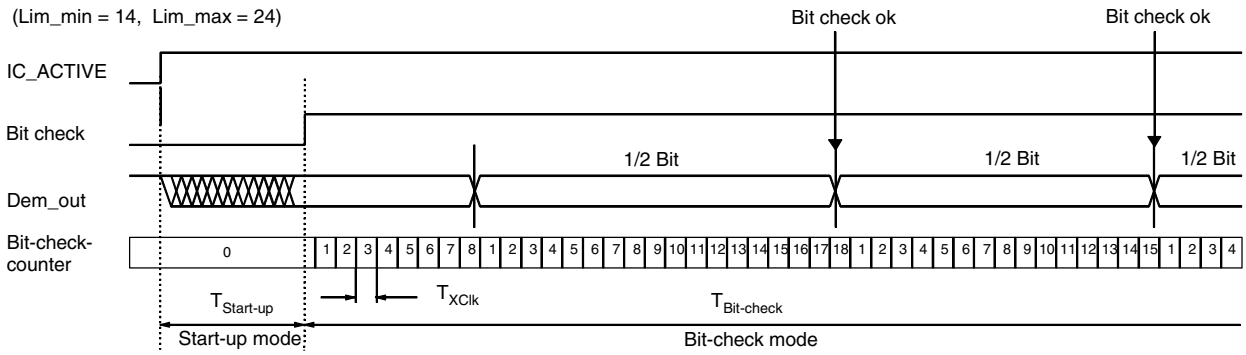


Figure 6-6. Timing Diagram for Failed Bit Check (Condition: CV_Lim < Lim_min)

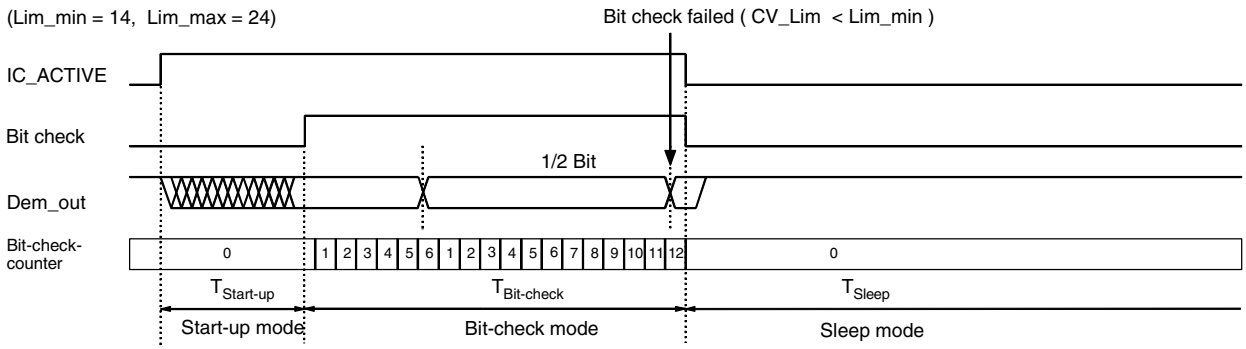
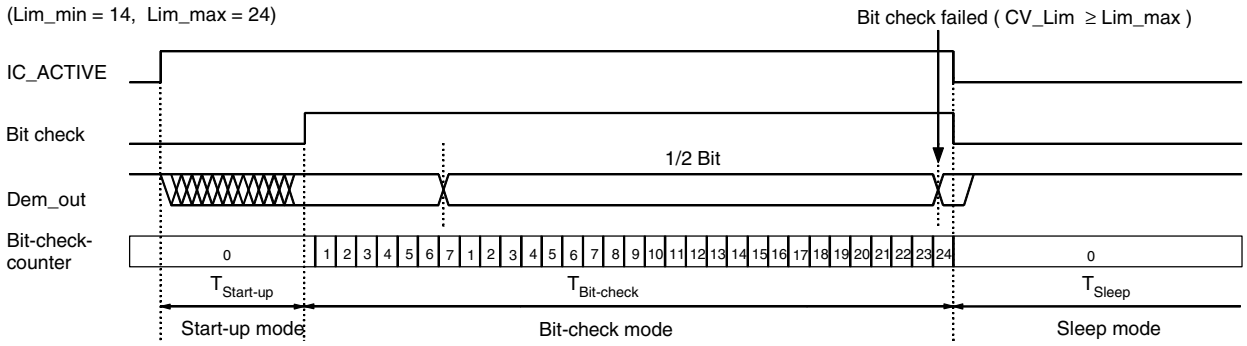


Figure 6-7. Timing Diagram for Failed Bit Check (Condition: CV_Lim ≥ Lim_max)



6.3.3 Duration of the Bit Check

If no transmitter signal is present during the bit check, the output of the ASK/FSK demodulator delivers random signals. The bit check is a statistical process and $T_{Bit\text{-}check}$ varies for each check. Therefore, an average value for $T_{Bit\text{-}check}$ is given in the electrical characteristics. $T_{Bit\text{-}check}$ depends on the selected baud-rate range and on T_{Clk}. A higher baud-rate range causes a lower value for $T_{Bit\text{-}check}$, resulting in lower current consumption in polling mode.

In the presence of a valid transmitter signal, $T_{Bit\text{-}check}$ is dependent on the frequency of that signal, f_{Sig}, and the count of the checked bits, $N_{Bit\text{-}check}$. A higher value for $N_{Bit\text{-}check}$ thereby results in a longer period for $T_{Bit\text{-}check}$, requiring a higher value for the transmitter preburst, $T_{Preburst}$.

6.3.4 Receiving Mode

If the bit check was successful for all bits specified by $N_{Bit\text{-}check}$, the receiver switches to receiving mode. As shown in Figure 6-3 on page 14, the internal data signal is then switched to pin DATA, and the data clock is available after the start bit has been detected (Figure 6-14 on page 20). A connected microcontroller can be woken up by the negative edge at pin DATA or by the data clock at pin DATA_CLK. The receiver stays in that condition until it is switched back to polling mode explicitly.

6.3.5 Digital Signal Processing

The data from the ASK/FSK demodulator (Dem_out) is digitally processed in different ways and converted into the output signal data. This processing depends on the selected baud-rate range (BR_Range). Figure 6-8 on page 17 illustrates how Dem_out is synchronized by the extended clock cycle T_{XClk}. This clock is also used for the bit-check counter. Data can change its state only after T_{XClk} has elapsed. The edge-to-edge time period t_{ee} of the Data signal, as a result, is always an integral multiple of T_{XClk}.

The minimum time period between two edges of the data signal is limited to $t_{ee} \geq T_{DATA\_min}$ (see Figure 6-9 on page 17). This implies an efficient suppression of spikes at the DATA output during data reception. At the same time, it limits the maximum frequency of edges at DATA. This eases the interrupt handling of a connected microcontroller.

The maximum time period for DATA to stay Low is limited to $T_{DATA\_L\_max}$. This function is employed to ensure a finite response time in programming or switching off the receiver via pin DATA. $T_{DATA\_L\_max}$ is thereby longer than the maximum time period indicated by the transmitter data stream. Figure 6-10 on page 17 shows an example where Dem_out remains Low after the receiver has switched to receiving mode.

Figure 6-8. Synchronization of the Demodulator Output

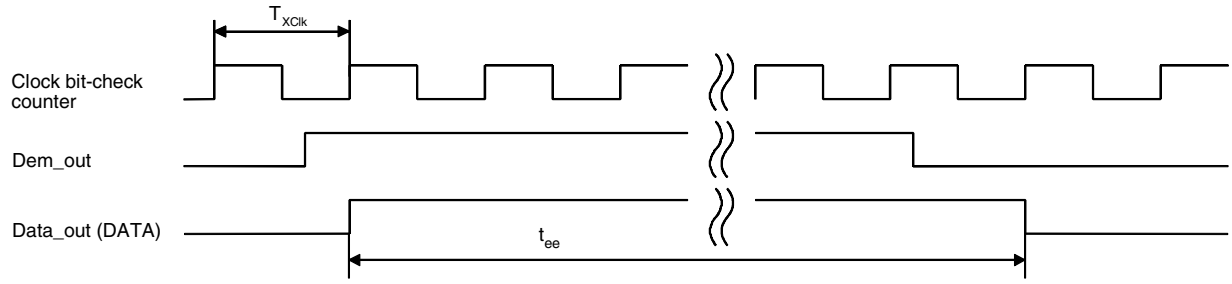


Figure 6-9. Debouncing of the Demodulator Output

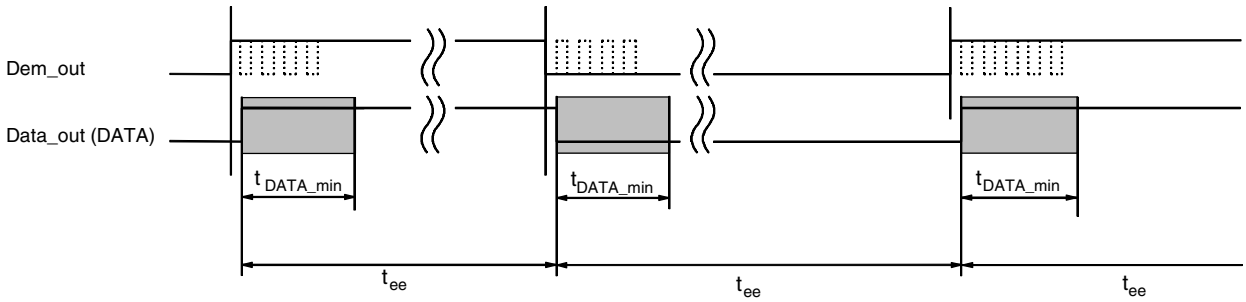
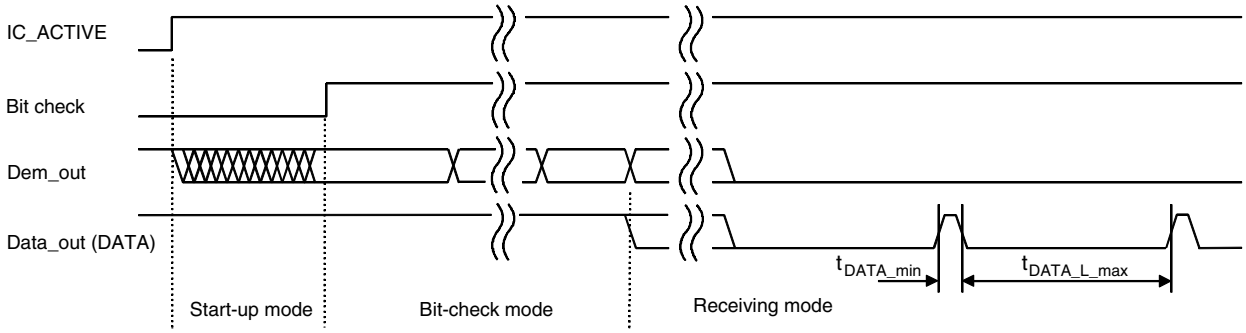


Figure 6-10. Steady L State Limited DATA Output Pattern After Transmission



After the end of a data transmission, the receiver remains active. Depending on the bit Noise_Disable in the OPMODE register, the output signal at pin DATA is high, or random noise pulses appear at pin DATA (see section “Digital Noise Suppression” on page 22). The edge-to-edge time period t_{ee} of the majority of these noise pulses is equal or slightly higher than T_{DATA_min}.

6.3.6 Switching the Receiver Back to Sleep Mode

The receiver can be set back to polling mode via pin DATA or via pin POLLING/_ON.

When using pin DATA, this pin must be pulled to Low by the connected microcontroller for the period t1. Figure 6-11 illustrates the timing of the OFF command (see also Figure 6-26 on page 29). The minimum value of t1 depends on BR_Range. The maximum value for t1 is not limited, but it is recommended not to exceed the specified value to prevent erasing the reset marker. (see section "Programming the Configuration Register" on page 28) Note also that an internal reset for the OPMODE and the LIMIT register will be generated if t1 exceeds the specified values. This item is explained in more detail in the section "Configuration of the Receiver" on page 24. Setting the receiver to sleep mode via DATA is achieved by programming bit 1 to be "1" during the register configuration. Only one sync pulse (t3) is issued.

The duration of the OFF command is determined by the sum of t1, t2 and t10. After the OFF command the sleep time T_{Sleep} elapses. Note that the capacitive load at pin DATA is limited (see section "Data Interface" on page 30).

Figure 6-11. Timing Diagram of the OFF command via Pin DATA

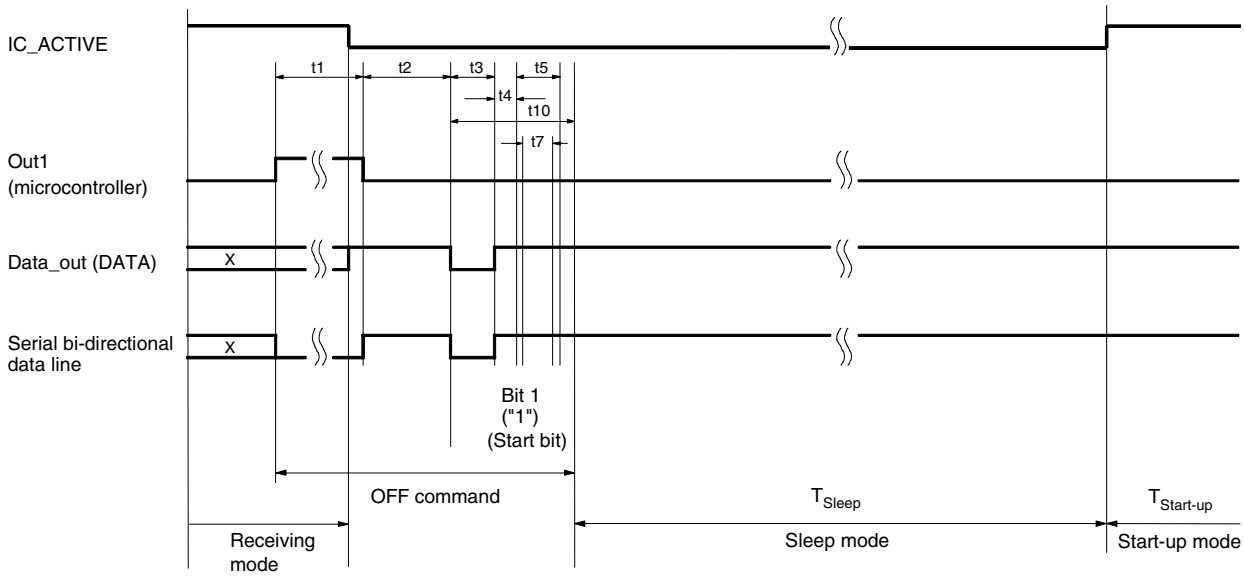


Figure 6-12. Timing Diagram of the OFF command via Pin POLLING/_ON

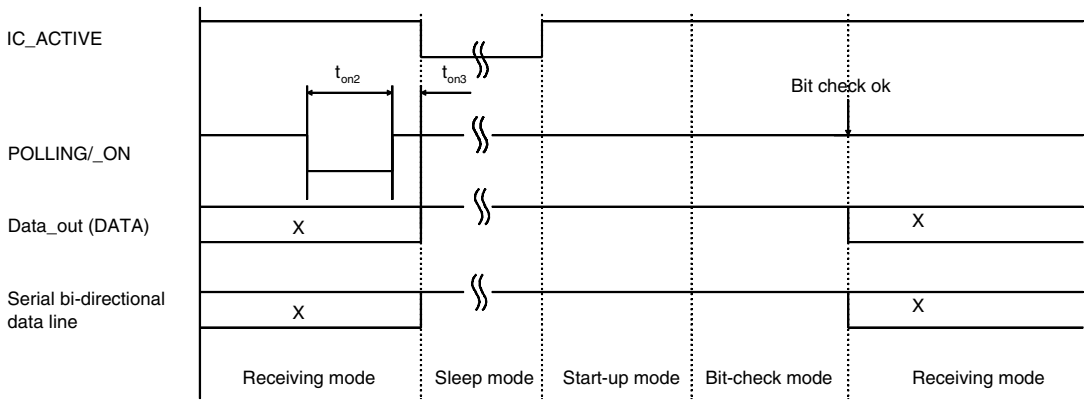


Figure 6-13. Activating the Receiving Mode via Pin POLLING/_ON

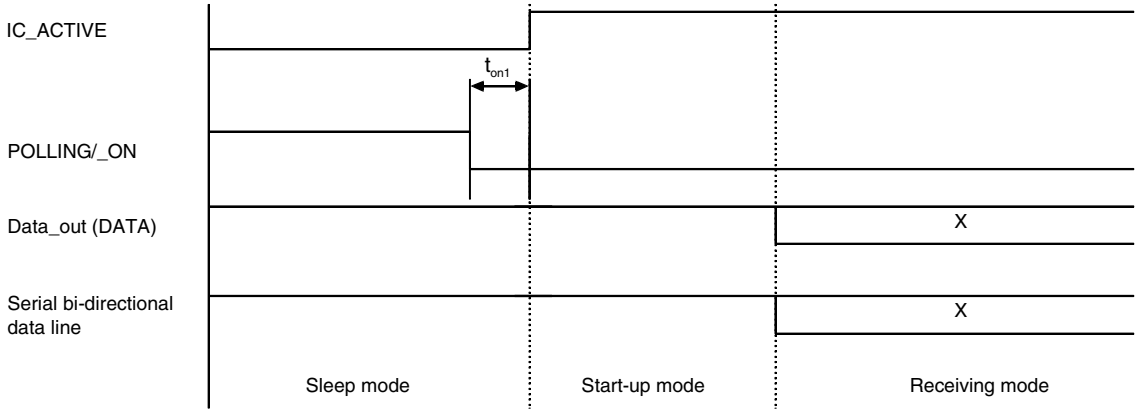


Figure 6-12 on page 18 illustrates how to set the receiver back to polling mode via pin POLLING/_ON. The pin POLLING/_ON must be held to low for the time period t_{on2}. After the positive edge on pin POLLING/_ON and the delay t_{on3}, the polling mode is active and the sleep time T_{Sleep} elapses.

This command is faster than using pin DATA, but at the cost of an additional connection to the microcontroller.

Figure 6-13 illustrates how to set the receiver to receive mode via the pin POLLING/_ON. The pin POLLING/_ON must be held to Low. After the delay t_{on1}, the receiver changes from sleep mode to start-up mode regardless of the programmed values for T_{Sleep} and $N_{Bit\text{-}check}$. As long as POLLING/_ON is held to Low, the values for T_{Sleep} and $N_{Bit\text{-}check}$ will be ignored, but not deleted (see section "Digital Noise Suppression" on page 22).

If the receiver is polled exclusively by a microcontroller, T_{Sleep} must be programmed to 31 (permanent sleep mode). In this case, the receiver remains in sleep mode as long as POLLING/_ON is held to High.

6.4 Data Clock

The pin DATA_CLK makes a data shift clock available to sample the data stream into a shift register. Using this data clock, a microcontroller can easily synchronize the data stream. This clock can only be used for Manchester- and Bi-phase-coded signals.

6.4.1 Generation of the Data Clock

After a successful bit check, the receiver switches from polling mode to receiving mode and the data stream is available at pin DATA. In receiving mode, the data clock control logic (Manchester/Bi-phase demodulator) is active and examines the incoming data stream. This is done, as in the bit check, by subsequent time frame checks where the distance between two edges is continuously compared to a programmable time window. As illustrated in Figure 6-14 on page 20, only two distances between two edges in Manchester- and Bi-phase-coded signals are valid (T and 2T).

The limits for T are the same as used for the bit check. They can be programmed in the LIMIT-register (Lim_min and Lim_max, see Table 6-10 on page 27 and Table 6-11 on page 27).

The limits for 2T are calculated as follows:

Lower limit of 2T: Lim_min_2T = (Lim_min + Lim_max) - (Lim_max - Lim_min)/2
Upper limit of 2T: Lim_max_2T = (Lim_min + Lim_max) + (Lim_max - Lim_min)/2

Note: If the result for “Lim_min_2T” or “Lim_max_2T” is not an integer value, it will be rounded up.

The data clock is available after the data clock control logic has detected the distance 2T (Start bit), and then issues pulses with a delay of t_{Delay} after the edges on pin DATA (see Figure 6-14).

If the data clock control logic detects a timing or logical error (Manchester code violation), as illustrated in Figure 6-15 and Figure 6-16 on page 21, it stops the output of the data clock. The receiver remains in receiving mode and starts with the bit check. If the bit check was successful and the start bit has been detected, the data clock control logic starts again with the generation of the data clock (see Figure 6-17 on page 21).

It is recommended to use the function of the data clock only in conjunction with the bit check 3, 6 or 9. If the bit check is set to 0 or the receiver is set to receiving mode via the pin POLLING/_ON, the data clock is available if the data clock control logic has detected the distance 2T (Start bit).

Note that for Bi-phase-coded signals, the data clock is issued at the end of the bit.

Figure 6-14. Timing Diagram of the Data Clock

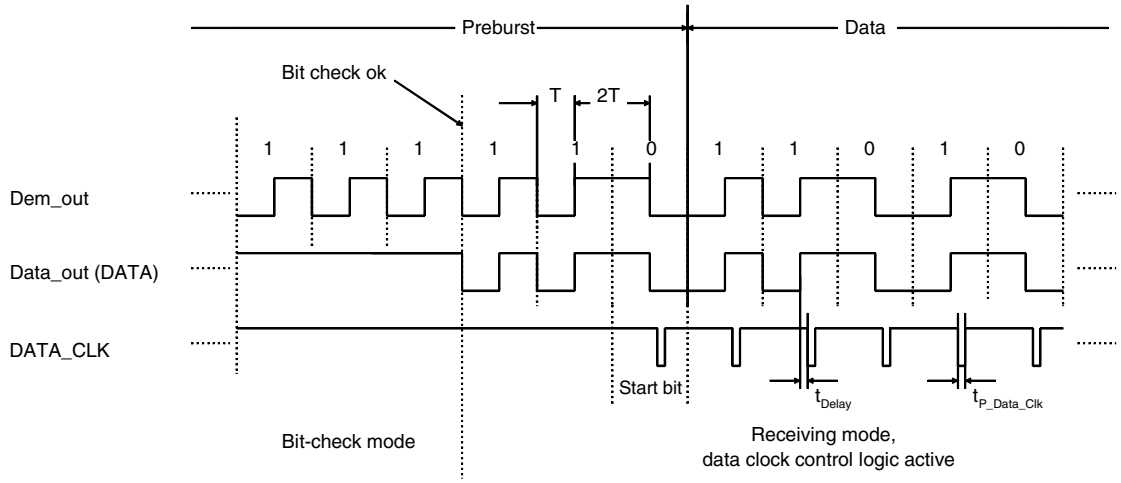


Figure 6-15. Data Clock Disappears Because of a Timing Error

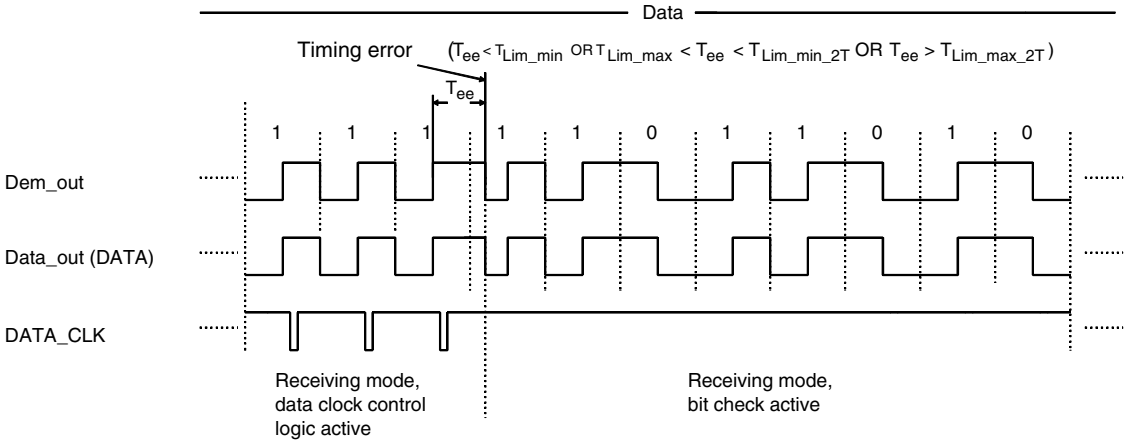


Figure 6-16. Data Clock Disappears Because of a Logical Error

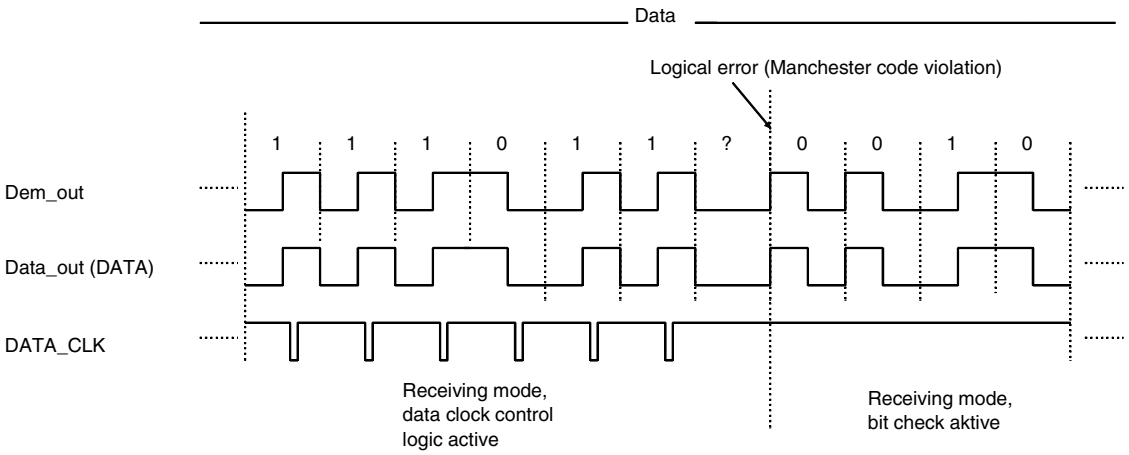
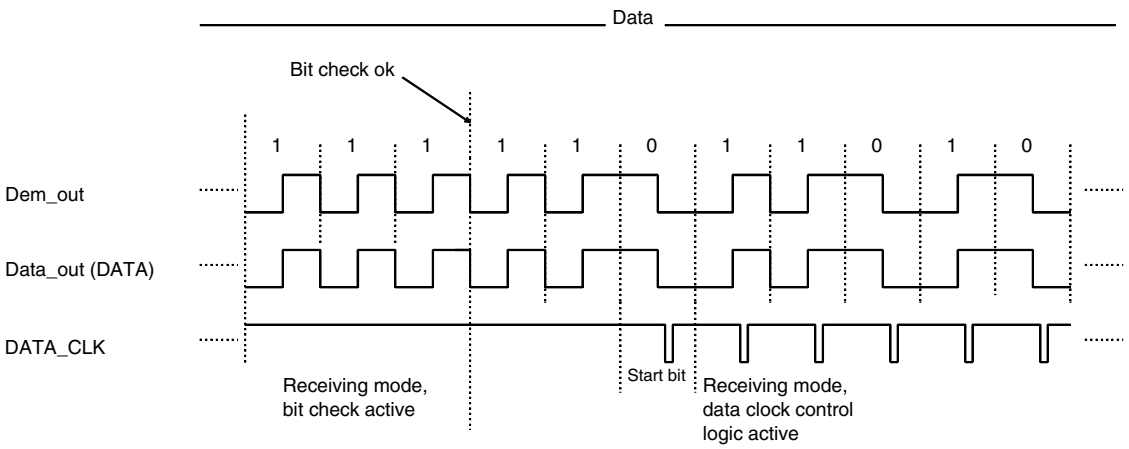


Figure 6-17. Output of the Data Clock After a Successful Bit Check



The delay of the data clock is calculated as follows:

$t_{Delay} = t_{Delay1} + t_{Delay2}$

t_{Delay1} is the delay between the internal signals Data_Out and Data_In. For the rising edge, t_{Delay1} depends on the capacitive load C_L at pin DATA and the external pull-up resistor R_{pup}. For the falling edge, t_{Delay1} depends additionally on the external voltage V_X (see Figure 6-18 on page 22, Figure 6-19 on page 22 and Figure 6-26 on page 29). When the level of Data_In is equal to the level of Data_Out, the data clock is issued after an additional delay t_{Delay2}.

Note that the capacitive load at pin DATA is limited. If the maximum tolerated capacitive load at pin DATA is exceeded, the data clock disappears (see section "Data Interface" on page 29).

Figure 6-18. Timing Characteristic of the Data Clock (Rising Edge on Pin DATA)

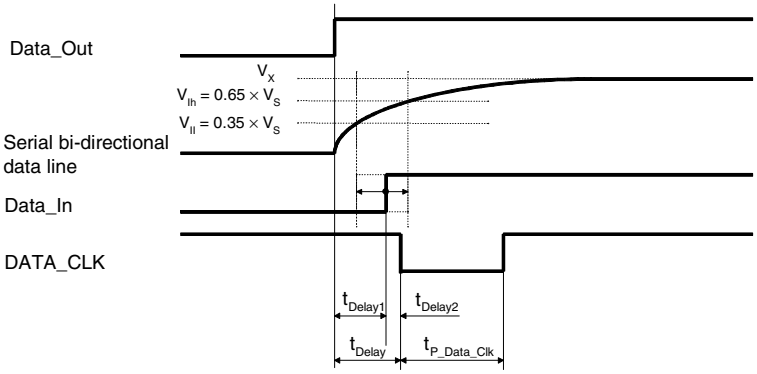
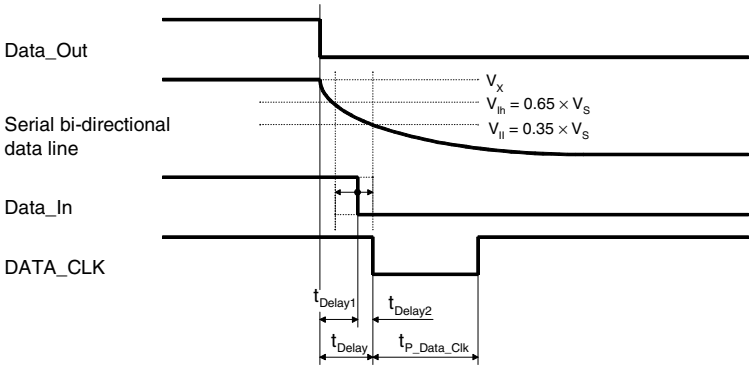


Figure 6-19. Timing Characteristic of the Data Clock (Falling Edge on Pin DATA)



6.5 Digital Noise Suppression

After a data transmission, digital noise appears on the data output (see Figure 6-20 on page 23). To prevent digital noise from keeping the connected microcontroller busy, it can be suppressed in two different ways.

6.5.1 Automatic Noise Suppression

The automatic noise suppression is illustrated in Figure 6-21 on page 23. If the bit Noise_Disable (Table 6-9 on page 26) in the OPMODE register is set to “1” (default), the receiver changes to bit-check mode at the end of a valid data stream. The digital noise is suppressed and the level at pin DATA is High in that case. The receiver changes back to receiving mode, if the bit check was successful.

This way of suppressing the noise is recommended if the data stream is Manchester or Bi-phase coded and is active after power on.

Figure 6-22 on page 23 illustrates the behavior of the data output at the end of a data stream. Note that if the last period of the data stream is a high period (rising edge to falling edge), a pulse occurs on pin DATA. The length of the pulse depends on the selected baud-rate range.

Figure 6-20. Output of Digital Noise at the End of the Data Stream

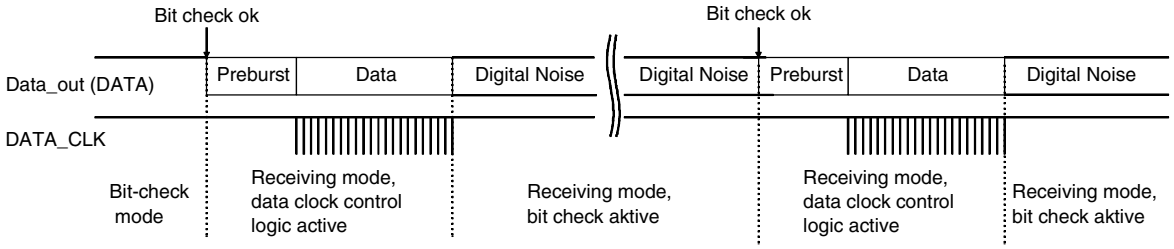


Figure 6-21. Automatic Noise Suppression

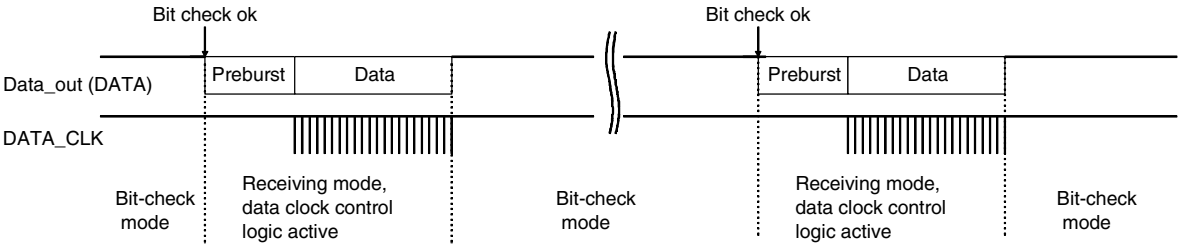
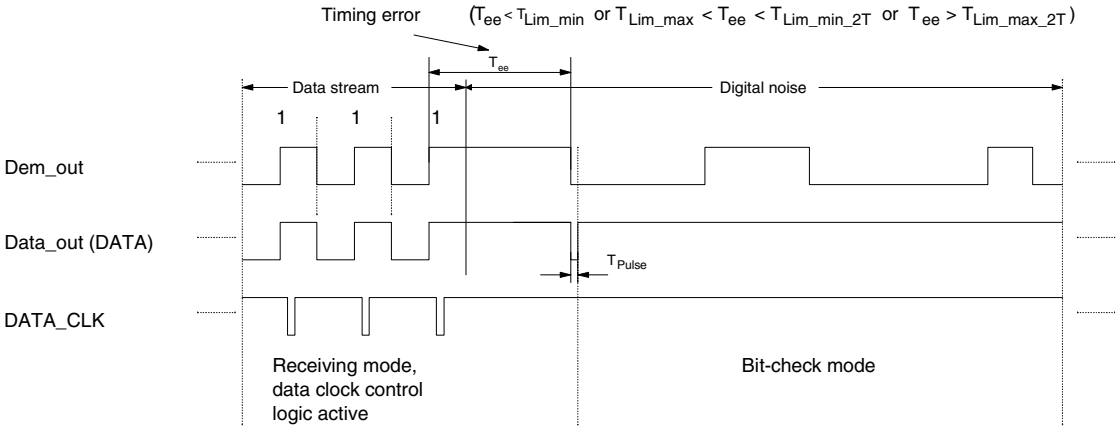


Figure 6-22. Occurrence of a Pulse at the End of the Data Stream

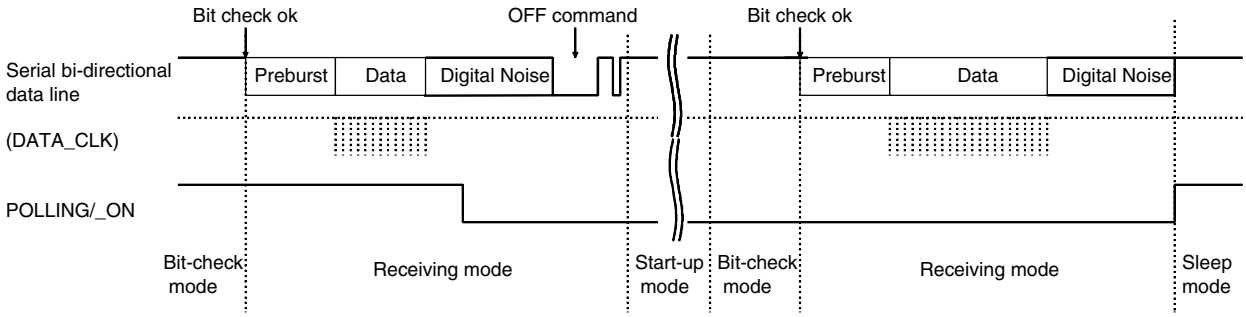


6.5.2 Controlled Noise Suppression by the Microcontroller

The controlled noise suppressionis illustrated in Figure 6-23 on page 24. If the bit Noise_Disable (see Table 6-9 on page 26) in the OPMODE register is set to “0”, digital noise appears at the end of a valid data stream. To suppress the noise, the pin POLLING/_ON must be set to Low. The receiver remains in receiving mode. Then, the OFF command causes the change to the start-up mode. The programmed sleep time (see Table 6-7 on page 26) will not be executed because the level at pin POLLING/_ON is Low, but the bit check is active. The OFF command activates the bit check also if the pin POLLING/_ON is held to Low. The receiver changes back to receiving mode if the bit check was successful. To activate the polling mode at the end of the data transmission, the pin POLLING/_ON must be set to High.

This way of suppressing the noise is recommended if the data stream is not Manchester or Bi-phase coded.

Figure 6-23. Controlled Noise Suppression



6.6 Configuration of the Receiver

The ATA5743 receiver is configured via two 12-bit RAM registers called OPMODE and LIMIT. The registers can be programmed by means of the bi-directional DATA port. If the register contents have changed due to a voltage drop, this condition is indicated by a certain output pattern called reset marker (RM). The receiver must be reprogrammed in that case. After a power-on reset (POR), the registers are set to default mode. If the receiver is operated in default mode, there is no need to program the registers. Table 6-3 on page 25 shows the structure of the registers. As seen in Table 6-1, bit 1 defines if the receiver is set back to polling mode via the OFF command (see section "Receiving Mode" on page 16) or if it is programmed. Bit 2 represents the register address. It selects the appropriate register to be programmed. To get a high programming reliability, bit 15 (Stop bit), at the end of the programming operation, must be set to "0".

Table 6-1. Effect of Bit 1 and Bit 2 on Programming the Registers

Bit 1	Bit 2	Action
1	x	The receiver is set back to polling mode (OFF command)
0	1	The OPMODE register is programmed
0	0	The LIMIT register is programmed

Table 6-2. Effect of Bit 15 on Programming the Register

Bit 15	Action
0	The values will be written into the register (OPMODE or LIMIT)
1	The values will not be written into the register

Table 6-3. Effect of the Configuration Words Within the Registers

Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15
OFF command														
1														
OPMODE register														
0	1	BR_Range		$N_{Bit-check}$		Modu-lation	Sleep					X Sleep	Noise Suppression	0
		Baud1	Baud0	BitChk1	BitChk0	ASK/_FSK	Sleep4	Sleep3	Sleep2	Sleep1	Sleep0	$X_{SleepStd}$	Noise_ Disable	
Default values of bits 3 to 14		0	0	0	1	0	0	0	1	1	0	0	1	
LIMIT register														
0	0	Lim_min						Lim_max						0
		Lim_ min5	Lim_ min4	Lim_ min3	Lim_ min2	Lim_ min1	Lim_ min0	Lim_ max5	Lim_ max4	Lim_ max3	Lim_ max2	Lim_ max1	Lim_max0	
Default values of bits 3 to 14		0	1	0	1	0	1	1	0	1	0	0	1	

Table 6-4 on page 25 to Table 6-11 on page 27 illustrate the effect of the individual configuration words. The default configuration is highlighted for each word.

BR_Range sets the appropriate baud-rate range and simultaneously defines XLim. XLim is used to define the bit-check limits T_{Lim_min} and T_{Lim_max} as shown in Table 6-10 on page 27 and Table 6-11 on page 27.

Table 6-4. Effect of the Configuration Word BR_Range

BR_Range		
Baud1	**Baud0**	**Baud-Rate Range/Extension Factor for Bit-Check Limits (XLim)**
0	0	BR_Range0 (application USA/Europe: BR_Range0 = 1.0 kBaud to 1.8 kBaud) XLim = 8 (default)
0	1	BR_Range1 (application USA/Europe: BR_Range1 = 1.8 kBaud to 3.2 kBaud) XLim = 4
1	0	BR_Range2 (application USA/Europe: BR_Range2 = 3.2 kBaud to 5.6 kBaud) XLim = 2
1	1	BR_Range3 (application USA/Europe: BR_Range3 = 5.6 kBaud to 10 kBaud) XLim = 1

Table 6-5. Effect of the Configuration Word $N_{Bit-check}$

$N_{Bit-check}$		
BitChk1	**BitChk0**	**Number of Bits to be Checked**
0	0	0
0	1	3 (default)
1	0	6
1	1	9