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ATA5745C/ATA5746C

UHF ASK/FSK Receiver

DATASHEET

Features

- Transparent RF receiver ICs for 315MHz (Atmel® ATA5746C) and 433.92MHz (Atmel ATA5745C) with high receiving sensitivity
- Fully integrated PLL with low phase noise VCO, PLL, and loop filter
- High FSK/ASK sensitivity:
  - –105dBm (Atmel ATA5746C, FSK, 9.6Kbits/s, Manchester, BER 10^{-3})
  - –114dBm (Atmel ATA5746C, ASK, 2.4Kbits/s, Manchester, BER 10^{-3})
  - –104dBm (Atmel ATA5745C, FSK, 9.6Kbits/s, Manchester, BER 10^{-3})
  - –113dBm (Atmel ATA5745C, ASK, 2.4Kbits/s, Manchester, BER 10^{-3})
- Supply current: 6.5mA in Active Mode (3V, 25°C, ASK Mode)
- Data rate: 1Kbit/s to 10Kbits/s Manchester ASK, 1Kbit/s to 20Kbits/s Manchester FSK with four programmable bit rate ranges
- Switching between modulation types ASK/FSK and different data rates possible in ≤ 1ms typically, without hardware modification on board to allow different modulation schemes for RKE, TPMS
- Low standby current: 50µA at 3V, 25°C
- ASK/FSK receiver uses a Low-IF architecture with high selectivity, blocking, and Low intermodulation (typical 3-dB blocking 68.0dBC at ±3MHz/74.0dBC at ±20.0MHz, system I1dBCP = –31dBm/system IIP3 = –24dBm)
- Telegram pause up to 52ms supported in ASK Mode
- Wide bandwidth AGC to handle large out-of-band blockers above the system I1dBCP
- 440-kHz IF frequency with 30-dB image rejection and 420-kHz IF bandwidth to support PLL transmitters with standard crystals or SAW-based transmitters
- RSSI (Received Signal Strength Indicator) with output signal dynamic range of 65dB
- Low in-band sensitivity change of typically ±2.0dB within ±160-kHz center frequency change in the complete temperature and supply voltage range
- Sophisticated threshold control and quasi-peak detector circuit in the data slicer
- Fast and stable XTO start-up circuit (> –1.4kΩ worst-case start impedance)
- Clock generation for microcontroller

- ESD protection at all pins (±4kV HBM, ±200V MM, ±500V FCDM)
- Dual supply voltage range: 2.7V to 3.3V or 4.5V to 5.5V
- Temperature range: –40°C to +105°C
- Small 5mm × 5mm QFN24 package

Applications

- Automotive keyless entry and tire pressure monitoring systems
- Alarm, telemetering and energy metering systems

Benefits

- Supports header and blanking periods of protocols common in RKE and TPM systems (up to 52ms in ASK Mode)
- All RF relevant functions are integrated. The single-ended RF input is suited for easy adaptation to λ / 4 or printed-loop antennas
- Allows a low-cost application with only 8 passive components
- Suitable for use in a receiver for joint RKE and TPMS
- Optimal bandwidth maximizes sensitivity while maintaining SAW transmitter compatibility
- Clock output provides an external microcontroller crystal-precision time reference
- Well suited for use with Atmel® PLL transmitter ATA5756/ATA5757

1. General Description

The Atmel® ATA5745C/ATA5746C is a UHF ASK/FSK transparent receiver IC with low power consumption supplied in a small QFN24 package (body 5mm × 5mm, pitch 0.65mm). Atmel ATA5745C is used in the 433MHz to 435MHz band of operation, and Atmel ATA5746C in 313MHz to 317MHz. The IC combines the functionality of remote keyless entry (RKE - typically low bit rate ASK) and tire pressure monitoring (TPM - typically high bit rate FSK) into one receiver under the control of an external microcontroller such as an Atmel ATmega48 (AVR®).

For improved image rejection and selectivity, the IF frequency is fixed to 440kHz. The IF block uses an 8th-order band pass yielding a receive bandwidth of 420kHz. This enables the use of the receiver in both SAW- and PLL-based transmitter systems utilizing various types of data-bit encoding such as pulse width modulation, Manchester modulation, variable pulse modulation, pulse position modulation, and NRZ. Prevailing encryption protocols such as Keeloq® are easily supported due to the receiver's ability to hold the current data slicer threshold for up to 52ms when incoming RF telegrams contain a blanking interval. This feature eliminates erroneous noise from appearing on the demodulated data output pin, and simplifies software decoding algorithms. The decoding of the data stream must be carried out by a connected microcontroller device. Because of the highly integrated design, the only required RF components are for the purpose of receiver antenna matching.

Atmel ATA5745C and Atmel ATA5746C support Manchester bit rates of 1Kbit/s to 10Kbits/s in ASK and 1Kbit/s to 20Kbits/s in FSK mode. The four discrete bit rate passbands are selectable and cover 1.0Kbit/s to 2.5Kbits/s, 2.0Kbits/s to 5.0Kbits/s, 4.0Kbits/s to 10.0Kbits/s, and 8.0Kbits/s to 10.0Kbits/s or 20.0Kbits/s (for ASK or FSK, respectively). The receiver contains an RSSI output to provide an indication of received signal strength and a SENSE input to allow the customer to select a threshold below which the DATA signal is gated off. ASK/FSK and bit rate ranges are selected by the connected microcontroller device via pins ASK_NFSK, BR0, and BR1.

Figure 1-1. System Block Diagram

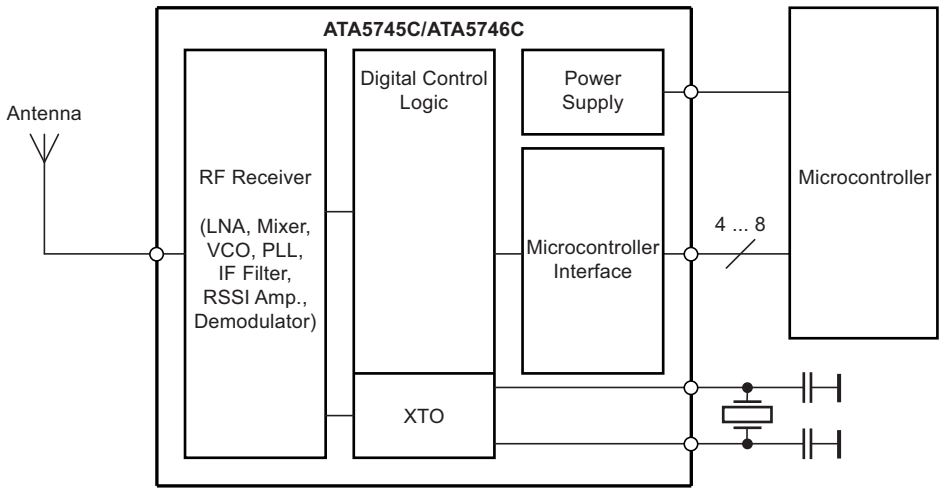


Figure 1-2. Pinning QFN24

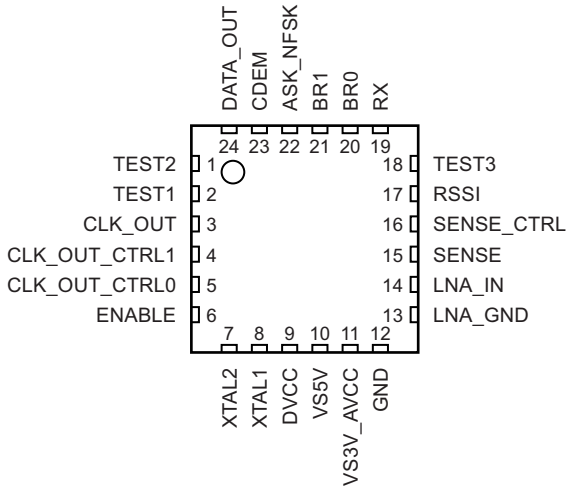
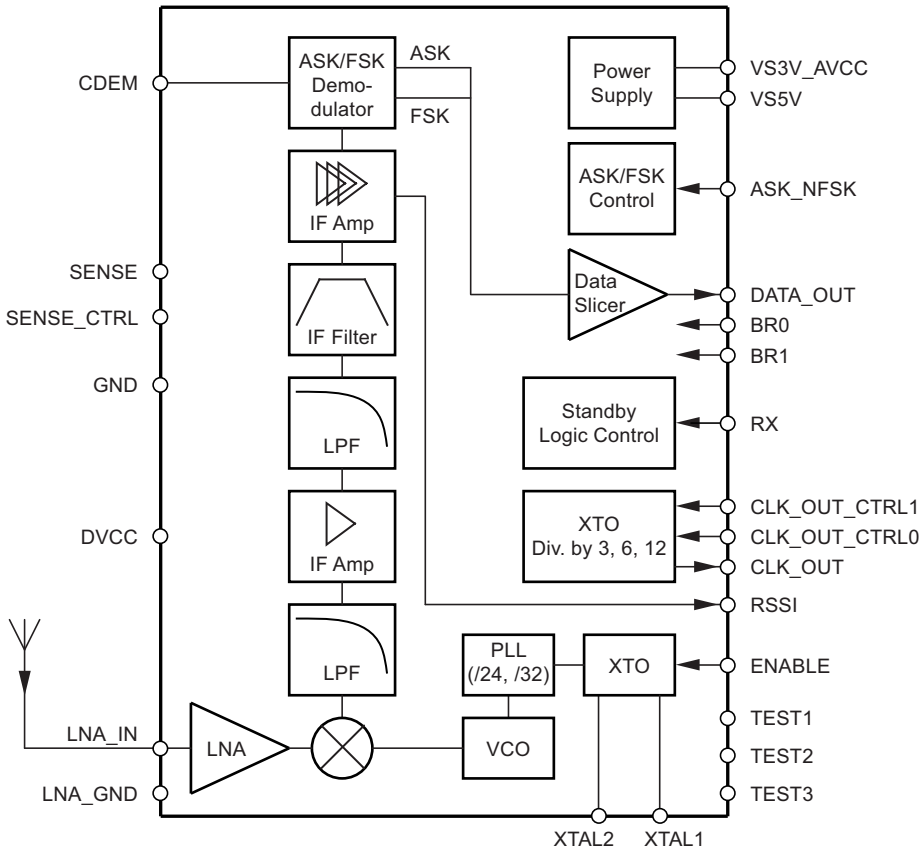


Table 1-1. Pin Description

Pin	Symbol	Function
1	TEST2	Test pin, during operation at GND
2	TEST1	Test pin, during operation at GND
3	CLK_OUT	Output to clock a connected microcontroller
4	CLK_OUT_CTRL1	Input to control CLK_OUT (MSB)
5	CLK_OUT_CTRL0	Input to control CLK_OUT (LSB)
6	ENABLE	Input to enable the XTO
7	XTAL2	Reference crystal
8	XTAL1	Reference crystal
9	DVCC	Digital voltage supply blocking
10	VS5V	Power supply input for voltage range 4.5V to 5.5V
11	VS3V_AVCC	Power supply input for voltage range 2.7V to 3.3V
12	GND	Ground
13	LNA_GND	RF ground
14	LNA_IN	RF input
15	SENSE	Sensitivity control resistor
16	SENSE_CTRL	Sensitivity selection Low: Normal sensitivity, High: Reduced sensitivity
17	RSSI	Output of the RSSI amplifier
18	TEST3	Test pin, during operation at GND
19	RX	Input to activate the receiver
20	BR0	Bit rate selection, LSB
21	BR1	Bit rate selection, MSB
22	ASK_NFSK	FSK/ASK selection Low: FSK, High: ASK
23	CDEM	Capacitor to adjust the lower cut-off frequency data filter
24	DATA_OUT	Data output
	GND	Ground/backplane (exposed die pad)

Figure 1-3. Block Diagram



2. RF Receiver

As seen in Figure 1-3 on page 5, the RF receiver consists of a low-noise amplifier (LNA), a local oscillator, and the signal processing part with mixer, IF filter, IF amplifier with analog RSSI, FSK/ASK demodulator, data filter, and data slicer.

In receive mode, the LNA pre-amplifies the received signal which is converted down to a 440-kHz intermediate frequency (IF), then filtered and amplified before it is fed into an FSK/ASK demodulator, data filter, and data slicer. The received signal strength indicator (RSSI) signal is available at the pin RSSI.

2.1 Low-IF Receiver

The receive path consists of a fully integrated low-IF receiver. It fulfills the sensitivity, blocking, selectivity, supply voltage, and supply current specification needed to design an automotive integrated receiver for RKE and TPM systems. A benefit of the integrated receive filter is that no external components needed.

At 315MHz, the Atmel® ATA5745C receiver (433.92MHz for the Atmel ATA5746C receiver) has a typical system noise figure of 6.0dB (7.0dB), a system I1dBCP of –31dBm (–30dBm), and a system IIP3 of –24dBm (–23dBm). The signal path is linear for out-of-band disturbers up to the I1dBCP and hence there is no AGC or switching of the LNA needed, and a better blocking performance is achieved. This receiver uses an IF (intermediate frequency) of 440kHz, the typical image rejection is 30dB and the typical 3-dB IF filter bandwidth is 420kHz (f_{IF} = 440kHz ± 210kHz, f_{lo_IF} = 230kHz and f_{hi_IF} = 650kHz). The demodulator needs a signal-to-noise ratio of 8.5dB for 10Kbits/s Manchester with ±38kHz frequency deviation in FSK mode, thus, the resulting sensitivity at 315MHz (433.92MHz) is typically –105dBm (–104dBm).

Due to the low phase noise and spurs of the synthesizer together with the 8th-order integrated IF filter, the receiver has a better selectivity and blocking performance than more complex double superhet receivers, without using external components and without numerous spurious receiving frequencies.

A low-IF architecture is also less sensitive to second-order intermodulation (IIP2) than direct conversion receivers where every pulse or amplitude modulated signal (especially the signals from TDMA systems like GSM) demodulates to the receiving signal band at second-order non-linearities.

2.2 Input Matching at LNA_IN

The measured input impedances as well as the values of a parallel equivalent circuit of these impedances can be seen in Table 2-1. The highest sensitivity is achieved with power matching of these impedances to the source impedance.

Table 2-1. Measured Input Impedances of the LNA_IN Pin

f_{RF} [MHz]	Z_{In}(RF_IN) [Ω]	R_{In_p}//C_{In_p} [pF]
315	(72.4 – j298)	1300Ω//1.60
433.92	(55 – j216)	900Ω//1.60

The matching of the LNA input to 50Ω is done using the circuit shown in Figure 2-1 and the values of the matching elements given in Table 2-2. The reflection coefficients were always ≤ –10dB. Note that value changes of C1 and L1 may be necessary to compensate individual board layout parasitics. The measured typical FSK and ASK Manchester-code sensitivities with a bit error rate (BER) of 10^{-3} are shown in Table 2-3 and Table 2-4 on page 7. These measurements were done with wire-wound inductors having quality factors reported in Table 2-2, resulting in estimated matching losses of 0.8dB at 315MHz and 433.92MHz. These losses can be estimated when calculating the parallel equivalent resistance of the inductor with $R_{loss} = 2 \times \pi \times f \times L \times Q_L$ and the matching loss with $10 \log(1+R_{In\_p} / R_{loss})$.

Figure 2-1. Input Matching to 50Ω

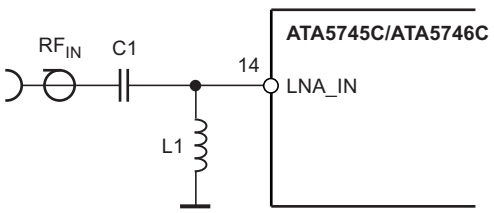


Table 2-2. Input Matching to 50Ω

f_{RF} [MHz]	C_1 [pF]	L_1 [nH]	Q_{L1}
315	2.2	68	20
433.92	2.2	36	15

Table 2-3. Measured Typical Sensitivity FSK, ±38 kHz, Manchester, BER = 10^{-3}

RF Frequency	BR_Range_0 1.0Kbit/s	BR_Range_0 2.5Kbits/s	BR_Range_1 5Kbits/s	BR_Range_2 10Kbits/s	BR_Range_3 10Kbits/s	BR_Range_3 20Kbits/s
315MHz	–108dBm	–108dBm	–107dBm	–105dBm	–104dBm	–104dBm
433.92MHz	–107dBm	–107dBm	–106dBm	–104dBm	–103dBm	–103dBm

Table 2-4. Measured Typical Sensitivity 100% ASK, Manchester, BER = 10^{-3}

RF Frequency	BR_Range_0 1.0Kbit/s	BR_Range_0 2.5Kbits/s	BR_Range_1 5Kbits/s	BR_Range_2 10Kbits/s	BR_Range_3 10Kbits/s
315MHz	–114dBm	–114dBm	–113dBm	–111dBm	–109dBm
433.92MHz	–113dBm	–113dBm	–112dBm	–110dBm	–108dBm

Conditions for the sensitivity measurement:

The given sensitivity values are valid for Manchester-modulated signals. For the sensitivity measurement the distance from edge to edge must be evaluated. As can be seen in Figure 6-1 on page 22, in a Manchester-modulated data stream, the time segments T_{EE} and $2 \times T_{EE}$ occur.

To reach the specified sensitivity for the evaluation of T_{EE} and $2 \times T_{EE}$ in the data stream, the following limits should be used (T_{EE} min, T_{EE} max, $2 \times T_{EE}$ min, $2 \times T_{EE}$ max).

Table 2-5. Limits for Sensitivity Measurements

Bit Rate	T_{EE} Min	T_{EE} Typ	T_{EE} Max	$2 \times T_{EE}$ Min	$2 \times T_{EE}$ Typ	$2 \times T_{EE}$ Max
1.0Kbit/s	260µs	500µs	790µs	800µs	1000µs	1340µs
2.4Kbits/s	110µs	208µs	310µs	320µs	416µs	525µs
5.0Kbits/s	55µs	100µs	155µs	160µs	200µs	260µs
9.6Kbits/s	27µs	52µs	78µs	81µs	104µs	131µs

2.3 Sensitivity Versus Supply Voltage, Temperature and Frequency Offset

To calculate the behavior of a transmission system, it is important to know the reduction of the sensitivity due to several influences. The most important are frequency offset due to crystal oscillator (XTO) and crystal frequency (XTAL) errors, temperature and supply voltage dependency of the noise figure, and IF-filter bandwidth of the receiver. Figure 2-2 and Figure 2-3 on page 8 show the typical sensitivity at 315MHz, ASK, 2.4Kbits/s and 9.6Kbits/s, Manchester, Figure 2-4 and Figure 2-5 on page 9 show a typical sensitivity at 315MHz, FSK, 2.4Kbits/s and 9.6Kbits/s, ±38kHz, Manchester versus the frequency offset between transmitter and receiver at T_{amb} = –40°C, +25°C, and +105°C and supply voltage VS = VS3V_AVCC = VS5V = 2.7V, 3.0V and 3.3V.

Figure 2-2. Measured Sensitivity (315MHz, ASK, 2.4Kbits/s, Manchester) Versus Frequency Offset

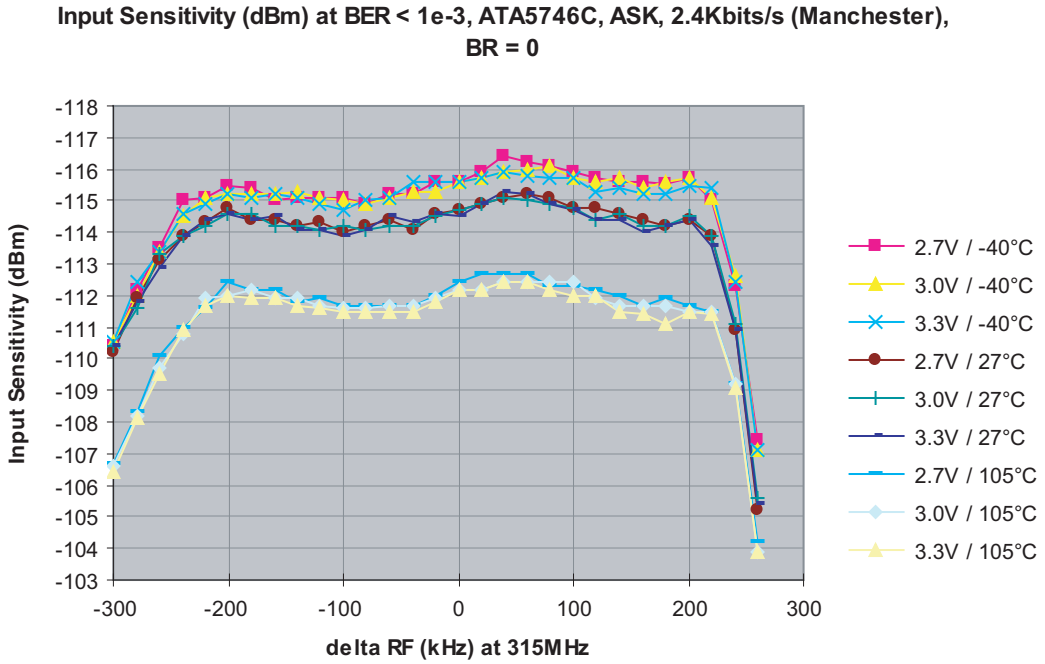


Figure 2-3. Measured Sensitivity (315MHz, ASK, 9.6Kbits/s, Manchester) Versus Frequency Offset

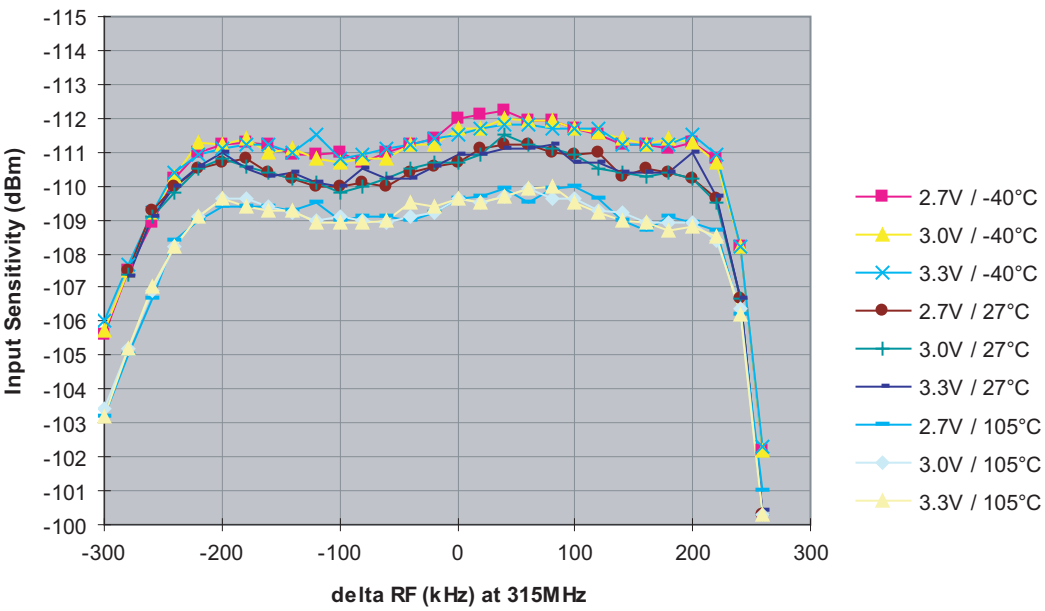


Figure 2-4. Measured Sensitivity (315MHz, FSK, 2.4Kbits/s, ±38kHz, Manchester) Versus Frequency Offset

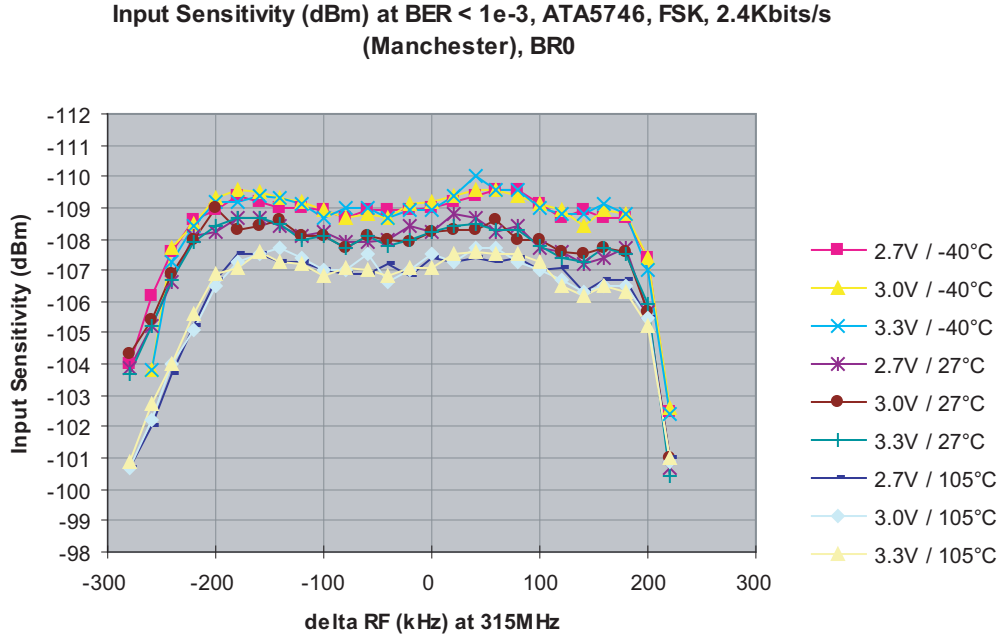
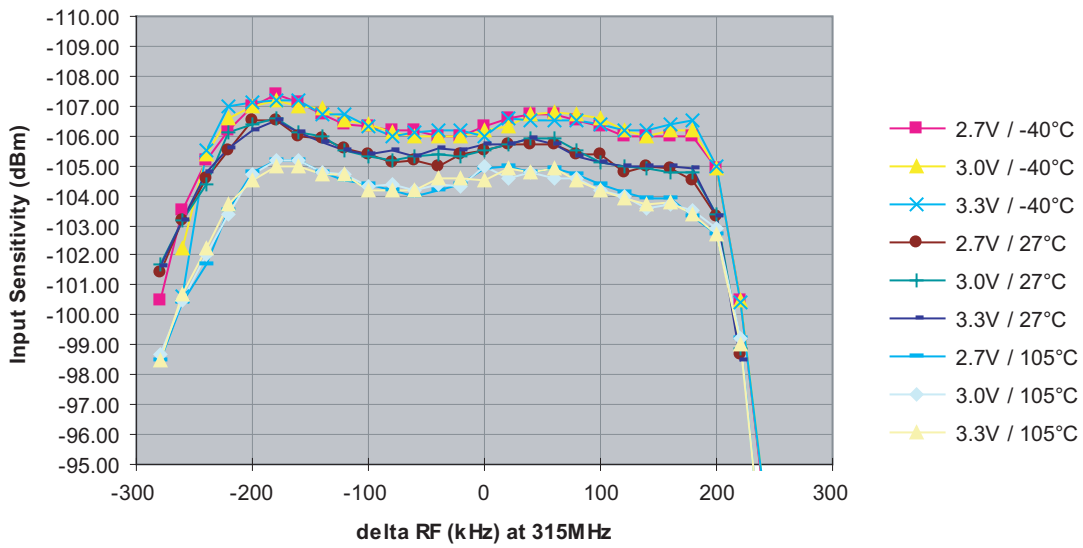


Figure 2-5. Measured Sensitivity (315MHz, FSK, 9.6Kbits/s, ±38kHz, Manchester) Versus Frequency Offset



As can be seen in Figure 2-5 on page 9, the supply voltage has almost no influence. The temperature has an influence of about ±1.0dB, and a frequency offset of ±160kHz also influences by about ±1dB. All these influences, combined with the sensitivity of a typical IC (–105dB), are then within a range of –103.0dBm and –107.0dBm over temperature, supply voltage, and frequency offset. The integrated IF filter has an additional production tolerance of ±10kHz, hence, a frequency offset between the receiver and the transmitter of ±160kHz can be accepted for XTAL and XTO tolerances.

Note: For the demodulator used in the Atmel ATA5745C/ATA5746C, the tolerable frequency offset does not change with the data frequency. Hence, the value of ±160kHz is valid for 1Kbit/s to 10Kbits/s.

This small sensitivity change over supply voltage, frequency offset, and temperature is very unusual in such a receiver. It is achieved by an internal, very fast, and automatic frequency correction in the FSK demodulator after the IF filter, which leads to a higher system margin. This frequency correction tracks the input frequency very quickly. If, however, the input frequency makes a larger step (for example, if the system changes between different communication partners), the receiver has to be restarted. This can be done by switching back to Standby mode and then again to Active mode (pin RX 1 ⟶ 0 ⟶ 1) or by generating a positive pulse on pin ASK_NFSK (0 ⟶ 1 ⟶ 0).

2.4 Frequency Accuracy of the Crystals in a Combined RKE and TPM System

In a tire pressure measurement system working at 315MHz and using an Atmel® ATA5756 as transmitter and an Atmel ATA5746C is receiver, the higher frequency tolerances and the tolerance of the frequency deviation of the transmitter has to be considered.

In the TPM transmitter, the crystal has a frequency error over temperature –40°C to 125°C, aging, and tolerance of ±80ppm (±25.2kHz at 315MHz). The tolerances of the XTO, the capacitors used for FSK modulation, and the stray capacitances cause an additional frequency error of ±30 ppm (±9.45kHz at 315MHz). The frequency deviation of such a transmitter varies between ±16kHz and ±24kHz, since a higher frequency deviation is equivalent to a frequency error this has to be considered as an additional
±24kHz – ±19.5kHz = ±4.5kHz frequency tolerance (19.5kHz is constant). All tolerances added, these transmitters have a worst-case frequency offset of ±39.15kHz.

For the receiver in the car, a tolerance of ±160kHz – ±39.15kHz = ±120.85kHz (±383.6ppm) remains. The needed frequency stability of the crystals over temperature and aging is ±383.6ppm – ±5ppm = ±378.6ppm. The aging of such a crystal is ±10ppm, leaving a reasonable ±368.6 ppm for the temperature dependency of the crystal frequency in the car.

Since the receiver in the car is able to receive these TPM transmitter signals with high frequency offsets, the component specification in the key can be largely relaxed.

This system calculation is based on worst-case tolerances of all the components; this leads in practice to a system with margin.

For a 433.92MHz TPM system using Atmel ATA5757 as transmitter and Atmel ATA5745C as receiver, the same calculation must be done, but since the RF frequency is higher, every ppm of crystal tolerances results in higher frequency offset and either the system must have lower tolerances or a lower margin at this frequency.

2.5 RX Supply Current Versus Temperature and Supply Voltage

Table 2-7 shows the typical supply current of the receiver in Active mode versus supply voltage and temperature with VS = VS3V_AVCC = VS5V.

Table 2-6. Measured Current in Active Mode ASK

VS = VS3V_AVCC = VS5V	2.7V	3.0V	3.3V
T_{amb} = –40°C	5.4mA	5.5mA	5.6mA
T_{amb} = 25°C	6.4mA	6.5mA	6.6mA
T_{amb} = 105°C	7.4mA	7.5mA	7.6mA

Table 2-7. Measured Current in Active Mode FSK

VS = VS3V_AVCC = VS5V	2.7V	3.0V	3.3V
T_{amb} = –40°C	5.6mA	5.7mA	5.8mA
T_{amb} = 25°C	6.6mA	6.7mA	6.8mA
T_{amb} = 105°C	7.6mA	7.7mA	7.8mA

2.6 Blocking, Selectivity

As can be seen in Figure 2-6 on page 11, and Figure 2-7 and Figure 2-8 on page 12, the receiver can receive signals 3dB higher than the sensitivity level in the presence of large blockers of –34.5dBm or –28dBm with small frequency offsets of ±3MHz or ±20MHz.

Figure 2-6, and Figure 2-7 on page 11 show the narrow-band blocking, and Figure 2-8 on page 12 shows the wide-band blocking characteristic. The measurements were done with a useful signal of 315MHz, FSK, 10Kbits/s, ±38kHz, Manchester, BR_Range2 with a level of –105dBm + 3dB = –102dBm, which is 3dB above the sensitivity level. The figures show how much larger than –102dBm a continuous wave signal can be, until the BER is higher than 10^{-3}. The measurements were done at the 50Ω input shown in Figure 2-1 on page 6. At 3MHz, for example, the blocker can be 67.5dBC higher than –102dBm, or –102dBm + 67.5dBC = –34.5dBm.

Figure 2-6. Close-in 3-dB Blocking Characteristic and Image Response at 315MHz

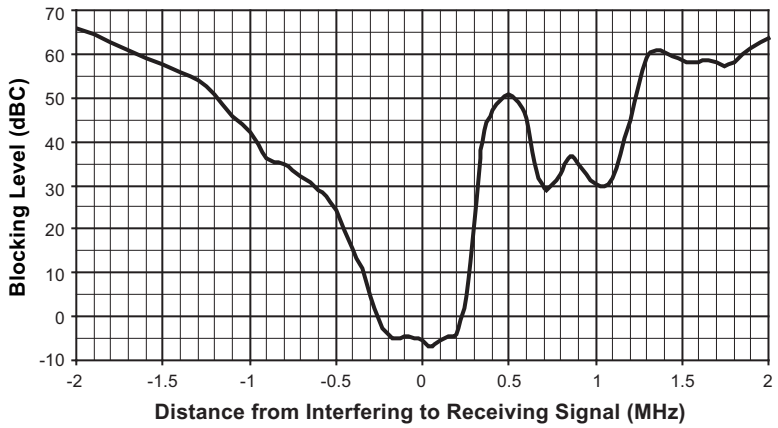


Figure 2-7. Narrow-band 3-dB Blocking Characteristic at 315MHz

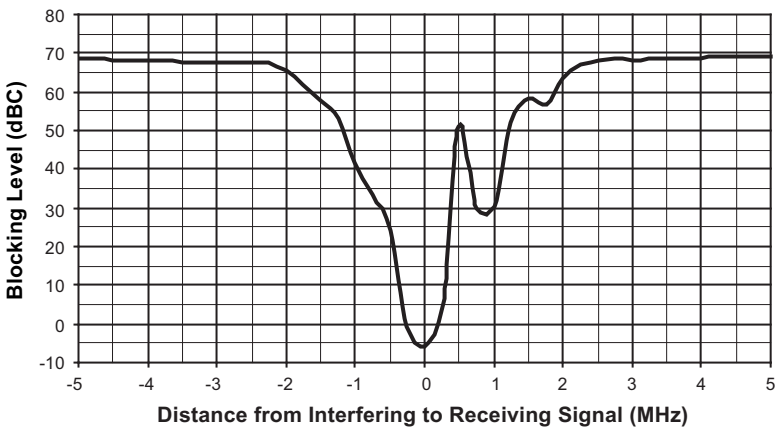


Figure 2-8. Wide-band 3-dB Blocking Characteristic at 315MHz

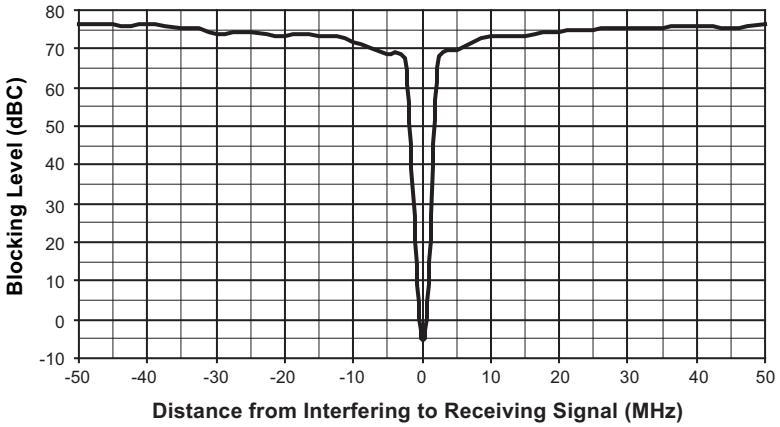


Table 2-8 shows the blocking performance measured relative to –102dBm for some frequencies. Note that sometimes the blocking is measured relative to the sensitivity level 104dBm (denoted dBS), instead of the carrier –102dBm (denoted dBC)

Table 2-8. Blocking 3 dB Above Sensitivity Level With BER < 10^{-3}

Frequency Offset	Blocking Level	Blocking
+1.5MHz	–44.5dBm	57.5dBC, 60.5dBS
–1.5MHz	–44.5dBm	57.5dBC, 60.5dBS
+2MHz	–39.0dBm	63dBC, 66dBS
–2MHz	–36.0dBm	66dBC, 69dBS
+3MHz	–34.5dBm	67.5dBC, 70.5dBS
–3MHz	–34.5dBm	67.5dBC, 70.5dBS
+20MHz	–28.0dBm	74dBC, 77dBS
–20MHz	–28.0dBm	74dBC, 77dBS

The Atmel® ATA5745C/ATA5746C can also receive FSK and ASK modulated signals if they are much higher than the I1dBCP. It can typically receive useful signals at –10dBm. This is often referred to as the nonlinear dynamic range (that is, the maximum to minimum receiving signal), and is 95dB for 10Kbits/s Manchester (FSK). This value is useful if the transmitter and receiver are very close to each other.

2.7 In-band Disturbers, Data Filter, Quasi-peak Detector, Data Slicer

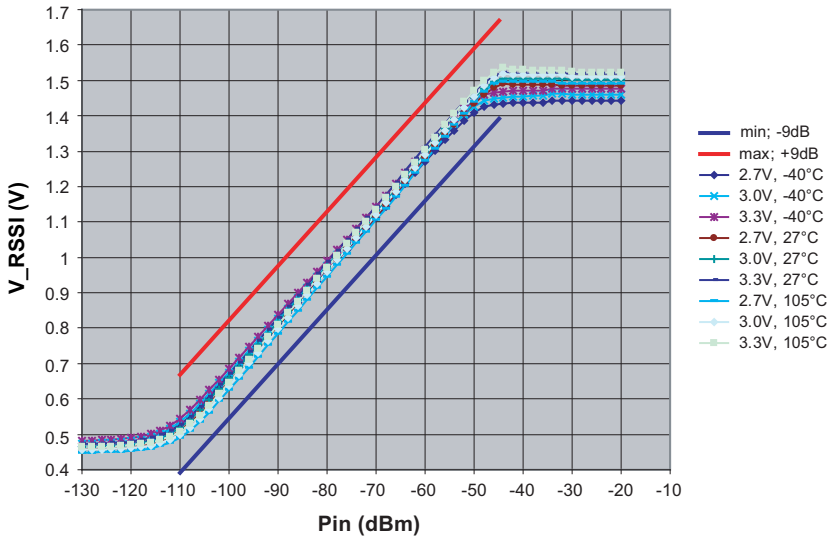
If a disturbing signal falls into the received band, or if a blocker is not a continuous wave, the performance of a receiver strongly depends on the circuits after the IF filter. Hence, the demodulator, data filter, and data slicer are important.

The data filter of the Atmel ATA5745C/ATA5746C functions also as a quasi-peak detector. This results in a good suppression of above mentioned disturbers and exhibits a good carrier-to-noise performance. The required useful-signal-to-disturbing-signal ratio, at a BER of $10^{-3,}$ is less than 14dB in ASK mode and less than 3dB (BR_Range_0 to BR_Range_2) and 6dB (BR_Range_3) in FSK mode. Due to the many different possible waveforms, these numbers are measured for the signal, as well as for disturbers, with peak amplitude values. Note that these values are worst-case values and are valid for any type of modulation and modulating frequency of the disturbing signal, as well as for the receiving signal. For many combinations, lower carrier-to-disturbing-signal ratios are needed.

2.8 RSSI Output

The output voltage of the pin RSSI is an analog voltage, proportional to the input power level. Using the RSSI output signal, the signal strength of different transmitters can be distinguished. The usable dynamic range of the RSSI amplifier is 65 dB, the input power range P(RF_{IN}) is –110dBm to –45dBm, and the gain is 15mV/dB. Figure 2-9 shows the RSSI characteristic of a typical device at 315MHz with VS3V_AVCC = VS5V = 2.7V to 3.3V and T_{amb} = –40°C to +105°C with a matched input as shown in Table 2-2 and Figure 2-1 on page 6. At 433.92MHz, 1dB more signal level is needed for the same RSSI results.

Figure 2-9. Typical RSSI Characteristic at 315MHz Versus Temperature and Supply Voltage



As can be seen in Figure 2-9 on page 13, for single devices there is a variance over temperature and supply voltage range of ±3dB. The total variance over production, temperature, and supply voltage range is ±9dB.

2.9 Frequency Synthesizer

The LO generates the carrier frequency for the mixer via a PLL synthesizer. The XTO (crystal oscillator) generates the reference frequency f_{XTO}. The VCO (voltage-controlled oscillator) generates the drive voltage frequency f_{LO} for the mixer. f_{LO} is divided by the factor 24 (Atmel® ATA5746C) or 32 (Atmel ATA5745C). The divided frequency is compared to f_{XTO} by the phase frequency detector. The current output of the phase frequency detector is connected to the fully integrated loop filter, and thereby generates the control voltage for the VCO. By means of that configuration, the VCO is controlled in a way, such that f_{LO} / 24 (f_{LO} / 32) is equal to f_{XTO}. If f_{LO} is determined, f_{XTO} can be calculated using the following formula: $f_{XTO} = f_{LO} / 24$ ($f_{XTO} = f_{LO} / 32$). The synthesizer has a phase noise of –130dBC/Hz at 3MHz and spurs of –75dBC.

Care must be taken with the harmonics of the CLK output signal, as well as with the harmonics produced by a microprocessor clocked using the signal, as these harmonics can disturb the reception of signals.

3. XTO

The XTO is an amplitude-regulated Pierce oscillator type with external load capacitances (2 × 16pF). Due to additional internal and board parasitics (C_P) of approximately 2pF on each side, the load capacitance amounts to 2 × 18pF (9pF total).

The XTO oscillation frequency f_{XTO} is the reference frequency for the integer-N synthesizer. When designing the system in terms of receiving and transmitting frequency offset, the accuracy of the crystal and XTO have to be considered.

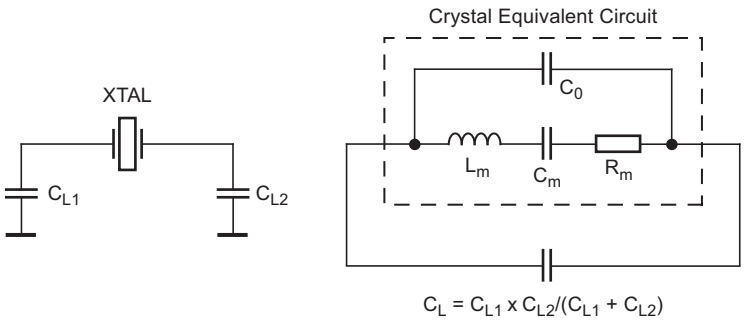
The XTO's additional pulling (including the R_M tolerance) is only ±5ppm. The XTAL versus temperature, aging, and tolerances is then the main source of frequency error in the local oscillator.

The XTO frequency depends on XTAL properties and the load capacitances $C_{L1,2}$ at pin XTAL1 and XTAL2. The pulling (p) of f_{XTO} from the nominal f_{XTAL} is calculated using the following formula:

$$p = \frac{C_m}{2} \times \frac{C_{LN} - C_L}{(C_O + C_{LN}) \times (C_O + C_L)} \times 10^{-6} \text{ppm}$$

C_m, the crystal's motional capacitance; C_0, the shunt capacitance; and C_{LN}, the nominal load capacitance of the XTAL, are found in the datasheet. C_L is the total actual load capacitance of the crystal in the circuit, and consists of C_{L1} and C_{L2} connected in series.

Figure 3-1. Crystal Equivalent Circuit



With $C_m \leq$ 10fF, $C_0 \geq$ 1.0pF, C_{LN} = 9pF and $C_{L1,2}$ = 16pF ±1%, the pulling amounts to P ≤ ±1ppm.

The C_0 of the XTAL has to be lower than C_{Lmin} / 2 = 7.9pF for a Pierce oscillator type in order to not enter the steep region of pulling versus load capacitance where there is risk of an unstable oscillation.

To ensure proper start-up behavior, the small signal gain and the negative resistance provided by this XTO at start is very large. For example, oscillation starts up even in the worst case with a crystal series resistance of 1.5kΩ at $C_0 \leq$ 2.2pF with this XTO. The negative resistance is approximately given by

$$\text{Re}\{\text{Zxtocore}\} = \text{Re}\left\{\frac{Z_1 \times Z_3 + Z_2 \times Z_3 + Z_1 \times Z_3 \times gm}{Z_1 + Z_2 + Z_3 + Z_1 \times Z_2 \times gm}\right\}$$

with Z_1 and Z_2 as complex impedances at pins XTAL1 and XTAL2, hence
$Z_1 = -j / (2 \times p \times f_{XTO} \times C_{L1}) + 5\Omega$ and $Z_2 = -j / (2 \times p \times f_{XTO} \times C_{L2}) + 5\Omega$.
Z_3 consists of crystal C_0 in parallel with an internal 110-kΩ resistor, hence
$Z_3 = -j / (2 \times p \times f_{XTO} \times C_0) / 110k\Omega$, gm is the internal transconductance between XTAL1 and XTAL2, with typically 20mS at 25°C.

With f_{XTO} = 13.5MHz, gm = 20mS, C_L = 9pF, and C_0 = 2.2pF, this results in a negative resistance of about 2kΩ. The worst case for technology, supply voltage, and temperature variations is then always higher than 1.4kΩ for $C_0 \leq$ 2.2pF.

Due to the large gain at start, the XTO is able to meet a very low start-up time. The oscillation start-up time can be estimated with the time constant τ.

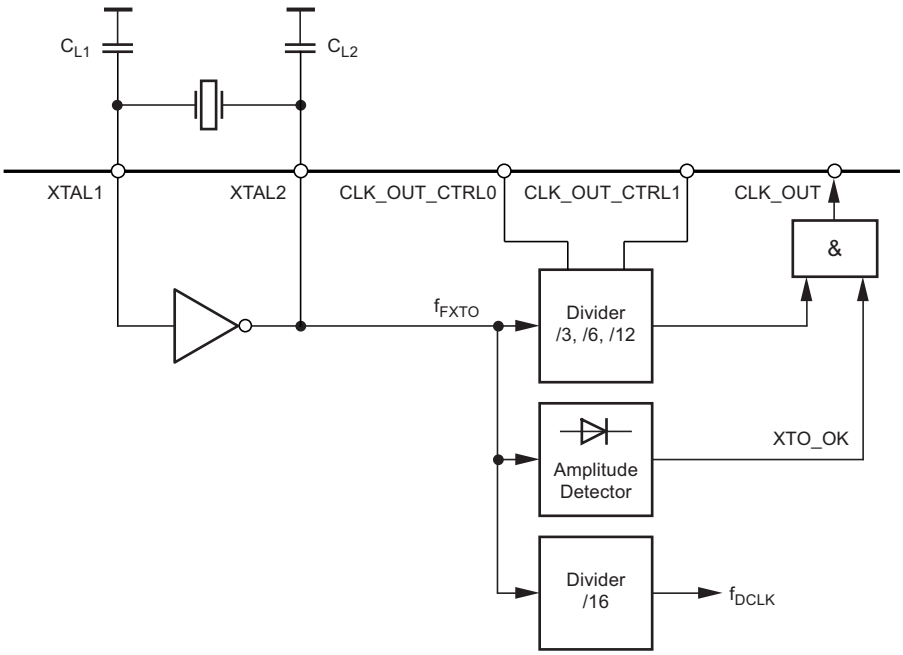
$$\tau = \frac{2}{4 \times \pi^2 \times f_{XTAL}^2 \times C_m \times (\text{Re}(Z_{xtocore}) + R_m)}$$

After 10τ to 20τ, an amplitude detector detects the oscillation amplitude and sets XTO_OK to High if the amplitude is large enough; this activates the CLK_OUT output if it is enabled via the pins CLK_OUT_CTRL0 and CLK_OUT_CTRL1. Note that the necessary conditions of the DVCC voltage also have to be fulfilled.

It is recommended to use a crystal with C_m = 3.0fF to 10fF, C_{LN} = 9pF, R_m < 120Ω and C_0 = 1.0pF to 2.2pF.

Lower values of C_m can be used, slightly increasing the start-up time. Lower values of C_0 or higher values of C_m (up to 15fF) can also be used, with only little influence on pulling.

Figure 3-2. XTO Block Diagram



The relationship between f_{XTO} and the f_{RF} is shown in Table 3-1.

Table 3-1. Calculation of f_{RF}

Frequency [MHz]	f_{XTO} [MHz]	f_{RF}
433.92 (Atmel ATA5745C)	13.57375	f_{XTO} x 32 – 440kHz
315.0 (Atmel ATA5746C)	13.1433	f_{XTO} x 24 – 440kHz

Attention must be paid to the harmonics of the CLK_OUT output signal f_{CLK_OUT} as well as to the harmonics produced by an microprocessor clocked with it, since these harmonics can disturb the reception of signals if they get to the RF input. If the CLK_OUT signal is used, it must be carefully laid out on the application PCB. The supply voltage of the microcontroller must also be carefully blocked.

3.1 Pin CLK_OUT

Pin CLK_OUT is an output to clock a connected microcontroller. The clock is available in Standby and Active modes. The frequency f_{CLK_OUT} can be adjusted via the pins CLK_OUT_CTRL0 and CLK_OUT_CTRL1, and is calculated as follows:

Table 3-2. Setting of f_{CLK_OUT}

CLK_OUT_CTRL1	CLK_OUT_CTRL0	Function
0	0	Clock on pin CLK_OUT is switched off (Low level on pin CLK_OUT)
0	1	$f_{CLK\_OUT} = f_{XTO} / 3$
1	0	$f_{CLK\_OUT} = f_{XTO} / 6$
1	1	$f_{CLK\_OUT} = f_{XTO} / 12$

The signal at CLK_OUT output has a nominal 50% duty cycle. To save current, it is recommended that CLK_OUT be switched off during Standby mode.

3.2 Basic Clock Cycle of the Digital Circuitry

The complete timing of the digital circuitry is derived from one clock. As seen in Figure 3-2 on page 15, this clock cycle, T_{DCLK}, is derived from the crystal oscillator (XTO) in combination with a divider.

$$f_{DCLK} = \frac{f_{XTO}}{16}$$

T_{DCLK} controls the following application relevant parameters:

- Debouncing of the data signal stream
- Start-up time of the RX signal path

The start-up time and the debounce characteristic depend on the selected bit rate range (BR_Range) which is defined by pins BR0 and BR1. The clock cycle T_{XDCLK} is defined by the following formulas for further reference:

BR_Range ⇒

BR_Range 0: $T_{XDCLK} = 8 \times T_{DCLK}$
BR_Range 1: $T_{XDCLK} = 4 \times T_{DCLK}$
BR_Range 2: $T_{XDCLK} = 2 \times T_{DCLK}$
BR_Range 3: $T_{XDCLK} = 1 \times T_{DCLK}$

4. Sensitivity Reduction

The output voltage of the RSSI amplifier is internally compared to a threshold voltage V_{Th_red}. V_{Th_red} is determined by the value of the external resistor R_{Sense}. R_{Sense} is connected between the pins SENSE and VS3V_AVCC (see Figure 10-1 on page 26). The output of the comparator is fed into the digital control logic. By this means, it is possible to operate the receiver at a lower sensitivity.

If the level on input pin SENSE_CTRL is low, the receiver operates at full sensitivity.

If the level on input pin SENSE_CTRL is high, the receiver operates at a lower sensitivity. The reduced sensitivity is defined by the value of R_{Sense}, the maximum sensitivity by the signal-to-noise ratio of the LNA input. The reduced sensitivity depends on the signal strength at the output of the RSSI amplifier.

Since different RF input networks may exhibit slightly different values for the LNA gain, the sensitivity values given in the electrical characteristics refer to a specific input matching. This matching is illustrated in Figure 2-1 on page 6 and exhibits the best possible sensitivity.

If the sensitivity reduction feature is not used, pin SENSE can be left open, pin SENSE_CTRL must be set to GND.

To operate with reduced sensitivity, pin SENSE_CTRL must be set to high before the RX signal path will be enabled by setting pin RX to high (see Figure 4-1 on page 17). As long as the RSSI level is lower than V_{Th_red} (defined by the external resistor R_{Sense}) no data stream is available on pin DATA_OUT (low level on pin DATA_OUT). An internal RS flip-flop will be set to high the first time the RSSI voltage crosses V_{Th_red}, and from then on the data stream will be available on pin DATA_OUT. From then on the receiver also works with full sensitivity. This makes sure that a telegram will not be interrupted if the RSSI level varies during the transmission. The RS flip-flop can be set back, and thus the receiver switched back to reduced sensitivity, by generating a positive pulse on pin ASK_NFSK (see Figure 4-2 on page 18). In FSK mode, operating with reduced sensitivity follows the same way.

Figure 4-1. Reduced Sensitivity Active

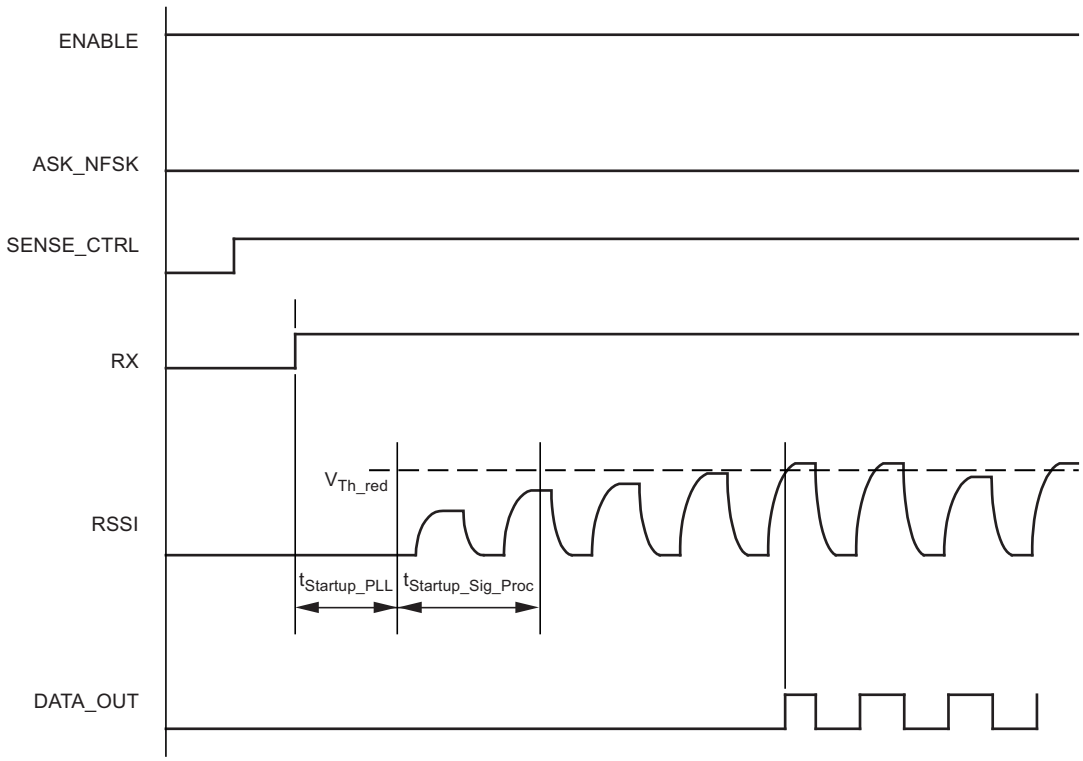
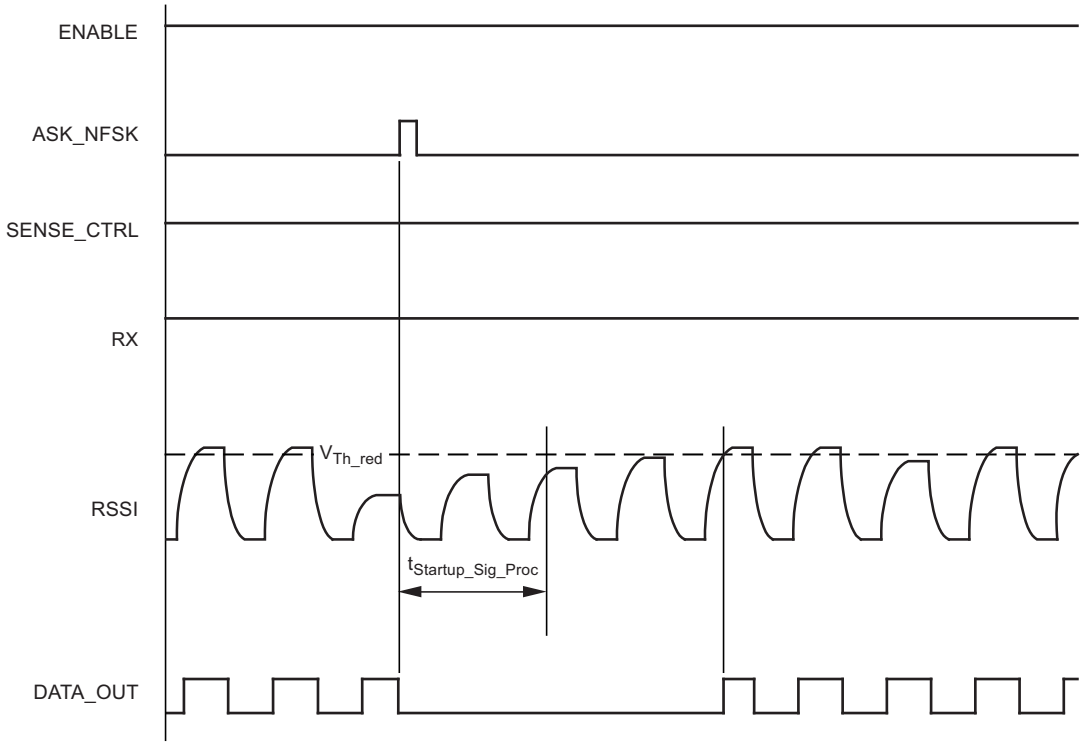
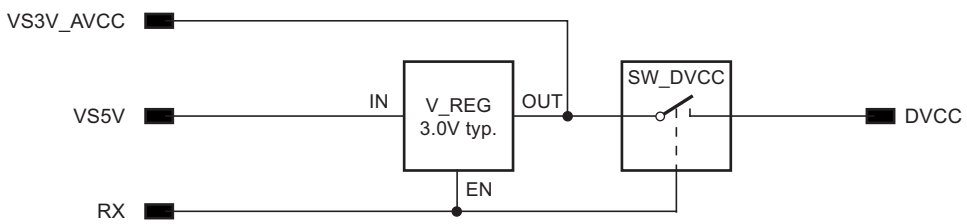


Figure 4-2. Restart Reduced Sensitivity



5. Power Supply

Figure 5-1. Power Supply



The supply voltage range of the Atmel® ATA5745C/ATA5746C is 2.7V to 3.3V or 4.5V to 5.5V.

Pin VS3V_AVCC is the supply voltage input for the range 2.7V to 3.3V, and is used in battery applications using a single lithium 3V cell. Pin VS5V is the voltage input for the range 4.5V to 5.5V (car applications) in this case the voltage regulator V_REG regulates VS3V_AVCC to typically 3.0V. If the voltage regulator is active, a blocking capacitor of 2.2µF has to be connected to VS3V_AVCC (see Figure 10-1 on page 26).

DVCC is the internal operating voltage of the digital control logic and is fed via the switch SW_DVCC by VS3V_AVCC. DVCC must be blocked on pin DVCC with 68nF (see Figure 9-1 on page 25 and Figure 10-1 on page 26).

Pin RX is the input to activate the RX signal processing and set the receiver to Active mode.

5.1 OFF Mode

A low level on pin RX and ENABLE will set the receiver to OFF mode (low power mode). In this mode, the crystal oscillator is shut down and no clock is available on pin CLK_OUT. The receiver is not sensitive to a transmitter signal in this mode.

Table 5-1. Standby Mode

RX	ENABLE	Function
0	0	OFF mode

5.2 Standby Mode

The receiver activates the Standby mode if pin ENABLE is set to “1”.

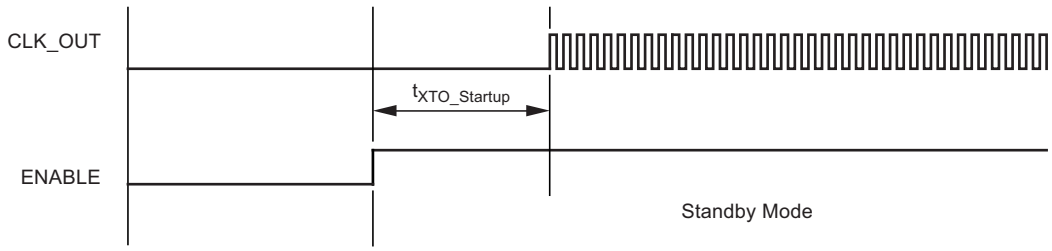
In Standby mode, the XTO is running and the clock on pin CLK_OUT is available after the start-up time of the XTO has elapsed (dependent on pin CLK_OUT_CTRL0 and CLK_OUT_CTRL1). During Standby mode, the receiver is not sensitive to a transmitter signal.

In Standby mode, the RX signal path is disabled and the power consumption $I_{Standby}$ is typically 50µA (CLK_OUT output off, VS3V_AVCC = VS5V = 3V). The exact value of this current is strongly dependent on the application and the exact operation mode, therefore check the section “Electrical Characteristics: General” on page 27 for the appropriate application case.

Table 5-2. Standby Mode

RX	ENABLE	Function
0	1	Standby mode

Figure 5-2. Standby Mode (CLK_OUT_CTRL0 or CLK_OUT_CTRL1 = 1)



5.3 Active Mode

The Active mode is enabled by setting the level on pin RX to high. In Active mode, the RX signal path is enabled and if a valid signal is present it will be transferred to the connected microcontroller.

Table 5-3. Active Mode

RX	ENABLE	Function
1	1	Active mode

During $T_{Startup\_PLL}$ the PLL is enabled and starts up. If the PLL is locked, the signal processing circuit starts up ($T_{Startup\_Sig\_Proc}$). After the start-up time, all circuits are in stable condition and ready to receive. The duration of the start-up sequence depends on the selected bit rate range.

Figure 5-3. Active Mode

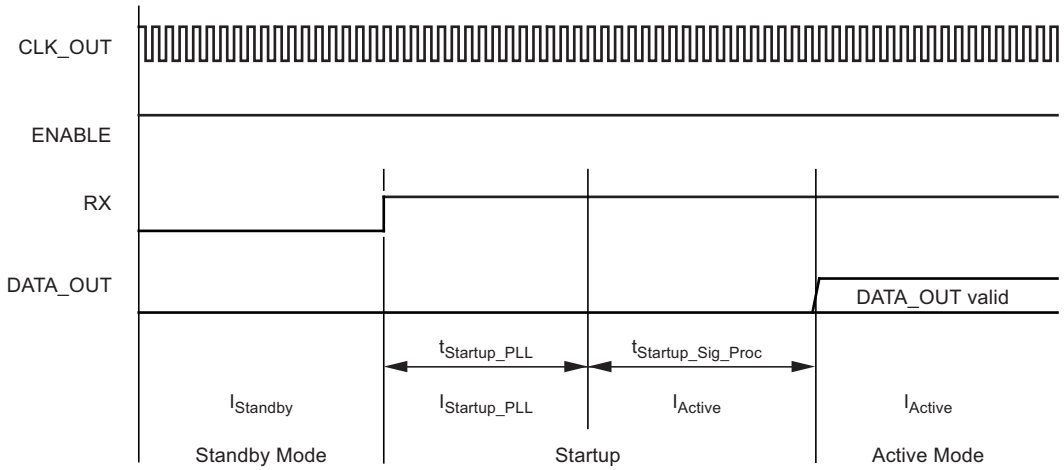


Table 5-4. Start-up Time

BR1	BR0	Atmel ATA5745C (433.92MHz)		Atmel ATA5746C (315MHz)	
		$T_{Startup\_PLL}$	$T_{Startup\_Sig\_Proc}$	$T_{Startup\_PLL}$	$T_{Startup\_Sig\_Proc}$
0	0	261µs	1096µs	269µs	1132µs
0	1		644µs		665µs
1	0		417µs		431µs
1	1		304µs		324µs

Table 5-5. Modulation Scheme

ASK_NFSK	RF_{IN} at Pin LNA_IN	Level at Pin DATA_OUT
0	f_{FSK_H}	1
	f_{FSK_L}	0
1	f_{ASK} on	1
	f_{ASK} off	0

6. Bit Rate Ranges

Configuration of the bit rate ranges is carried out via the two pins BR0 and BR1. The microcontroller uses these two interface lines to set the corner frequencies of the band-pass data filter. Switching the bit rate ranges while the RF front end is in Active mode can be done on the fly and will not take longer than 100 µs if done while remaining in either ASK or FSK mode. If the modulation scheme is changed at the same time, the switching time is ($T_{Startup\_Sig\_Proc}$, see Figure 7-1 on page 23). Each BR_Range is defined by a minimum edge-to-edge time. To maintain full sensitivity of the receiver, edge-to-edge transition times of incoming data should not be less than the minimum for the selected BR_Range.

Table 6-1. BR Ranges ASK

BR1	BR0	BR_Range	Recommended Bit Rate (Manchester)(2)	Minimum Edge-to-edge Time Period T_{EE} of the Data Signal(3)	Edge-to-edge Time Period T_{EE} of the Data Signal During the Start-up Period(4)
0	0	BR_Range0	1.0Kbit/s to 2.5Kbits/s	200µs	200µs to 500µs
0	1	BR_Range1	2.0Kbits/s to 5.0Kbits/s	100µs	100µs to 250µs
1	0	BR_Range2	4.0Kbits/s to 10.0Kbits/s	50µs	50µs to 125µs
1	1	BR_Range3	8.0Kbits/s to 10.0Kbits/s	50µs	50µs to 62.5µs

Table 6-2. BR Ranges FSK

BR1	BR0	BR_Range	Recommended Bit Rate (Manchester)(2)	Minimum Edge-to-edge Time Period T_{EE} of the Data Signal(3)	Edge-to-edge Time Period T_{EE} of the Data Signal During the Start-up Period(4)
0	0	BR_Range0	1.0Kbit/s to 2.5Kbits/s	200µs	200µs to 500µs
0	1	BR_Range1	2.0Kbits/s to 5.0Kbits/s	100µs	100µs to 250µs
1	0	BR_Range2	4.0Kbits/s to 10.0Kbits/s	50µs	50µs to 125µs
1	1	BR_Range3	8.0Kbits/s to 20.0Kbits/s	25µs	25µs to 62.5µs

Notes:
1. If during the start-up period ($T_{Startup\_PLL}$ + $T_{Startup\_Sig\_Proc}$) there is no RF signal, the data filter settles to the noise floor, leading to noise on pin DATA_OUT.
2. As can be seen, a bit stream of, for example, 2.5Kbits/s can be received in BR_Range0 and BR_Range1 (overlapping BR_Ranges). To get the full sensitivity, always use the lowest possible BR_Range (here, BR_Range0). The advantage in the next higher BR_Range (BR_Range1) is the shorter start-up period, meaning lower current consumption during Polling mode. Thus, it is a decision between sensitivity and current consumption.
3. The receiver is also capable of receiving non-Manchester-modulated signals, such as PWM, PPM, VPWM, NRZ. In ASK mode, the header and blanking periods occurring in Keeloq-like protocols (up to 52ms) are supported.
4. To ensure an accurate settling of the data filter during the start-up period ($T_{Startup\_PLL}$ + $T_{Startup\_Sig\_Proc}$), the edge-to-edge time T_{EE} of the data signal (preamble) must be inside the given limits during this period.

Figure 6-1. Examples of Supported Modulation Formats

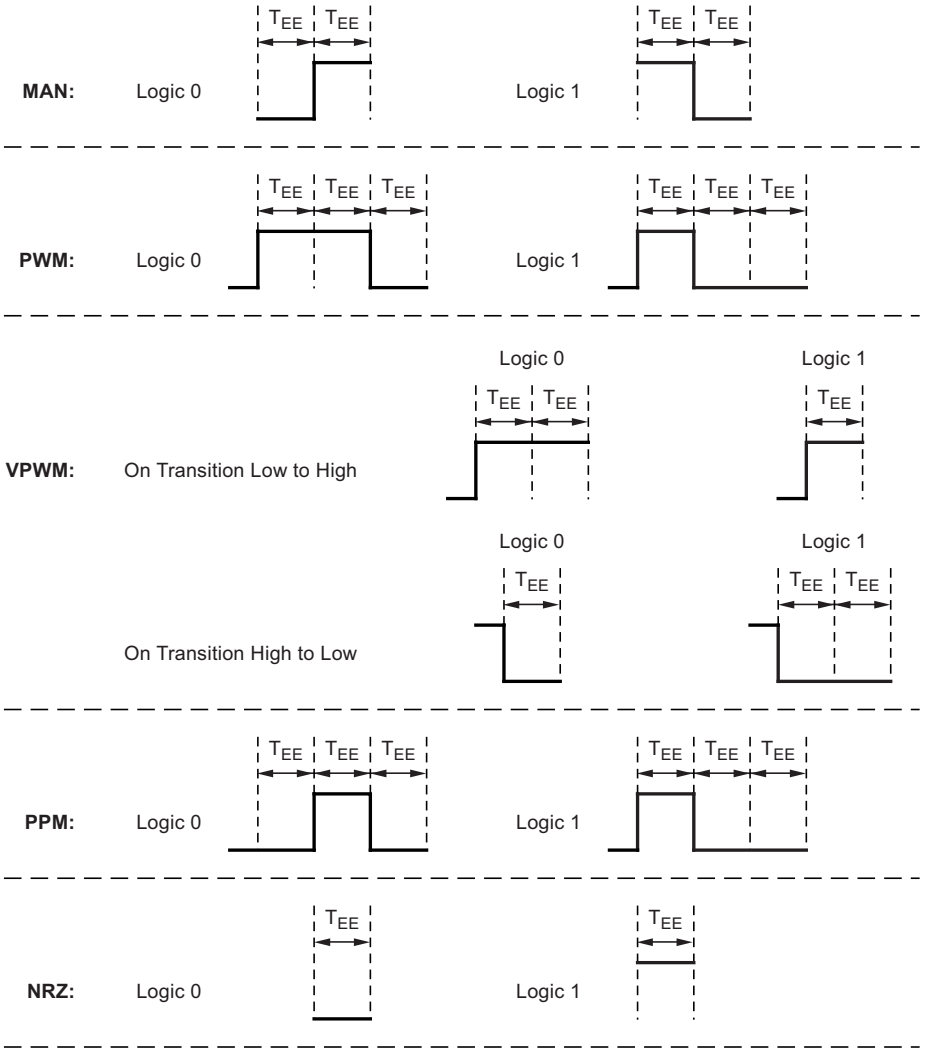
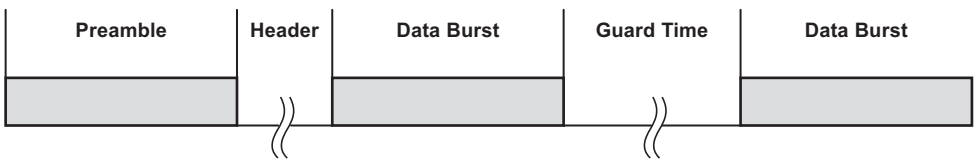


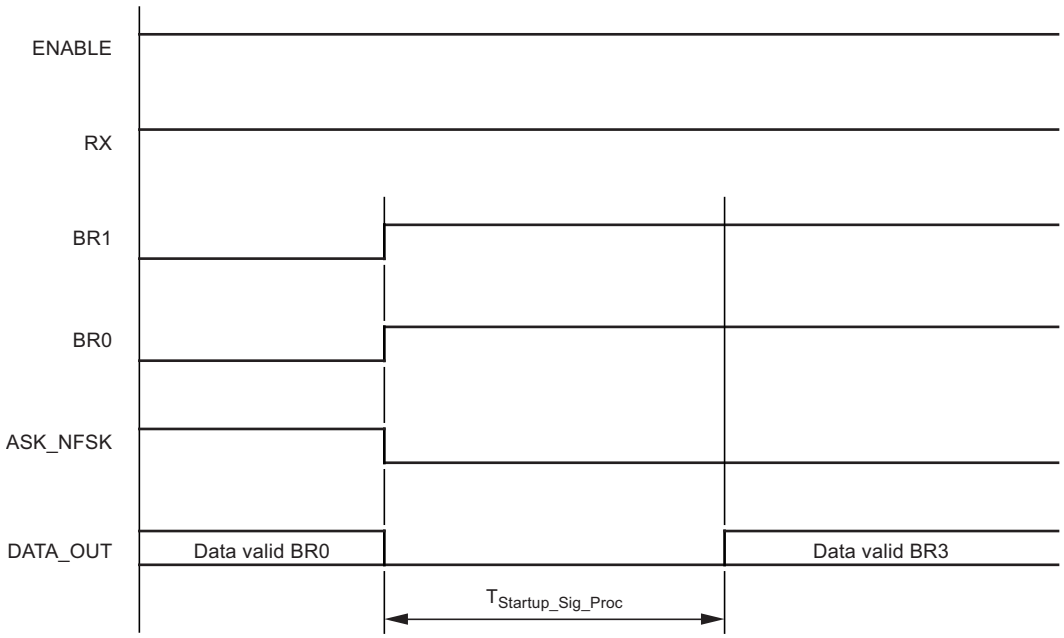
Figure 6-2. Supported Header and Blanking Periods



7. ASK_NFSK

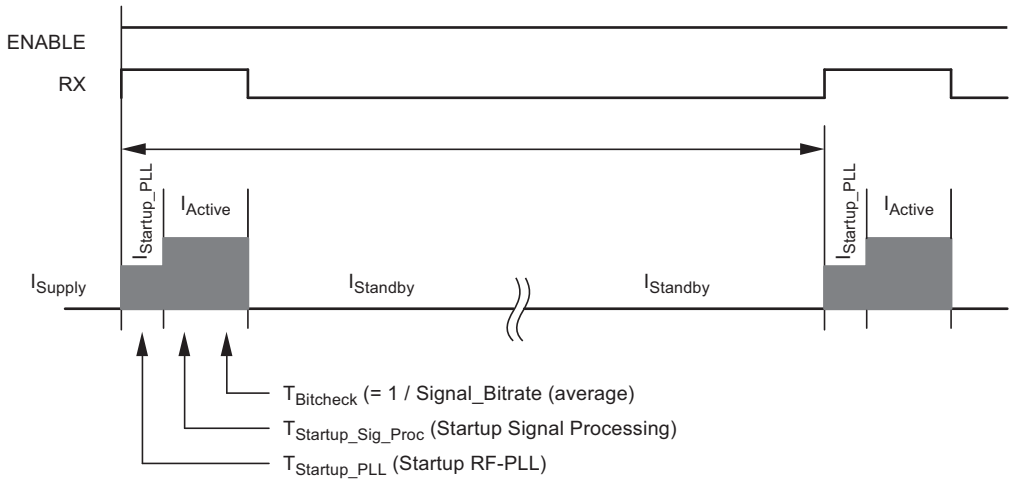
The ASK_NFSK pin allows the microcontroller to rapidly switch the RF front end between demodulation modes. A logic 1 on this pin selects ASK mode, and a logic 0 FSK mode. The time to change modes ($T_{Startup\_Sig\_Proc}$) depends on the bit rate range being selected (not current bit rate range) and is given in Table 5-4 on page 20. This response time is specified for applications that require an ASK preamble followed by FSK data (for typical TPM applications). During $T_{Startup\_Sig\_Proc}$, the level on pin DATA_OUT is low.

Figure 7-1. ASK Preamble 2.4Kbits/s followed by FSK Data 9.6Kbits/s



8. Polling Current Calculation

Figure 8-1. Polling Cycle



In an RKE and TPM system, the average chip current in Polling mode, $I_{Polling}$, is an important parameter. The polling period must be controlled by the connected microcontroller via the pins ENABLE and RX. The polling current can be calculated as follows:

$$I_{Polling} = (T_{Startup\_PLL} / T_{Polling\_Period}) \times I_{Startup\_PLL} + (T_{Startup\_Sig\_Proc} / T_{Polling\_Period}) \times I_{Active} + (T_{Bitcheck} / T_{Polling\_Period}) \times I_{Active} + (T_{Polling\_Period} - T_{Startup\_PLL} - T_{Startup\_Sig\_Proc} - T_{Bitcheck}) / T_{Polling\_Period} \times I_{Standby}$$

$T_{Startup\_PLL}$: depends on 315MHz/433.92MHz application.

$T_{Startup\_Sig\_Proc}$: depends on 315MHz/433.92MHz application and the selected bit rate range.

$T_{Bitcheck}$: depends on the signal bit rate (1 / Signal_Bit_Rate).

$T_{Polling\_Period}$: depends on the transmitter telegram (preburst).

$I_{Startup\_PLL}$: depends on 3V or 5V application and the setting of pin CLK_OUT.

I_{Active}: depends on 3V or 5V application, ASK or FSK mode and the setting of pin CLK_OUT.

$I_{Standby}$: depends on 3V or 5V application and the setting of pin CLK_OUT.

Example:- 315-MHz application (Atmel ATA5746C), bit rate: 9.6Kbits/s,

$T_{Polling\_Period}$ = 8ms

--> $T_{Startup\_PLL}$ = 269µs

--> $T_{Startup\_Sig\_Proc}$ = 324µs (Bit Rate Range 3)

--> $T_{Bitcheck}$ = 104µs

3V application; ASK mode, CLK_OUT disabled

--> $I_{Startup\_PLL}$ = 4.5mA

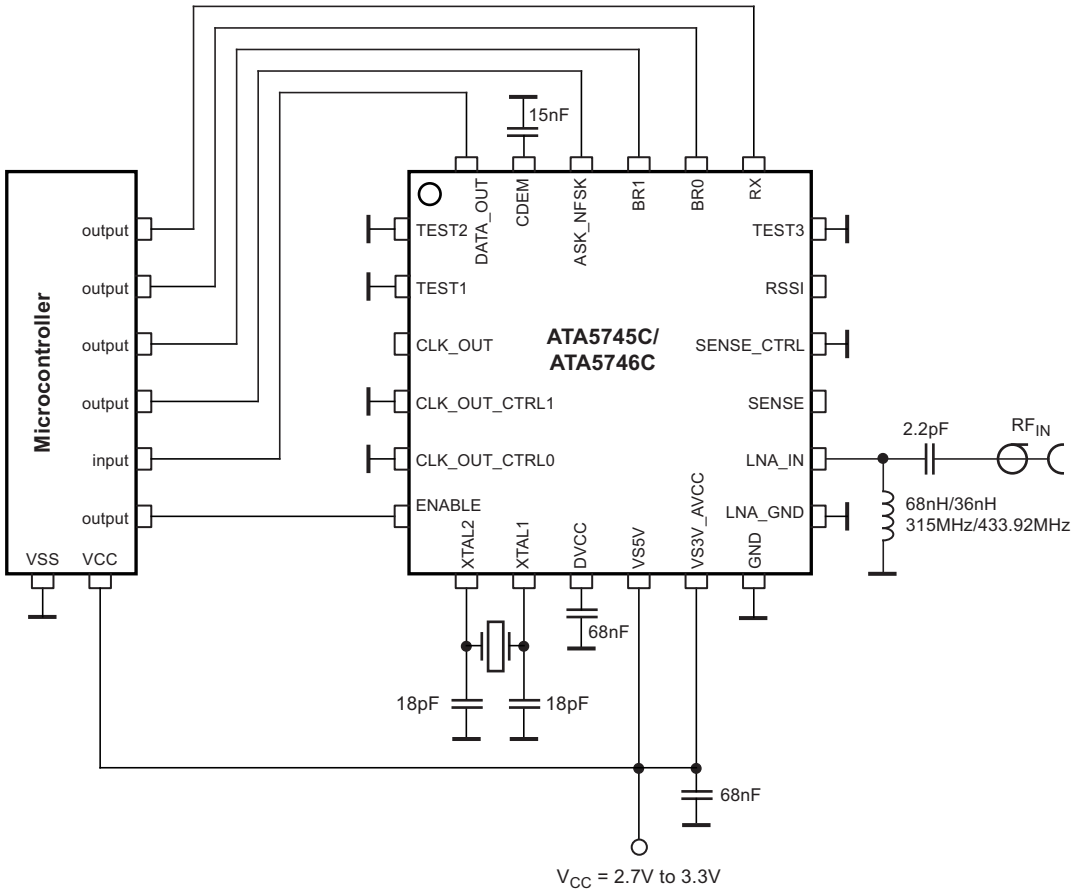
--> I_{Active} = 6.5mA

--> $I_{Standby}$ = 0.05mA

--> $I_{Polling}$ = 0.545mA

9. 3V Application

Figure 9-1. 3V Application



Note: Paddle (backplane) must be connected to GND