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ATA5823/ATA5824

UHF ASK/FSK Transceiver

DATASHEET

Features

- High FSK sensitivity: –105.5dBm at 20Kbit/s/–109dBm at 2.4Kbit/s (433.92MHz)
- High ASK sensitivity: –111.5dBm at 10Kbit/s/–116dBm at 2.4Kbit/s (100% ASK, carrier level 433.92MHz)
- Low supply current: 10.5mA in RX and TX mode (3V/TX with 5dBm/433.92MHz)
- Data rate 1 to 20Kbit/s Manchester FSK, 1 to 10Kbit/s Manchester ASK
- ASK/FSK receiver uses a low IF architecture with high selectivity, blocking and low intermodulation (typical 3dB blocking 55.5dBC at ±750kHz/60.5dBC at ±1.5MHz and 67dBC at ±10MHz, system I1dBCP = –30dBm/system IIP3 = –20dBm)
- Wide bandwidth AGC to handle large outband blockers above the system I1dBCP
- 226kHz IF (intermediate frequency) with 30dB image rejection and 220kHz system bandwidth to support TPM transmitters using Atmel® ATA5756/ATA5757 transmitters with standard crystals
- Transmitter uses closed loop FSK modulation with fractional-N synthesizer with high PLL bandwidth and an excellent isolation between PLL and PA
- Tolerances of XTAL compensated by fractional-N synthesizer with 800Hz RF resolution
- Integrated RX/TX-switch, single-ended RF input and output
- RSSI (received signal strength indicator)
- Communication to microcontroller with SPI interface working at 500kBit/s maximum
- Configurable self polling and RX/TX protocol handling with FIFO-RAM buffering of received and transmitted data
- 1 push button input and 1 wake-up input are active in power-down mode
- Integrated XTAL capacitors
- PA efficiency: up to 38% (433.92MHz/10dBm/3V)
- Low In-band sensitivity change of typically ±2.0dB within ±75kHz center frequency change in the complete temperature and supply voltage range

- Fully integrated PLL with low phase noise VCO, PLL loop filter and full support of multi-channel operation with arbitrary channel distance due to fractional-N synthesizer
- Sophisticated threshold control and quasi-peak detector circuit in the data slicer
- 433.92MHz, and 315MHz without external VCO and PLL components
- Efficient XTO start-up circuit (> –1.5kΩ worst case start impedance)
- Changing of modulation type ASK/FSK and data rate without component changes to allow different modulation schemes in TPM and RKE
- Minimal external circuitry requirements for complete system solution
- Adjustable output power: 0 to 10dBm adjusted and stabilized with external resistor, programmable output power with 0.5dB steps with internal resistor
- Clock and interrupt generation for microcontroller
- ESD protection at all pins (±2.5kV HBM, ±200V MM, ±500V FCDM)
- Supply voltage range: 2.15V to 3.6V or 4.4V to 5.25V
- Typical power-down current < 10nA
- Temperature range: –40°C to +105°C
- Small 7mm × 7mm QFN48 package

Applications

- Automotive keyless entry and passive entry go (handsfree car access)
- Tire pressure monitoring systems
- Remote control systems
- Alarm and telemetering systems
- Energy metering
- Home automation

Benefits

- No SAW device needed in key fob designs to meet automotive specifications
- Low system cost due to very high system integration level
- Only one crystal needed in system
- Less demanding specification for the microcontroller due to handling of power-down mode, delivering of clock and complete handling of receive/transmit protocol and polling
- Single-ended design with high isolation of PLL/VCO from PA and the power supply allows a loop antenna in the key fob to surround the whole application
- Integration of tire pressure monitoring, passive entry and remote keyless entry

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1. General Description

The Atmel® ATA5823/ATA5824 is a highly integrated UHF ASK/FSK multi-channel half-duplex transceiver with low power consumption supplied in a small 7mm × 7mm QFN48 package. The receive part is built as a fully integrated low-IF receiver, whereas direct PLL modulation with the fractional-N synthesizer is used for FSK transmission and switching of the power amplifier for ASK transmission.

The device supports data rates of 1Kbit/s to 20Kbit/s (FSK) and 1Kbit/s to 10Kbit/s (ASK) in Manchester, Bi-phase and other codes in transparent mode. The Atmel ATA5824 can be used in the 433MHz to 435MHz band and the Atmel ATA5823 in the 313MHz to 316MHz band. The very high system integration level results in few numbers of external components needed.

Due to its blocking and selectivity performance, together with a typical narrow-band key-fob loop antenna with 15dB to 20dB loss, a bulky blocking SAW is not needed in the key fob application. Additionally, the building blocks needed for a typical RKE and access control system on both sides, the base and the mobile stations, are fully integrated.

Its digital control logic with self polling and protocol generation provides a fast challenge response system without using a high-performance microcontroller. Therefore, the Atmel ATA5823/ATA5824 contains a FIFO buffer RAM and can compose and receive the physical messages themselves. This provides more time for the microcontroller to carry out other functions such as calculating crypto algorithms, composing the logical messages and controlling other devices. Due to that, a standard 4-/8-bit microcontroller without special periphery and clocked with the delivered CLK output of about 4.5MHz is sufficient to control the communication link. This is especially valid for passive entry go and access control systems, where within less than 100 ms several communication responses with arbitration of the communication partner have to be handled. It is hence possible to design bi-directional RKE and passive entry go systems with a fast challenge response crypto function and prevention against relay attacks.

Figure 1-1. System Block Diagram
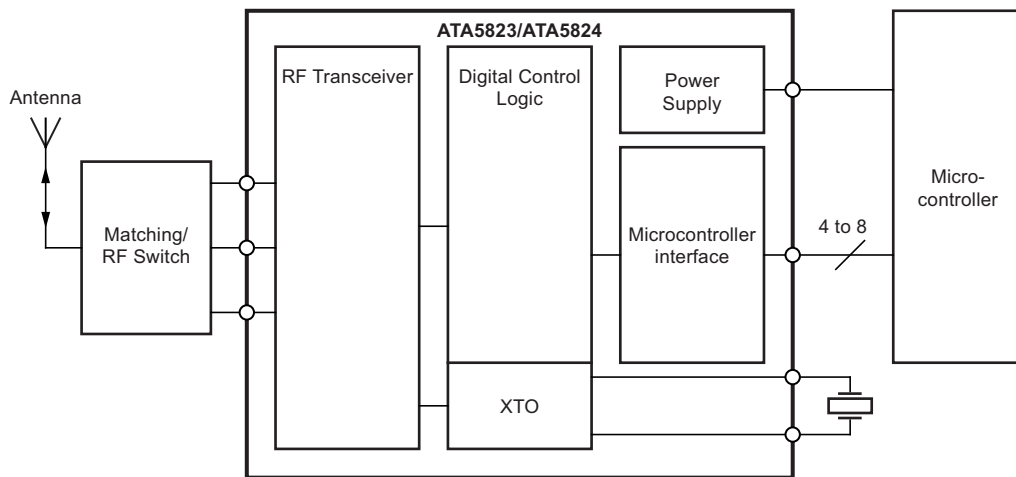
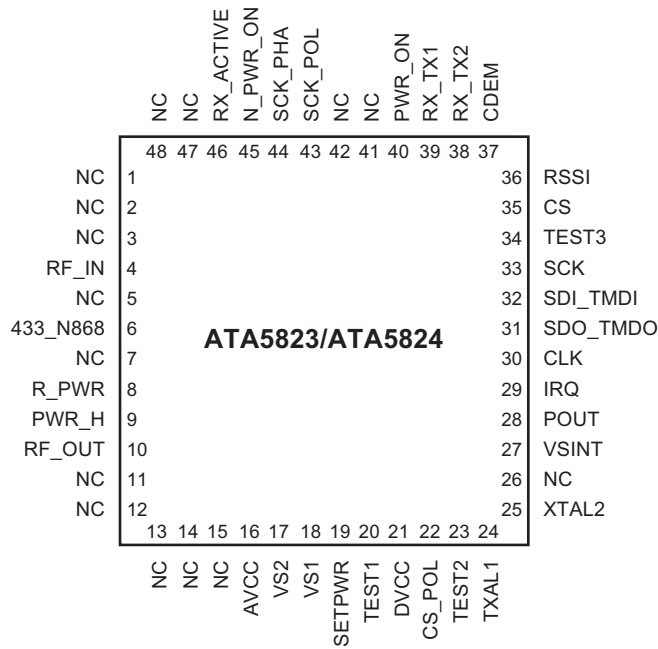# 2. Pin Configuration

Figure 2-1. Pinning QFN48

Table 2-1. Pin Description

Pin	Symbol	Function
1	NC	Not connected
2	NC	Not connected
3	NC	Not connected
4	RF_IN	RF input
5	NC	Not connected
6	433_N868	Selects RF input/output frequency range
7	NC	Not connected
8	R_PWR	Resistor to adjust output power
9	PWR_H	Pin to select output power
10	RF_OUT	RF output
11	NC	Not connected
12	NC	Not connected
13	NC	Not connected
14	NC	Not connected
15	NC	Not connected
16	AVCC	Blocking of the analog voltage supply
17	VS2	Power supply input for voltage range 4.4V to 5.6V
18	VS1	Power supply input for voltage range 2.15V to 3.6V
19	SETPWR	Internal Programmable Resistor to adjust output power
20	TEST1	Test input, at GND during operation
21	DVCC	Blocking of the digital voltage supply

Table 2-1. Pin Description (Continued)

Pin	Symbol	Function
22	CS_POL	Select polarity of pin CS
23	TEST2	Test input, at GND during operation
24	XTAL1	Reference crystal
25	XTAL2	Reference crystal
26	NC	Not connected
27	VSINT	Microcontroller interface supply voltage
28	POUT	Programmable output
29	IRQ	Interrupt request
30	CLK	Clock output to connect a microcontroller
31	SDO_TMDO	Serial data out/transparent mode data out
32	SDI_TMDI	Serial data in/transparent mode data in
33	SCK	Serial clock
34	TEST3	Test output open during operation
35	CS	Chip select for serial interface
36	RSSI	Output of the RSSI amplifier
37	CDEM	Capacitor to adjust the lower cut-off frequency data filter
38	RX_TX2	Has to be connected GND
39	RX_TX1	Switch pin to decouple LNA in TX mode (RKE mode)
40	PWR_ON	Input to switch on the system (active high)
41	NC	Not connected
42	NC	Not connected
43	SCK_POL	Polarity of the serial clock
44	SCK_PHA	Phase of the serial clock
45	N_PWR_ON	Keyboard input (can also be used to switch on the system, active low)
46	RX_ACTIVE	Indicates RX operation mode
47	NC	Not connected
48	NC	Not connected
	GND	Ground/Backplane (exposed die pad)

Figure 2-2. Block Diagram

ATA5823/ATA5824 [DATASHEET]
4829G–RKE–01/15

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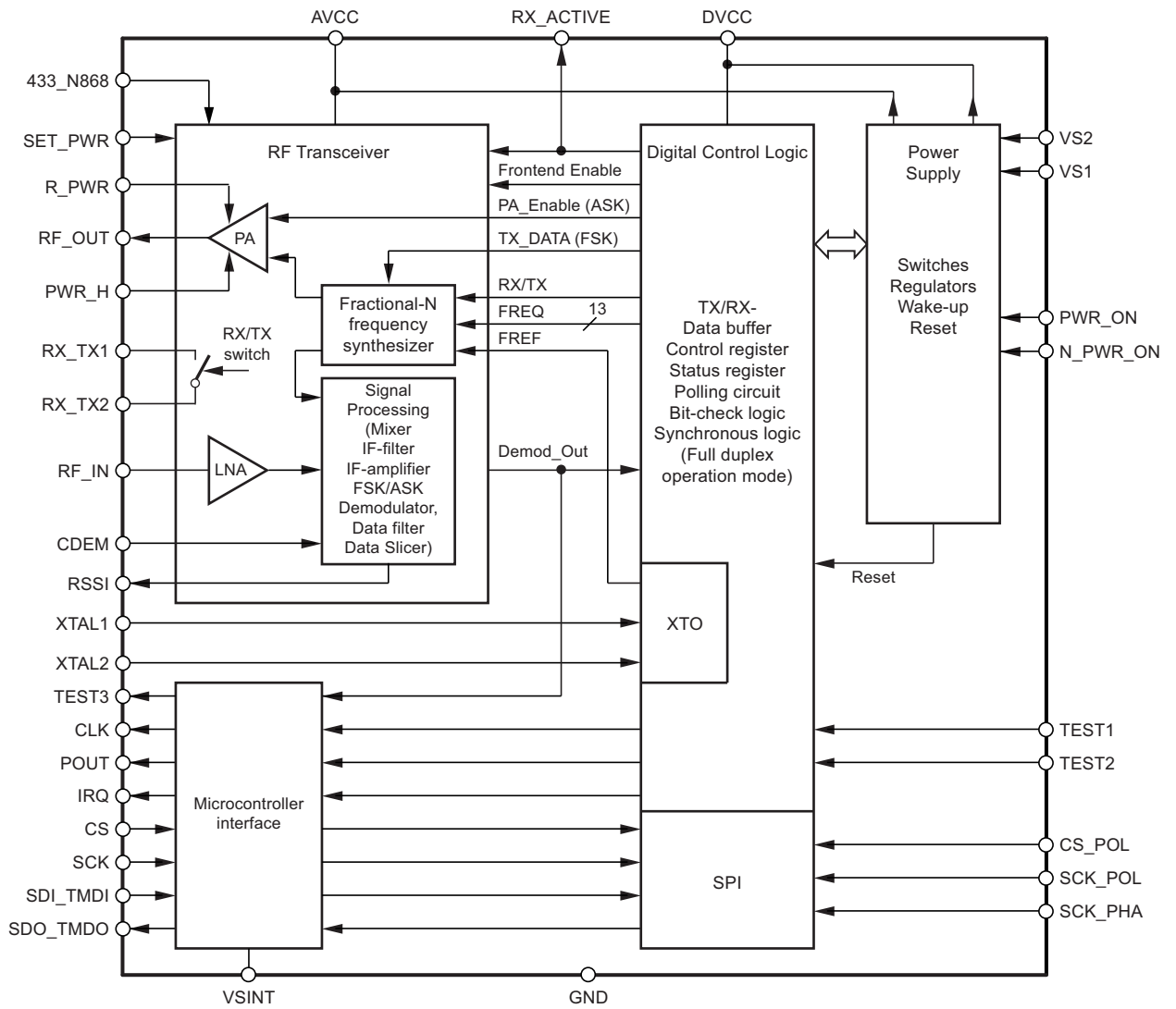
3. Typical Key Fob Application for Bi-directional RKE

Figure 3-1. Typical Key Fob Application for Bi-directional RKE with 5dBm TX Power, 433.92MHz
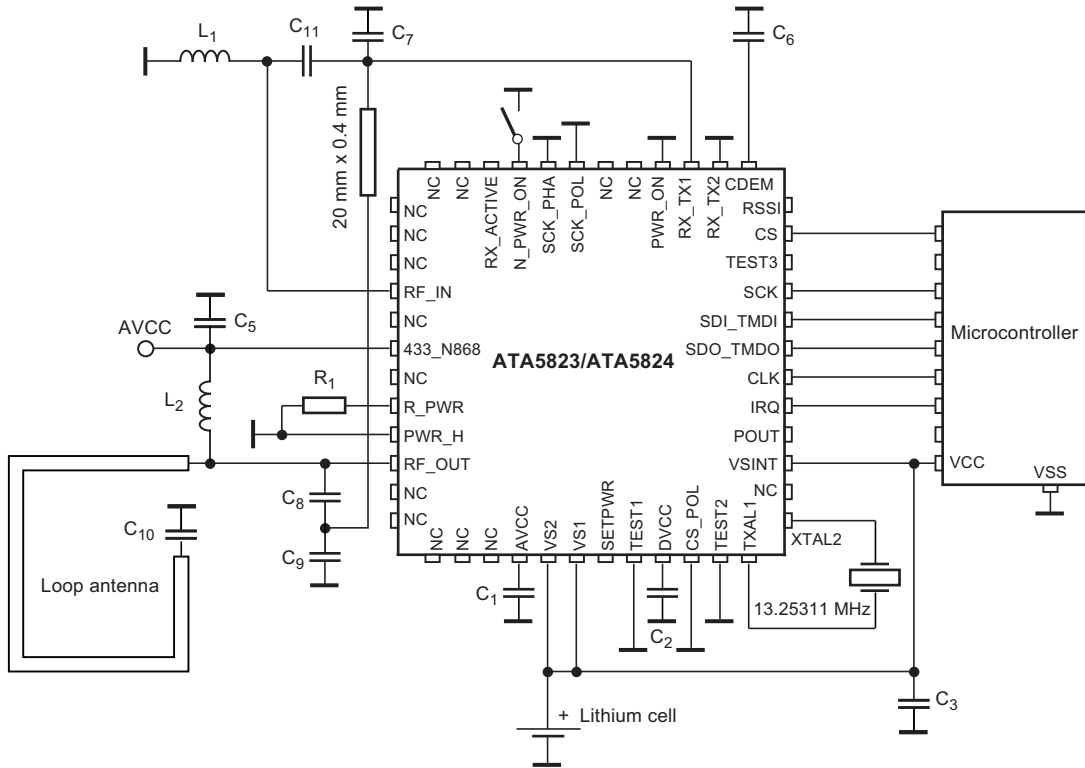

shows a typical 433.92MHz RKE key fob application. The external components are 10 capacitors, 1 resistor, 2 inductors and a crystal. C_1 to C_3 are 68nF voltage supply blocking capacitors. C_5 is a 10nF supply blocking capacitor. C_6 is a 15nF fixed capacitor used for the internal quasi-peak detector and for the high-pass frequency of the data filter. C_7 to C_{11} are RF matching capacitors in the range of 1pF to 33pF. L_1 is a matching inductor of about 5.6nH to 56nH. L_2 is a feed inductor of about 120nH. A load capacitor of 9pF for the crystal is integrated. R_1 is typically 22kΩ and sets the output power to about 5.5dBm. The loop antenna's quality factor is somewhat reduced by this application due to the quality factor of L_2 and the RX/TX switch. On the other hand, this lower quality factor is necessary to have a robust design with a bandwidth that is wide enough for production tolerances. Due to the single-ended and ground-referenced design, the loop antenna can be a free-form wire around the application as it is usually employed in RKE unidirectional systems. The Atmel® ATA5823/ATA5824 provides sufficient isolation and robust pulling behavior of internal circuits from the supply voltage as well as an integrated VCO inductor to allow this. Since the efficiency of a loop antenna is proportional to the square of the surrounded area, it is beneficial to have a large loop around the application board with a lower quality factor to relax the tolerance specification of the RF matching components and to get a high antenna efficiency in spite of their lower quality factor.

4. Typical Car Application for Bi-directional RKE

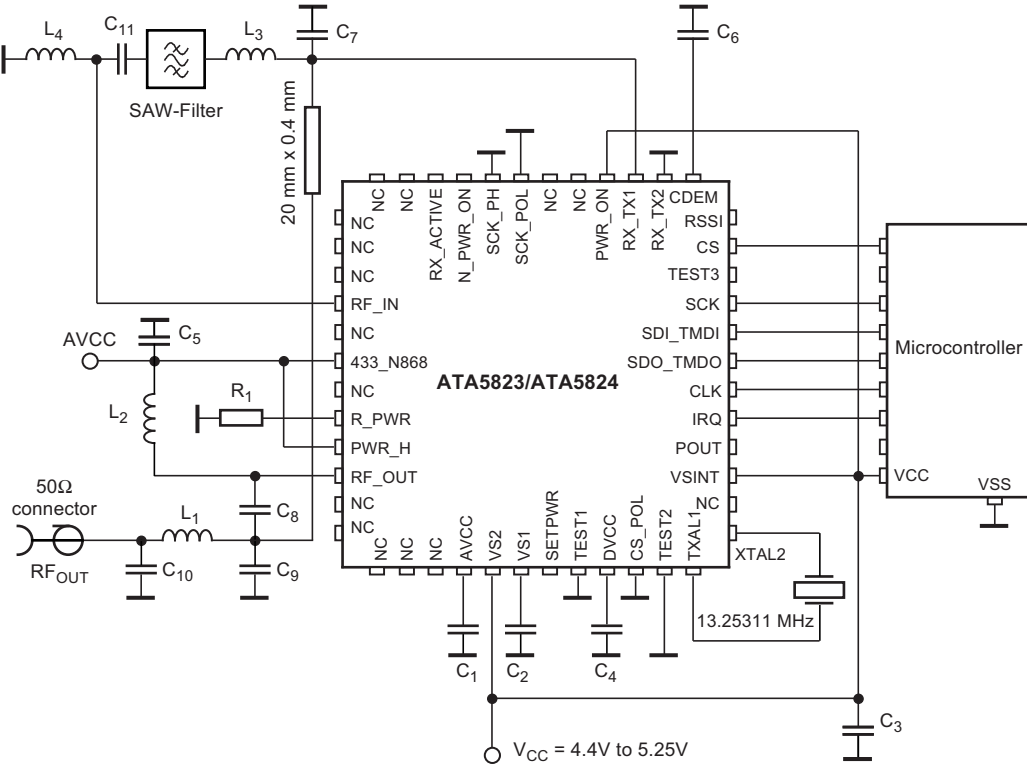**Figure 4-1.** Typical Car Application for Bi-directional RKE with 10dBm TX Power, 433.92MHz

Figure 4-1 shows a typical 433.92MHz V_{CC} = 4.4V to 5.25V RKE car application. The external components are 11 capacitors, 1 resistor, 4 inductors, a SAW filter and a crystal. C_1, C_3 and C_4 are 68nF voltage supply blocking capacitors. C_2 is a 2.2µF supply blocking capacitor for the internal voltage regulator. C_5 is a 10nF supply blocking capacitor. C_6 is a 15nF fixed capacitor used for the internal quasi-peak detector and for the high-pass frequency of the data filter. C_7 to C_{11} are RF matching capacitors in the range of 1pF to 33pF. L_2 to L_4 are matching inductors of about 5.6nH to 56nH. A load capacitor for the crystal of 9pF is integrated. R_1 is typically 22kΩ and sets the output power at RF_{OUT} to about 10dBm. Since a quarter wave or PCB antenna, which has high efficiency and wideband operation, is typically used here, it is recommended to use a SAW filter to achieve high sensitivity in case of powerful out-of-band blockers. L_1, C_{10} and C_9 together form a low-pass filter, which is needed to filter out the harmonics in the transmitted signal to meet regulations.

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5.   RF Transceiver in Half-duplex Mode

According to Figure 2-2 on page 6, the RF transceiver consists of an LNA (Low-Noise Amplifier), PA (Power Amplifier), RX/TX switch, fractional-N frequency synthesizer and the signal processing part with mixer, IF filter, IF amplifier with analog RSSI, FSK/ASK demodulator, data filter and data slicer.

In receive mode the LNA pre-amplifies the received signal which is converted down to 226kHz intermediate frequency (IF), filtered and amplified before it is fed into an FSK/ASK demodulator, data filter and data slicer. The RSSI (Received Signal Strength Indicator) signal and the raw digital output signal of the demodulator are available at the pins RSSI and on TEST3 (open drain output). The demodulated data signal Demod_Out is fed into the digital control logic where it is evaluated and buffered as described in section "Digital Control Logic" on page 32.

In transmit mode the fractional-N frequency synthesizer generates the TX frequency which is fed into the PA. In ASK mode the PA is modulated by the signal PA_Enable. In FSK mode the PA is enabled and the signal TX_DATA (FSK) modulates the fractional-N frequency synthesizer. The frequency deviation is digitally controlled and internally fixed to about ±19.5kHz (see Table 6-1 on page 25 for exact values). The transmit data can also be buffered as described in section "Digital Control Logic" on page 32. A lock detector within the synthesizer ensures that the transmission will only start if the synthesizer is locked.

In half-duplex mode the RX/TX switch can be used to combine the LNA input and the PA output to a single antenna with a minimum of losses.

Transparent modes without buffering of RX and TX data are also available to allow protocols and coding schemes other than the internal supported Manchester encoding, like PWM and pulse position coding.

5.1   Low-IF Receiver

The receive path consists of a fully integrated low-IF receiver. It fulfills the sensitivity, blocking, selectivity, supply voltage and supply current specification needed to manufacture an automotive key fob for RKE and PEG systems without the use of a SAW blocking filter (see Figure 3-1 on page 7). The receiver can be connected to the roof antenna in the car when using an additional blocking SAW front-end filter as shown in Figure 4-1 on page 8.

At 433.92MHz the receiver has a typical system noise figure of 6.5dB, a system I1dBCP of –30dBm and a system IIP3 of –20dBm. The signal path is linear for disturbers up to the I1dBCP and there is hence no AGC or switching of the LNA needed to achieve a better blocking performance. This receiver uses an IF of about 226kHz (see Section 14. "Electrical Characteristics: General" on page 61 number 2.10 for exact values), the typical image rejection is 30dB and the typical 3dB system bandwidth is 220kHz (f_{IF} = 226kHz ±110kHz, f_{lo_IF} = 116kHz and f_{hi_IF} = 336kHz). The demodulator needs a signal to noise ratio of 8dB for 20Kbit/s Manchester with ±19.5kHz frequency deviation in FSK mode, thus, the resulting sensitivity at 433.92MHz is typically –105.5dBm.

Due to the low phase noise and spurious of the synthesizer in receive mode[1] together with the eighth order integrated IF filter the receiver has a better selectivity and blocking performance than more complex double superhet receivers, without using external components and without numerous spurious receiving frequencies.

Note: 1.   –120dBC/Hz at ±1MHz and –72dBC at ±f_{XTO} at 433.92MHz

A low-IF architecture is also less sensitive to second-order intermodulation (IIP2) than direct conversion receivers where every pulse or amplitude modulated signal (especially the signals from TDMA systems like GSM) demodulates to the receiving signal band at second-order non-linearities.

5.2 Input Matching at RF_IN

The measured input impedances as well as the values of a parallel equivalent circuit of these impedances can be seen in Table 5-1. The highest sensitivity is achieved with power matching of these impedances to the source impedance of 50Ω.

Table 5-1. Measured Input Impedances of the RF_IN Pin

f_{RF}/MHz	Z_{In}(RF_IN)	$R_{In\_p}//C_{In\_p}$
315	(44-j233)Ω	1278Ω//2.1pF
433.92	(32-j169)Ω	925Ω//2.1pF

The matching of the LNA Input to 50Ω was done with the circuit according to Figure 5-1 and with the values of the matching elements given in Table 5-2. The reflection coefficients were always ≤ –10dB. Note that value changes of C_1 and L_1 may be necessary to compensate individual board layout parasitics. The measured typical FSK and ASK Manchester code sensitivities with a Bit Error Rate (BER) of 10^{-3} are shown in Table 5-3 on page 10 and Table 5-4 on page 10. These measurements were done with multilayer inductors having quality factors according to Table 5-2, resulting in estimated matching losses of 0.8dB at 315MHz and 0.8dB at 433.92MHz. These losses can be estimated when calculating the parallel equivalent resistance of the inductor with $R_{loss} = 2 \times \pi \times f \times L \times Q_L$ and the matching loss with $10 \log(1+R_{In\_p}/R_{loss})$.

With an ideal inductor, for example, the sensitivity at 433.92MHz/FSK/20Kbit/s/ ±19.5kHz/Manchester can be improved from –105.5dBm to –106.7dBm. The sensitivity also depends on the values in the registers of the control logic which examines the incoming data stream. The examination limits must be programmed in control registers 5 and 6. The measurements in Table 5-3 and Table 5-4 on page 10 are based on the values of registers 5 and 6 according to Table 11-3 on page 55.

Figure 5-1. Input Matching to 50Ω
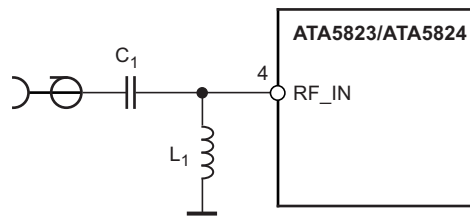
Table 5-2. Input Matching to 50Ω

f_{RF}/MHz	C_1/pF	L_1/nH	Q_{L1}
315	2.4	47	65
433.92	1.8	27	67

Table 5-3. Measured Typical Sensitivity 433.92MHz, FSK, ±19.5kHz, Manchester, BER = 10^{-3}

| RF Frequency	BR_Range_0 1.0Kbit/s	BR_Range_0 2.4Kbit/s	BR_Range_1 5.0Kbit/s	BR_Range_2 10Kbit/s	BR_Range_3 20Kbit/s
315MHz	–109.5dBm	–110.0dBm	–109.0dBm	–107.5dBm	–106.5dBm
433.92MHz	–108.5dBm	–109.0dBm	–108.0dBm	–106.5dBm	–105.5dBm

Table 5-4. Measured Typical Sensitivity 433.92 MHz, 100% ASK, Manchester, BER = 10^{-3}

RF Frequency	BR_Range_0 1.0Kbit/s	BR_Range_0 2.4Kbit/s	BR_Range_1 5.0Kbit/s	BR_Range_2 10Kbit/s	
315MHz	–117.0dBm	–117.0dBm	–114.5dBm	–112.5dBm	
433.92MHz	–116.0dBm	–116.0dBm	–113.5dBm	–111.5dBm	

5.3 Sensitivity versus Supply Voltage, Temperature and Frequency Offset

To calculate the behavior of a transmission system it is important to know the reduction of the sensitivity due to several influences. The most important are frequency offset due to crystal oscillator (XTO) and crystal frequency (XTAL) errors, temperature and supply voltage dependency of the noise figure and IF filter bandwidth of the receiver. Figure 5-2 shows the typical sensitivity at 433.92MHz/FSK/20Kbit/s/±19.5kHz/Manchester versus the frequency offset between transmitter and receiver at T_{amb} = –40°C, +25°C and +105°C and supply voltage $V_S = V_{S1} = V_{S2}$ = 2.15V, 3.0V and 3.6V.

Figure 5-2. Measured Sensitivity 433.92MHz/FSK/20Kbit/s/±19.5kHz/Manchester versus Frequency Offset, Temperature and Supply Voltage
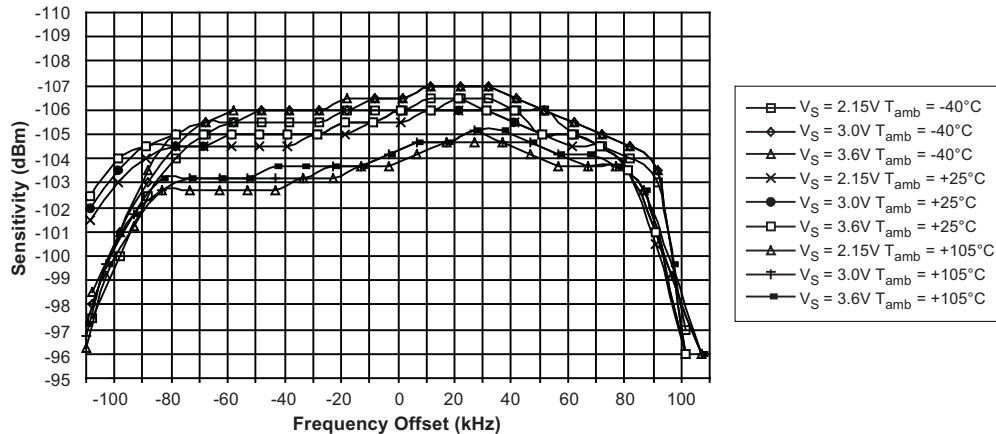
As can be seen in Figure 5-2 on page 11 the supply voltage has almost no influence on the sensitivity. The temperature has an influence of about +1.5/–0.7dB and a frequency offset of ±85kHz also influences by about ±1dB. All these influences, combined with the sensitivity of a typical IC (–105.5dBm), are then within a range of –102.5dBm and –107dBm overtemperature, supply voltage and frequency offset. The integrated IF filter has an additional production tolerance of ±10kHz, hence, a frequency offset between the receiver and the transmitter of ±75kHz can be accepted for XTAL and XTO tolerances.

Note: For the demodulator used in the Atmel ATA5823/ATA5824, the tolerable frequency offset does not change with the data frequency, hence, the value of ±75kHz is valid for 1Kbit/s to 20Kbit/s.

This small sensitivity change over supply voltage, frequency offset and temperature is very unusual in such a receiver. It is achieved by an internal, very fast and automatic frequency correction in the FSK demodulator after the IF filter, which leads to a higher system margin. This frequency correction tracks the input frequency very quickly, if however, the input frequency makes a larger step (e.g., if the system changes between different communication partners), the receiver has to be restarted. This can be done by switching back to IDLE mode and then again to RX mode. For that purpose, an automatic mode is also available. This automatic mode switches to IDLE mode and back into RX mode every time a bit error occurs (see section "Digital Control Logic" on page 32).

5.4 Frequency Accuracy of the Crystals in Bi-directional RKE/PEG

The XTO is an amplitude regulated Pierce type oscillator with integrated load capacitors. The initial tolerances (due to the frequency tolerance of the XTAL, the integrated capacitors on XTAL1, XTAL2 and the XTO's initial transconductance gm) can be compensated to a value within ±0.5ppm by measuring the CLK output frequency and tuning of f_{RF} by programming the control registers 2 and 3 (see Table 9-7 on page 34 and Table 9-10 on page 35). The XTO then has a remaining influence of less than ±2ppm overtemperature and supply voltage due to the bandgap controlled gm of the XTO. Thus only 2.5ppm add to the frequency stability of the used crystals overtemperature and aging.

The needed frequency stability of the used crystals **overtemperature and aging** is hence
±75kHz/433.92MHz – 2 × ±2.5ppm = ±167.84ppm for 433.92MHz. Thus, the used crystals in receiver and transmitter each need to be better than ±83.9ppm for 433.92MHz.

5.5 Frequency Accuracy of the Crystals in a Combined RKE/PEG and TPM System

In a tire pressure measurement system working at 433.92MHz and using a TPM transmitter Atmel® ATA5757 and a transceiver Atmel ATA5824 as a receiver, the higher frequency tolerances and the tolerance of the frequency deviation of this transmitter has to be considered.

In the TPM transmitter the crystal has an frequency error overtemperature –40°C to +125°C, aging and tolerance of ±80ppm (±34.7kHz at 433.92MHz). The tolerances of the XTO, the capacitors used for FSK-Modulation and the stray capacitors, causing an additional frequency error of ±30ppm (±13kHz at 433.92MHz). The frequency deviation of such a transmitter varies between ±16kHz and ±24kHz, since a higher frequency deviation is equivalent to an frequency error, this has to be considered as an additional ±24kHz – ±19.5kHz = ±4.5kHz frequency tolerance. All tolerances added, these transmitters have a worst case frequency offset of ±52.2kHz.

For the transceiver in the car a tolerance of ±75kHz – ±52.2kHz = ±22.8kHz (±52.5ppm) remains. The needed frequency stability of the used crystals **overtemperature and aging** is ±52.5ppm – ±2.5ppm = ±50ppm. The aging of such a crystal is ±10ppm leaving reasonable ±40ppm for the temperature dependency of the crystal frequency in the car.

Since the transceiver in the car is able to receive these TPM transmitter signals with high frequency offsets, the component specification in the key can be largely relaxed.

This system calculation is based on worst case tolerances of all the components, this leads in practice to a system with margin.

For a 315MHz TPM system using a TPM transmitter Atmel ATA5756 and a transceiver Atmel ATA5823 as receiver the same calculation must be done, but since the RF frequency is lower, every ppm of crystal tolerances results in less frequency offset and either the system can have higher tolerances or a higher margin there.

5.6 RX Supply Current versus Temperature and Supply Voltage

Table 5-5 shows the typical supply current at 433.92MHz of the transceiver in RX mode versus supply voltage and temperature with $V_S = V_{S1} = V_{S2}$. As can be seen the supply current at V_S = 2.15V and $T_{amb =}$ –40°C is less than at V_S = 3V/T_{amb} = 25° which helps to enlarge the battery lifetime within a key fob application because this is also the operation point where a lithium cell has the worst performance. The typical supply current at 315MHz in RX mode is about the same as for 433.92MHz.

**Table 5-5.   Measured 433.92MHz Receive Supply Current in FSK mode**

| $V_S = V_{S1} = V_{S2}$	2.15V	3.0V	3.6V
T_{amb} = –40°C	8.2mA	8.8mA	9.2mA
T_{amb} = 25°C	9.7mA	10.3mA	10.8mA
T_{amb} = 105°C	11.2mA	11.9mA	12.4mA

5.7 Blocking, Selectivity

As can be seen in Figure 5-3, Figure 5-4 and Figure 5-5 on page 13, the receiver can receive signals 3dB higher than the sensitivity level in presence of large blockers of –44.5dBm/-36.0dBm with small frequency offsets of ±1/±10MHz.

Figure 5-3 and Figure 5-4 on page 13 shows the close-in and narrow-band blocking and Figure 5-5 on page 13 the wide-band blocking characteristic. The measurements were done with a useful signal of 433.92MHz/FSK/20Kbit/s/±19.5kHz/Manchester with a level of –105.5dBm + 3dB = –102.5dBm which is 3dB above the sensitivity level. The figures show by how much a continuous wave signal can be larger than –102.5dBm until the BER is higher than 10^{-3}. The measurements were done at the 50Ω input according to Figure 5-1 on page 10. At 1MHz, for example, the blocker can be 58dBC higher than –102.5dBm which is –102.5dBm +58dBC = –44.5dBm. These blocking figures, together with the good intermodulation performance, avoid the additional need of a SAW filter in the key fob application.

Figure 5-3.   Close In 3dB Blocking Characteristic and Image Response at 433.92MHz
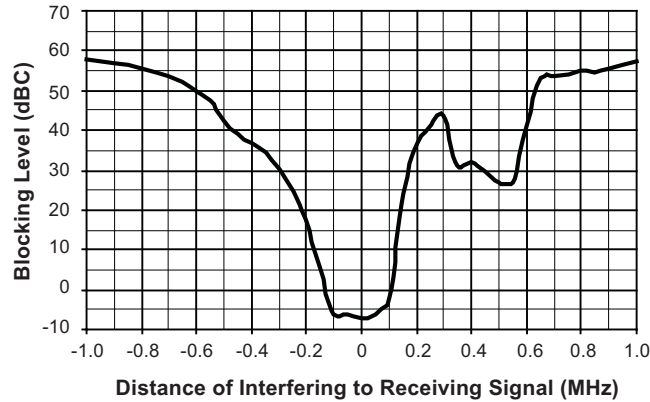
Figure 5-4.   Narrow Band 3dB Blocking Characteristic at 433.92MHz
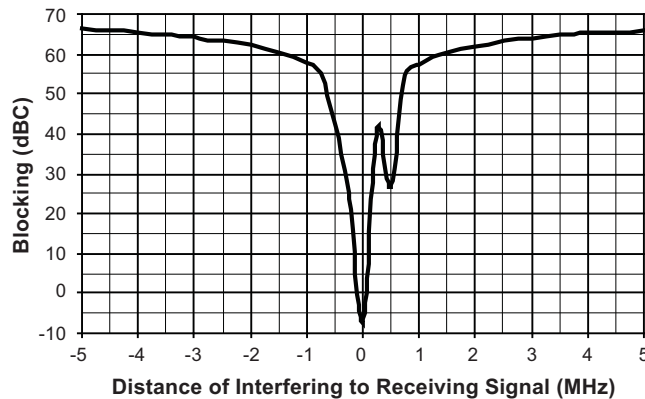
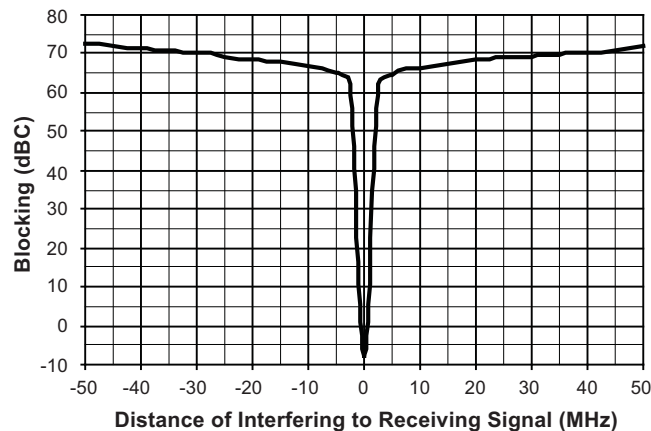**Figure 5-5.   Wide Band 3dB Blocking Characteristic at 433.92MHz**

Table 5-6 shows the blocking performance measured relative to –102.5dBm for some frequencies. Note that sometimes the blocking is measured relative to the sensitivity level –105.5dBm (denoted dBS) instead of the carrier –102.5dBm (denoted dBC).

Table 5-6.   Blocking 3 dB Above Sensitivity Level with BER < 10^{-3}

Frequency Offset	Blocker Level	Blocking
+0.75MHz	–47.5dBm	55.0dBC/58.0dBS
–0.75MHz	–47.5dBm	55.0dBC/58.0dBS
+1.0MHz	–44.5dBm	58.0dBC/61.0dBS
–1.0MHz	–44.5dBm	58.0dBC/61.0dBS
+1.5MHz	–42.0dBm	60.5dBC/63.5dBS
–1.5MHz	–42.0dBm	60.5dBC/63.5dBS
+10MHz	–35.5dBm	67.0dBC/70.0dBS
–10MHz	–35.5dBm	67.0dBC/70.0dBS

The Atmel® ATA5823/ATA5824 can also receive FSK and ASK modulated signals if they are much higher than the I1dBCP. It can typically receive useful signals at +10dBm. This is often referred to as the nonlinear dynamic range which is the maximum to minimum receiving signal which is 115.5dB for 433.92MHz/FSK/20Kbit/s/±19.5kHz/ Manchester. This value is useful if two transceivers have to communicate and are very close to each other.

In a keyless entry system there is another blocking characteristic that has to be considered. A keyless entry system has a typical service range of about 30 m with a receiver sensitivity of about –106dBm to –109dBm. In some cases, large blockers limit this service range, and it is important to know how large this blockers can be until the system doesn't work anymore and the user has to use its key. With a recommended sensitivity of about –85dBm, the system works just around the car. Figure 5-6 and Figure 5-7 on page 15 show the blocking performance in this important case with a useful signal of –85dBm 433.92MHz/FSK/20Kbit/s/±19.5kHz/ Manchester.

As can be seen the system works even with blockers above the compression point. This is due to a wide bandwidth automatic gain control that begins to work if blockers above the compression point are at the antenna input and increasing the current in the LNA/Mixer to get a better compression point needed to handle these large blockers.

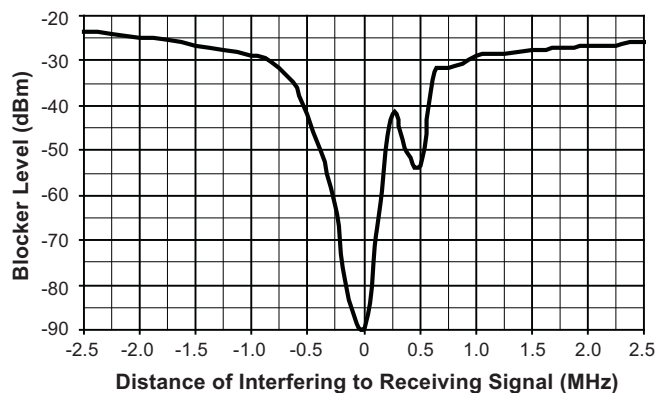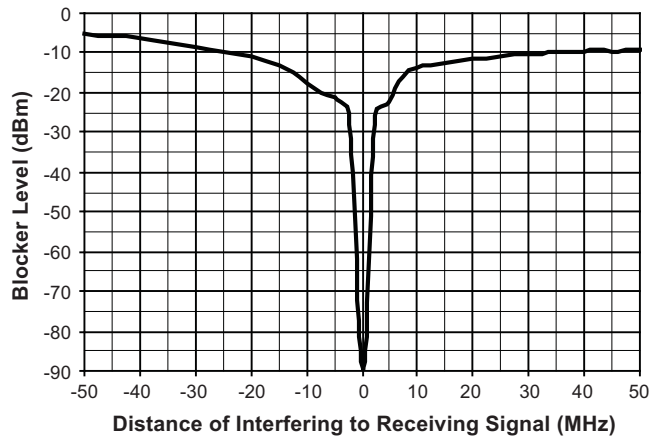**Figure 5-6.   ±2.5MHz Blocking Characteristic for –85dBm Useful Signal at 433.92MHz**

Figure 5-7. ±50MHz Blocking Characteristic for –85dBm Useful Signal at 433.92MHz

This high blocking performance makes it even possible for some applications using quarter wave whip antennas to use a simple LC band-pass filter instead of a SAW filter in the receiver. When designing such a LC filter, take into account that the 3dB blocking at 433.92MHz/2 = 216.96MHz is 42dBC and at 433.92MHz/3 = 144.64MHz is 47dBC a . And especially that at $3 \times$ (433.92MHz + 226kHz)+226kHz = 1302.664MHz the receiver has a second LO harmonic receiving frequency with only 17dBC blocking.

5.8 Inband Disturbers, Data Filter, Quasi-peak Detector, Data Slicer

If a disturbing signal falls into the received band, or a blocker is not a continuous wave, the performance of a receiver strongly depends on the circuits after the IF filter. Hence the demodulator, data filter and data slicer are important in that case.

The data filter of the Atmel® ATA5823/ATA5824 implies a quasi-peak detector. This results in a good suppression of above mentioned disturbers and exhibits a good carrier to noise performance. The required ratio of useful signal to disturbing signal, at a BER of 10^{-3} is less than 12dB in ASK mode and less than 3dB (BR_Range_0 ... BR_Range_2) and 6dB (BR_Range_3) in FSK mode. Due to the many different possible waveforms these numbers are measured for signal as well as for disturbers with peak amplitude values. Note that these values are worst case values and are valid for any type of modulation and modulating frequency of the disturbing signal as well as the receiving signal. For many combinations, lower carrier to disturbing signal ratios are needed.

5.9 TEST3 Output

The internal raw output signal of the demodulator Demod_Out is available at pin TEST3. TEST3 is an open drain output and must be connected to a pull-up resistor if it is used (typically 100kΩ), otherwise no signal is present at that pin. This signal is mainly used for debugging purposes during the setup of a new application, since the received data signal can be seen there without any digital processing.

5.10 RSSI Output

The output voltage of the pin RSSI is an analog voltage, proportional to the input power level. Using the RSSI output signal, the signal strength of different transmitters can be distinguished. The usable dynamic range of the RSSI amplifier is 70dB, the input power range P_{RFIN} is –115dBm to –45dBm and the gain is 8mV/dB. Figure 5-8 on page 16 shows the RSSI characteristic of a typical device at 433.92MHz with V_{S1} = V_{S2} = 2.15V to 3.6V and T_{amb} = –40°C to +105°C with a matched input according to Table 5-2 on page 10 and Figure 5-1 on page 10. At 315MHz about 1dB less signal level is needed for the same RSSI results.

Figure 5-8. Typical RSSI Characteristic at 433.92MHz versus Temperature and Supply Voltage
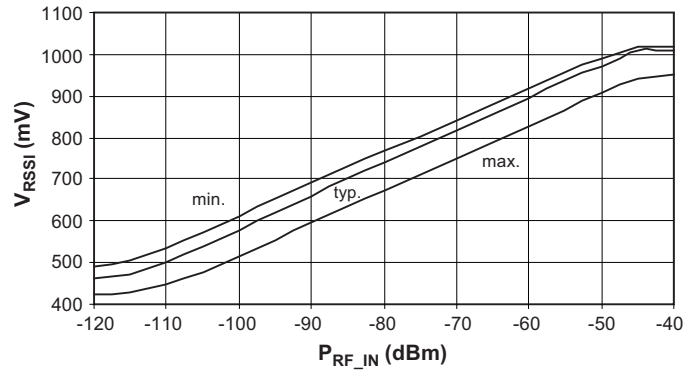
5.11 Frequency Synthesizer and Channel Selection

The synthesizer is a fully integrated fractional-N design with internal loop filters for receive and transmit mode. The XTO frequency f_{XTO} is the reference frequency FREF for the synthesizer. The bits FR0 to FR12 in control registers 2 and 3 (see Table 9-7 on page 34 and Table 9-10 on page 35) are used to adjust the deviation of f_{XTO}. In half-duplex transmit mode, at 433.92MHz, the carrier has a phase noise of –111dBC/Hz at 1MHz and spurious at FREF of –70dBC with a high PLL loop bandwidth allowing the direct modulation of the carrier with 20Kbit/s Manchester data. Due to the closed loop modulation, any spurious caused by this modulation are effectively filtered out as can be seen in Figure 5-11 on page 18. In RX mode the synthesizer has a phase noise of –120dBC/Hz at 1MHz and spurious of –72dBC.

The initial tolerances of the crystal oscillator due to crystal frequency tolerances, internal capacitor tolerances and the parasitics of the board have to be compensated at manufacturing setup with control registers 2 and 3 as can be seen in Table 6-1 on page 25. The other control words for the synthesizer needed for ASK, FSK and receive/transmit switching are calculated internally. The RF (Radio Frequency) resolution is equal to the XTO frequency divided by 16384 which is 777.1Hz at 315.0MHz and 808.9Hz at 433.92MHz.

The frequency control word FREQ in control registers 2 and 3 can be programmed in the range of 1000 to 6900, hence every frequency within the 433MHz ISM bands can be programmed as receive and as transmit frequency and the position of channels within these ISM bands can be chosen arbitrarily (see Table 6-1 on page 25).
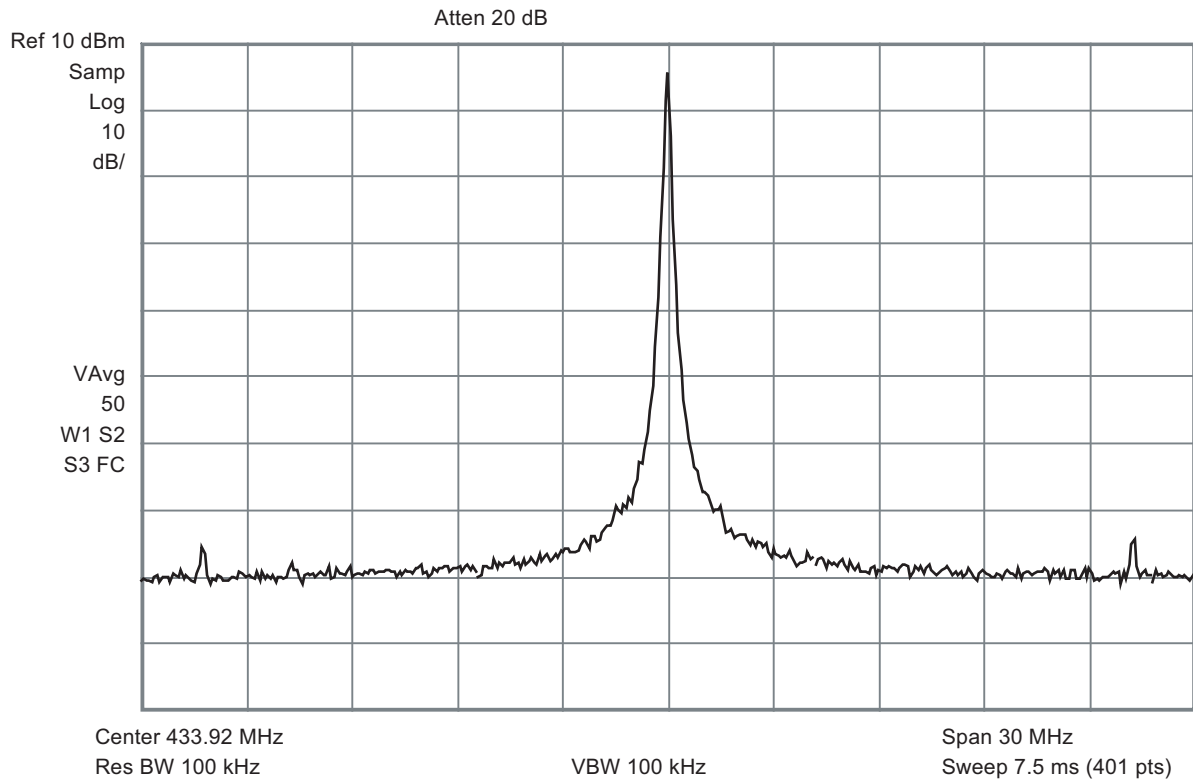
Care must be taken regarding the harmonics of the CLK output signal as well as to the harmonics produced by a microprocessor clocked with it, since these harmonics can disturb the reception of signals. In a single channel system using FREQ = 3803 to 4053 ensures that harmonics of this signal, do not disturb the receive mode.
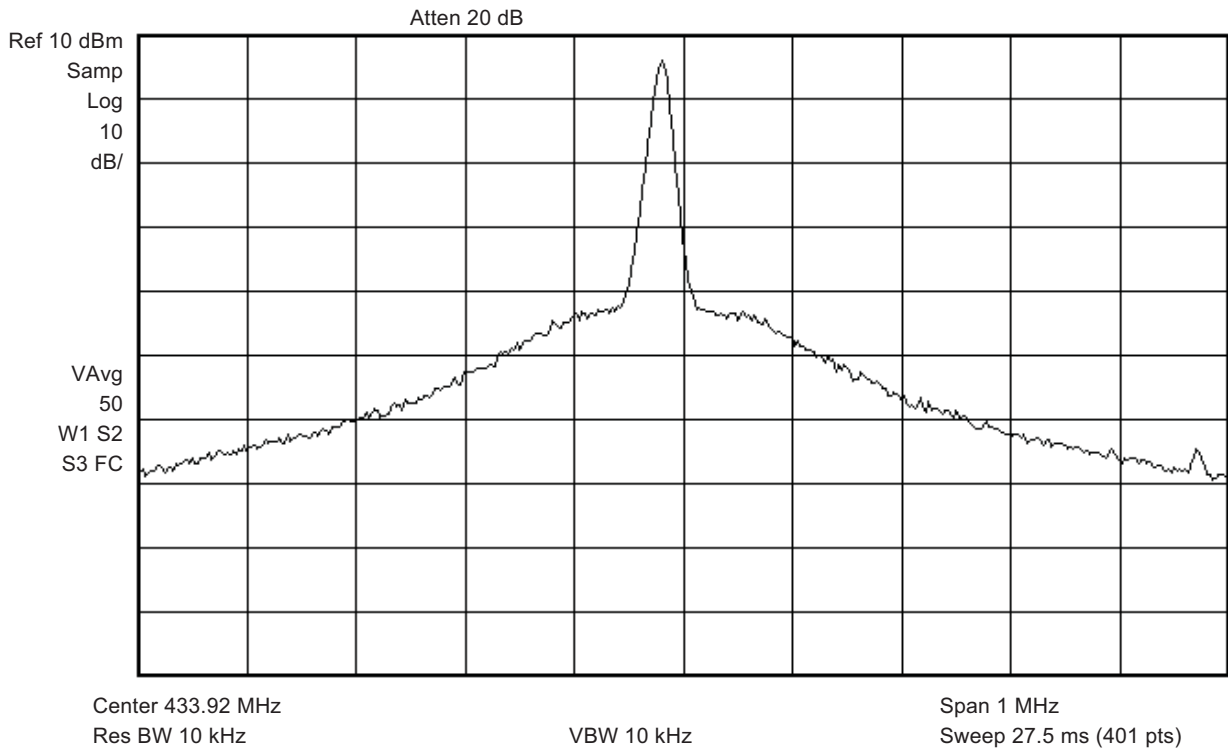
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5.12 FSK/ASK Transmission

Due to the fast modulation capability of the synthesizer and the high resolution, the carrier can be internally FSK modulated which simplifies the application of the transceiver. The deviation of the transmitted signal is ±24 digital frequency steps of the synthesizer which is equal to ±18.65kHz for 315MHz and ±19.41kHz for 433.92MHz.

Due to closed loop modulation with PLL filtering, the modulated spectrum is very clean, meeting ETSI and CEPT regulations when using a simple LC filter for the power amplifier harmonics as it is shown in Figure 4-1. In ASK mode the frequency is internally connected to the center of the FSK transmission and the power amplifier is switched on and off to perform the modulation. Figure 5-9 to Figure 5-11 on page 18 show the spectrum of the FSK modulation with pseudo-random data with 20Kbit/s/±19.41kHz/Manchester and 5dBm output power.

Figure 5-9. FSK-modulated TX Spectrum (433.92MHz/20Kbit/s/±19.41kHz/Manchester Code)

Figure 5-10. Unmodulated TX Spectrum 433.92MHz - 19.41kHz (f$_{FSK\_L}$)

Atten 20 dB

Ref 10 dBm
Samp
Log
10
dB/

VAvg
50
W1 S2
S3 FC

Center 433.92 MHz   VBW 10 kHz   Span 1 MHz
Res BW 10 kHz   Sweep 27.5 ms (401 pts)

Figure 5-11. FSK-modulated TX Spectrum (433.92MHz/20Kbit/s/±19.41kHz/Manchester Code)

Atten 20 dB

Ref 10 dBm
Samp
Log
10
dB/

VAvg
50
W1 S2
S3 FC

Center 433.92 MHz   VBW 10 kHz   Span 1 MHz
Res BW 10 kHz   Sweep 27.5 ms (401 pts)

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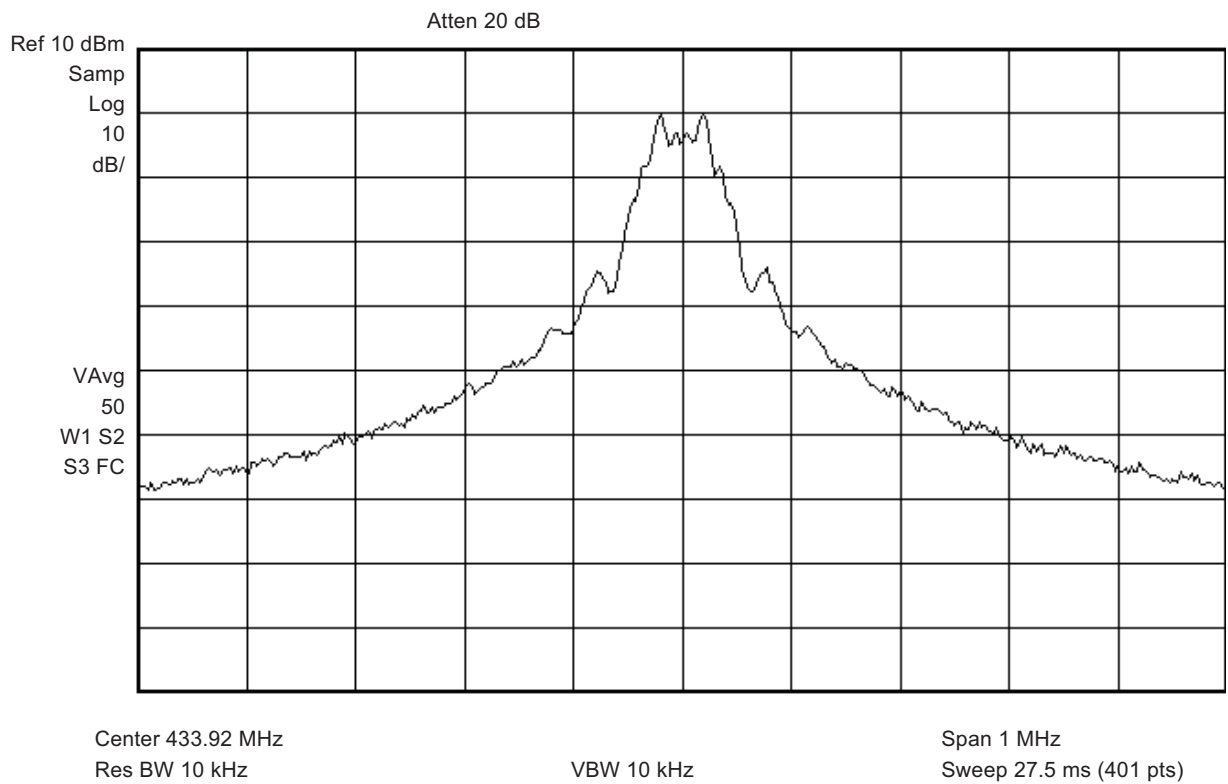
5.13 Output Power Setting and PA Matching at RF_OUT

The Power Amplifier (PA) is a single-ended open collector stage which delivers a current pulse which is nearly independent of supply voltage, temperature and tolerances due to band-gap stabilization. Resistor R_1 (see Figure 5-12 on page 20) sets a reference current which controls the current in the PA. A higher resistor value results in a lower reference current, a lower output power and a lower current consumption of the PA. The usable range of R_1 is 15kΩ to 56kΩ. The PWR_H pin switches the output power range between about 0dBm to 5dBm (PWR_H = GND) and 5dBm to 10dBm (PWR_H = AVCC) by multiplying this reference current with a factor 1 (PWR_H = GND) and 2.5 (PWR_H = AVCC) which corresponds to about 5dB more output power.

If the PA is switched off in TX mode, the current consumption without output stage and with $V_{S1} = V_{S2}$ = 3V, T_{amb} = 25°C is typically 6.95mA for 315MHz and 433.92MHz.

The maximum output power is achieved with optimum load resistances R_{Lopt} according to Table 5-7 on page 20. The compensation of the 1.0pF output capacitance of the RF_OUT pin will be achieved by absorbing it into the matching network, consisting of L_1, C_1, C_3 as shown in Figure 5-12 on page 20. There must be also a low resistive DC path to AVCC to deliver the DC current of the power amplifier's last stage. The matching of the PA output was done with the circuit according to Figure 5-12 on page 20 with the values in Table 5-7. Note that value changes of these elements may be necessary to compensate individual board layout parasitics.

Example:
According to Table 5-7 on page 20, with a frequency of 433.92MHz and output power of 11dBm, the overall current consumption is typically 17.8mA. Hence the PA needs 17.8mA - 6.95mA = 10.85mA in this mode which corresponds to an overall power amplifier efficiency of the PA of $(10^{(11dBm/10)} \times 1mW)/(3V \times 10.85mA) \times 100\%$ = 38.6% in this case.

Using a higher resistor in this example of R1 = 1.091 $\times$ 22kΩ = 24kΩ results in 9.1% less current in the PA of 10.85mA/1.091 = 9.95mA and 10 $\times$ log(1.091) = 0.38dB less output power if using a new load resistance of 300Ω $\times$ 1.091 = 327Ω. The resulting output power is then 11dBm – 0.38dB = 10.6dBm and the overall current consumption is 6.95mA + 9.95mA = 16.9mA.

The values of Table 5-7 on page 20 were measured with standard multi-layer chip inductors with quality factors Q according to Table 5-7 on page 20.

Looking to the 433.92MHz/11dBm case with the quality factor of Q_{L1} = 43 the loss in this inductor L_1 is estimated with the parallel equivalent resistance of the inductor $R_{loss} = 2 \times \pi \times f \times L1 \times Q_{L1}$ and the matching loss with 10 log (1 + R_{Lopt}/R_{loss}) which is equal to 0.32dB losses in this inductor. Taking this into account the PA efficiency is then 42% instead of 38.6%.

Be aware that the high power mode (PWR_H = AVCC) can only be used with a supply voltage higher than 2.7V, whereas the low power mode (PWR_H = GND) can be used down to 2.15V as can be seen in the section "Electrical Characteristics: General" on page 61.

The supply blocking capacitor C_2 (10nF) in Figure 5-12 on page 20 has to be placed close to the matching network because of the RF current flowing through it.

An internal programmable resistor SETPWR is programmable with the control register 8, described in Table 9-25 on page 39. It can be used in conjunction with an external resistor to adjust the output power by connection it. To do that the output power should be adjusted with an external resistor about 50% lower than needed for the target output power and reduced with the programmable resistor during production test until the target power is as close as possible to the target. For example, if using 433.92MHz at 5dBm, a resistor of 12k instead of 24k is used and values of PWSET between 25 and 29 can be used to achieve an output power within 5dBm ±0.5dB over production. Note that this resistor is temperature stable but has tolerances of ±20% and introduces, therefore, additional output power tolerances, it is recommended to adjust output power during the production test if using the SETPWR resistor.

Figure 5-12. Power Setting and Output Matching
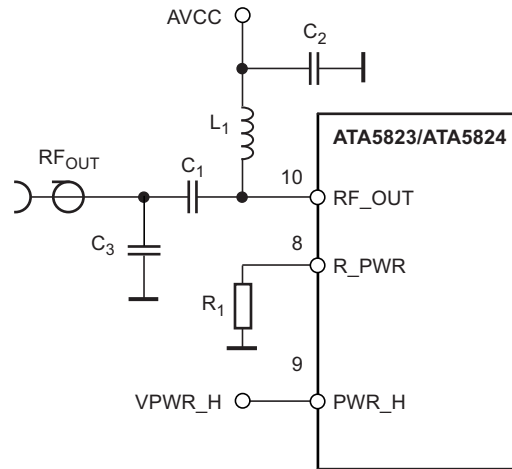
Table 5-7. Measured Output Power and Current Consumption with $V_{S1} = V_{S2} = 3V$, $T_{amb} = 25°C$

Frequency (MHz)	TX Current (mA)	Output Power (dBm)	R1 (kΩ)	VPWR_H	R_{Lopt} (Ω)	L_1 (nH)	Q_{L1}	C_1 (pF)	C_3 (pF)
315	8.5	0.4	56	0	2500	82	28	1.5	0
315	10.5	5.7	27	0	920	68	32	2.2	0
315	16.7	10.5	27	AVCC	350	56	35	3.9	0
433.92	8.6	0.1	56	0	2300	56	40	0.75	0
433.92	11.2	6.2	22	0	890	47	38	1.5	0
433.92	17.8	11	22	AVCC	300	33	43	2.7	0

5.14 Output Power and TX Supply Current versus Supply Voltage and Temperature

Table 5-8 shows the measurement of the output power for a typical device with $V_{S1} = V_{S2} = V_S$ in the 433.92MHz and 6.2dBm case versus temperature and supply voltage measured according to Figure 5-12 on page 20 with components according to Table 5-7 on page 20. As opposed to the receiver sensitivity the supply voltage has here the major impact on output power variations because of the large signal behavior of a power amplifier. Thus a 5V system using the internal voltage regulator shows much less variation than a 2.15V to 3.6V battery system because the AVCC supply voltage is 3.25V ±0.25V for a 5V system.

The reason is that the amplitude at the output RF_OUT with optimum load resistance is AVCC – 0.4V and the power is proportional to $(AVCC – 0.4V)^2$ if the load impedance is not changed. This means that the theoretical output power reduction if reducing the supply voltage from 3.0V to 2.15V is $10 \log ((3V – 0.4V)^2/(2.15V – 0.4V)^2) = 3.4dB$. Table 5-8 shows that principle behavior in the measurements. This is not the same case for higher voltages, since here, increasing the supply voltage from 3V to 3.6V should theoretical increase the power by 1.8dB, but only 0.9dB in the measurements shows that the amplitude does not increase with the supply voltage because the load impedance is optimized for 3V and the output amplitude stays more constant because of the current source nature of the output.

Table 5-8.   Measured Output Power and Supply Current at 433.92MHz, PWR_H = GND

$V_S = V_{S1} = V_{S2}$	2.15V	3.0V	3.6V
T_{amb} = –40°C	9.25mA 3.2dBm	10.19mA 5.5dBm	10.78mA 6.2dBm
T_{amb} = +25°C	10.2mA 3.4dBm	11.19mA 6.2dBm	11.79mA 7.1dBm
T_{amb} = +105°C	10.9mA 3.0dBm	12.02mA 5.4dBm	12.73mA 6.3dBm

Table 5-9 shows the relative changes of the output power of a typical device compared to 3.0V/25°C. As can be seen, a temperature change to –40°C as well as to +105°C reduces the power by less than 1dB due to the band-gap regulated output current. Measurements of all the cases in Table 5-7 on page 20 overtemperature and supply voltage have shown about the same relative behavior as shown in Table 5-9.

Table 5-9.   Measurements of Typical Output Power Relative to 3V/25°C

| $V_S = V_{S1} = V_{S2}$	2.15V	3.0V	3.6V
T_{amb} = –40°C	–3.0dB	–0.7dB	0dB
T_{amb} = +25°C	–2.8dB	0dB	+0.9dB
T_{amb} = +105°C	–3.2dB	–0.8dB	+0.1dB

5.15   RX/TX Switch

The RX/TX switch decouples the LNA from the PA in TX mode, and directs the received power to the LNA in RX mode. To do this, it has a low impedance to GND in TX mode and a high impedance to GND in RX mode. The pin 38 (RX_TX2) must always be connected to GND in the application. To design a proper RX/TX decoupling a linear simulation tool for radio frequency design together with the measured device impedances of Table 5-1 on page 10, Table 5-7 on page 20, Table 5-10 on page 21 and Table 5-11 on page 22 should be used. The exact element values have to be found on board. Figure 5-13 on page 21 shows an approximate equivalent circuit of the switch. The principal switching operation is described here according to the application of Figure 3-1 on page 7. The application of Figure 4-1 on page 8 works similarly.

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Table 5-10.   Impedance of the RX/TX Switch RX_TX2 Shorted to GND

Frequency	Z(RX_TX1) TX mode	Z(RX_TX1) RX mode
315MHz	$(4.8 + j3.2)\Omega$	$(11.3 – j214)\Omega$
433.92MHz	$(4.5 + j4.3)\Omega$	$(10.3 – j153)\Omega$

Figure 5-13. Equivalent Circuit of the Switch
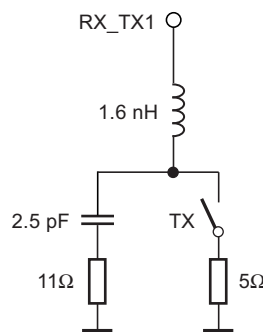
5.16 Matching Network in TX Mode

In TX mode the 20mm long and 0.4mm wide transmission line which is much shorter than $\lambda/4$ is approximately switched in parallel to the capacitor C_9 to GND. The antenna connection between C_8 and C_9 has an impedance of about 50Ω looking from the transmission line into the loop antenna with pin RF_OUT, L_2, C_{10}, C_8 and C_9 connected (using a C_9 without the added 7.6pF capacitor as discussed later). The transmission line can be approximated with a 16nH inductor in series with a 1.5Ω resistor, the closed switch can be approximated according to Table 5-10 with the series connection of 1.6nH and 5Ω in this mode. To have a parallel resonant high impedance circuit with little RF power going into it looking, from the loop antenna into the transmission line a capacitor of about 7.6pF to GND is needed at the beginning of the transmission line (this capacitor is later absorbed into C_9, which is then higher as needed for 50Ω transformation). To keep the 50Ω impedance in RX mode at the end of this transmission line C_7 has to be also about 7.6pF. This reduces the TX power by about 0.5dB at 433.92MHz compared to the case where the LNA path is completely disconnected.

5.17 Matching Network in RX Mode

In RX mode the RF_OUT pin has a high impedance of about $7k\Omega$ in parallel with 1.0pF at 433.92MHz as can be seen in Table 5-11 on page 22. This together with the losses of the inductor L_2 with 120nH and $Q_{L2} = 25$ gives about $3.7k\Omega$ loss impedance at RF_OUT. Since the optimum load impedance in TX mode for the power amplifier at RF_OUT is 890Ω the loss associated with the inductor L_2 and the RF_OUT pin can be estimated to be $10 \times \log(1 + 890/3700) = 0.95$dB compared to the optimum matched loop antenna without L_2 and RF_OUT. The switch represents, in this mode at 433.92MHz, about an inductor of 1.6nH in series with the parallel connection of 2.5pF and $2.0k\Omega$. Since the impedance level at pin RX_TX1 in RX mode is about 50Ω there is only a negligible damping of the received signal by about 0.1dB. When matching the LNA to the loop antenna the transmission line and the 7.6pF part of C_9 has to be taken into account when choosing the values of C_{11} and L_1 so that the impedance seen from the loop antenna into the transmission line with the 7.6pF capacitor connected is 50Ω.

Since the loop antenna in RX mode is loaded by the LNA input impedance the loaded Q of the loop antenna is lowered by about a factor of 2 in RX mode hence the antenna bandwidth is higher than in TX mode.

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Table 5-11. Impedance RF_OUT Pin in RX mode

Frequency	Z(RF_OUT)RX	$R_P//C_P$
315MHz	$36\Omega - j\,502\Omega$	$7k\Omega//1.0pF$
433.92MHz	$19\Omega - j\,366\Omega$	$7k\Omega//1.0pF$

Note that if matching to 50Ω, like in Figure 4-1 on page 8, a high Q wire wound inductor with a Q > 70 should be used for L_2 to minimize its contribution to RX losses which will otherwise be dominant. The RX and TX losses will be in the range of 1.0dB there.

6. XTO

The XTO is an amplitude regulated Pierce oscillator type with integrated load capacitances (2×18pF with a tolerance of $\pm 17\%$) hence $C_{Lmin} = 7.4$pF and $C_{Lmax} = 10.6$pF. The XTO oscillation frequency f_{XTO} is the reference frequency FREF for the fractional-N synthesizer. When designing the system in terms of receiving and transmitting frequency offset the accuracy of the crystal and XTO have to be considered.

The synthesizer can adjust the local oscillator frequency for the initial frequency error in f_{XTO}. This is done at nominal supply voltage and temperature with the control registers 2 and 3 (see and). The remaining local oscillator tolerance at nominal supply voltage and temperature is then < ± 0.5ppm. The XTO's gm has very low influence of less than ± 2ppm on the frequency at nominal supply voltage and temperature.

In a single channel system less than ± 150ppm should be corrected to avoid that harmonics of the CLK output disturb the receive mode. If the CLK is not used, or carefully layouted on the application PCB (as needed for multi channel systems), more than ± 150ppm can be compensated.

The additional XTO pulling is only ± 2ppm, overtemperature and supply voltage. The XTAL versus temperature and its aging is then the main source of frequency error in the local oscillator.

The XTO frequency depends on XTAL properties and the load capacitances $C_{L1,\,2}$ at pin XTAL1 and XTAL2. The pulling of f_{XTO} from the nominal f_{XTAL} is calculated using the following formula
:

$$P = \frac{C_m}{2} \times \frac{C_{LN} - C_L}{(C_0 + C_{LN}) \times (C_0 + C_L)} \times 10^6 \text{ ppm.}$$

C_m is the crystal's motional, C_0 the shunt and C_{LN} the nominal load capacitance of the XTAL found in its datasheet. C_L is the total actual load capacitance of the crystal in the circuit and consists of C_{L1} and C_{L2} in series connection.

Figure 6-1. XTAL with Load Capacitances

$$C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2})$$
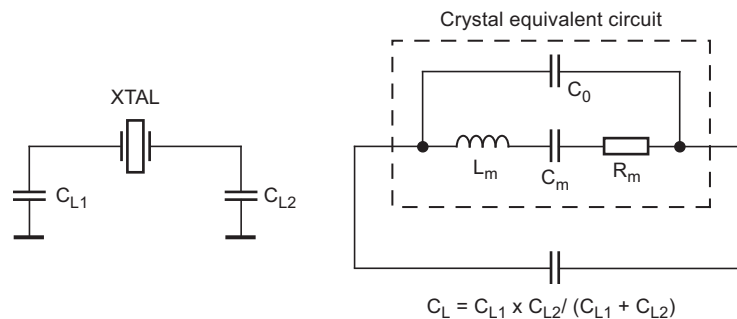
With $C_m \le 14$fF, $C_0 \ge 1.5$pF, $C_{LN} = 9$pF and $C_L = 7.4$pF to 10.6pF the pulling amounts to $P \le \pm 100$ppm and with $C_m \le 7$fF, $C_0 \ge 1.5$pF, $C_{LN} = 9$pF and $C_L = 7.4$pF to 10.6pF the pulling is $P \le \pm 50$ppm.

Since typical crystals have less than ± 50ppm tolerance at 25°C, the compensation is not critical and can, in both cases, be done with the ± 150ppm.

C_0 of the XTAL has to be lower than $C_{Lmin}/2 = 3.7$pF for a Pierce oscillator type in order to not enter the steep region of pulling versus load capacitance where there is a risk of an unstable oscillation.

To ensure proper start-up behavior the small signal gain, and thus the negative resistance provided by this XTO at start is very large. For example oscillation starts up, even in worst case, with a crystal series resistance of 1.5kΩ at $C_0 \le 2.2$pF with this XTO. The negative resistance is approximately given by

$$\text{Re}\{Z_{XTOcore}\} = \text{Re}\left\{\frac{Z_1 \times Z_3 + Z_2 \times Z_3 + Z_1 \times Z_2 \times Z_3 \times g_m}{Z_1 + Z_2 + Z_3 + Z_1 \times Z_2 \times g_m}\right\}$$

with Z_1, Z_2 as complex impedances at pin XTAL1 and XTAL2 hence
$Z_1 = -j/(2 \times \pi \times f_{XTO} \times C_{L1}) + 5\Omega$ and $Z_2 = -j/(2 \times \pi \times f_{XTO} \times C_{L2}) + 5\Omega$.

Z_3 consists of crystals C_0 in parallel with an internal 110kΩ resistor hence
$Z_3 = -j/(2 \times \pi \times f_{XTO} \times C_0) /110k\Omega$, gm is the internal transconductance between XTAL1 and XTAL2 with typically 19ms at 25°C.

With f_{XTO} = 13.5MHz, gm = 19ms, C_L = 9pF, C_0 = 2.2pF this results in a negative resistance of about 2kΩ. The worst case for technological, supply voltage and temperature variations is then for $C_0 \leq$ 2.2pF always higher than 1.5kΩ.

Due to the large gain at start, the XTO is able to meet a very low start-up time. The oscillation start-up time can be estimated with the time constant τ.

$$\tau = \frac{2}{4 \times \pi^2 \times f_m^2 \times C_m \times (\text{Re}(Z_{XTOcore}) + R_m)}$$

After 10τ to 20τ, an amplitude detector detects the oscillation amplitude and sets XTO_OK to High if the amplitude is large enough. This activates the CLK output if CLK_ON and CLK_EN in control register 3 are High (see Table 9-12 on page 35). Note that the necessary conditions of the DVCC voltage also have to be fulfilled (see Figure 6-2 on page 24 and Figure 7-1 on page 27).

To save current in IDLE and Sleep mode, the load capacitors partially are switched off in this modes with S_1 and S_2 seen in Figure 6-2 on page 24.

It is recommended to use a crystal with C_m = 3.0fF to 7.0fF, C_{LN} = 9pF, R_m < 120Ω and C_0 = 1.0pF to 2.2pF.

Lower values of C_m can be used, this increases slightly the start-up time. Lower values of C_0 or higher values of C_m (up to 15fF) can also be used, this has only little influence to pulling.

Figure 6-2. XTO Block Diagram
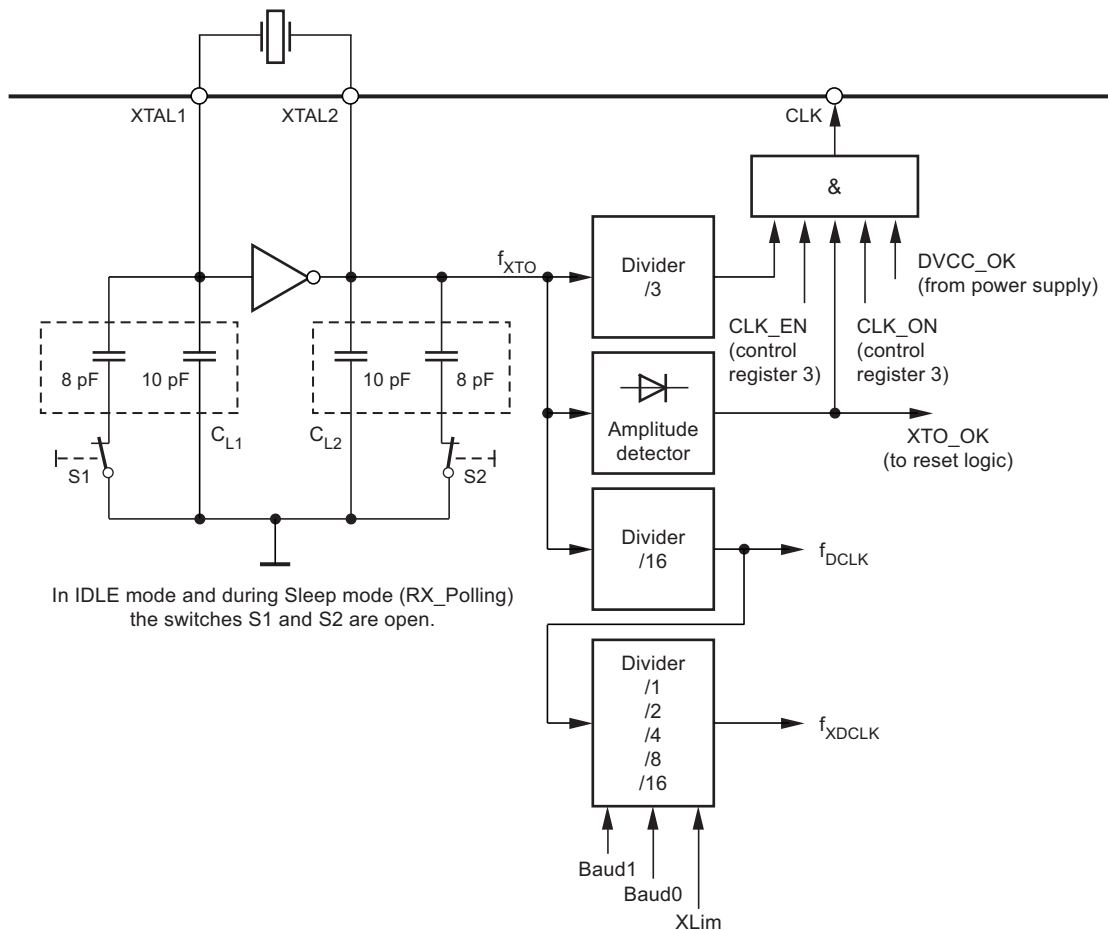
To find the right values used in the control registers 2 and 3 (see Table 9-7 on page 34 and Table 9-10 on page 35) the relationship between f_{XTO} and the f_{RF} is shown in Table 6-1. To determine the right content, the frequency at pin CLK, as well as the output frequency at RF_OUT in ASK mode can be measured, than the FREQ value can be calculated according to Table 6-1 so that f_{RF} is exactly the desired radio frequency.

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Table 6-1. Calculation of f_{RF}

Frequency (MHz)	Pin 6 433_N868	CREG1 Bit(4) FS	f_{XTO} (MHz)	$f_{RF} = f_{TX\_ASK} = f_{RX}$	$f_{TX\_FSK\_L} = f_{TX\_FSK\_L(FD)}$	$f_{TX\_FSK\_H}$	$f_{TX\_FSK\_H(FD)}$	Frequency Resolution
315.0	AVCC	1	12.73193	$f_{XTO} \times \left(24,5 + \dfrac{FREQ + 24,5}{16384}\right)$	$f_{RF} -$ 18.65kHz	$f_{RF} +$ 18.65 kHz	$f_{RF} +$ 208.23kHz	777.1Hz
433.92	AVCC	0	13.25311	$f_{XTO} \times \left(32,5 + \dfrac{FREQ + 24,5}{16384}\right)$	$f_{RF} -$ 19.41kHz	$f_{RF} +$ 19.41kHz	$f_{RF} +$ 203.74kHz	808.9Hz

The variable FREQ depends on the bit PLL_MODE in control register 1 and the parameter FREQ2 and FREQ3, which are defined by the bits FR0 to FR12 in control register 2 and 3 and is calculated as follows:

FREQ = FREQ2 + FREQ3

Care must be taken with the harmonics of the CLK output signal f_{CLK}, as well as to the harmonics produced by an microprocessor clocked with it, since these harmonics can disturb the reception of signals if they get to the RF input. In a single channel system the use of FREQ = 3803 to 4053 ensures that harmonics of this signal do not disturb the receive mode. In a multichannel system the CLK signal can either be not used or carefully layouted on the application PCB. The supply voltage of the microcontroller must also be carefully blocked in a multichannel system.

6.1 Pin CLK

Pin CLK is an output to clock a connected microcontroller. The clock frequency f_{CLK} is calculated as follows:

$$f_{CLK} = \frac{f_{XTO}}{3}$$

The signal at CLK output has a nominal 50% duty cycle.

If the bit CLK_EN in control register 3 is set to 0, the clock is disabled permanently.

If the bit CLK_EN is set to 1 and bit CLK_ON (control register 3) is set to 0, the clock is disabled as well. If bit CLK_ON is set to 1 and thus the clock is enabled if the Bit-check is ok (RX, RX Polling, FD mode (Slave)), an event on pin N_PWR_ON occurs or the bit Power_On in the status register is 1.

Figure 6-3. Clock Timing