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ATA6562/3

High-Speed CAN Transceiver with Standby Mode

Features

- Fully ISO 11898-2, ISO 11898-2: 2016 and SAE J2962-2 Compliant
- CAN FD Ready
- Communication Speed up to 5 Mbps
- Low Electromagnetic Emission (EME) and High Electromagnetic Immunity (EMI)
- Differential Receiver with Wide Common Mode Range
- ATA6562: Silent Mode
- Remote Wake-Up Capability via CAN Bus - Wake-Up on Pattern (WUP), as Specified in ISO 11898-2: 2016, 3.8 µs Activity Filter Time
- Functional Behavior Predictable under All Supply Conditions
- Transceiver Disengages from the Bus When Not Powered Up
- RXD Recessive Clamping Detection
- High Electrostatic Discharge (ESD) Handling Capability on the Bus Pins
- Bus Pins Protected Against Transients in Automotive Environments
- Transmit Data (TXD) Dominant Time-Out Function
- Undervoltage Detection on VCC and VIO Pins
- CANH/CANL Short-Circuit and Overtemperature Protected
- Fulfills the OEM “Hardware Requirements for LIN, CAN and FlexRay Interfaces in Automotive Applications, Rev. 1.3"
- Qualified According to AEC-Q100
- Two Ambient Temperature Grades Available:
  - ATA6562-GAQW1, ATA6563-GAQW1, ATA6562-GBQW1 and ATA6563-GBQW1 up to T_{amb} = +125°C
  - ATA6562-GAQW0, ATA6563-GAQW0, ATA6562-GBQW0 and ATA6563-GBQW0 up to T_{amb} = +150°C
- Packages: SOIC8, VDFN8 with Wettable Flanks (Moisture Sensitivity Level 1)

Applications

Classical CAN and CAN FD networks in Automotive, Industrial, Aerospace, Medical and Consumer applications.

General Description

The ATA6562/ATA6563 is a high-speed CAN transceiver that provides an interface between a controller area network (CAN) protocol controller and the physical two-wire CAN bus.

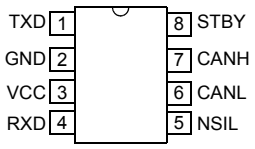
The transceiver is designed for high-speed (up to 5 Mbps) CAN applications in the automotive industry, providing differential transmit and receive capability to (a microcontroller with) a CAN protocol controller. It offers improved electromagnetic compatibility (EMC) and electrostatic discharge (ESD) performance, as well as features such as:

- Ideal passive behavior to the CAN bus when the supply voltage is off
- Direct interfacing to microcontrollers with supply voltages from 3V to 5V (ATA6563)

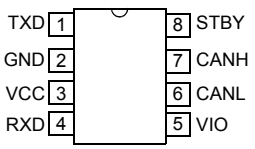
Three operating modes together with the dedicated fail-safe features make the ATA6562/ATA6563 an excellent choice for all types of high-speed CAN networks, especially in nodes requiring low-power mode with wake-up capability via the CAN bus.

Package Types

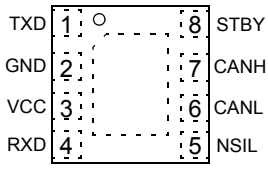
ATA6562
SOIC



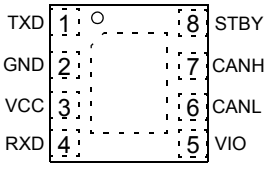
ATA6563
SOIC



ATA6562
3 x 3 VDFN* with wettable flanks



ATA6563
3 x 3 VDFN* with wettable flanks



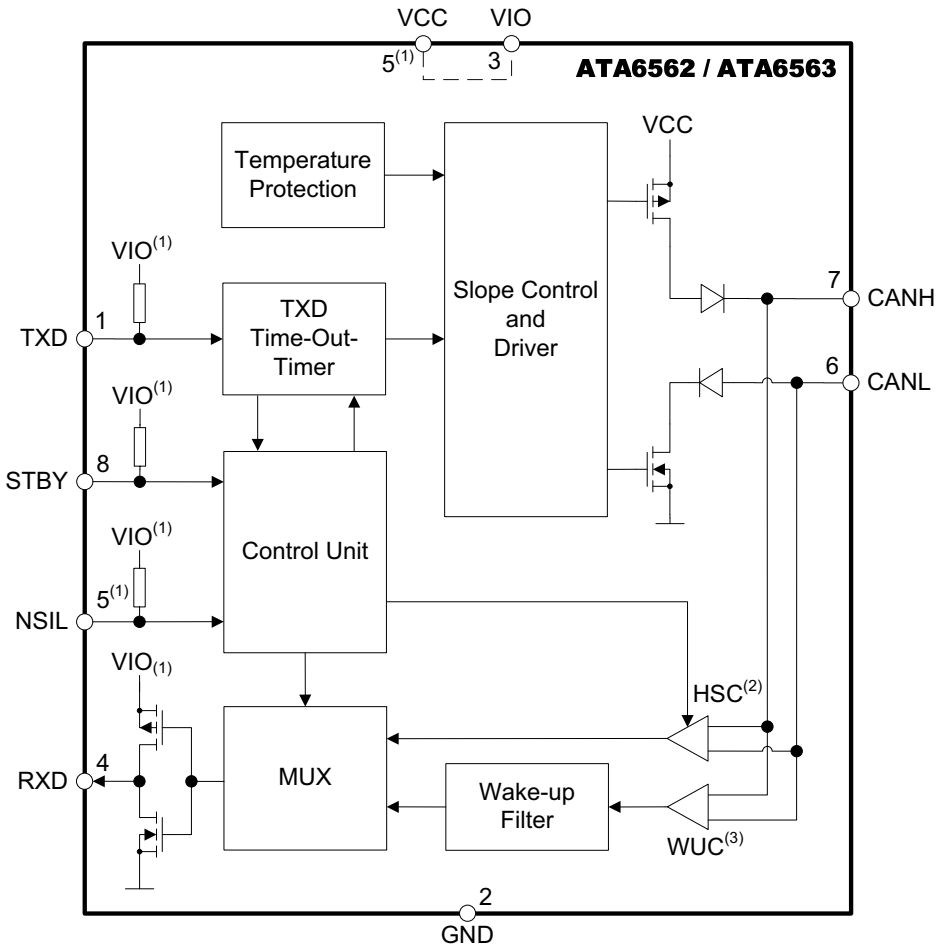
*Includes Exposed Thermal Pad (EP); see Table 1-2.

ATA6562/ATA6563 Family Members

Device	VIO Pin	NSIL	Grade 0	Grade 1	VDFN8	SOIC8	Description
ATA6562-GAQW0		X	X			X	Standby mode and Silent mode
ATA6562-GAQW1		X		X		X	Standby mode and Silent mode
ATA6562-GBQW0		X	X		X		Standby mode and Silent mode
ATA6562-GBQW1		X		X	X		Standby mode and Silent mode
ATA6563-GAQW0	X		X			X	Standby mode, VIO - pin for compatibility with 3.3V and 5V microcontroller
ATA6563-GAQW1	X			X		X	Standby mode, VIO - pin for compatibility with 3.3V and 5V microcontroller
ATA6563-GBQW0	X		X		X		Standby mode, VIO-pin for compatibility with 3.3V and 5V microcontroller
ATA6563-GBQW1	X			X	X		Standby mode, VIO - pin for compatibility with 3.3V and 5V microcontroller

Note: For ordering information, see the Product Identification System section.

Functional Block Diagram



Notes: 1. Pin 5: ATA6563: VIO
ATA6562: NSIL (the VIO line and the VCC line are internally connected)
2. HSC: High-speed comparator
3. WUC: Wake-up comparator

1.0 FUNCTIONAL DESCRIPTION

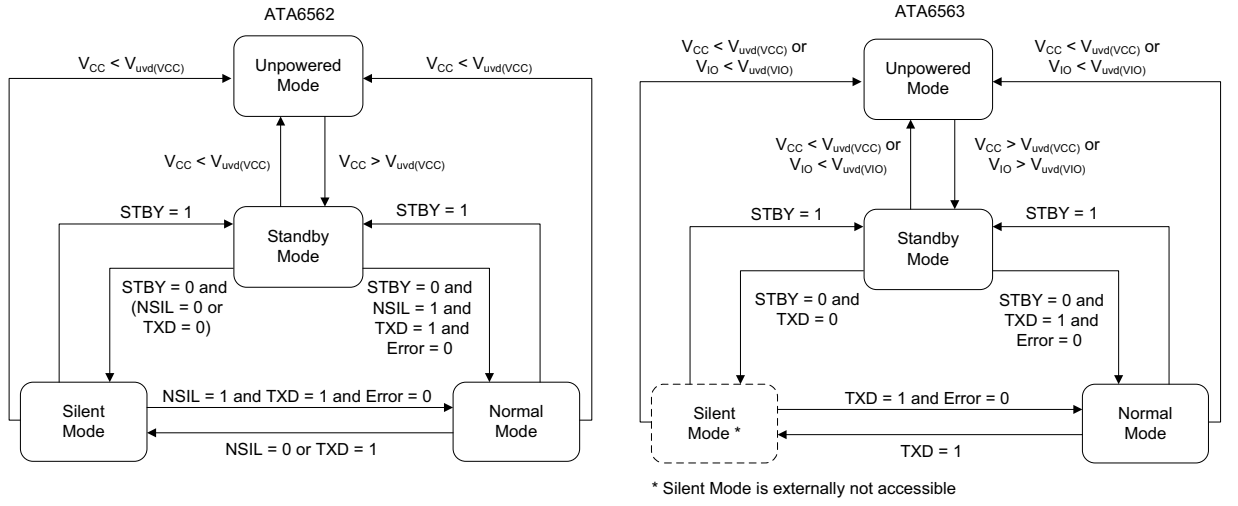
The ATA6562/ATA6563 is a stand-alone dual high-speed CAN transceiver compliant with the ISO 11898-2, ISO 11898-2: 2016, ISO 11898-5 and SAE J2962-2 CAN standards. It provides a very low current consumption in Standby mode and wake-up capability via the CAN bus. There are two versions available, only differing in the function of pin 5:

- ATA6562: The pin 5 is the control input for Silent mode NSIL, allowing the ATA6562 to only receive data but not send data via the bus. The output driver stage is disabled. The VIO line and the VCC line are internally connected, this sets the signal levels of the TXD, RXD, STBY, and NSIL pins to levels compatible with 5V microcontrollers.
- ATA6563: The pin 5 is the VIO pin and should be connected to the microcontroller supply voltage. This allows direct interfacing to microcontrollers with supply voltages down to 3V and adjusts the signal levels of the TXD, RXD, and STBY pins to the I/O levels of the microcontroller. The I/O ports are supplied by the VIO pin.

1.1 Operating Modes

Each of the transceivers supports three operating modes: Unpowered, Standby and Normal. The ATA6562 additionally has the Silent mode. These modes can be selected via the STBY and NSIL pin. See Figure 1-1 and Table 1-1 for a description of the operating modes.

FIGURE 1-1: OPERATING MODES



Note: For the ATA6563 NSIL is internally set to “1”.

TABLE 1-1: OPERATING MODES

Mode	Inputs			Outputs	
	STBY	NSIL	PIN TXD	CAN Driver	Pin RXD
Unpowered	X(3)	X(3)	X(3)	Recessive	Recessive
Standby	HIGH	X(3)	X(3)	Recessive	Active(4)
Silent (only for ATA6562)	LOW	LOW	X(3)	Recessive	Active(1)
Normal	LOW	HIGH(2)	LOW	Dominant	LOW
	LOW	HIGH(2)	HIGH	Recessive	HIGH

Note 1: LOW if the CAN bus is dominant, HIGH if the CAN bus is recessive.
2: Internally pulled up if not bonded out.
3: Irrelevant
4: Reflects the bus only for wake-up

1.1.1 NORMAL MODE

A low level on the STBY pin together with a high level on pin TXD selects the Normal mode. In this mode the transceiver is able to transmit and receive data via the CANH and CANL bus lines (see Functional Block Diagram). The output driver stage is active and drives data from the TXD input to the CAN bus. The high-speed comparator (HSC) converts the analog

data on the bus lines into digital data which is output to pin RXD. The bus biasing is set to $V_{VCC}/2$ and the undervoltage monitoring of VCC is active.

The slope of the output signals on the bus lines is controlled and optimized in a way that guarantees the lowest possible electromagnetic emission (EME).

To switch the device in normal operating mode, set the STBY pin to low and the TXD pin to high (see Table 1-1 and Figure 1-2). The STBY pin provides a pull-up resistor to VIO, thus ensuring a defined level if the pin is open.

Please note that the device cannot enter Normal mode as long as TXD is at ground level.

The switching into Normal mode is depicted in the following two figures.

FIGURE 1-2: SWITCHING FROM STANDBY MODE TO NORMAL MODE (NSIL = HIGH)

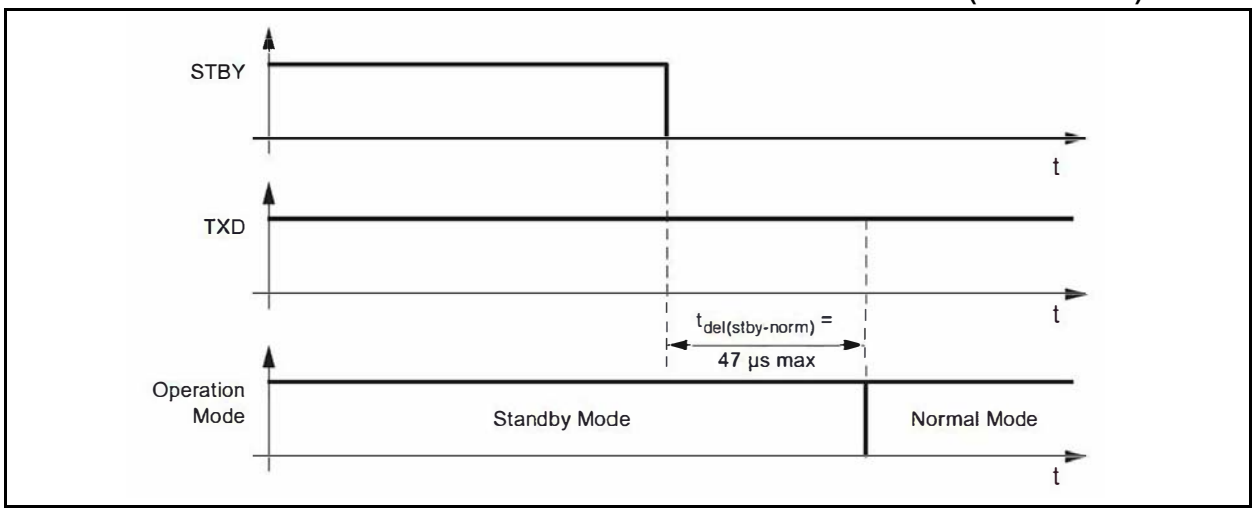
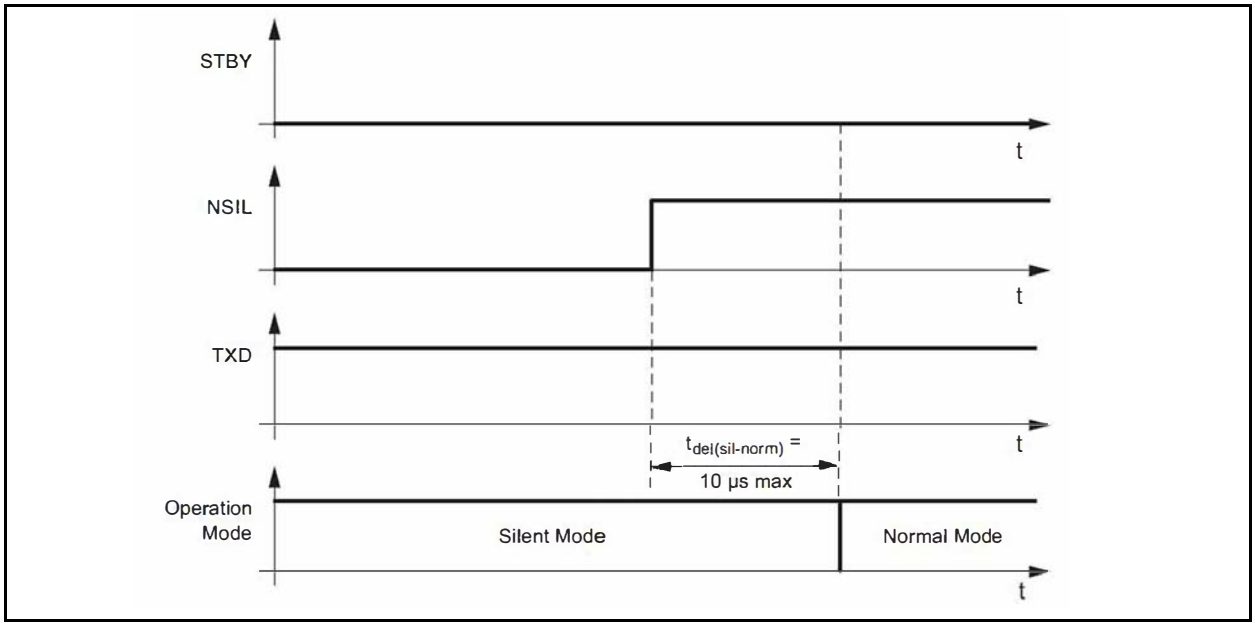


FIGURE 1-3: SWITCHING FROM SILENT MODE TO NORMAL MODE



1.1.2 SILENT MODE (ONLY WITH THE ATA6562)

A low level on the NSIL pin (available on pin 5) and on the STBY pin selects Silent mode. This receive-only mode can be used to test the connection of the bus medium. In Silent mode the ATA6562 can still receive data from the bus, but the transmitter is disabled and therefore no data can be sent to the CAN bus. The bus pins are released to recessive state. All other IC

functions, including the high-speed comparator (HSC), continue to operate as they do in Normal mode. Silent mode can be used to prevent a faulty CAN controller from disrupting all network communications.

1.1.3 STANDBY MODE

A high level on the STBY pin selects Standby mode. In this mode the transceiver is not able to transmit or correctly receive data via the bus lines. The transmitter and the high-speed comparator (HSC) are switched off to reduce current consumption.

For ATA6562 only: In the event the NSIL input pin is set to low in Standby mode, the internal pull-up resistor causes an additional quiescent current from VIO to GND. Microchip recommends setting the NSIL pin to high in Standby mode.

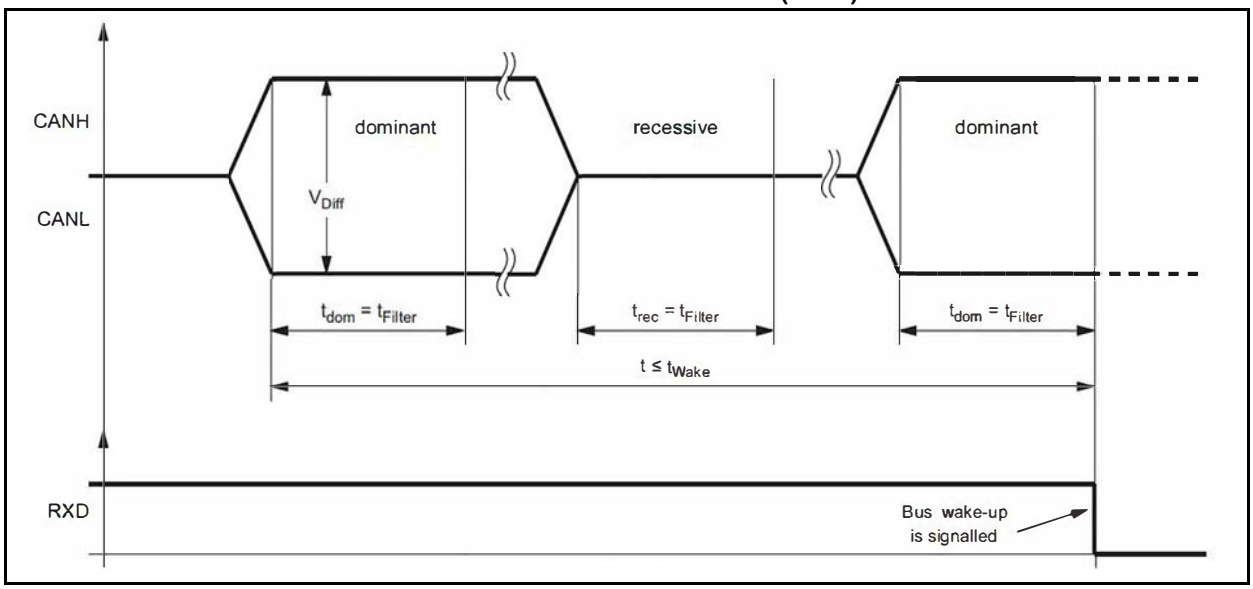
1.1.3.1 Remote Wake-up via the CAN Bus

In Standby mode the bus lines are biased to ground to reduce current consumption to a minimum. The ATA6562/ATA6563 monitors the bus lines for a valid wake-up pattern as specified in the ISO 11898-2: 2016. This filtering helps to avoid spurious wake-up events, which would be triggered by scenarios such as a dominant clamped bus or by a dominant phase due to noise, spikes on the bus, automotive transients or EMI.

The wake-up pattern consists of at least two consecutive dominant bus levels for a duration of at least t_{Filter}, each separated by a recessive bus level with a duration of at least t_{Filter}. Dominant or recessive bus levels shorter than t_{Filter} are always being ignored. The complete dominant-recessive-dominant pattern as shown in Figure 1-4, must be received within the bus wake-up time-out time t_{Wake} to be recognized as a valid wake-up pattern. Otherwise, the internal wake-up logic is reset and then the complete wake-up pattern must be retransmitted to trigger a wake-up event. Pin RXD remains at high level until a valid wake-up event has been detected.

During Normal mode, at a VCC undervoltage condition or when the complete wake-up pattern is not received within t_{Wake}, no wake-up is signalled at the RXD pin.

FIGURE 1-4: TIMING OF THE BUS WAKE-UP PATTERN (WUP) IN STANDBY MODE



When a valid CAN wake-up pattern is detected on the bus, the RXD pin switches to low to signal a wake-up request. A transition to Normal mode is not triggered until the STBY pin is forced back to low by the microcontroller.

1.2 Fail-safe Features

1.2.1 TXD DOMINANT TIME-OUT FUNCTION

A TXD dominant time-out timer is started when the TXD pin is set to low. If the low state on the TXD pin persists for longer than $t_{to(dom)TXD}$, the transmitter is disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when the the TXD pin is set to high. If the low state on the TXD pin was longer than $t_{to(dom)TXD}$, then the TXD pin has to be set to high longer 4 µs in order to reset the TXD dominant time-out timer..

1.2.2 INTERNAL PULL-UP STRUCTURE AT THE TXD AND STBY INPUT PINS

The TXD and STBY pins have an internal pull-up to VIO. This ensures a safe, defined state in case one or both pins are left floating. Pull-up currents flow in these

pins in all states, meaning all pins should be in high state during Standby mode to minimize the current consumption.

1.2.3 UNDERVOLTAGE DETECTION ON PIN VCC

If V_{VCC} or V_{VIO} drops below its undervoltage detection levels ($V_{uvd(VCC)}$ and $V_{uvd(VIO)}$)(see Section 2.0, Electrical Characteristics), the transceiver switches off and disengages from the bus until V_{VCC} and V_{VIO} has recovered. The low-power wake-up comparator is only switched off during a VCC and VIO undervoltage. The logic state of the STBY pin is ignored until the V_{VCC} voltage or V_{VIO} voltage has recovered.

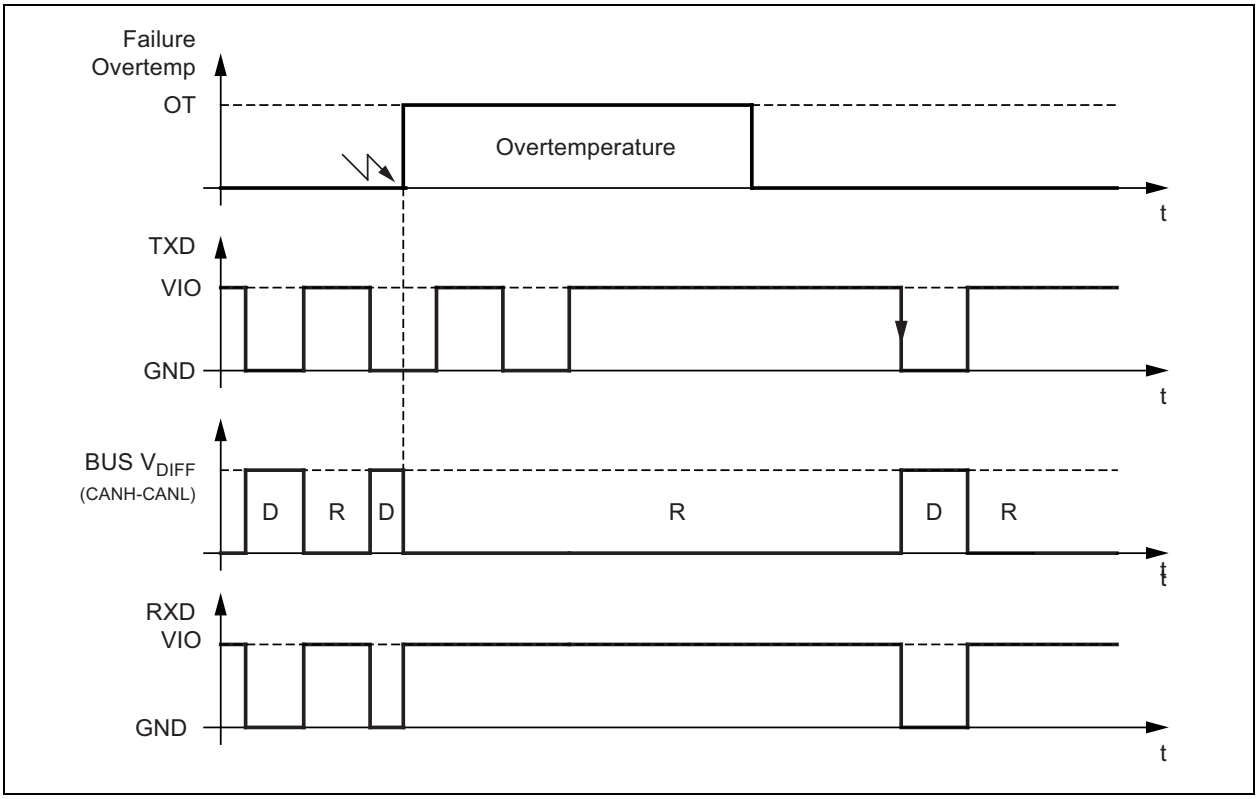
1.2.4 BUS WAKE UP ONLY AT DEDICATED WAKE-UP PATTERN

Due to the implementation of the wake-up filtering the ATA6562/ATA6563 does not wake-up when the bus is in a long dominant phase, it only wakes up at a dedicated wake-up pattern as specified in the ISO 11898-2: 2016. This means for a valid wake-up at least two consecutive dominant bus levels for a duration of at least t_{Filter}, each separated by a recessive bus level with a duration of at least t_{Filter} must be received via the bus. Dominant or recessive bus levels shorter than t_{Filter} are always being ignored. The complete dominant-recessive-dominant pattern as shown in Figure 1-4, must be received within the bus wake-up time-out time t_{Wake} to be recognized as a valid wake-up pattern. This filtering leads to a higher robustness against EMI and transients and reduces therefore the risk of an unwanted bus wake- up significantly.

1.2.5 OVERTEMPERATURE PROTECTION

The output drivers are protected against overtemperature conditions. If the junction temperature exceeds the shutdown junction temperature, T_{Jsd}, the output drivers are disabled until the junction temperature drops below T_{Jsd} and pin TXD is at high level again. The TXD condition ensures that output driver oscillations due to temperature drift are avoided.

FIGURE 1-5: RELEASE OF TRANSMISSION AFTER OVERTEMPERATURE CONDITION



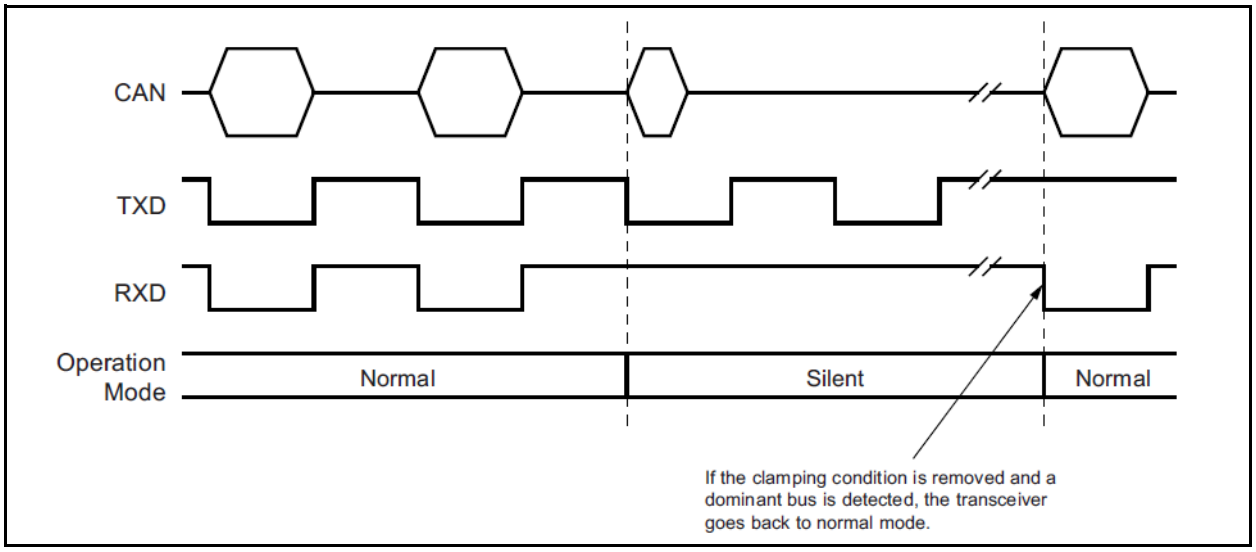
1.2.6 SHORT-CIRCUIT PROTECTION OF THE BUS PINS

The CANH and CANL bus outputs are short-circuit protected, either against GND or a positive supply voltage. A current-limiting circuit protects the transceiver against damage. If the device is heating up due to a continuous short on CANH or CANL, the internal overtemperature protection switches the bus transmitter off.

1.2.7 RXD RECESSIVE CLAMPING

This fail-safe feature prevents the controller from sending data on the bus if its RXD is clamped to HIGH (e.g., recessive). That is, if the RXD pin cannot signalize a dominant bus condition because it is e.g, shorted to VCC, the transmitter within ATA6562/ATA6563 is disabled to avoid possible data collisions on the bus. In Normal and Silent mode (only ATA6562), the device permanently compares the state of the high-speed comparator (HSC) with the state of the RXD pin. If the HSC indicates a dominant bus state for more than t_{RC_det} without the RXD pin doing the same, a recessive clamping situation is detected and the transceiver is forced into Silent mode. This Fail-safe mode is released by either entering Standby or Unpowered mode or if the RXD pin is showing a dominant (e.g., low) level again.

FIGURE 1-6: RXD RECESSIVE CLAMPING DETECTION



1.3 Pin Description

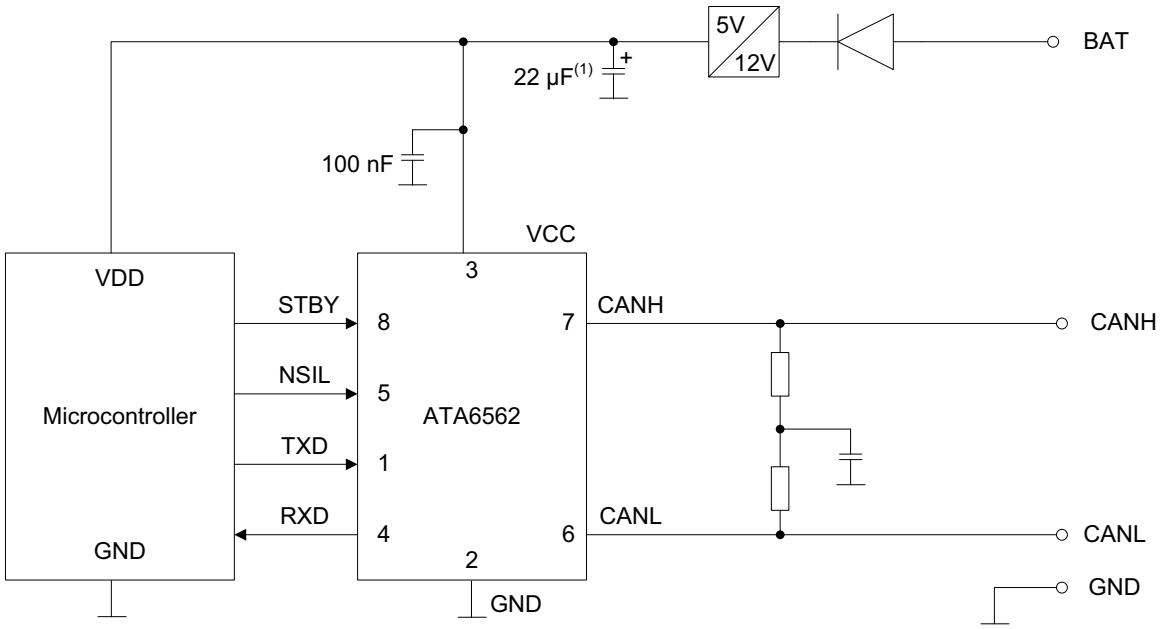
The descriptions of the pins are listed in Table 1-2.

TABLE 1-2: PIN FUNCTION TABLE

ATA6562		ATA6563		Pin Name	Description
SOIC8	VDFN8	SOIC8	VDFN8		
1	1	1	1	TXD	Transmit data input
2	2	2	2	GND	Ground1 supply
3	3	3	3	VCC	Supply voltage
4	4	4	4	RXD	Receive data output; reads out data from the bus lines
—	—	5	5	VIO	Supply voltage for I/O level adapter
5	5	—	—	NSIL	Silent mode control input (low active);
6	6	6	6	CANL	Low-level CAN bus line
7	7	7	7	CANH	High-level CAN bus line
8	8	8	8	STBY	Standby mode control input
—	9	—	9	EP	Exposed Thermal Pad: Heat slug, internally connected to the GND pin.

1.4 Typical Application

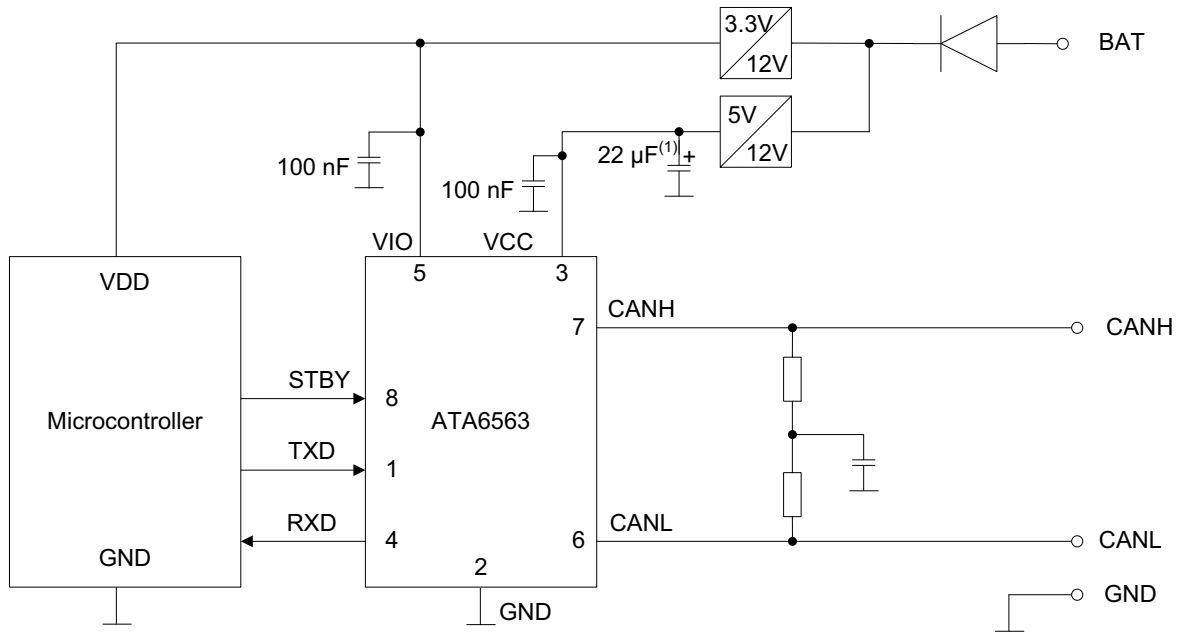
Typical Application ATA6562



(1) The size of this capacitor depends on the used external voltage regulator

Note: For VDFN8 package: EP (heatslug) must always be connected to GND.

Typical Application ATA6563



(1) The size of this capacitor depends on the used external voltage regulator

Note: For VDFN8 package: EP (heatslug) must always be connected to GND.

2.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

DC Voltage at CANH, CANL (V_{CANH}, V_{CANL}) .....–27 to +42V
Transient Voltage at CANH, CANL (according to ISO 7637 part 2) (V_{CANH}, V_{CANL}) .....–150 to +100V
Max. differential bus voltage (V_{Diff}).....–5 to +18V
DC voltage on all other pins (V_X) .....–0.3 to +5.5V
ESD according to IBEE CAN EMC - Test specification following IEC 61000-4-2 — Pin CANH, CANL .....±8 kV
ESD (HBM following STM5.1 with 1.5 kΩ/100 pF) - Pins CANH, CANL to GND..... ±6 kV
Component Level ESD (HBM according to ANSI/ESD STM5.1, JESD22-A114, AEC-Q100 (002) .....±4 kV
CDM ESD STM 5.3.1 .....±750V
ESD machine model AEC-Q100-RevF(003).....±200V
Virtual Junction Temperature (T_{VJ}).....–40 to +175°C
Storage Temperature Range (T_{stg}) .....-55°C to +150°C

† Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 2-1: ELECTRICAL CHARACTERISTICS

Electrical Specifications: The values below are valid for each of the two identical integrated CAN transceivers.
Grade 1: T_{amb} = -40°C to +125°C and Grade 0: T_{amb} = -40°C to +150°C; V_{VCC} = 4.5V to 5.5V; R_L = 60Ω, C_L = 100 pF unless specified otherwise; all voltages are defined in relation to ground; positive currents flow into the IC.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply, Pin VCC						
Supply Voltage	V_{VCC}	4.5	—	5.5	V	
Supply Current in Silent Mode	I_{VCC_sil}	1.9	2.5	3.0	mA	Silent mode, $V_{TXD} = V_{VIO}$
Supply Current in Normal Mode	I_{VCC_rec}	2	—	5	mA	recessive, $V_{TXD} = V_{VIO}$
	I_{VCC_dom}	30	50	70	mA	dominant, V_{TXD} = 0V
	I_{VCC_short}	—	—	85	mA	short between CANH and CANL(**Note 1**)
Supply Current in Standby Mode	I_{VCC_STBY}	—	—	12	µA	VCC = VIO, $V_{TXD} = V_{NSIL} = V_{VIO}$
	I_{VCC_STBY}	—	7	—	µA	T_a = 25°C (**Note 3**)
Undervoltage Detection Threshold on Pin VCC	$V_{uvd(VCC)}$	2.75	—	4.5	V	
I/O Level Adapter Supply, Pin VIO (only with the ATA6563)						
Supply voltage on pin VIO	V_{VIO}	2.8	—	5.5	V	
Supply current on pin VIO	I_{VIO_rec}	10	80	250	µA	Normal and Silent mode recessive, $V_{TXD} = V_{VIO}$
	I_{VIO_dom}	50	350	500	µA	Normal and Silent mode dominant, V_{TXD} = 0V
	I_{VIO_STBY}	—	—	1	µA	Standby mode

Note 1: 100% correlation tested
2: Characterized on samples
3: Design parameter

TABLE 2-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: The values below are valid for each of the two identical integrated CAN transceivers.

Grade 1: T_{amb} = -40°C to +125°C and Grade 0: T_{amb} = -40°C to +150°C; V_{VCC} = 4.5V to 5.5V; R_L = 60Ω, C_L = 100 pF unless specified otherwise; all voltages are defined in relation to ground; positive currents flow into the IC.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Undervoltage detection threshold on pin VIO	$V_{uvd(VIO)}$	1.3	—	2.7	V	
Mode Control Input, Pin NSIL and STBY						
High-level Input Voltage	V_{IH}	$0.7 \times V_{VIO}$	—	$V_{VIO}+0.3$	V	
Low-level Input Voltage	V_{IL}	–0.3	—	$0.3 \times V_{VIO}$	V	
Pull- up Resistor to VCC	R_{pu}	75	125	175	kΩ	V_{STBY} = 0V, V_{NSIL} = 0V
High-level Leakage Current	I_L	–2	—	+2	µA	$V_{STBY} = V_{VIO}$, $V_{NSIL} = V_{VIO}$
CAN Transmit Data Input, Pin TXD						
High-level Input Voltage	V_{IH}	$0.7 \times V_{VIO}$	—	$V_{VIO}+0.3$	V	
Low-level Input Voltage	V_{IL}	–0.3	—	$0.3 \times V_{VIO}$	V	
Pull-up Resistor to VCC	R_{TXD}	20	35	50	kΩ	V_{TXD} = 0V
High-level Leakage Current	I_{TXD}	–2	—	+2	µA	Normal mode, $V_{TXD} = V_{VIO}$
Input Capacitance	C_{TXD}	—	5	10	pF	Note 3
CAN Receive Data Output, Pin RXD						
High-level Output Current	I_{OH}	–8	—	–1	mA	Normal mode, $V_{RXD} = V_{VIO} – 0.4V$, $V_{VIO} = V_{VCC}$
Low-level Output Current, Bus Dominant	I_{OL}	2	—	12	mA	Normal mode, V_{RXD} = 0.4V, bus dominant
Bus Lines, Pins CANH and CANL						
Single Ended Dominant Output Voltage	$V_{O(dom)}$	2.75	3.5	4.5	V	V_{TXD} = 0V, $t < t_{to(dom)TXD}$ R_L = 50Ω to 65Ω pin CANH (**Note 1**)
		0.5	1.5	2.25	V	V_{TXD} = 0V, $t < t_{to(dom)TXD}$ R_L = 50Ω to 65Ω pin CANL (**Note 1**)
Transmitter Voltage Symmetry	V_{Sym}	0.9	1.0	1.1		$V_{Sym} = (V_{CANH} + V_{CANL}) / V_{VCC}$ (**Note 3**)
Bus Differential Output Voltage	V_{Diff}	1.5	—	3	V	V_{TXD} = 0V, $t < t_{to(dom)TXD}$ R_L = 45Ω to 65Ω
		1.5	—	3.3	V	R_L = 70Ω (**Note 3**)
		1.5	—	5	V	R_L = 2240Ω (**Note 3**)
		–50	—	+50	mV	V_{VCC} = 4.75V to 5.25V $V_{TXD} = V_{VIO}$, receive, no load
Recessive Output Voltage	$V_{O(rec)}$	2	0.5* V_{VCC}	3	V	Normal and Silent mode, $V_{TXD} = V_{VIO}$, no load
	$V_{O(rec)}$	–0.1	—	+0.1	V	Standby mode, $V_{TXD} = V_{VIO}$, no load

Note 1: 100% correlation tested

2: Characterized on samples

3: Design parameter

TABLE 2-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: The values below are valid for each of the two identical integrated CAN transceivers.

Grade 1: T_{amb} = -40°C to +125°C and Grade 0: T_{amb} = -40°C to +150°C; V_{VCC} = 4.5V to 5.5V; R_L = 60Ω, C_L = 100 pF unless specified otherwise; all voltages are defined in relation to ground; positive currents flow into the IC.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Differential Receiver Threshold Voltage	$V_{th(RX)dif}$	0.5	0.7	0.9	V	Normal and Silent mode (HSC), $V_{cm(CAN)}$ = –27V to +27V
	$V_{th(RX)dif}$	0.4	0.7	1.1	V	Standby mode (WUC), $V_{cm(CAN)}$ = –27V to +27V(**Note 1**)
Differential Receiver Hysteresis Voltage	$V_{hys(RX)dif}$	50	120	200	mV	Normal and Silent mode (HSC), $V_{cm(CAN)}$ = –27V to +27V (**Note 1**)
Dominant Output Current	$I_{IO(dom)}$	–75	—	–35	mA	V_{TXD} = 0V, t < $t_{to(dom)TXD}$, V_{VCC} = 5V pin CANH, V_{CANH} = –5V
		35	—	75	mA	V_{TXD} = 0V, t < $t_{to(dom)TXD}$, V_{VCC} = 5V pin CANL, V_{CANL} = +40V
Recessive Output Current	$I_{IO(rec)}$	–5	—	+5	mA	Normal and Silent mode, V_{TXD} = V_{VIO}, no load, V_{CANH} = V_{CANL} = –27V to +32V
Leakage Current	$I_{IO(leak)}$	–5	0	+5	µA	V_{VCC} = V_{VIO} = 0V, V_{CANH} = V_{CANL} = 5V
	$I_{IO(leak)}$	–5	0	+5	µA	VCC = VIO connected to GND with R = 47kΩ V_{CANH} = V_{CANL} = 5V(**Note 3**)
Input Resistance	R_i	9	15	28	kΩ	V_{CANH} = V_{CANL} = 4V
	R_i	9	15	28	kΩ	–2V ≤ V_{CANH} ≤ +7V, –2V ≤ V_{CANL} ≤ +7V(**Note 3**)
Input Resistance Deviation	ΔR_i	–1	0	+1	%	Between CANH and CANL V_{CANH} = V_{CANL} = 4V (**Note 1**)
	ΔR_i	–1	0	+1	%	Between CANH and CANL –2V ≤ V_{CANH} ≤ +7V, –2V ≤ V_{CANL} ≤ +7V (**Note 3**)
Differential Input Resistance	$R_{i(dif)}$	18	30	56	kΩ	V_{CANH} = V_{CANL} = 4V (**Note 1**)
	$R_{i(dif)}$	18	30	56	kΩ	–2V ≤ V_{CANH} ≤ +7V, –2V ≤ V_{CANL} ≤ +7V (**Note 3**)
Common-mode Input Capacitance	$C_{i(cm)}$	—	—	20	pF	Note 3
Differential Input Capacitance	$C_{i(dif)}$	—	—	10	pF	Note 3
Differential Bus Voltage Range for RECESSIVE State Detection	V_{Diff_rec}	–3	—	+0.5	V	Normal and Silent mode (HSC) –27V ≤ V_{CANH} ≤ +27V, –27V ≤ V_{CANL} ≤ +27V (**Note 3**)
	V_{Diff_rec}	–3	—	+0.4	V	Standby mode (WUC) –27V ≤ V_{CANH} ≤ +27V, –27V ≤ V_{CANL} ≤ +27V(**Note 3**)

Note 1: 100% correlation tested

2: Characterized on samples

3: Design parameter

TABLE 2-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: The values below are valid for each of the two identical integrated CAN transceivers.

Grade 1: T_{amb} = -40°C to +125°C and Grade 0: T_{amb} = -40°C to +150°C; V_{VCC} = 4.5V to 5.5V; R_L = 60Ω, C_L = 100 pF unless specified otherwise; all voltages are defined in relation to ground; positive currents flow into the IC.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Differential Bus Voltage Range for DOMINANT State Detection	V_{Diff_dom}	0.9	—	8.0	V	Normal and Silent mode (HSC) –27V ≤ V_{CANH} ≤ +27V, –27V ≤ V_{CANL} ≤ +27V (**Note 3**)
	V_{Diff_dom}	1.15	—	8.0	V	Standby mode (WUC) –27V ≤ V_{CANH} ≤ +27V, –27V ≤ V_{CANL} ≤ +27V (**Note 3**)
Transceiver Timing, Pins CANH, CANL, TXD, and RXD, see Figure 2-1 and Figure 2-3						
Delay Time from TXD to Bus Dominant	$t_{d(TXD-busdom)}$	40	—	130	ns	Normal mode (**Note 2**)
Delay Time from TXD to Bus Recessive	$t_{d(TXD-busrec)}$	40	—	130	ns	Normal mode (**Note 2**)
Delay Time from Bus Dominant to RXD	$t_{d(busdom-RXD)}$	20	—	100	ns	Normal mode (**Note 2**)
Delay Time from Bus Recessive to RXD	$t_{d(busrec-RXD)}$	20	—	100	ns	Normal mode (**Note 2**)
Propagation Delay from TXD to RXD	$t_{PD(TXD-RXD)}$	40	—	210	ns	Normal mode, Rising edge at pin TXD R_L = 60Ω, C_L = 100 pF
		40	—	200	ns	Normal mode, Falling edge at pin TXD R_L = 60Ω, C_L = 100 pF
	$t_{PD(TXD-RXD)}$	—	—	300	ns	Normal mode, Rising edge at pin TXD R_L = 150Ω, C_L = 100 pF (**Note 3**)
		—	—	300	ns	Normal mode, Falling edge at pin TXD R_L = 150Ω, C_L = 100pF (**Note 3**)
TXD Dominant Time-Out Time	$t_{to(dom)TXD}$	0.8	—	3	ms	V_{TXD} = 0V, Normal mode
Bus Wake-up Time-Out Time	t_{Wake}	0.8	—	3	ms	Standby mode
Min. Dominant/Recessive Bus Wake-up Time	t_{Filter}	0.5	3	3.8	µs	Standby mode
Delay Time for Standby Mode to Normal Mode Transition	$t_{del(stby-norm)}$	—	—	47	µs	Falling edge at pin STBY
Delay Time for Normal Mode to Standby Mode Transition	$t_{del(norm-stby)}$	—	—	5	µs	Rising edge at pin STBY (**Note 3**)
Delay time for Normal mode to Silent mode transition	$t_{del(norm-sil)}$	—	—	10	µs	Falling edge at pin NSIL STBY = LOW (**Note 3**)
Delay time for Silent mode to Normal mode transition	$t_{del(sil-norm)}$	—	—	10	µs	Rising edge at pin NSIL STBY = LOW (**Note 3**)
Delay time for Silent mode to Standby mode transition	$t_{del(sil-stby)}$	—	—	5	µs	Rising edge at pin STBY NSIL = LOW (**Note 3**)

Note 1: 100% correlation tested

2: Characterized on samples

3: Design parameter

TABLE 2-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: The values below are valid for each of the two identical integrated CAN transceivers.

Grade 1: T_{amb} = -40°C to +125°C and Grade 0: T_{amb} = -40°C to +150°C; V_{VCC} = 4.5V to 5.5V; R_L = 60Ω, C_L = 100 pF unless specified otherwise; all voltages are defined in relation to ground; positive currents flow into the IC.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Delay time for Standby mode to Silent mode transition	$t_{del(stby-sil)}$	—	—	47	µs	Rising edge at pin STBY NSIL = LOW (**Note 3**)
Debouncing Time for Recessive Clamping State Detection	t_{RC_det}	—	90	—	ns	V(CANH-CANL) > 900mV RXD = high (**Note 3**)
Transceiver Timing for higher Bit Rates, Pins CANH, CANL, TXD, and RXD, see Figure 2-1 and Figure 2-3, external capacitor on the RXD pin C_{RXD} ≤ 20 pF						
Recessive Bit Time on Pin RXD	$t_{Bit(RXD)}$	400	—	550	ns	Normal mode, $t_{Bit(TXD)}$ = 500 ns (**Note 1**)
		120	—	220	ns	Normal mode, $t_{Bit(TXD)}$ = 200 ns
Recessive Bit Time on the Bus	$t_{Bit(Bus)}$	435	—	530	ns	Normal mode, $t_{Bit(TXD)}$ = 500 ns (**Note 1**)
		155	—	210	ns	Normal mode, $t_{Bit(TXD)}$ = 200 ns
Receiver Timing Symmetry	Δt_{Rec}	–65	—	+40	ns	Normal mode, $t_{Bit(TXD)}$ = 500 ns $\Delta t_{Rec} = t_{Bit(RXD)} - t_{Bit(Bus)}$ (**Note 1**)
		–45	—	+15	ns	Normal mode, $t_{Bit(TXD)}$ = 200 ns $\Delta t_{Rec} = t_{Bit(RXD)} - t_{Bit(Bus)}$

Note 1: 100% correlation tested

2: Characterized on samples

3: Design parameter

TABLE 2-2: TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units
Thermal Characteristics SOIC8					
Thermal resistance Virtual Junction to Ambient	R_{thvJA}	—	145	—	K/W
Thermal Shutdown of the Bus Drivers					
ATA6562-GAQW1, ATA6563-GAQW1 (Grade 1)	T_{Jsd}	150	175	195	°C
ATA6562-GAQW0, ATA6563-GAQW0 (Grade 0)	T_{Jsd}	160	175	195	°C
Thermal Characteristics VDFN8					
Thermal Resistance Virtual Junction to Heat Slug	R_{thvJC}	—	10	—	K/W
Thermal Resistance Virtual Junction to Ambient, where Heat Slug is soldered to PCB according to JEDEC	R_{thvJA}	—	50	—	K/W
Thermal Shutdown of the Bus Drivers					
ATA6562-GBQW1, ATA6563-GBQW1 (Grade 1)	T_{Jsd}	150	175	195	°C
ATA6562-GBQW0, ATA6563-GBQW0 (Grade 0)	T_{Jsd}	160	175	195	°C

FIGURE 2-1: TIMING TEST CIRCUIT FOR THE ATA6562/3 CAN TRANSCEIVER

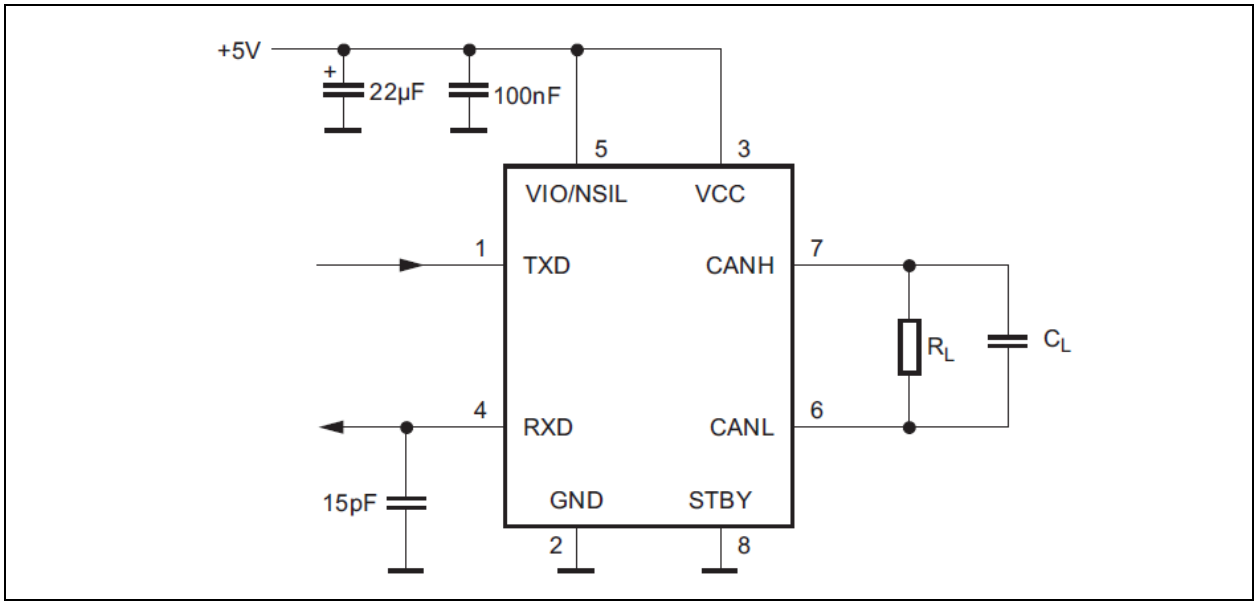


FIGURE 2-2: CAN TRANSCEIVER TIMING DIAGRAM 1

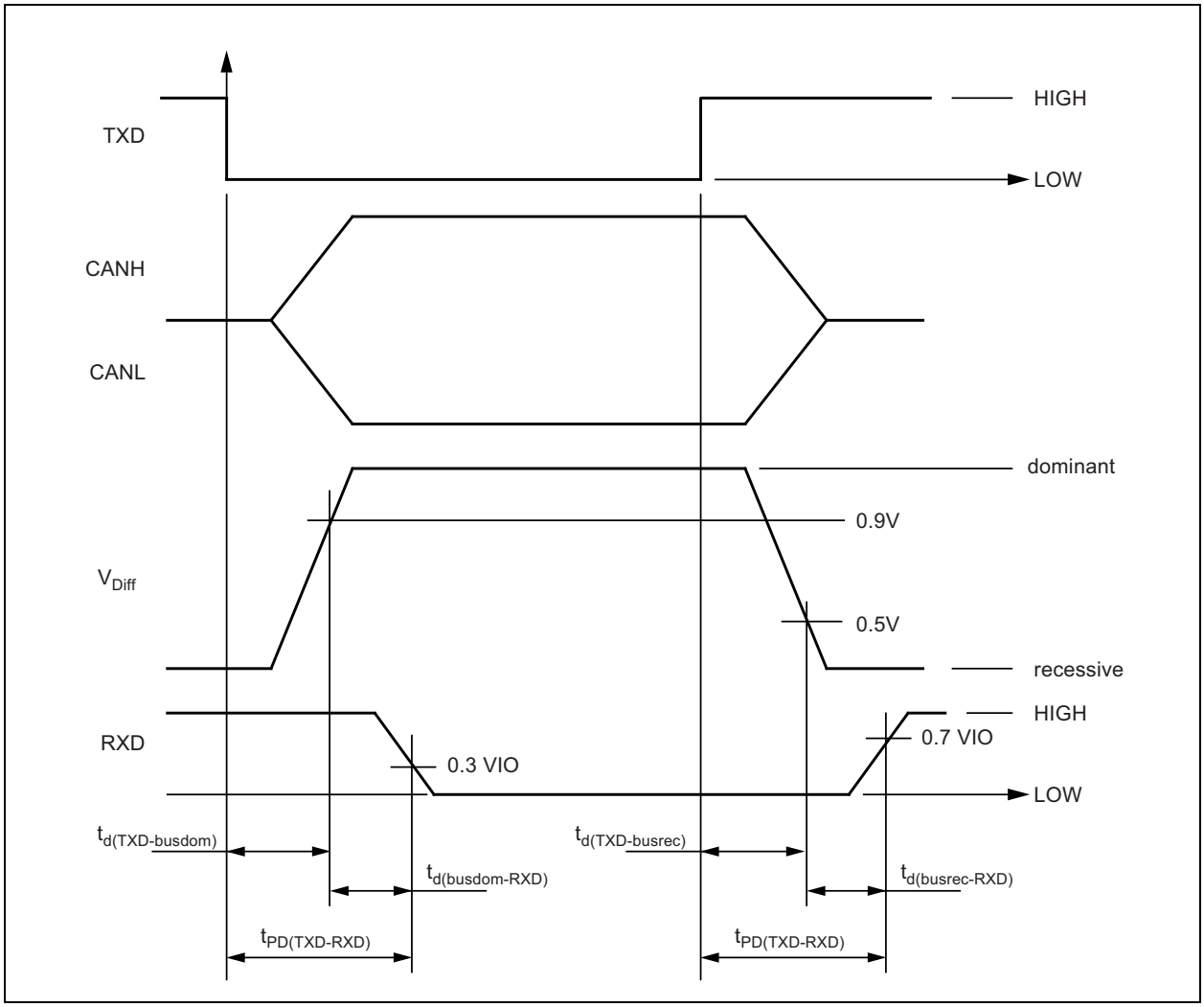
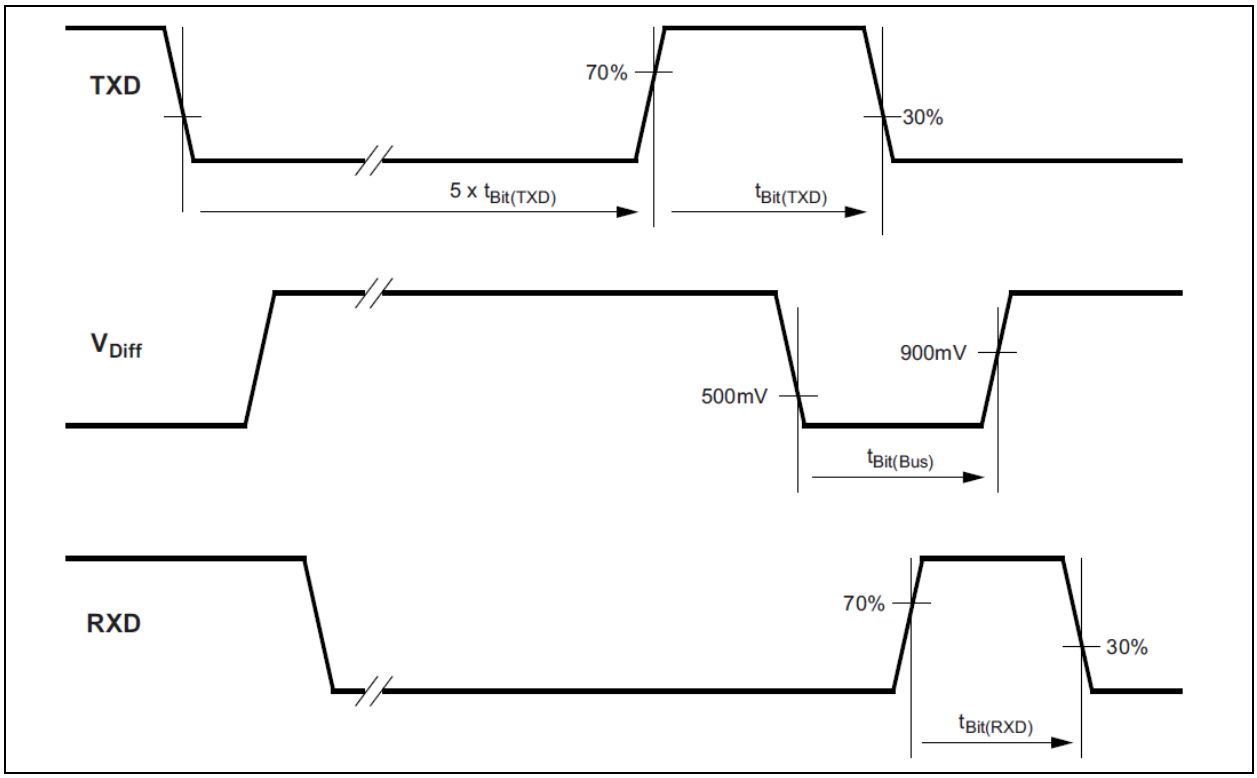


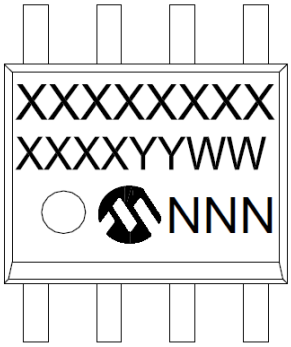
FIGURE 2-3: CAN TRANSCEIVER TIMING DIAGRAM 2



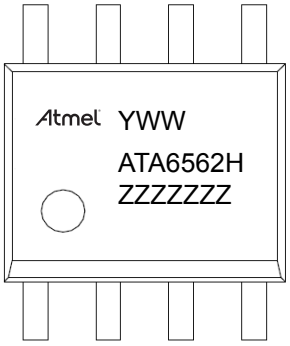
3.0 PACKAGING INFORMATION

3.1 Package Marking Information

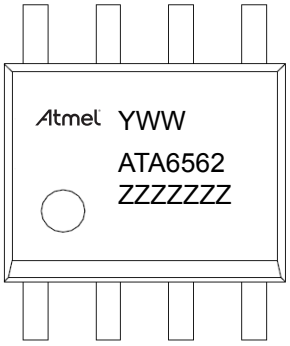
8-Lead SOIC



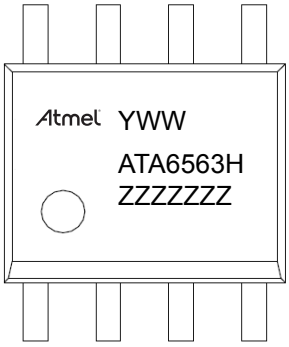
Example
ATA6562 Grade 0



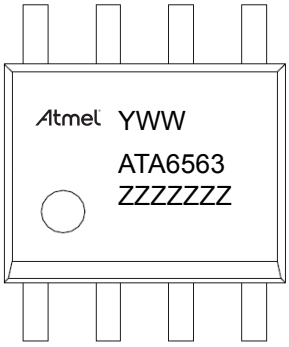
Example
ATA6562 Grade 1



Example
ATA6563 Grade 0



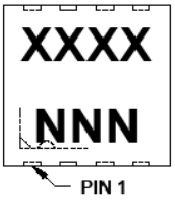
Example
ATA6563 Grade 1



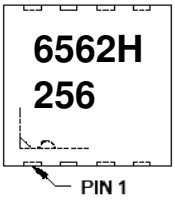
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

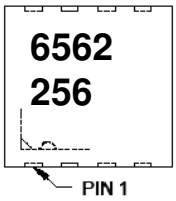
8-Lead 3 X 3 mm VDFN



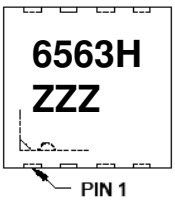
Example
ATA6562 Grade 0



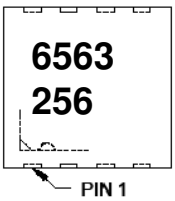
Example
ATA6562 Grade 1



Example
ATA6563 Grade 0



Example
ATA6563 Grade 1

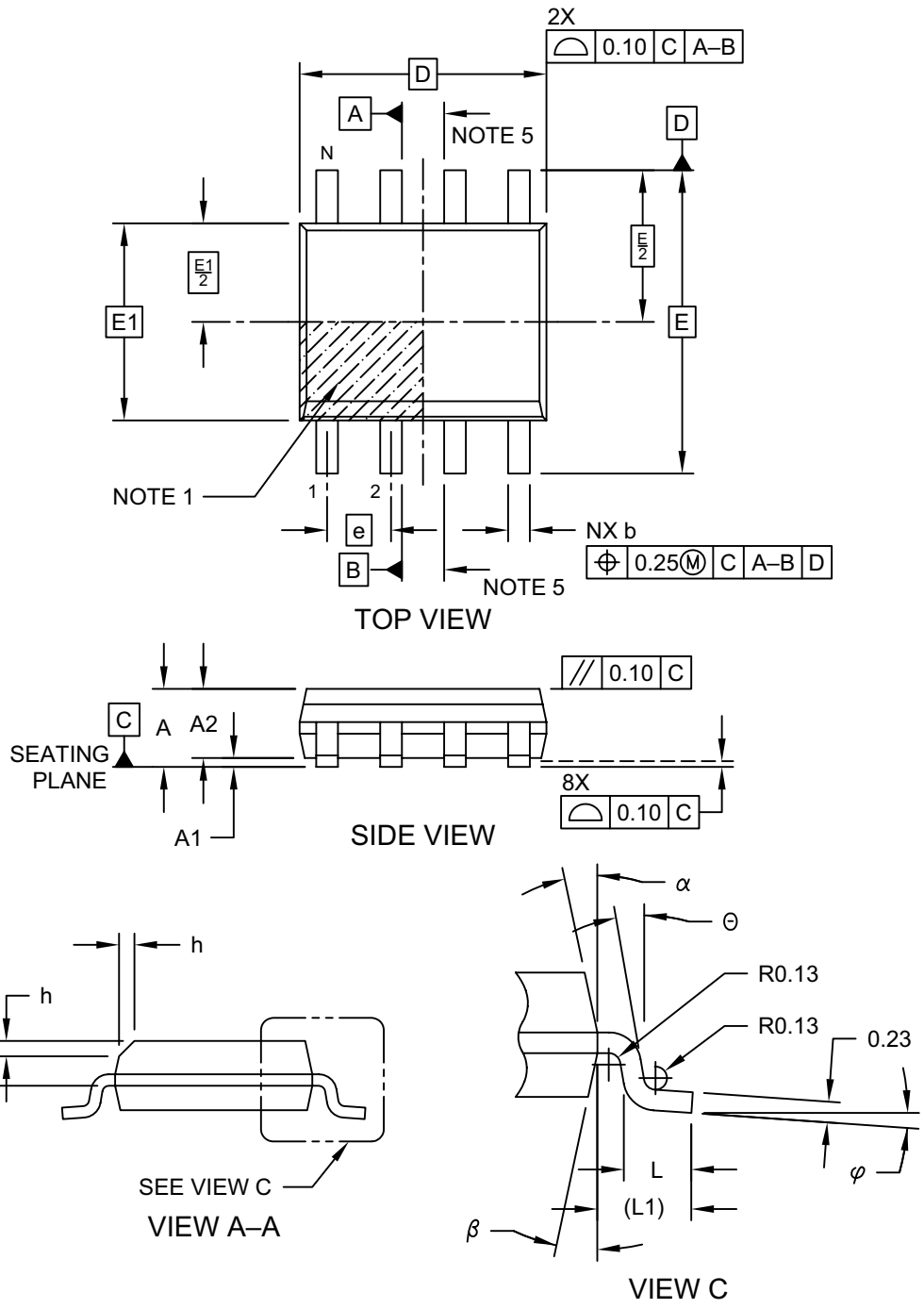


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

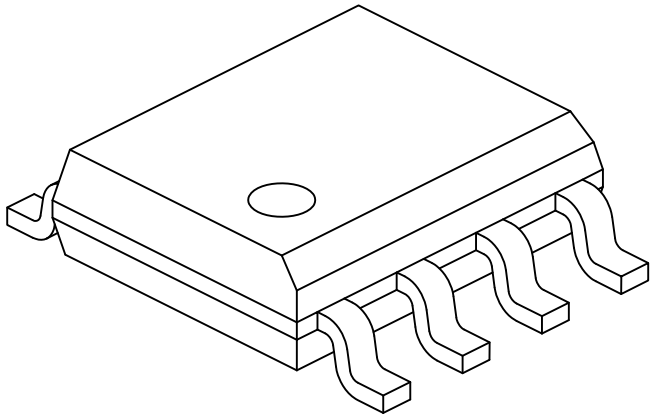
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057-SN Rev D Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

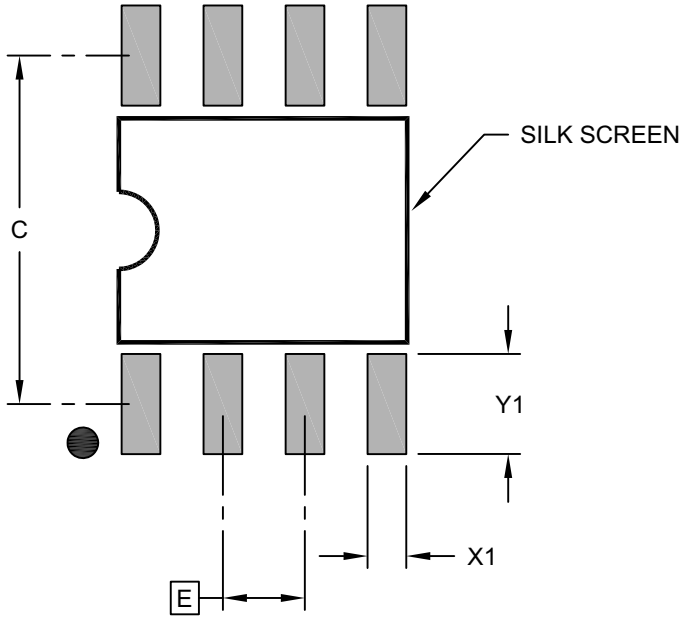
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev D Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

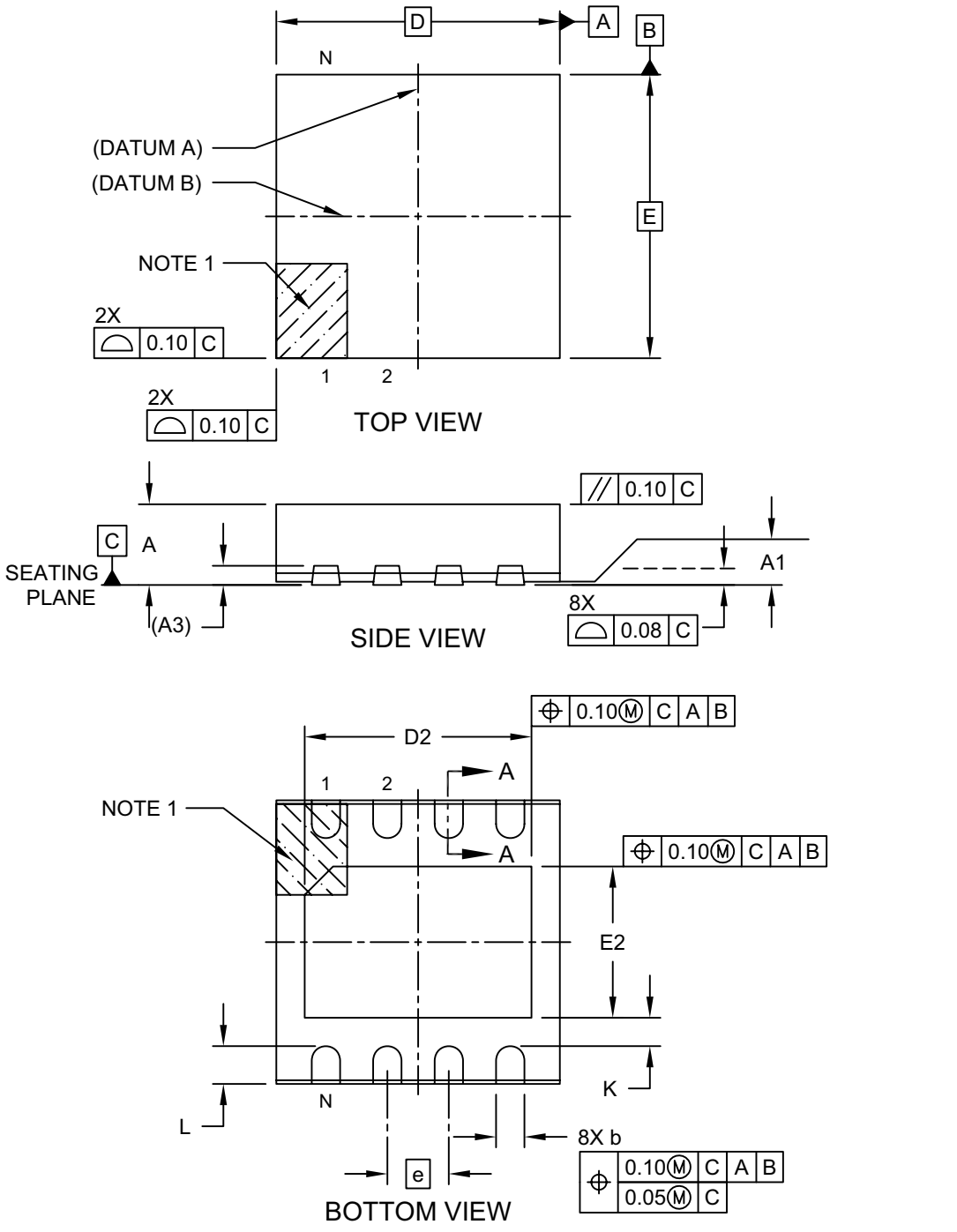
1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-SN Rev B

8-Lead Very Thin Plastic Dual Flat, No Lead Package (Q8B) - 3x3 mm Body [VDFN]
With 2.40x1.60 mm Exposed Pad and Stepped Wettable Flanks

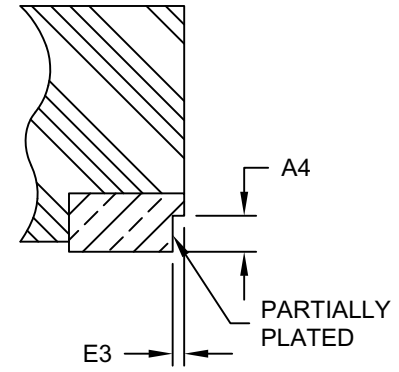
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



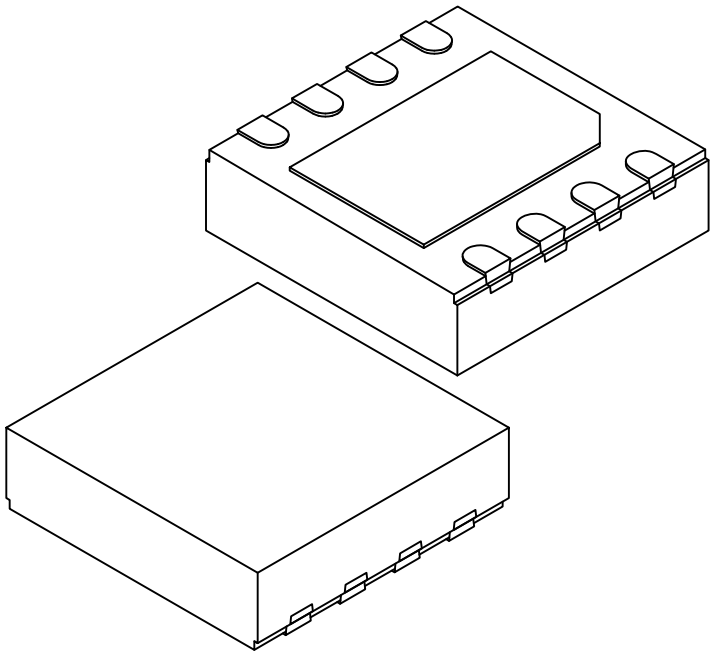
Microchip Technology Drawing C04-21358 Rev B Sheet 1 of 2

8-Lead Very Thin Plastic Dual Flat, No Lead Package (Q8B) - 3x3 mm Body [VDFN] With 2.40x1.60 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



SECTION A–A



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.03	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Length	D2	2.30	2.40	2.50
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.50	1.60	1.70
Terminal Width	b	0.25	0.30	0.35
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.20	-	-
Wettable Flank Step Cut Depth	A4	0.10	0.13	0.15
Wettable Flank Step Cut Width	E3	-	-	0.04

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

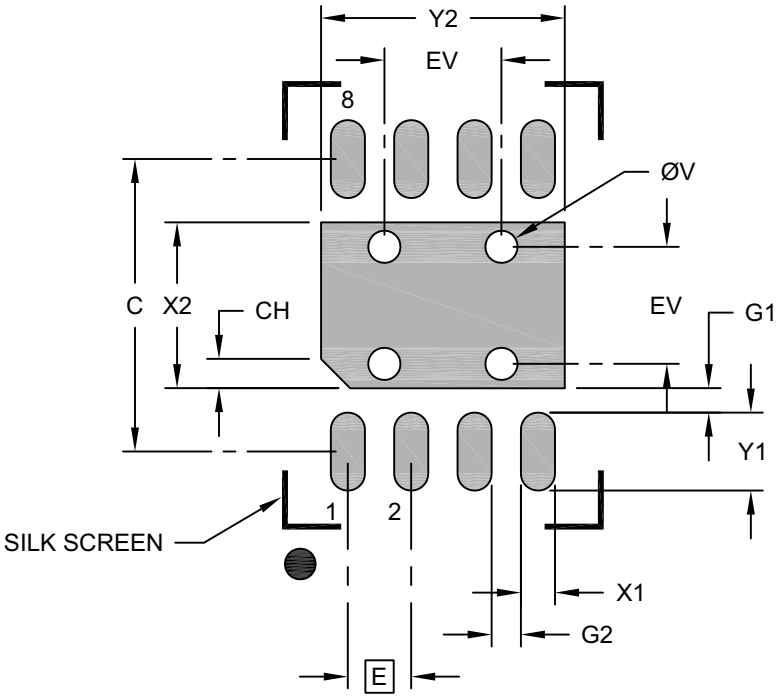
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21358 Rev B Sheet 2 of 2

8-Lead Very Thin Plastic Dual Flat, No Lead Package (Q8B) - 3x3 mm Body [VDFN] With 2.40x1.60 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	X2			1.70
Optional Center Pad Length	Y2			2.50
Contact Pad Spacing	C		3.00	
Contact Pad Width (X8)	X1			0.35
Contact Pad Length (X8)	Y1			0.80
Contact Pad to Center Pad (X8)	G1	0.20		
Contact Pad to Contact Pad (X6)	G2	0.20		
Pin 1 Index Chamfer	CH	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-23358 Rev B

APPENDIX A: REVISION HISTORY

Revision B (August 2017)

The following is the list of modifications:

1. Added new devices ATA6562-GBQW0 and ATA6563-GBQW0 and updated the related information across the document.
2. Updated Section , Features.
3. Updated Section , ATA6562/ATA6563 Family Members
4. Updated Section TABLE 2-2:, Temperature Specifications
5. Updated Section 3.1, Package Marking Information
6. Updated Section , Product Identification System
7. Various typographical edits.

Revision A (June 2017)

- Original Release of this Document.
- This document replaces Atmel - 9389C-11/16ATA6562/3