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ATA6565

Dual High-Speed CAN Transceiver with Standby Mode

Features

- Fully ISO 11898-2, ISO 11898-5, ISO 11898-2: 2016 and SAE J2962-2 Compliant
- CAN FD Ready
- Communication Speed up to 5 Mbps
- Low Electromagnetic Emission (EME) and High Electromagnetic Immunity (EMI)
- Differential Receiver with Wide Common-Mode Range
- Remote Wake-up Capability via CAN Bus – Wake-up on Pattern (WUP) as Specified in ISO 11898-2: 2016, 3.8 µs Activity Filter Time
- Functional Behavior Predictable Under All Supply Conditions
- Transceiver Disengages from the Bus when Not Powered Up
- RXD Recessive Clamping Detection
- High Electrostatic Discharge (ESD) Handling Capability on the Bus Pins
- Bus Pins Protected Against Transients in Automotive Environments
- Transmit Data (TXD) Dominant Time-out Function
- Undervoltage Detection on VCC Pin
- Bus Pins Short-Circuit and Overtemperature Protected
- Fulfills the OEM *"Hardware Requirements for LIN, CAN and FlexRay™ Interfaces in Automotive Applications"*, Rev. 1.3
- Qualified According to AEC-Q100
- Two Ambient Temperature Grades Available:
  - ATA6565-GCQW1 and ATA6565-GNQW1 up to T_{amb} = +125°C
  - ATA6565-GCQW0 and ATA6565-GNQW0 up to T_{amb} = +150°C
- 14-Lead SOIC Package and 14-Lead VDFN Package with Wettable Flanks (Moisture Sensitivity Level 1)

Applications

Classical CAN and CAN FD networks in Automotive, Industrial, Aerospace, Medical and Consumer applications.

General Description

The ATA6565 is a fully integrated, dual high-speed CAN transceiver with two completely independent and separated high-speed CAN transceivers integrated in one package (only the GND pins, GND1 and GND2, are internally connected). Each of the two identical transceivers provides an interface between a Controller Area Network (CAN) protocol controller and a physical two-wire CAN bus.

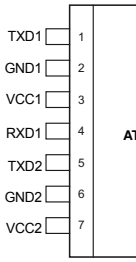
The device is designed for high-speed (up to 5 Mbps) CAN applications in the automotive industry, providing differential transmit and receive capability to (a micro-controller with) a CAN protocol controller. It offers improved Electromagnetic Compatibility (EMC) and Electrostatic Discharge (ESD) performance, as well as features such as:

- Ideal passive behavior to the CAN bus when the supply voltage is off
- Very low current consumption in Standby mode with bus wake-up capability

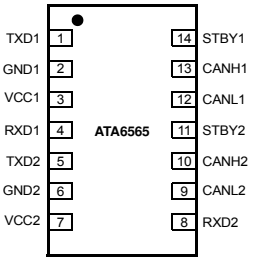
Two operating modes, together with the dedicated fail-safe features, make the ATA6565 an excellent choice for all types of high-speed CAN networks. The ATA6565 includes more than one high-speed CAN interface which requires a Low-Power mode with wake-up capability via the CAN bus. These features are especially valuable for body control units and gateways.

Package Types

ATA6565
14-Pin SOIC



ATA6565
3 x 4.5 mm
14-Pin VDFN



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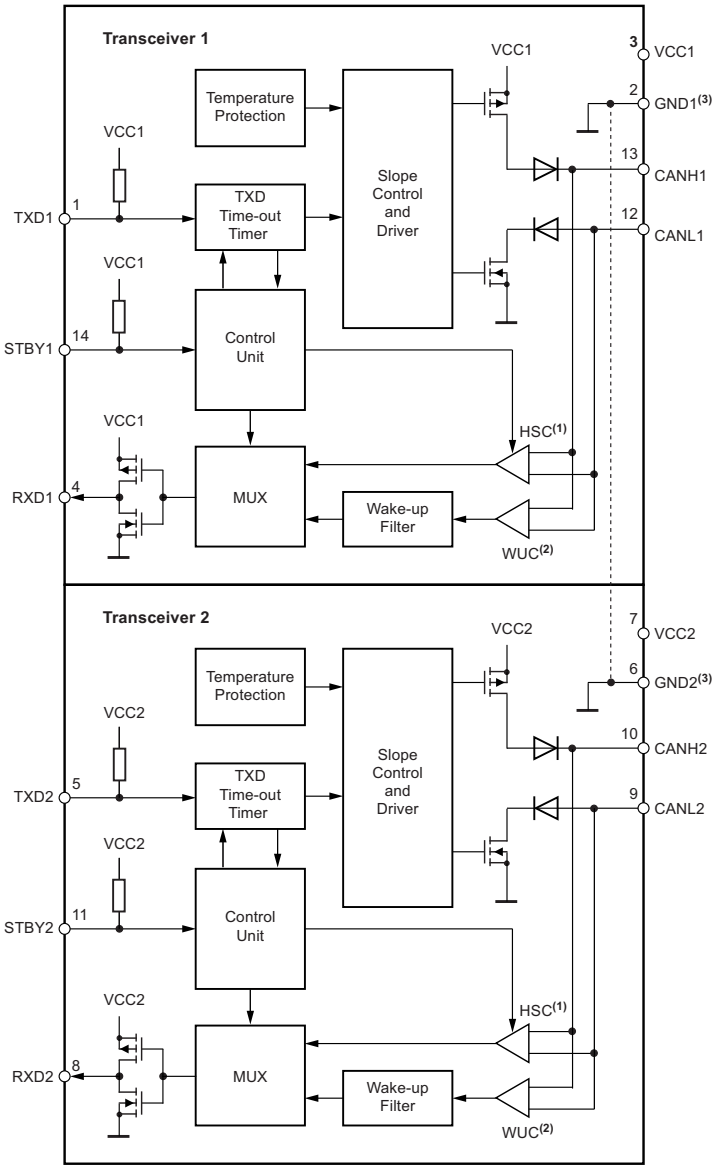
ATA6565 Family Members

Device	Grade 0	Grade 1	SOIC14	VDFN14
ATA6565-GNQW1		X	X	
ATA6565-GNQW0	X		X	
ATA6565-GCQW1		X		X
ATA6565-GCQW0	X			X

Note: For ordering information, see the **"Product Identification System"** section.

Block Diagram



Note 1: HSC: High-Speed Comparator.
2: WUC: Wake-up Comparator.
3: GND1 and GND2 are internally connected.

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1.0 FUNCTIONAL DESCRIPTION

The ATA6565 is a stand-alone, dual high-speed CAN transceiver, compliant with the ISO 11898-2, ISO 11898-5, ISO 11898-2: 2016 and SAE J2962-2 standards. Each of the two transceivers provides a very low current consumption in Standby mode and wake-up capability via the CAN bus.

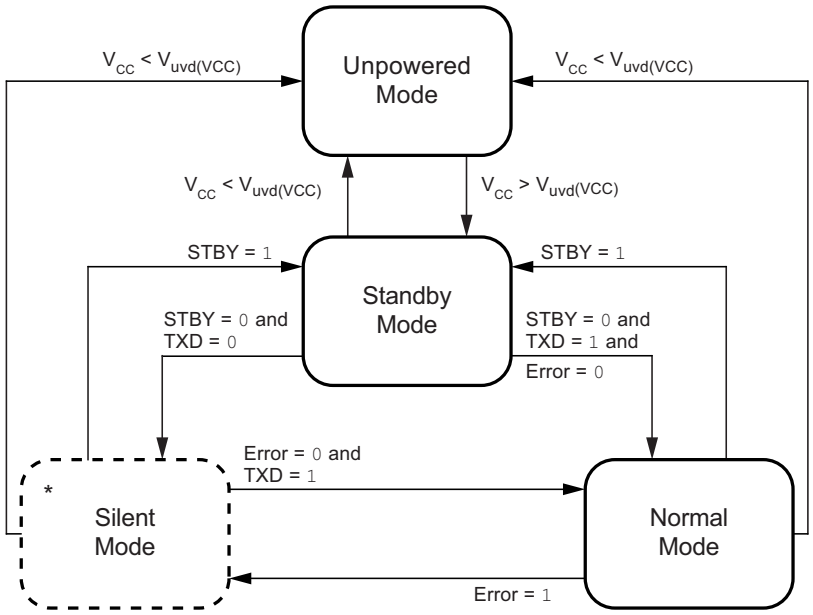
The functions described in the following text apply to each of the two identical high-speed CAN transceivers integrated in the ATA6565. Therefore, if for example, the CANH pin is stated, this applies to each of the two transceivers, meaning CANH1 and CANH2. The two transceivers are identical and there is no internal connection between them (with the exception of the GND pins, GND1 and GND2), so they work completely independently.

1.1 Operating Modes

Each of the transceivers supports three operating modes: Unpowered, Standby and Normal. Additionally, there is the internal Silent mode, which is not externally accessible. This mode is a Receive Only mode, which means the CAN drivers are deactivated and only data from the bus can be received.

The operating modes can be selected via the STBY pins (STBY1 and STBY2). See Figure 1-1 and Table 1-1 for a description of the operating modes.

FIGURE 1-1: OPERATING MODES



* Silent mode is externally not accessible. In this mode, the transceiver can only receive data from the bus, but the transmitter is disabled.

TABLE 1-1: OPERATING MODES

Mode	Inputs		Outputs	
	STBY	Pin TXD	CAN Driver	Pin RXD
Unpowered	X(1)	X(1)	Recessive	Recessive
Standby	High	X(1)	Recessive	Active(2)
Normal	Low	Low	Dominant	Low
	Low	High	Recessive	High

Note 1: Irrelevant.

2: Reflects the bus only for wake-up.

1.1.1 NORMAL MODE

A low level on the STBY pin, together with a high level on the TXD pin, selects the Normal mode. In this mode, the transceiver is able to transmit and receive data via the CANH and CANL bus lines (see the **Block Diagram**). The output driver stage is active and drives data from the TXD input to the CAN bus. The High-Speed Comparator (HSC) converts the analog data on the bus lines into digital data, which is output to pin RXD. The bus biasing is set to $V_{VCC}/2$ and the undervoltage monitoring of V_{VCC} is active.

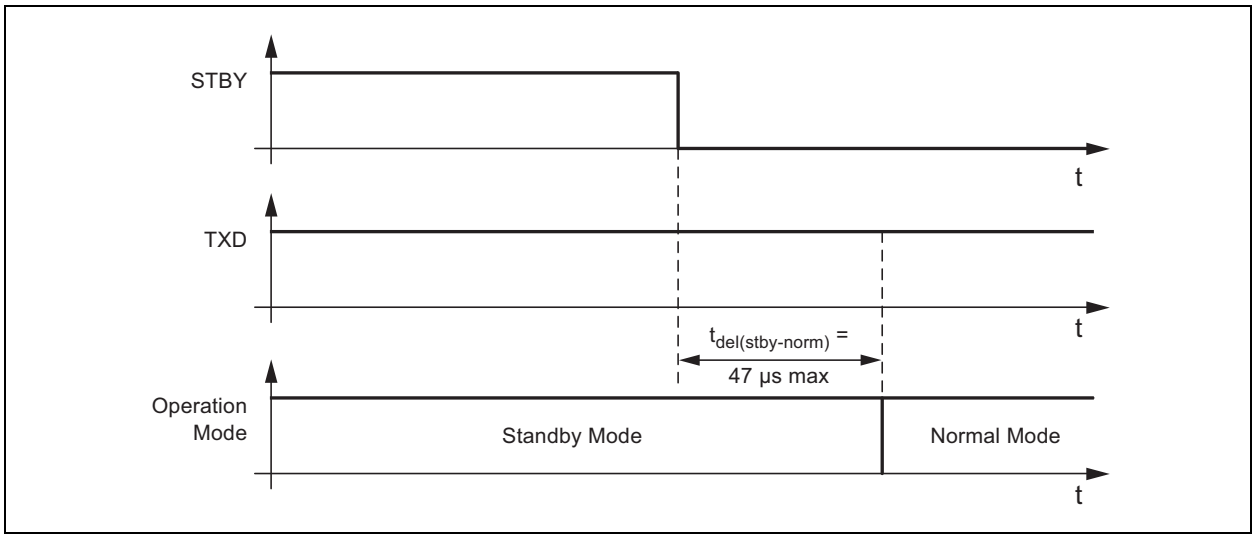
The slope of the output signals on the bus lines is controlled and optimized in a way that ensures the lowest possible Electromagnetic Emission (EME).

To switch the device to Normal Operating mode, set the STBY pin to low and the TXD pin to high (see Table 1-1 and Figure 1-2). The STBY pin provides a pull-up resistor to VCC, thus ensuring a defined level if the pin is open.

Please note that the device cannot enter Normal mode as long as TXD is at ground level.

The switching into Normal mode is depicted in Figure 1-2.

FIGURE 1-2: SWITCHING FROM STANDBY MODE TO NORMAL MODE



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1.1.2 STANDBY MODE

A high level on the STBY pin selects Standby mode. In this mode, the transceiver is not able to transmit or correctly receive data via the bus lines. The transmitter and the High-Speed Comparator (HSC) are switched off to reduce current consumption.

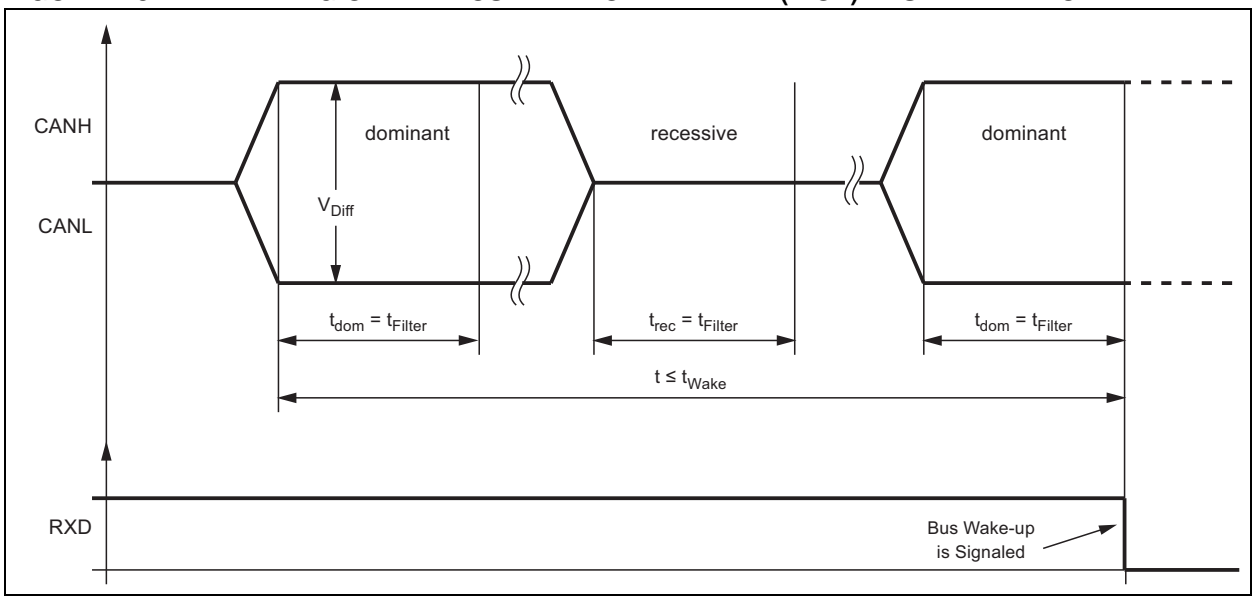
1.1.2.1 Remote Wake-up via the CAN Bus

In Standby mode, the bus lines are biased to ground to reduce current consumption to a minimum. The device monitors the bus lines for a valid wake-up pattern, as specified in the ISO 11898-2: 2016. This filtering helps to avoid spurious wake-up events which would be triggered by scenarios, such as a dominant clamped bus or by a dominant phase due to noise, spikes on the bus, automotive transients or EMI.

The wake-up pattern consists of at least two consecutive dominant bus levels for a duration of at least t_{Filter}, each separated by a recessive bus level with a duration of at least t_{Filter}. Dominant or recessive bus levels shorter than t_{Filter} are always ignored. The complete dominant-recessive-dominant pattern, as shown in Figure 1-3, must be received within the bus wake-up time-out time, t_{Wake}, to be recognized as a valid wake-up pattern. Otherwise, the internal wake-up logic is reset and then the complete wake-up pattern must be retransmitted to trigger a wake-up event. The RXD pin remains at a high level until a valid wake-up event has been detected.

During Normal mode, at a VCC undervoltage condition or when the complete wake-up pattern is not received within t_{Wake}, no wake-up is signaled at the RXD pin.

FIGURE 1-3: TIMING OF THE BUS WAKE-UP PATTERN (WUP) IN STANDBY MODE



When a valid CAN wake-up pattern is detected on the bus, the RXD pin switches to low to signal a wake-up request. A transition to Normal mode is not triggered until the STBY pin is forced back to low by the microcontroller.

1.2 Fail-Safe Features

1.2.1 TXD DOMINANT TIME-OUT FUNCTION

A TXD dominant time-out timer is started when the TXD pin is set to low. If the low state on the TXD pin persists for longer than $t_{to(dom)TXD}$, the transmitter is disabled, releasing the bus lines to the recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when the TXD pin is set to high. If the low state on the TXD pin was longer than $t_{to(dom)TXD}$, then the TXD pin has to be set to high ≥ 4 µs in order to reset the TXD dominant time-out timer.

1.2.2 INTERNAL PULL-UP STRUCTURE AT THE TXD AND STBY INPUT PINS

The TXD and STBY pins have an internal pull-up to VCC. This ensures a safe, defined state in case one or both pins are left floating. Pull-up currents flow in these pins in all states, meaning all pins should be in a high state during Standby mode to minimize the current consumption.

1.2.3 UNDERVOLTAGE DETECTION ON PIN VCC

If V_{VCC} drops below its undervoltage detection level, $V_{uvd(VCC)}$ (see **Section 2.0 "Electrical Characteristics"**), the transceiver switches off and disengages from the bus until V_{VCC} has recovered. The low-power

wake-up comparator is only switched off during a VCC undervoltage. The logic state of the STBY pin is ignored until the VCC voltage has recovered.

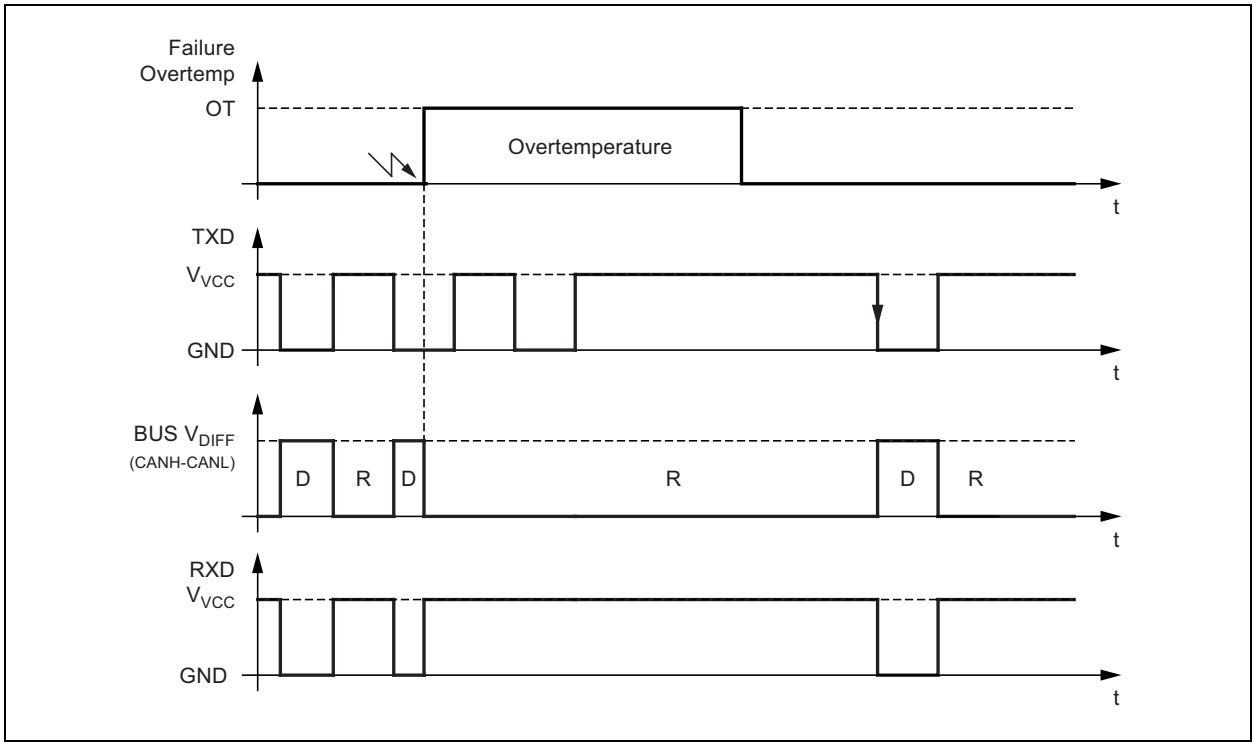
1.2.4 BUS WAKE-UP ONLY AT DEDICATED WAKE-UP PATTERN

Due to the implementation of the wake-up filtering, the transceiver does not wake-up when the bus is in a long dominant phase; it only wakes up at a dedicated wake-up pattern, as specified in the ISO 11898-2: 2016. This means for a valid wake-up, at least two consecutive dominant bus levels for a duration of at least, t_{Filter}, each separated by a recessive bus level with a duration of at least, t_{Filter}, must be received via the bus. Dominant or recessive bus levels shorter than t_{Filter} are always ignored. The complete dominant-recessive-dominant pattern, as shown in Figure 1-3, must be received within the bus wake-up time-out time, t_{Wake}, to be recognized as a valid wake-up pattern. This filtering leads to a higher robustness against EMI and transients, and therefore, significantly reduces the risk of an unwanted bus wake-up.

1.2.5 OVERTEMPERATURE PROTECTION

The output drivers are protected against overtemperature conditions. If the junction temperature exceeds the shut-down junction temperature, T_{Jsd}, the output drivers are disabled until the junction temperature drops below T_{Jsd} and pin TXD is at a high level again. This TXD condition ensures that output driver oscillations, due to temperature drift, are avoided.

FIGURE 1-4: RELEASE OF TRANSMISSION AFTER OVERTEMPERATURE CONDITION



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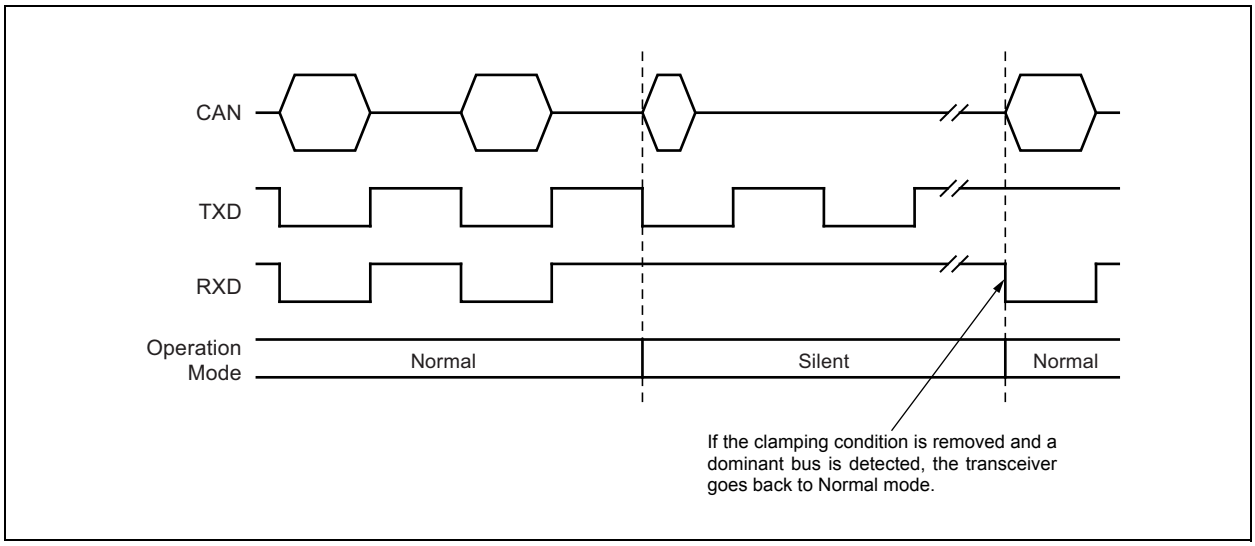
1.2.6 SHORT-CIRCUIT PROTECTION OF THE BUS PINS

The CANH and CANL bus outputs are short-circuit protected, either against GND or a positive supply voltage. A current-limiting circuit protects the transceiver against damage. If the device is heating up due to a continuous short on CANH or CANL, the internal overtemperature protection switches the bus transmitter off.

1.2.7 RXD RECESSIVE CLAMPING

This fail-safe feature prevents the controller from sending data on the bus if its RXD is clamped to high (e.g., recessive). That is, if the RXD pin cannot signalize a dominant bus condition (e.g., because it is shorted to VCC), the transmitter is disabled to avoid possible data collisions on the bus. In Normal mode, the device permanently compares the state of the High-Speed Comparator (HSC) with the state of the RXD pin. If the HSC indicates a dominant bus state for more than t_{RC_det}, without the RXD pin doing the same, a recessive clamping situation is detected and the transceiver is forced into Silent mode. This Fail-Safe mode is released by either entering Standby or Unpowered mode, or if the RXD pin is showing a dominant (e.g., low) level again.

FIGURE 1-5: RXD RECESSIVE CLAMPING DETECTION



1.3 Pin Description

The descriptions of the pins are listed in Table 1-2.

TABLE 1-2: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	TXD1	Transmit Data Input 1
2	GND1	Ground 1, Internally Connected to GND2
3	VCC1	Supply Voltage of Transceiver 1
4	RXD1	Receive Data Output 1; Reads out Data from the Bus Lines of Transceiver 1
5	TXD2	Transmit Data Input 2
6	GND2	Ground 2, Internally Connected to GND1
7	VCC2	Supply Voltage of Transceiver 2
8	RXD2	Receive Data Output 2; Reads out Data from the Bus Lines of Transceiver 2
9	CANL2	Low-Level CAN Bus Line 2
10	CANH2	High-Level CAN Bus Line 2
11	STBY2	Standby Mode Control Input of Transceiver 2
12	CANL1	Low-Level CAN Bus Line 1
13	CANH1	High-Level CAN Bus Line 1
14	STBY1	Standby Mode Control Input of Transceiver 1
15	EP(1)	Exposed Thermal Pad: Heat Slug, Internally Connected to the GND Pins

Note 1: Only for the VDFN package

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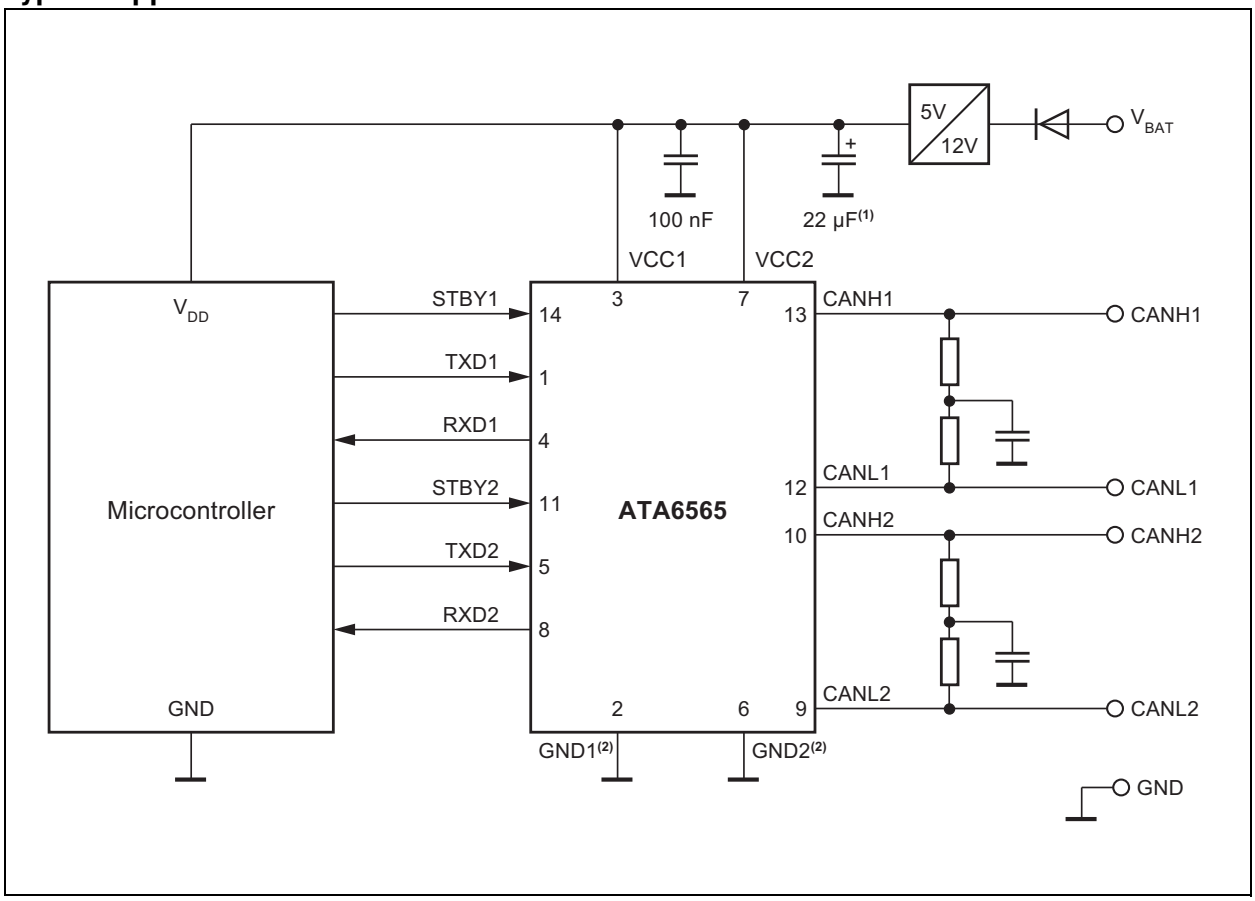
Typical Application



NOTES:

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2.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

DC Voltage at CANH1, CANL1, CANH2, CANL2 (V_{CANH}, V_{CANL}) .....–27 to +42V

Transient Voltage at CANH, CANL (according to ISO 7637, Part 2) (V_{CANH}, V_{CANL}).....–150 to +100V

Max. Differential Bus Voltage (V_{Diff}).....–5 to +18V

DC Voltage on All Other Pins (V_X) .....–0.3 to +5.5V

ESD according to IBEE CAN EMC – Test Specification following IEC 61000-4-2 – Pins CANH1, CANL1, CANH2, CANL2 .....±8 kV

ESD (HBM following STM5.1 with 1.5 kΩ/100 pF) – Pins CANH1, CANL1, CANH2, CANL2 to GND .....±6 kV

Component Level ESD (HBM according to ANSI/ESD STM5.1, JESD22-A114, AEC-Q100 (002) .....±4 kV

CDM ESD STM 5.3.1 .....±750V

ESD Machine Model AEC-Q100-RevF(003).....±200V

Virtual Junction Temperature (T_{vJ}).....–40 to +175°C

Storage Temperature Range (T_{stg}) .....–55°C to +150°C

† Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 2-1: ELECTRICAL CHARACTERISTICS

Electrical Specifications: The values below are valid for each of the two identical integrated CAN transceivers. Grade 1: T_{amb} = -40°C to +125°C and Grade 0: T_{amb} = –40°C to +150°C; V_{VCC} = 4.5V to 5.5V; R_L = 60Ω, C_L = 100 pF unless specified otherwise; all voltages are defined in relation to ground; positive currents flow into the IC.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply, Pin VCC						
Supply Voltage	V_{VCC}	4.5	—	5.5	V	
Supply Current in Silent Mode	I_{VCC_sil}	1.9	2.5	3.0	mA	Silent mode, $V_{TXD} = V_{VCC}$
Supply Current in Normal Mode	I_{VCC_rec}	2	—	5	mA	Recessive, $V_{TXD} = V_{VCC}$
	I_{VCC_dom}	30	50	70	mA	Dominant, V_{TXD} = 0V
	I_{VCC_short}	—	—	85	mA	Short between CANH and CANL (**Note 1**)
Supply Current in Standby Mode	I_{VCC_STBY}	—	—	12	µA	$V_{TXD} = V_{VCC}$
	I_{VCC_STBY}	—	7	—	µA	T_{amb} = +25°C (**Note 3**)
Undervoltage Detection Threshold on Pin VCC	$V_{uvd(VCC)}$	2.75	—	4.5	V	
Mode Control Input, Pin STBY						
High-Level Input Voltage	V_{IH}	$0.7 \times V_{VCC}$	—	V_{VCC} + 0.3	V	
Low-Level Input Voltage	V_{IL}	–0.3	—	$0.3 \times V_{VCC}$	V	
Pull-up Resistor to VCC	R_{pu}	75	125	175	kΩ	V_{STBY} = 0V
High-Level Leakage Current	I_L	–2	—	+2	µA	$V_{STBY} = V_{VCC}$

Note 1: 100% correlation tested.

2: Characterized on samples.

3: Design parameter.

TABLE 2-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: The values below are valid for each of the two identical integrated CAN transceivers. Grade 1: T_{amb} = -40°C to +125°C and Grade 0: T_{amb} = –40°C to +150°C; V_{VCC} = 4.5V to 5.5V; R_L = 60Ω, C_L = 100 pF unless specified otherwise; all voltages are defined in relation to ground; positive currents flow into the IC.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
CAN Transmit Data Input, Pin TXD						
High-Level Input Voltage	V_{IH}	0.7 × V_{VCC}	—	V_{VCC} + 0.3	V	
Low-Level Input Voltage	V_{IL}	–0.3	—	0.3 × V_{VCC}	V	
Pull-up Resistor to VCC	R_{TXD}	20	35	50	kΩ	V_{TXD} = 0V
High-Level Leakage Current	I_{TXD}	–2	—	+2	µA	Normal mode, V_{TXD} = V_{VCC}
Input Capacitance	C_{TXD}	—	5	10	pF	**(Note 3)**
CAN Receive Data Output, Pin RXD						
High-Level Output Current	I_{OH}	–8	—	-1	mA	Normal mode, V_{RXD} = V_{VCC} – 0.4V
Low-Level Output Current, Bus Dominant	I_{OL}	2	—	12	mA	Normal mode, V_{RXD} = 0.4V
Bus Lines, Pins CANH and CANL						
Single-Ended Dominant Output Voltage	$V_{O(dom)}$	2.75	3.5	4.5	V	V_{TXD} = 0V, t < $t_{to(dom)TXD}$, R_L = 50W to 65W, CANH pin **(Note 1)**
		0.5	1.5	2.25	V	V_{TXD} = 0V, t < $t_{to(dom)TXD}$, R_L = 50W to 65W, CANL pin **(Note 1)**
Transmitter Voltage Symmetry	V_{Sym}	0.9	1.0	1.1	—	V_{Sym} = (V_{CANH} + V_{CANL})/V_{VCC} **(Note 3)**
Bus Differential Output Voltage	V_{Diff}	1.5	—	3	V	V_{TXD} = 0V, t < $t_{to(dom)TXD}$, R_L = 45Ω to 65Ω
		1.5	—	3.3	V	R_L = 70Ω **(Note 3)**
		1.5	—	5	V	R_L = 2240Ω **(Note 3)**
		–50	—	+50	mV	V_{VCC} = 4.75V to 5.25V, V_{TXD} = V_{VCC}, receive, no load
Recessive Output Voltage	$V_{O(rec)}$	2	0.5 * V_{VCC}	3	V	Normal and Silent mode, V_{TXD} = V_{VCC}, no load
	$V_{O(rec)}$	–0.1	—	+0.1	V	Standby mode, V_{TXD} = V_{VCC}, no load
Differential Receiver Threshold Voltage	$V_{th(RX)dif}$	0.5	0.7	0.9	V	Normal and Silent mode (HSC), $V_{cm(CAN)}$ = -27V to +27V
	$V_{th(RX)dif}$	0.4	0.7	1.1	V	Standby mode (WUC), $V_{cm(CAN)}$ = -27V to +27V **(Note 1)**
Differential Receiver Hysteresis Voltage	$V_{hys(RX)dif}$	50	120	200	mV	Normal and Silent mode (HSC), $V_{cm(CAN)}$ = -27V to +27V
Dominant Output Current	$I_{IO(dom)}$	–75	—	-35	mA	V_{TXD} = 0V, t < $t_{to(dom)TXD}$, V_{VCC} = 5V, CANH pin, V_{CANH} = -5V
		35	—	75	mA	V_{TXD} = 0V, t < $t_{to(dom)TXD}$, V_{VCC} = 5V, CANL pin, V_{CANL} = +40V

Note 1: 100% correlation tested.

2: Characterized on samples.

3: Design parameter.

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TABLE 2-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: The values below are valid for each of the two identical integrated CAN transceivers. Grade 1: T_{amb} = -40°C to +125°C and Grade 0: T_{amb} = –40°C to +150°C; V_{VCC} = 4.5V to 5.5V; R_L = 60Ω, C_L = 100 pF unless specified otherwise; all voltages are defined in relation to ground; positive currents flow into the IC.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Recessive Output Current	$I_{IO(rec)}$	–5	—	+5	mA	Normal and Silent mode, $V_{TXD} = V_{VCC}$, no load, $V_{CANH} = V_{CANL}$ = –27V to +32V
Leakage Current	$I_{IO(leak)}$	–5	0	+5	µA	V_{VCC} = 0V, $V_{CANH} = V_{CANL}$ = 5V
	$I_{IO(leak)}$	–5	0	+5	µA	VCC is connected to GND with R = 47kΩ, $V_{CANH} = V_{CANL}$ = 5V **(Note 3)**
Input Resistance	R_i	9	15	28	kΩ	$V_{CANH} = V_{CANL}$ = 4V
	R_i	9	15	28	kΩ	–2V ≤ V_{CANH} ≤ +7V, –2V ≤ V_{CANL} ≤ +7V **(Note 3)**
Input Resistance Deviation	ΔR_i	–1	0	+1	%	Between CANH and CANL, $V_{CANH} = V_{CANL}$ = 4V
	ΔR_i	–1	0	+1	%	Between CANH and CANL, –2V ≤ V_{CANH} ≤ +7V, –2V ≤ V_{CANL} ≤ +7V **(Note 3)**
Differential Input Resistance	$R_{i(dif)}$	18	30	56	kΩ	$V_{CANH} = V_{CANL}$ = 4V
	$R_{i(dif)}$	18	30	56	kΩ	–2V ≤ V_{CANH} ≤ +7V, –2V ≤ V_{CANL} ≤ +7V **(Note 3)**
Common-Mode Input Capacitance	$C_{i(cm)}$	—	—	20	pF	**(Note 3)**
Differential Input Capacitance	$C_{i(dif)}$	—	—	10	pF	**(Note 3)**
Differential Bus Voltage Range for Recessive State Detection	V_{Diff_rec}	–3	—	+0.5	V	Normal and Silent mode (HSC), –27V ≤ V_{CANH} ≤ +27V, –27V ≤ V_{CANL} ≤ +27V **(Note 3)**
	V_{Diff_rec}	–3	—	+0.4	V	Standby mode (WUC) –27V ≤ V_{CANH} ≤ +27V, –27V ≤ V_{CANL} ≤ +27V **(Note 3)**
Differential Bus Voltage Range for Dominant State Detection	V_{Diff_dom}	0.9	—	8.0	V	Normal and Silent mode (HSC), –27V ≤ V_{CANH} ≤ +27V, –27V ≤ V_{CANL} ≤ +27V **(Note 3)**
	V_{Diff_dom}	1.15	—	8.0	V	Standby mode (WUC), –27V ≤ V_{CANH} ≤ +27V, –27V ≤ V_{CANL} ≤ +27V **(Note 3)**

Note 1: 100% correlation tested.

2: Characterized on samples.

3: Design parameter.

TABLE 2-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: The values below are valid for each of the two identical integrated CAN transceivers. Grade 1: T_{amb} = -40°C to +125°C and Grade 0: T_{amb} = –40°C to +150°C; V_{VCC} = 4.5V to 5.5V; R_L = 60Ω, C_L = 100 pF unless specified otherwise; all voltages are defined in relation to ground; positive currents flow into the IC.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Transceiver Timing, Pins CANH, CANL, TXD and RXD (see Figure 2-1 and Figure 2-3)						
Delay Time from TXD to Bus Dominant	$t_{d(TXD-busdom)}$	40	—	130	ns	Normal mode **(Note 2)**
Delay Time from TXD to Bus Recessive	$t_{d(TXD-busrec)}$	40	—	130	ns	Normal mode **(Note 2)**
Delay Time from Bus Dominant to RXD	$t_{d(busdom-RXD)}$	20	—	100	ns	Normal mode **(Note 2)**
Delay Time from Bus Recessive to RXD	$t_{d(busrec-RXD)}$	20	—	100	ns	Normal mode **(Note 2)**
Propagation Delay from TXD to RXD	$t_{PD(TXD-RXD)}$	40	—	210	ns	Normal mode, rising edge at TXD pin, R_L = 60Ω, C_L = 100 pF
		40	—	200	ns	Normal mode, falling edge at TXD pin, R_L = 60Ω, C_L = 100 pF
	$t_{PD(TXD-RXD)}$	—	—	300	ns	Normal mode, rising edge at TXD pin, R_L = 150Ω, C_L = 100 pF **(Note 3)**
		—	—	300	ns	Normal mode, falling edge at TXD pin, R_L = 150Ω, C_L = 100pF **(Note 3)**
TXD Dominant Time-out Time	$t_{to(dom)TXD}$	0.8	—	3	ms	V_{TXD} = 0V, Normal mode
Bus Wake-up Time-out Time	t_{Wake}	0.8	—	3	ms	Standby mode
Min. Dominant/Recessive Bus Wake-up Time	t_{Filter}	0.5	3	3.8	µs	Standby mode
Delay Time for Standby Mode to Normal Mode Transition	$t_{del(stby-norm)}$	—	—	47	µs	Falling edge at STBY pin
Delay Time for Normal Mode to Standby Mode Transition	$t_{del(norm-stby)}$	—	—	5	µs	Rising edge at STBY pin **(Note 3)**

Note 1: 100% correlation tested.

2: Characterized on samples.

3: Design parameter.

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TABLE 2-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: The values below are valid for each of the two identical integrated CAN transceivers. Grade 1: T_{amb} = -40°C to +125°C and Grade 0: T_{amb} = –40°C to +150°C; V_{VCC} = 4.5V to 5.5V; R_L = 60Ω, C_L = 100 pF unless specified otherwise; all voltages are defined in relation to ground; positive currents flow into the IC.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Transceiver Timing for Higher Bit Rates, Pins CANH, CANL, TXD and RXD (see Figure 2-1 and Figure 2-3), External Capacitor on the RXD Pin, C_{RXD} ≤ 20 pF						
Debouncing Time for Recessive Clamping State Detection	t_{RC_det}	—	—	90	ns	$V_{(CANH-CANL)}$ > 900 mV, RXD = high **(Note 3)**
Recessive Bit Time on RXD	$t_{Bit(RXD)}$	400	—	550	ns	Normal mode, $t_{Bit(TXD)}$ = 500 ns **(Note 1)**
		120	—	220	ns	Normal mode, $t_{Bit(TXD)}$ = 200 ns
Recessive Bit Time on the Bus	$t_{Bit(Bus)}$	435	—	530	ns	Normal mode, $t_{Bit(TXD)}$ = 500 ns **(Note 1)**
		155	—	210	ns	Normal mode, $t_{Bit(TXD)}$ = 200 ns
Receiver Timing Symmetry	Δt_{Rec}	-65	—	+40	ns	Normal mode, $t_{Bit(TXD)}$ = 500 ns, $\Delta t_{Rec} = t_{Bit(RXD)} - t_{Bit(Bus)}$ **(Note 1)**
		–45	—	+15	ns	Normal mode, $t_{Bit(TXD)}$ = 200 ns, $\Delta t_{Rec} = t_{Bit(RXD)} - t_{Bit(Bus)}$

Note 1: 100% correlation tested.
2: Characterized on samples.
3: Design parameter.

TABLE 2-2: TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units
14-Lead SOIC					
Thermal Shutdown of the Bus Drivers for ATA6565-GNQW1 (Grade 1)	T_{Jsd}	150	175	190	°C
Thermal Shutdown of the Bus Drivers for ATA6565-GNQW0 (Grade 0)	T_{Jsd}	160	175	190	°C
Thermal Resistance Virtual Junction to Ambient, where IC is soldered to PCB according to JEDEC	R_{thvJA}	—	110	—	K/W
14-Lead VDFN					
Thermal Shutdown of the Bus Drivers for ATA6565-GCQW1 (Grade 1)	T_{Jsd}	150	175	195	°C
Thermal Shutdown of the Bus Drivers for ATA6565-GCQW0 (Grade 0)	T_{Jsd}	160	175	195	°C
Thermal Resistance Virtual Junction to Heat Slug	R_{thvJC}	—	8	—	K/W
Thermal Resistance Virtual Junction to Ambient, where Heat Slug is Soldered to PCB according to JEDEC	R_{thvJA}	—	45	—	K/W

FIGURE 2-1: TIMING TEST CIRCUIT FOR THE ATA6565 CAN TRANSCEIVER

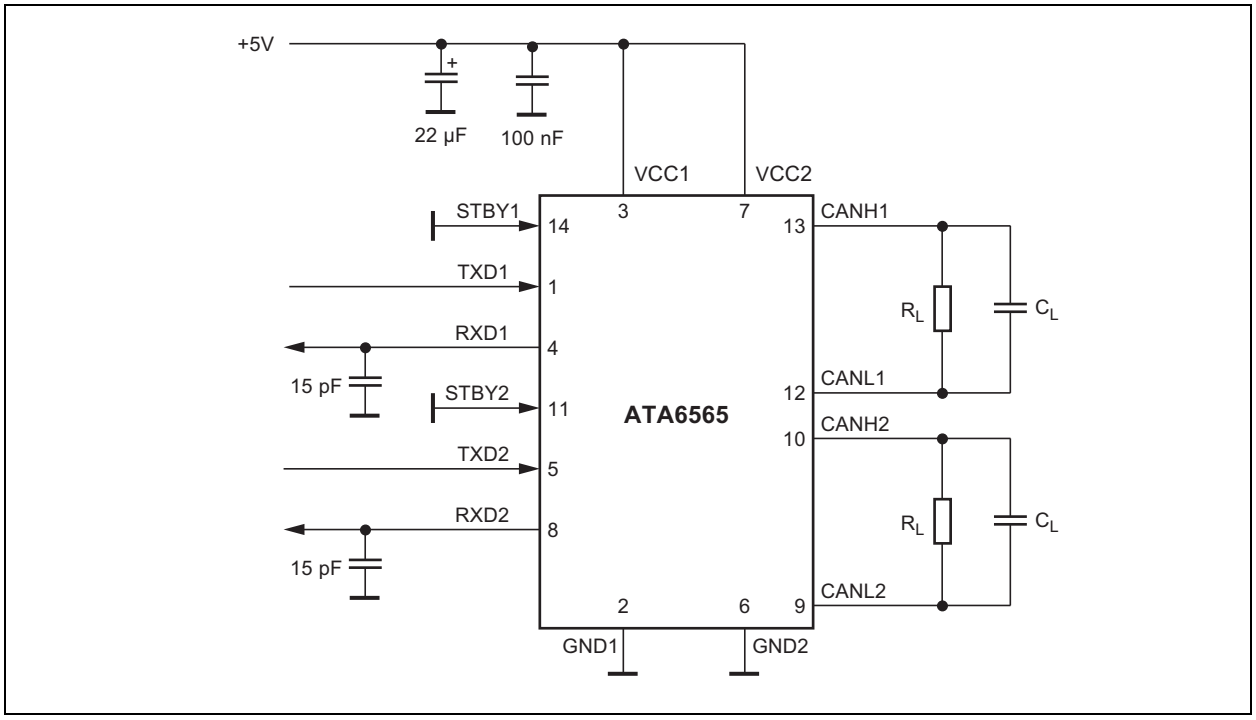

FIGURE 2-2: CAN TRANSCEIVER TIMING DIAGRAM 1

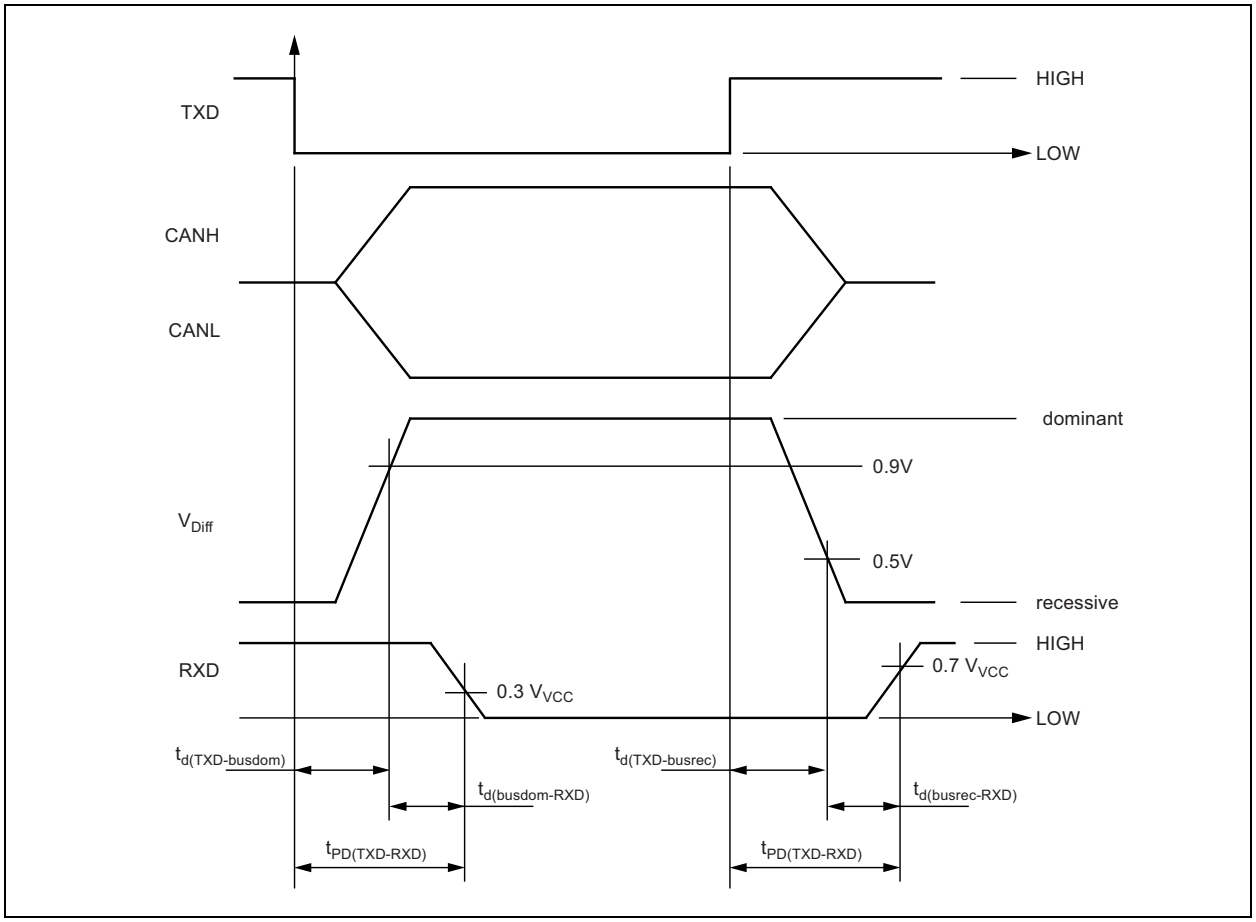

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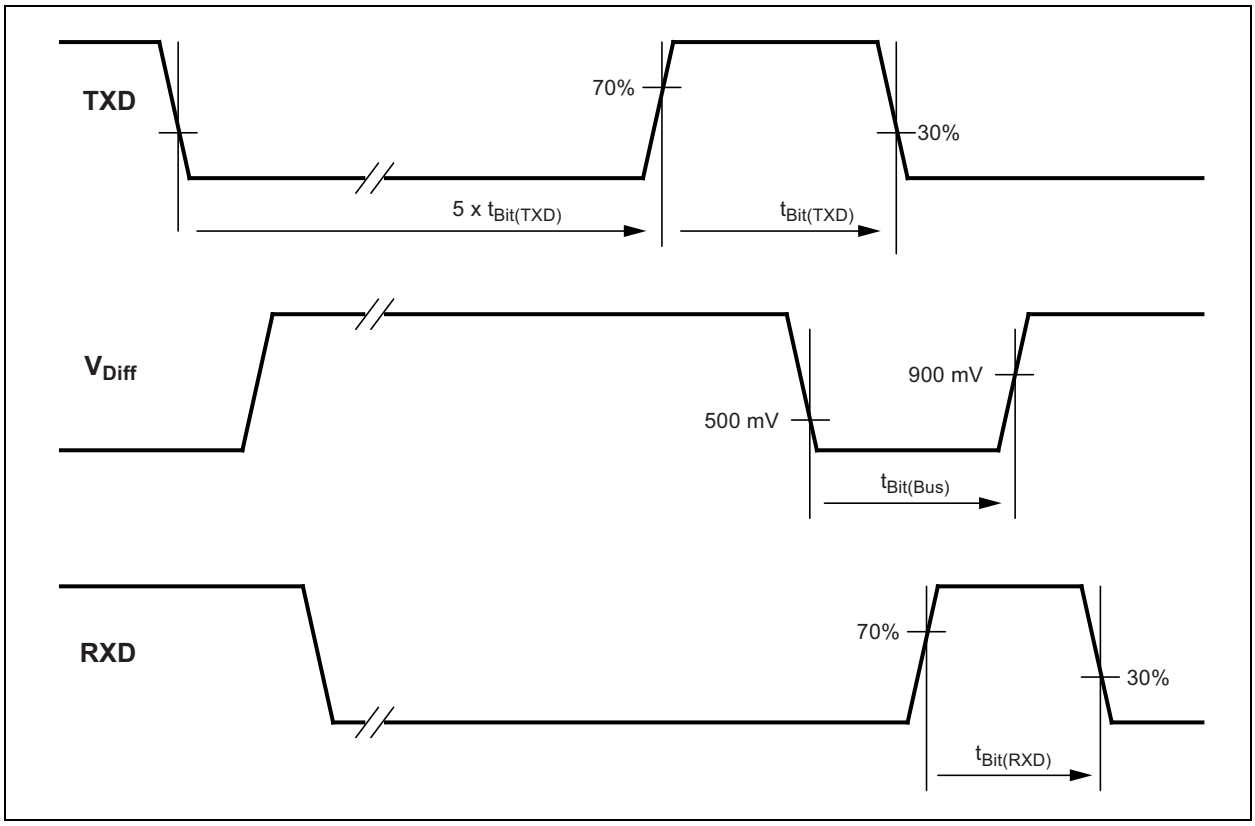
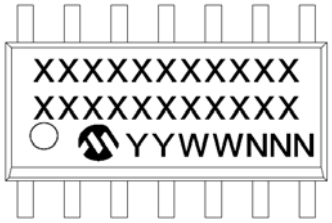
FIGURE 2-3: CAN TRANSCEIVER TIMING DIAGRAM 2



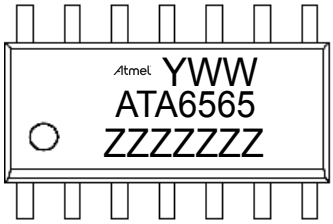
3.0 PACKAGING INFORMATION

3.1 Package Marking Information

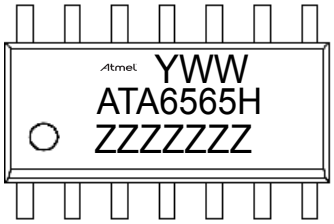
14-Lead SOIC



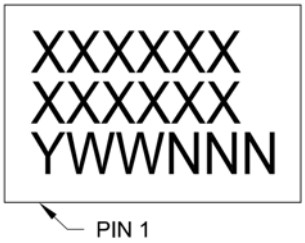
Example, Grade 1



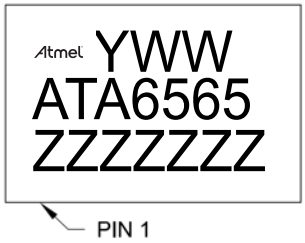
Example, Grade 0



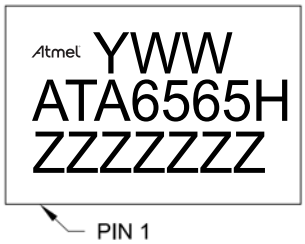
14-Lead 4.5 x 3 mm VDFN



Example, Grade 1



Example, Grade 0



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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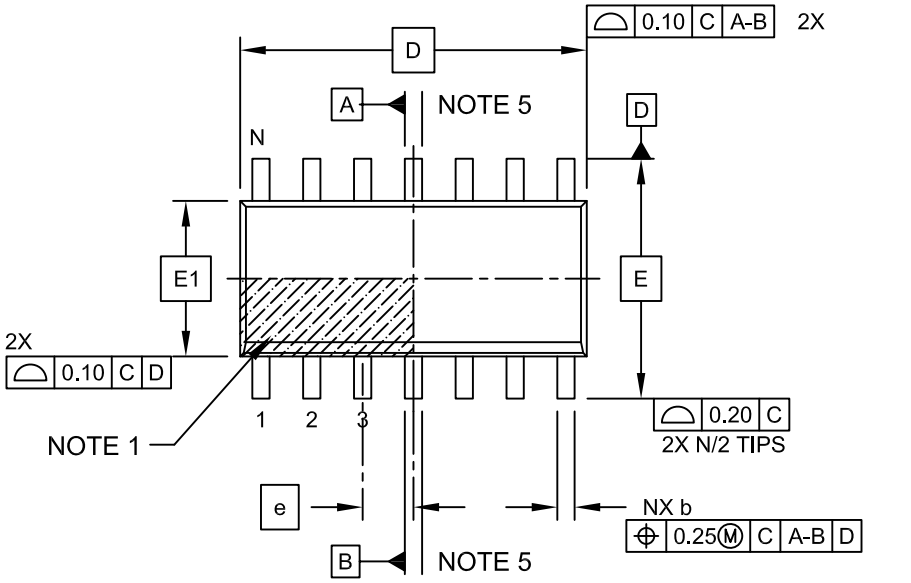
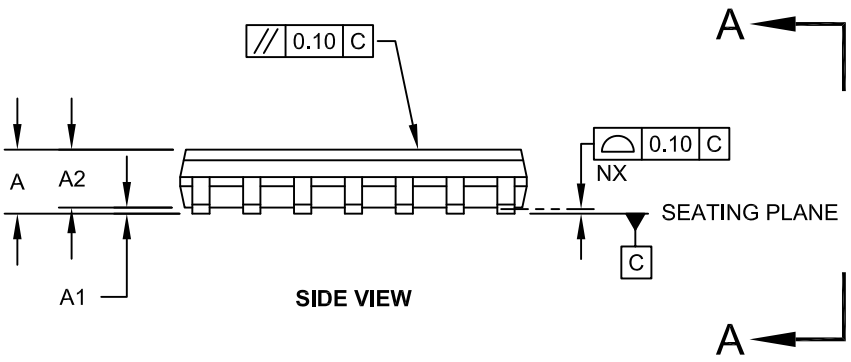
14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

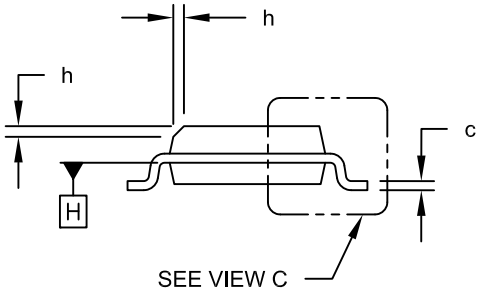
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

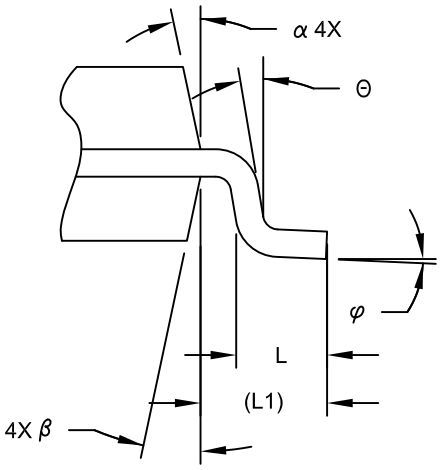


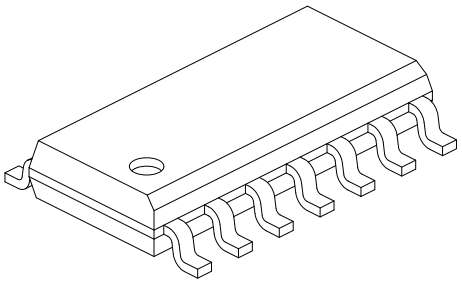
VIEW A-A

Microchip Technology Drawing No. C04-065C Sheet 1 of 2

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





VIEW C

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		8.65 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.10	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-065C Sheet 2 of 2

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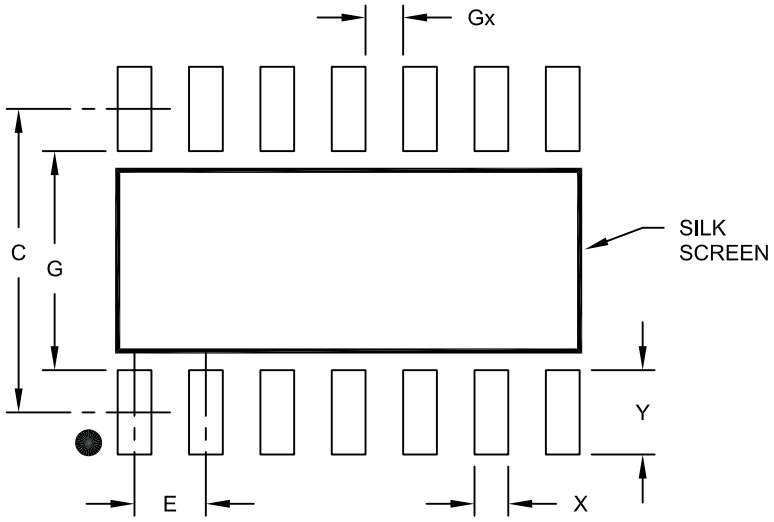
14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width	X			0.60
Contact Pad Length	Y			1.50
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	3.90		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065A

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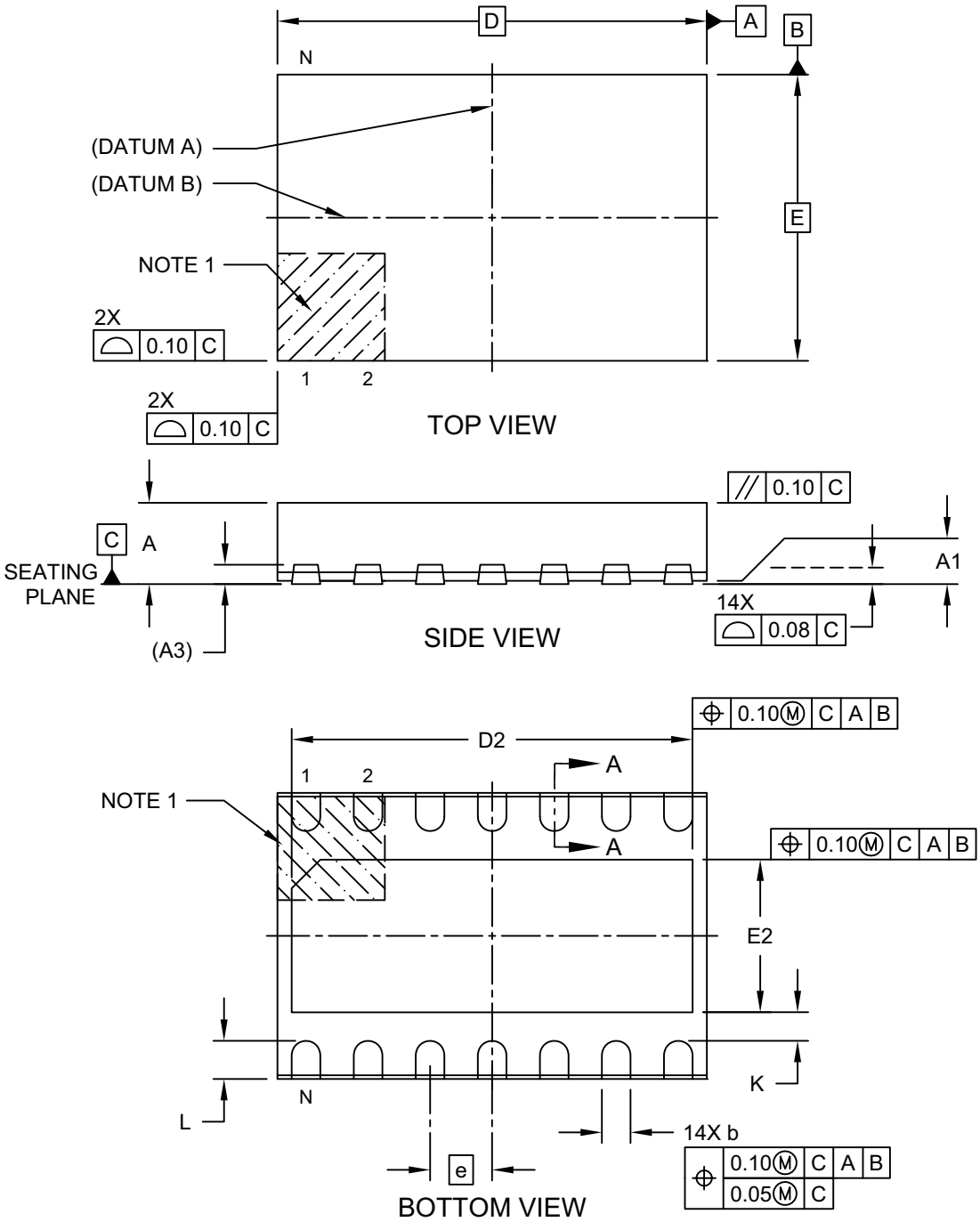
14-Lead Very Thin Plastic Dual Flat, No Lead Package (QBB) - 4.5x3 mm Body [VDFN] With 1.6x4.2 mm Exposed Pad and Stepped Wettable Flanks

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-21361 Rev A Sheet 1 of 2

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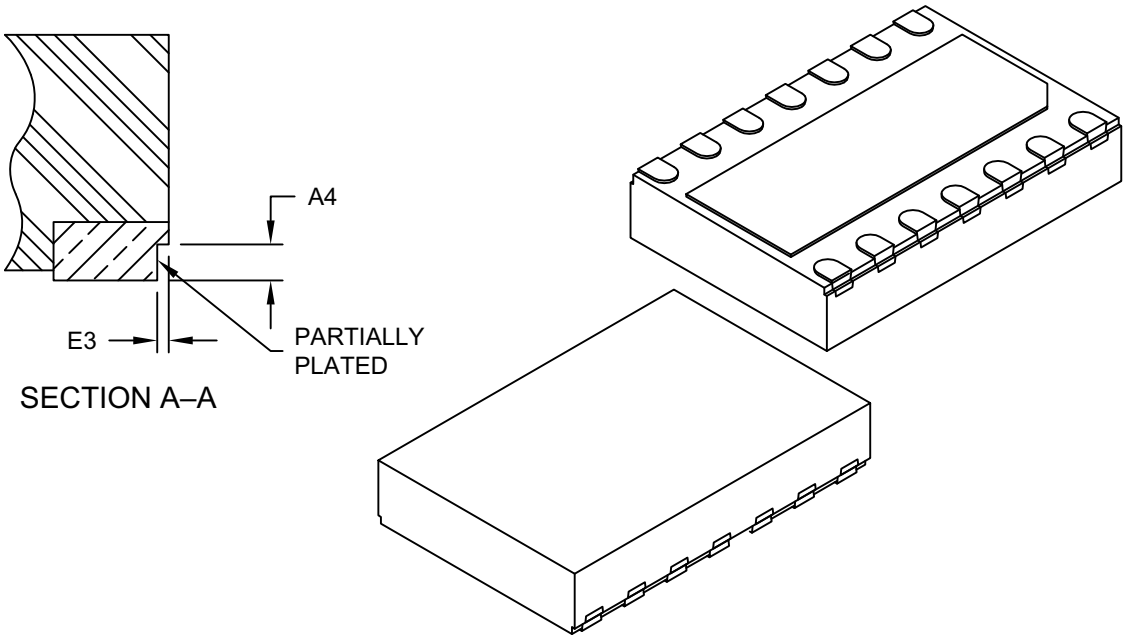
14-Lead Very Thin Plastic Dual Flat, No Lead Package (QBB) - 4.5x3 mm Body [VDFN] With 1.6x4.2 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		14	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.03	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		4.50 BSC	
Exposed Pad Length	D2	4.15	4.20	4.25
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.55	1.60	1.65
Terminal Width	b	0.27	0.32	0.37
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.20	-	-
Wettable Flank Step Cut Depth	A4	0.10	0.13	0.15
Wettable Flank Step Cut Width	E3	-	-	0.04

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

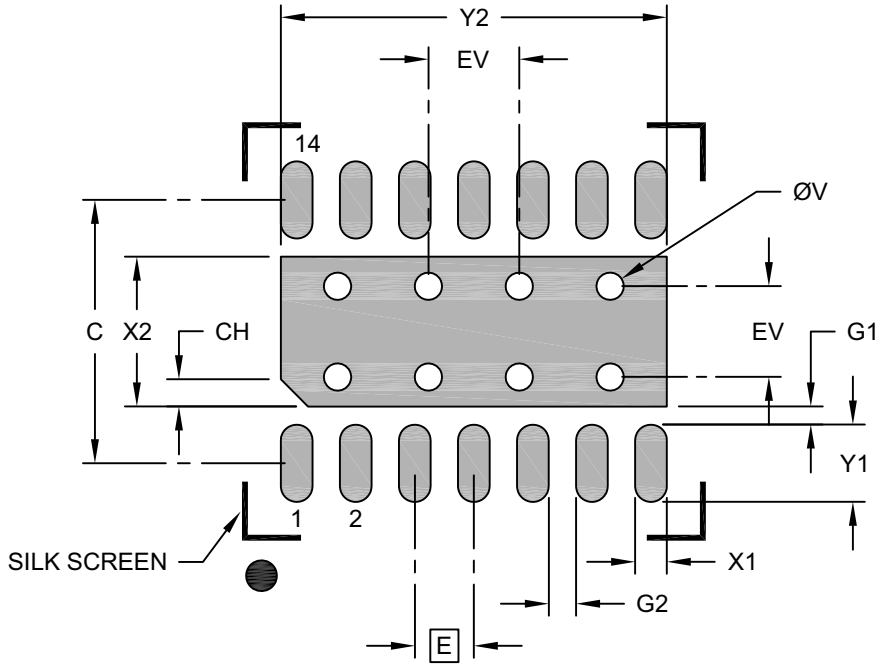
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21361 Rev A Sheet 2 of 2

14-Lead Very Thin Plastic Dual Flat, No Lead Package (QBB) - 4.5x3 mm Body [VDFN] With 1.6x4.2 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	X2			1.65
Optional Center Pad Length	Y2			4.25
Contact Pad Spacing	C		2.90	
Contact Pad Width (X14)	X1			0.35
Contact Pad Length (X14)	Y1			0.85
Pin 1 Index Chamfer	CH		0.30	
Contact Pad to Center Pad (X14)	G1	0.20		
Contact Pad to Center Pad (X12)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-23361 Rev A

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APPENDIX A: REVISION HISTORY

Revision B (September 2017)

The following is the list of modifications:

- Added the new devices ATA6565-GNQW0 and ATA656- GNQW1 and updated the related information across the document.
- Updated Package Types section.
- Updated ATA6565 Family Members section.
- Modified Figure 1-3.
- Updated Section 1.3, Pin Description.
- Updated Temperature Specifications.
- Updated Section 3.0, Packaging Information.
- Updated the Product Identification System.
- Fixed minor typographical errors.

Revision A (June 2017)

- Original Release of this Document.
- This document replaces Atmel - 9364G-11/16.